DS26LV32AQML 3V Enhanced CMOS Quad Differential Line Receiver

Check for Samples: DS26LV32AQML

FEATURES

- **Comparable to Both TIA/EIA-422 and ITU-T V.11 Standards**
- **Low Power CMOS Design (30 mW typical)**
- **Interoperable with Existing 5V RS-422 Networks**
- **Receiver OPEN Input Failsafe Feature**
- **Pin Compatible with DS26C32AT**

DESCRIPTION

The DS26LV32A is a high speed quad differential CMOS receiver that is comparable to TIA/EIA-422-B and ITU-T V.11 standards, but with a specified common mode voltage range of -0.5V to +5.5V due to the lower operating supply voltage of 3.0V to 3.6V. The TRI-STATE enables, EN and $\overline{EN}$, allow the device to be active High or active Low. The enables are common to all four receivers. The receiver output (RO) is specified to be High when the inputs are left open. The receiver can detect signals as low as ±200mV over the common mode range of -0.5V to +5.5V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Connection Diagram

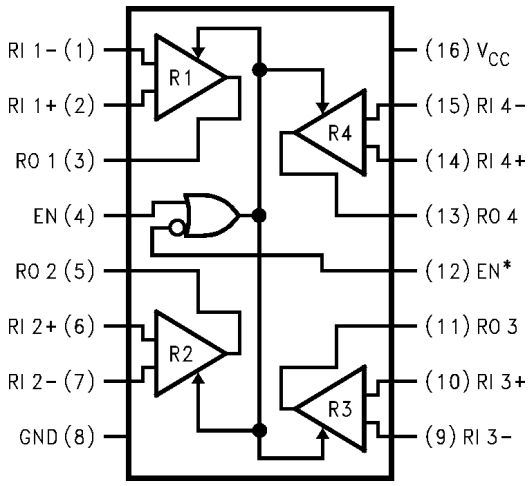


Figure 1. CLGA Package- Top View
See Package Number NAD0016A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})	7.0V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{Diff})	±14V
Enable Input Voltage (V_I)	-0.5V to V_{CC}+0.5V
Storage Temperature Range (T_{Stg})	-65°C ≤ T_A ≤ +150°C
Lead Temperature (T_L) Soldering, 4 seconds	260°C
Maximum Power Dissipation +25°C (2)	1087mW
Thermal Resistance	
θ_{JA}	138°C/W
θ_{JC}	13.5°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not verify specific performance limits. For verified specifications and test conditions, see the Electrical Characteristics. The verified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) Derate CERPAK 7.3mW/°C above +25°C.

Recommended Operating Conditions

Supply Voltage (v_{CC})	3.0V to 3.6V
Operating Temperature Range (T_A)	−55°C ≤ T_A ≤ +125°C

Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

DS26LV32AQML Electrical Characteristics DC Parameters

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
V_{Th}	Minimum Differential Input Voltage	V_{CC} = 3.0/3.6V, $V_O = V_{OH}$ or V_{OL}, -0.5V < V_{CM} < +5.5V		-200	+200	mV	1, 2, 3
R_I	Input Resistance	V_{CC} = 3.6V, -0.5V < V_{CM} < +5.5V, One input AC Gnd		5.0		KΩ	1, 2, 3
I_I	Input Current	V_{CC} = 3.6V, V_I = +5.5V Other Input = Gnd		0.0	+1.8	mA	1, 2, 3
		V_{CC} = 3.6V, V_I = -0.5V Other Input = Gnd		0.0	-1.8	mA	1, 2, 3
		V_{CC} = 0V, V_I = +5.5V Other Input = Gnd		0.0	+1.8	mA	1, 2, 3
		V_{CC} = 0V, V_I = -0.5V Other Input = Gnd		0.0	-1.8	mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 3.0V, V_{Diff} = +1V, I_O = -6.0mA		2.4		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 3.0V, V_{Diff} = -1V, I_O = 6.0mA			0.5	V	1, 2, 3
V_{IH}	Minimum Enable High Level Voltage		(1)	2.0		V	1, 2, 3
V_{IL}	Maximum Enable Low Level Voltage		(1)		0.8	V	1, 2, 3
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{CC} = 3.6V, $V_O = V_{CC}$ or Gnd Enable = V_{IL}, $\overline{\text{Enable}}$ = V_{IH}			±50	µA	1, 2, 3
I_{En}	Maximum Enable Input Current	V_{CC} = 3.6V, $V_I = V_{CC}$ or Gnd			±1.0	µA	1, 2, 3
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, No Load, En, $\overline{\text{En}}$ = V_{CC} or Gnd, -0.5V<V_{CM}<+5.5V			20	mA	1, 2, 3
I_{OS}	Output Short Circuit Current	V_{CC} = 3.0V/3.6V, V_O = 0V, V_{Diff} = +1V	(2)	-10	-70	mA	1, 2, 3

(1) Parameter tested Go-No-Go only.
(2) Short one output at a time to Gnd.

DS26LV32AQML Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.
AC: V_{CC} = 3.0/3.6V, C_L = 50pF

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
t_{PLH}	Input to Output Propagation Delay	V_{CM} = 1.5V	(1)	6.0	45	nS	9, 10, 11
t_{PHL}	Input to Output Propagation Delay	V_{CM} = 1.5V	(1)	6.0	45	nS	9, 10, 11
t_{SK1}	Skew tpHLD-tpLHD (same channel)				6.0	nS	9, 10, 11
t_{SK2}	Pin to Pin Skew (Same device)				6.0	nS	9, 10, 11
t_{PLZ}	Output Disable Time	2KΩ to V_{CC}	(2)		50	nS	9, 10, 11
t_{PZL}	Output Enable Time	2KΩ to V_{CC}	(2)		50	nS	9, 10, 11
t_{PHZ}	Output Disable Time	2KΩ to Gnd	(2)		50	nS	9, 10, 11
t_{PZH}	Output Enable Time	2KΩ to Gnd	(2)		50	nS	9, 10, 11

(1) Generator waveform is specified as follows: f = 1MHz, Duty Cycle = 50%, Z_O = 50Ω, $t_R = t_F \le$ 6nS. Receiver inputs = 1V to 2V with measure points equal to 1.5V on the inputs to 1/2 V_{CC} on the outputs.
(2) Generator waveform is specified as follows: f = 1MHz, Duty Cycle = 50%, Z_O = 50Ω, $t_R = t_F \le$ 6nS. En/$\overline{\text{En}}$ inputs = 0V to 3V with measure points equal to 1.5V on the inputs, to 1/2 V_{CC} on the outputs for Z_L and Z_H, and (V_{OL} + 0.3V) for L_Z, and (V_{OH}.- 0.3V) for H_Z.

REVISION HISTORY

Released	Revision	Section	Originator	Changes
3/01/06	*	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNDS26LV32A-X Rev 0A0 will be archived.
4/15/2013	A		TIS	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9858501QFA	ACTIVE	CFP	NAD	16	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26LV32AW-QML Q 5962-98585 01QFA ACO 01QFA >T	Samples
DS26LV32AW-QML	ACTIVE	CFP	NAD	16	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26LV32AW-QML Q 5962-98585 01QFA ACO 01QFA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

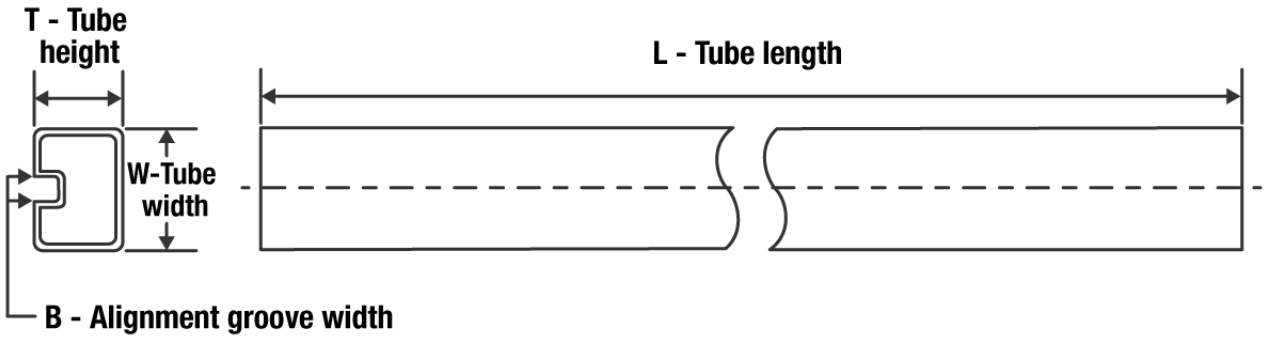
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

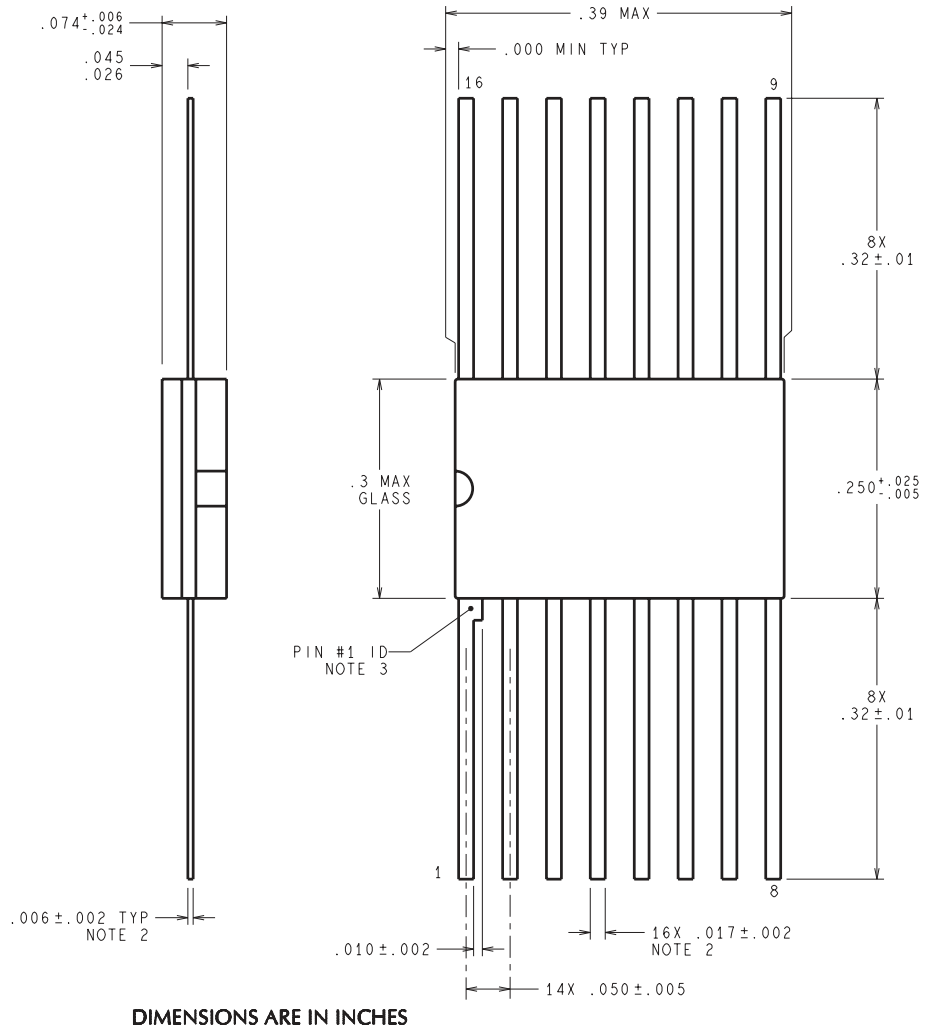
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9858501QFA	NAD	CFP	16	19	502	23	9398	9.78
DS26LV32AW-QML	NAD	CFP	16	19	502	23	9398	9.78

NAD0016A



DIMENSIONS ARE IN INCHES

W16A (Rev T)

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