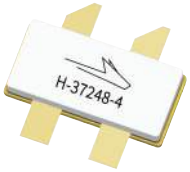
PTFB181702FC

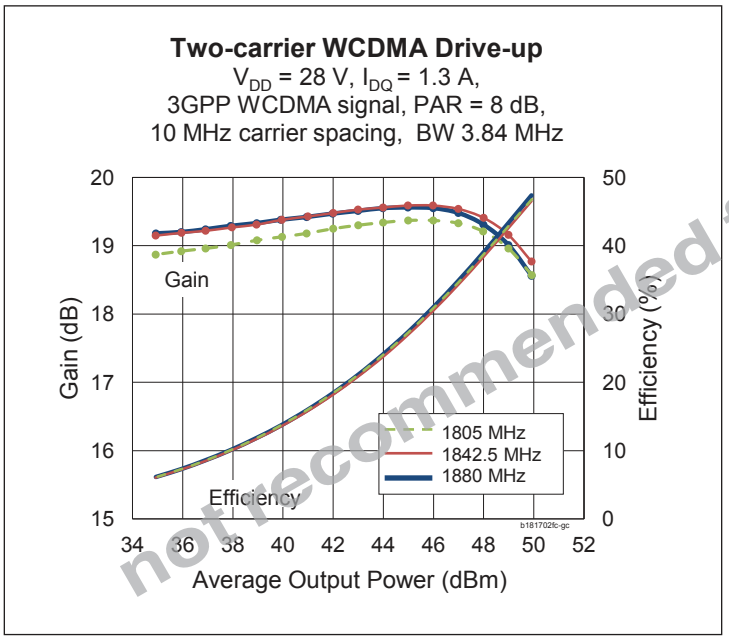
Thermally-Enhanced High Power RF LDMOS FET
170 W, 28 V, 1805 – 1880 MHz

Description

The PTFB181702FC is a 170-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications. Features include input and output matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PTFB181702FC
Package H-37248-4





not recommended for new design

Features

- Broadband internal matching
- Typical CW performance, 1842 MHz, 28 V
  - Output power at P_{1dB} = 180 W
  - Efficiency = 58%
  - Gain = 18.5 dB
- Capable of handling 10:1 VSWR @28 V, 170 W (CW) output power
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Two-carrier WCDMA Specifications (tested in Wolfspeed test fixture)
V_{DD} = 28 V, I_{DQ} = 1300 mA, P_{OUT} = 30 W avg, f_1 = 1870 MHz, f_2 = 1880 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	18	19	—	dB
Drain Efficiency	η_D	24	26	—	%
Intermodulation Distortion	IMD	—	–35	–33	dBc

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.11	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 650 mA	V_{GS}	2.5	3.0	3.5	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA

Maximum Ratings

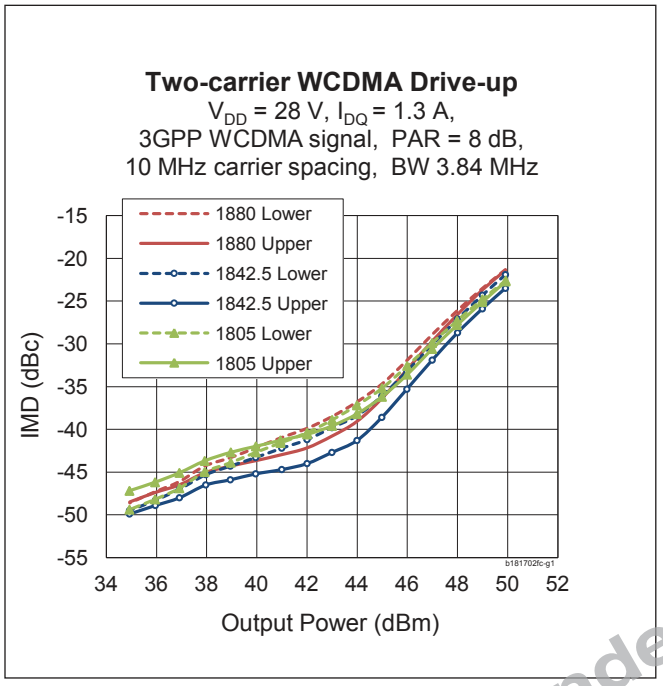
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 170 W CW)	$R_{\theta JC}$	0.27	°C/W

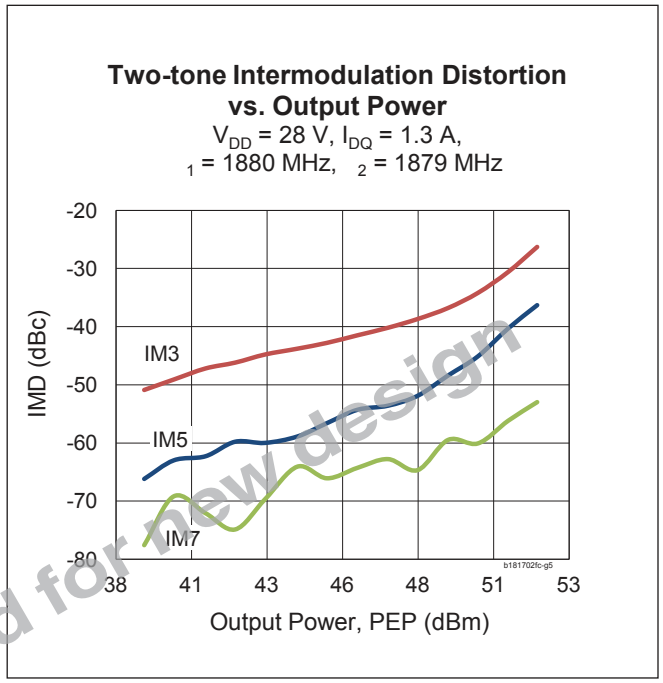
Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTFB181702FC V1 R0	PTFB181702FC-V1-R0	H-37248-4, earless flange	Tape & Reel, 50 pcs
PTFB181702FC V1 R250	PTFB181702FC-V1-R250	H-37248-4, earless flange	Tape & Reel, 250 pcs

not recommended for new design

Typical Performance (data taken in a production test fixture)





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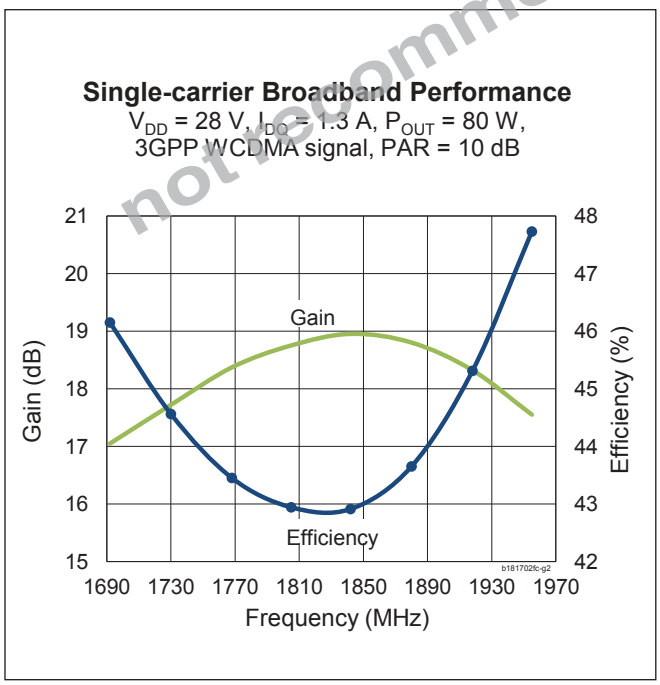
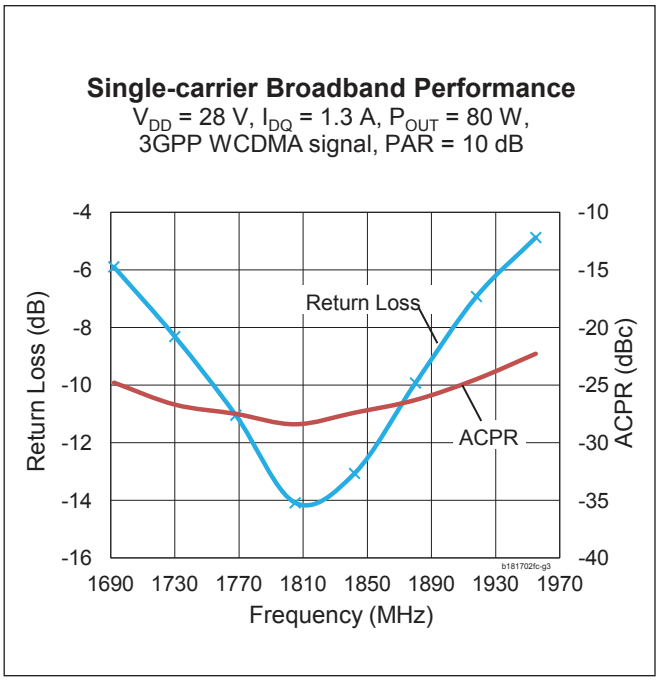
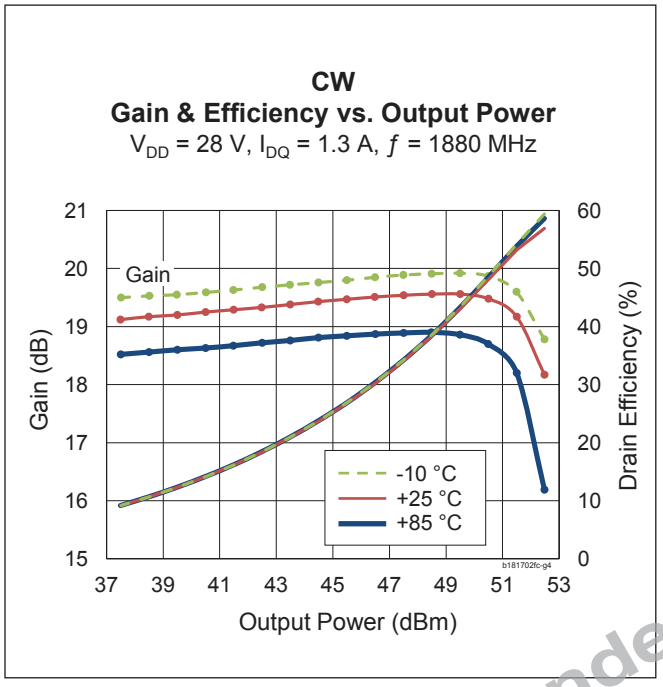
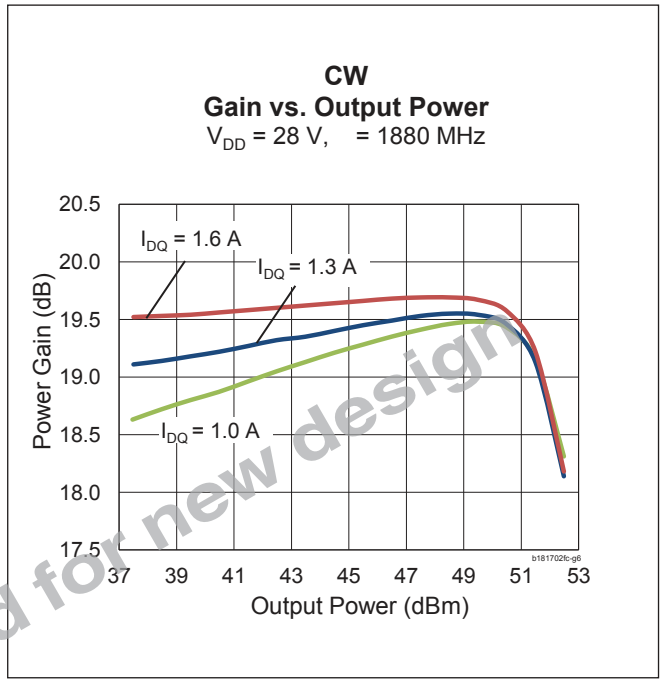




Typical Performance (cont.)





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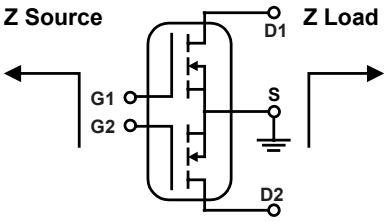
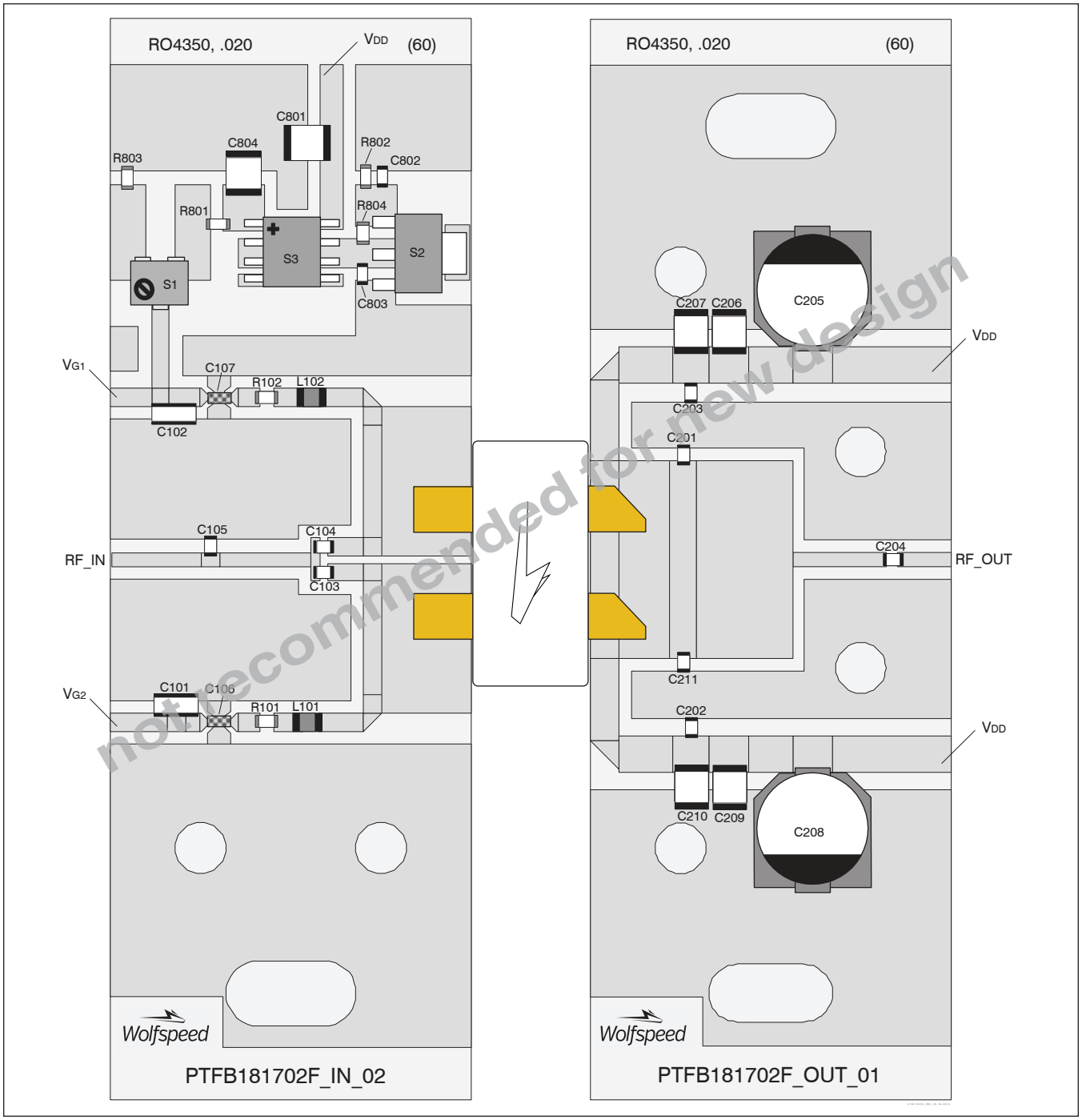
Broadband Circuit Impedance

Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
1805	2.99	–6.14	1.87	–4.46
1825	2.99	–6.08	1.52	–4.50
1845	3.00	–6.03	1.35	–4.34
1865	3.00	–5.97	1.25	–4.19
1880	3.00	–5.94	1.20	–4.08



Reference Circuit



*Reference circuit assembly diagram (not to scale)**

Reference Circuit (cont.)

Reference Circuit Assembly	
DUT	PTFB181702FC
Test Fixture Part No.	LTN/PTFB181702FC
PCB	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66
Find Gerber files for this test fixture on the Wolfspeed Web site at *http://www.wolfspeed.com/RF*	

Components Information

Component	Description	Suggested Supplier	P/N
Input			
C101, C102	Capacitor, 10 µF	Digi-Key	490-4393-2-ND
C103, C104	Capacitor, 18 pF	ATC	ATC800A180JT250XT
C105	Capacitor, 1.5 pF	ATC	ATC800A1R5BT250XT
C106, C107	EMI Suppression Capacitor	Digi-Key	NFM18PS105R0J3D-ND
C801, C804	Capacitor, 10 µF	Digi-Key	587-1818-2-ND
C802	Chip capacitor, 1000 pF	Digi-Key	PCC1772CT-ND
C803	Capacitor, 1 µF	Digi-Key	490-4736-2-ND
L101, L102	Inductor, 27.3 nH	Coilcraft	0908SQ-27NGLB
R101, R102, R803	Resistor, 10 ohm	Digi-Key	P10GTR-ND
R801	Resistor, 100 ohm	Digi-Key	P100GTR-ND
R802	Resistor, 1300 ohm	Digi-Key	P1.3KGTR-ND
R804	Resistor, 1200 ohm	Digi-Key	P1.2KGTR-ND
S1	Potentiometer, 2k Ω	Digi-Key	3224W-202ECT-ND
S2	Transistor	Digi-Key	BCP56-ND
S3	Voltage Regulator	Digi-Key	LM7805
Output			
C201, C211	Chip capacitor, 1.2 pF	ATC	ATC800A1R2BT250XT
C202, C203, C204	Chip capacitor, 18 pF	ATC	ATC800A180JT250XT
C205, C208	Capacitor, 220 µF	Digi-Key	PCE4444TR-ND
C206, C207, C209, C210	Capacitor, 10 µF	Digi-Key	587-1818-2-ND

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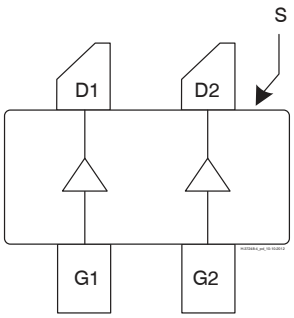
Pinout Diagram (top view)

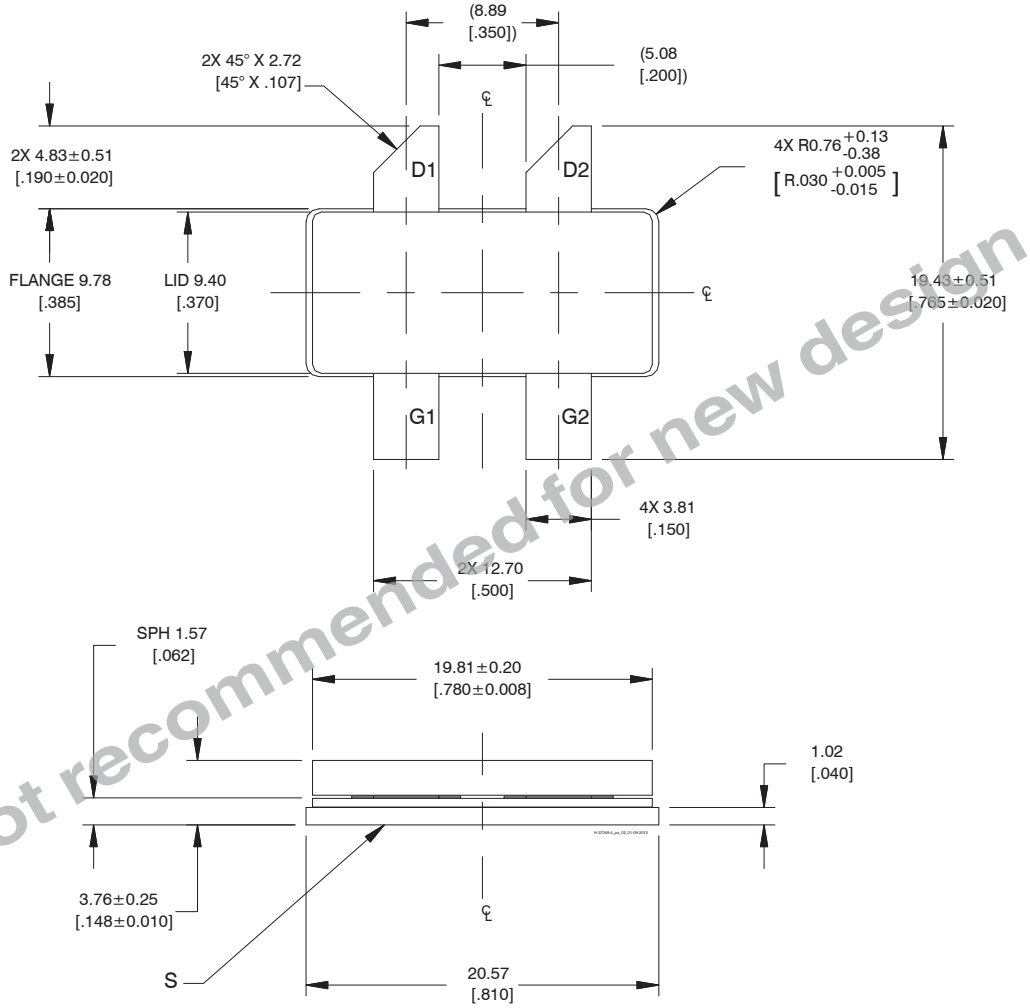


Pin	Description
D1	Drain Device 1
D2	Drain Device 2
G1	Gate Device 1
G2	Gate Device 2
S	Source (flange)

Lead connections for PTFB181702FC

Package Outline Specifications

Package H-37248-4



not recommended for new design

Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.076/–0.025 mm [0.004+0.003/–0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2012-05-29	Advance	All	Data Sheet reflects advance specification for product development
02	2012-10-15	Advance	All	Data sheet reflects released product specifications
02.1	2016-06-10	Production	2, 7	Updated ordering code to R0, revised package outline-minor changes
03	2018-02-21	Production	All	Not recommended for new design
04	2018-08-20	Production	All	Converted to Wolfspeed data sheet

not recommended for new design

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Notes

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