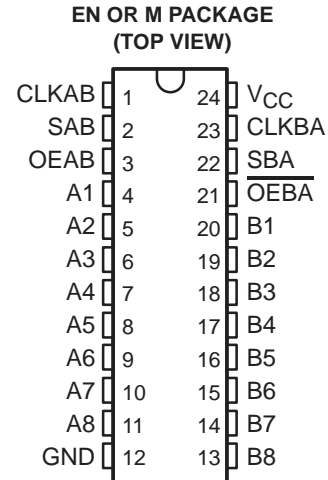


# CD74FCT654 BiCMOS OCTAL BUS TRANSCEIVER AND REGISTER WITH OPEN-COLLECTOR AND 3-STATE OUTPUTS

SCBS732 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Open-Collector Outputs on A Bus, 3-State Outputs on B Bus
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From  $V_{CC}$
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Package Options Include Plastic Small-Outline (M) Package and Standard Plastic (EN) DIP



## description

The CD74FCT654 is an octal bus transceiver and register with open-collector and 3-state outputs. It consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and OEBA) inputs control the transceiver functions. Select-control (SAB and SBA) inputs select real-time-data or stored-data transfer. The select-control circuitry eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored data and real-time data. A low input level selects real-time data, and a high input level selects stored data.

The device uses a small-geometry BiCMOS technology. The output state is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

The CD74FCT654 has noninverted outputs with open drains on the A outputs and 3-state outputs on the B side. Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the state of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The CD74FCT654 is characterized for operation from 0°C to 70°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

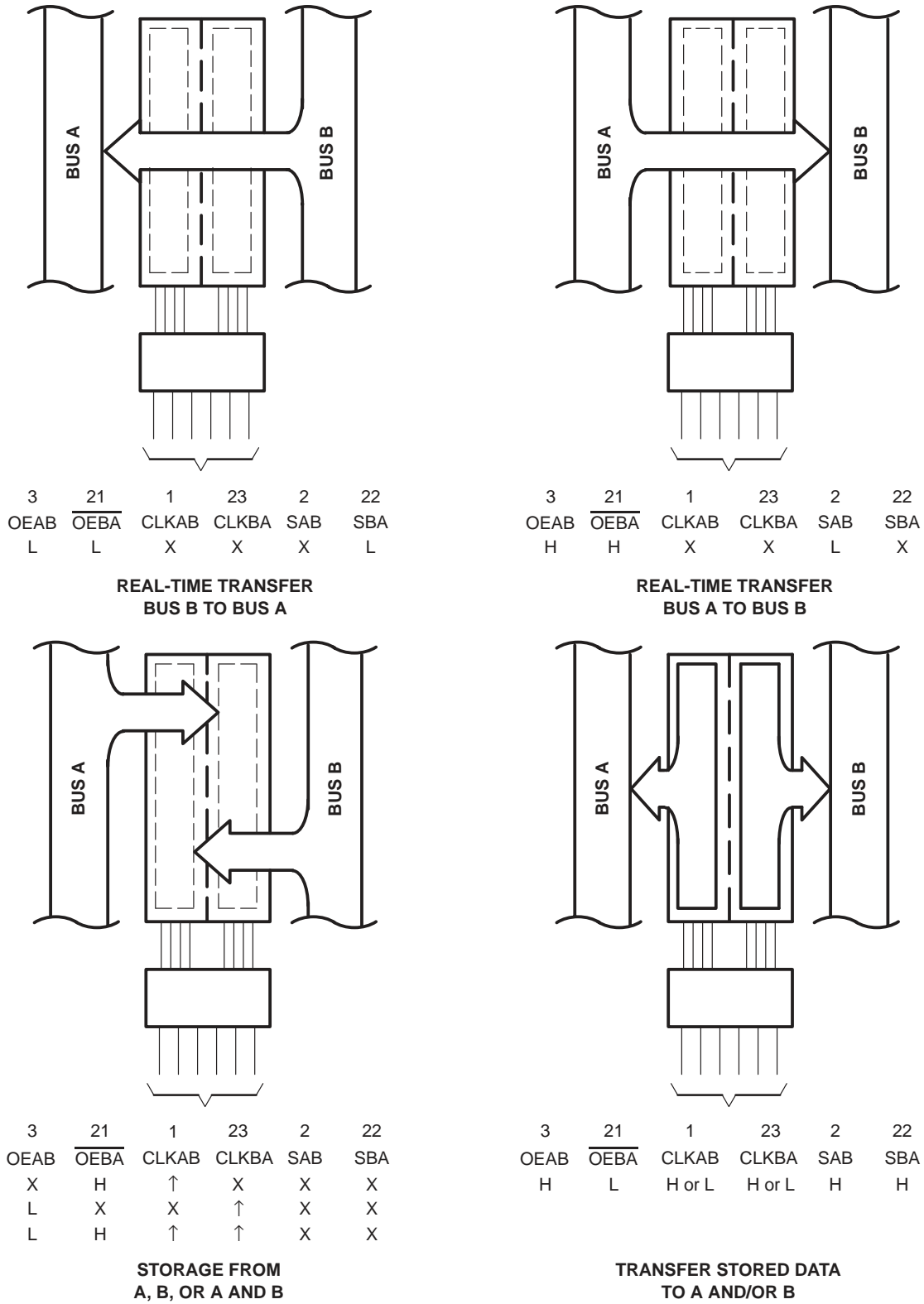
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**CD74FCT654**  
**BiCMOS OCTAL BUS TRANSCEIVER AND REGISTER**  
**WITH OPEN-COLLECTOR AND 3-STATE OUTPUTS**

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**Figure 1. Bus-Management Functions**

# CD74FCT654

## BiCMOS OCTAL BUS TRANSCEIVER AND REGISTER WITH OPEN-COLLECTOR AND 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation‡
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified§	Store A, hold B
H	H	↑	↑	X§	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified§	Input	Hold A, store B
L	L	↑	↑	X	X§	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

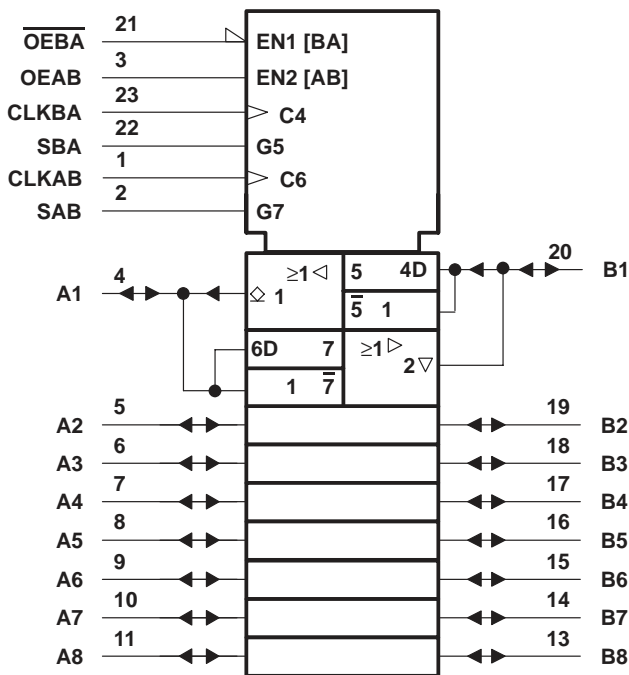
† The data output functions can be enabled or disabled by various level combinations at OEAB or OEBA. Data input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ To prevent excess currents in the high-impedance (isolation) state, all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

§ Select control = L (Clocks can occur simultaneously.)

Select control = H (Clocks must be staggered to load both registers.)

### logic symbol¶

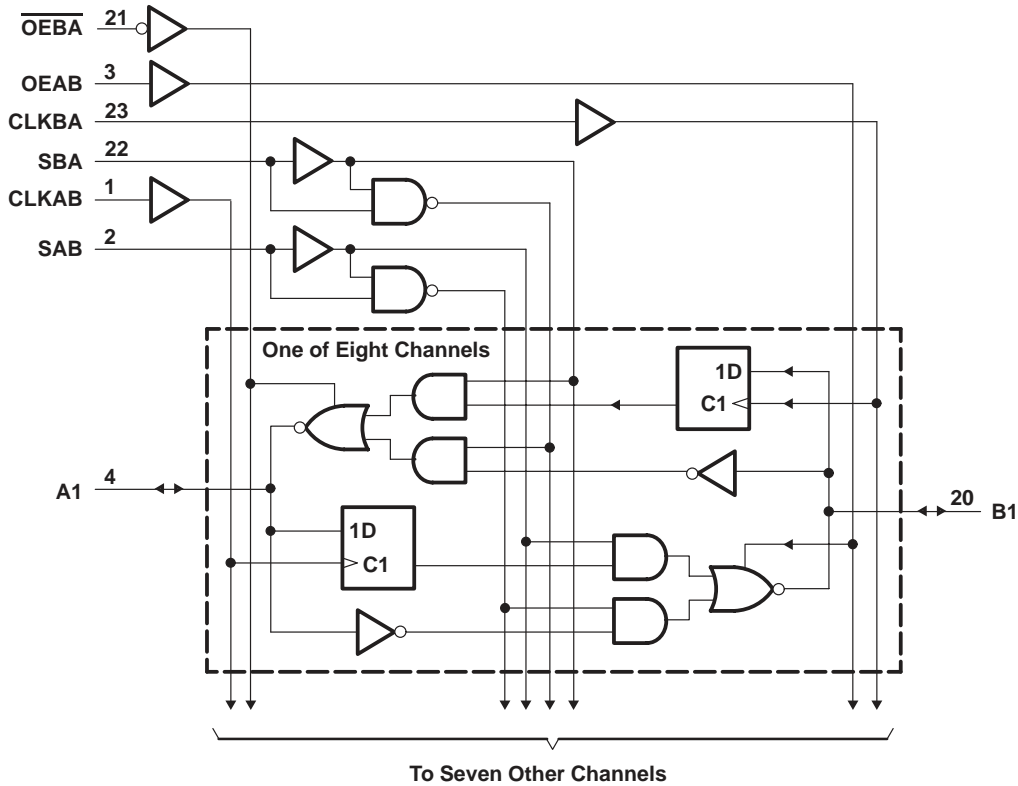


¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

DC supply voltage range, $V_{CC}$ .....	-0.5 V to 6 V
DC input clamp current, $I_{IK}$ ( $V_I < -0.5$ V) .....	-20 mA
DC output clamp current, $I_{OK}$ ( $V_O < -0.5$ V) .....	-50 mA
DC output sink current per output pin, $I_{OL}$ .....	70 mA
DC output source current per output pin, $I_{OH}$ .....	-30 mA
Continuous current through $V_{CC}$ , $I_{CC}$ .....	140 mA
Continuous current through GND .....	528 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): EN package .....	67°C/W
..... M package .....	46°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.



# CD74FCT654

## BiCMOS OCTAL BUS TRANSCEIVER AND REGISTER WITH OPEN-COLLECTOR AND 3-STATE OUTPUTS

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### recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5.25	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-15	mA
I <sub>OL</sub>	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V <sub>IK</sub>	I <sub>I</sub> = -18 mA	4.75 V		-1.2		-1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = -15 mA	4.75 V	2.4		2.4		V
V <sub>OL</sub>	I <sub>OL</sub> = 64 mA	4.75 V		0.55	0.55		V
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.25 V		±0.1	±1		μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.25 V		±0.5	±10		μA
I <sub>OS</sub> <sup>†</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = 0	5.25 V		-60	-60		mA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.25 V		8	80		μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.25 V		1.6	1.6		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			10	10		pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			15	15		pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

### timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 2)

		MIN	MAX	UNIT	
f <sub>clock</sub>	Clock frequency		80	MHz	
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high		6	ns
		CLKAB or CLKBA low		6	ns
t <sub>su</sub>	Setup time	A before CLKAB↑ or B before CLKBA↑		4	ns
t <sub>h</sub>	Hold time	A after CLKAB↑ or B after CLKBA↑		2	ns



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switching characteristics over recommended operating temperature conditions (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C		UNIT
			MIN	MAX	
f <sub>max</sub>			80		MHz
t <sub>pd</sub>	CLKAB	B	6.8	2 9	ns
t <sub>PLZ</sub>	CLKBA	A	6.8	2 9	ns
t <sub>PZL</sub>			6.8	2 9	
t <sub>pd</sub>	A	B	6.8	2 9	ns
t <sub>PLZ</sub>	B	A	6.8	2 9	ns
t <sub>PZL</sub>			6.8	2 9	
t <sub>pd</sub>	SAB†	B	8.3	2 11	ns
t <sub>PLZ</sub>	SBA†	A	6.8	2 9	ns
t <sub>PZL</sub>			6.8	2 9	
t <sub>en</sub>	OEAB	B	11.3	2 15	ns
t <sub>dis</sub>	OEAB	B	6.8	2 9	ns
t <sub>PLZ</sub>	$\overline{\text{OEBA}}$	A	6.8	2 9	ns
t <sub>PZL</sub>			11.3	2 15	

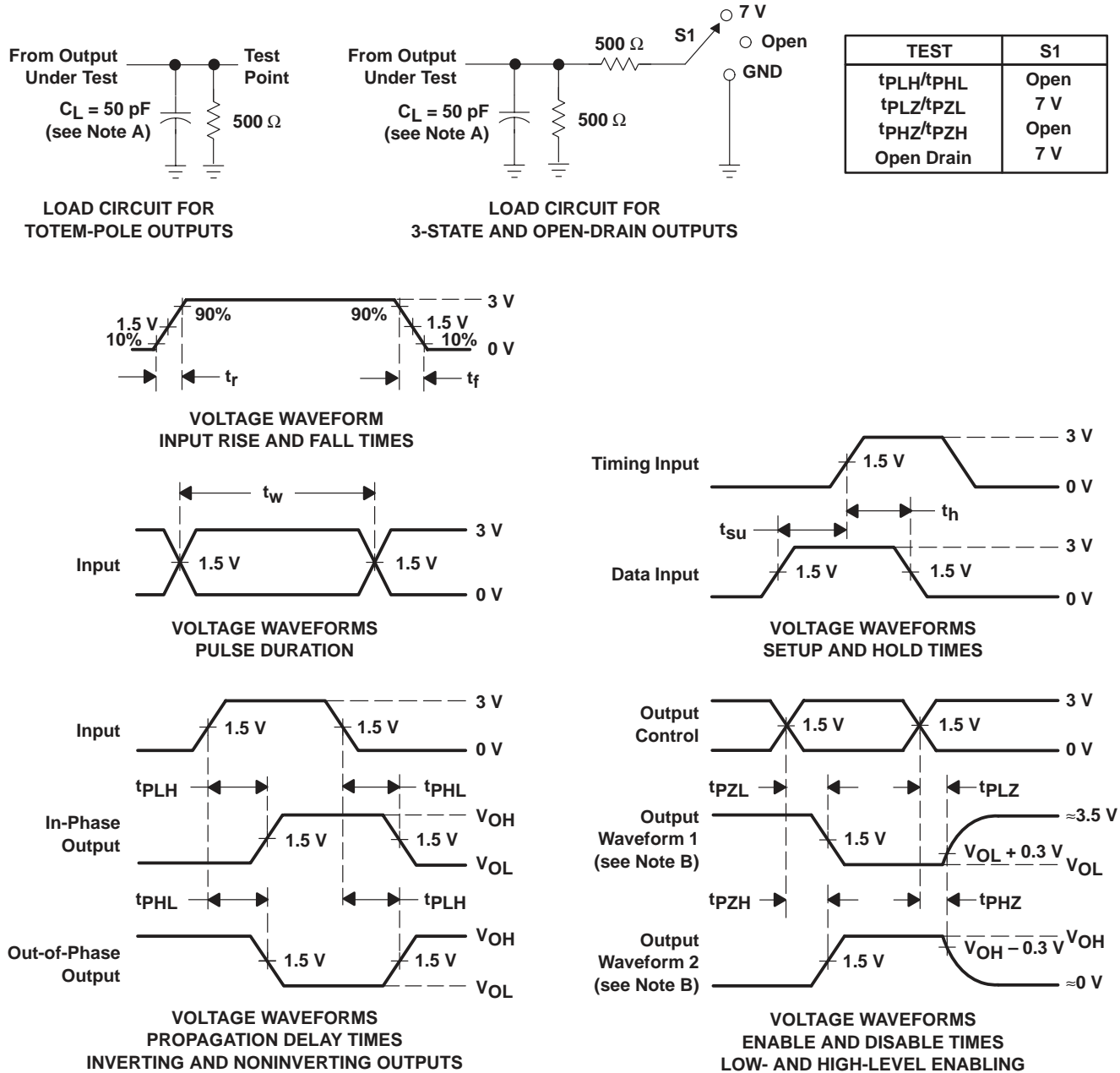
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		1		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		0.5		V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V



**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 2.5$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74FCT654EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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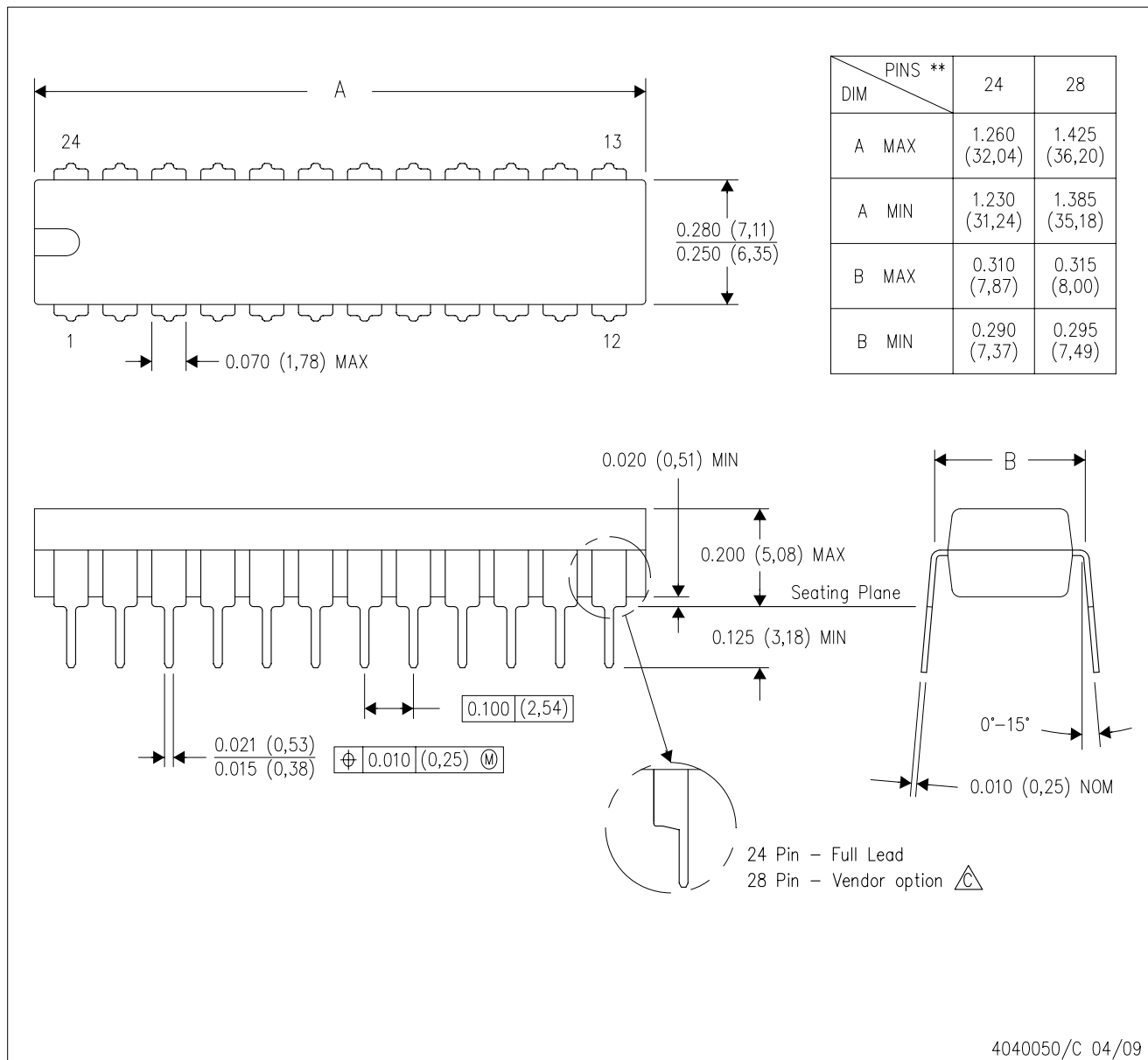
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# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

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