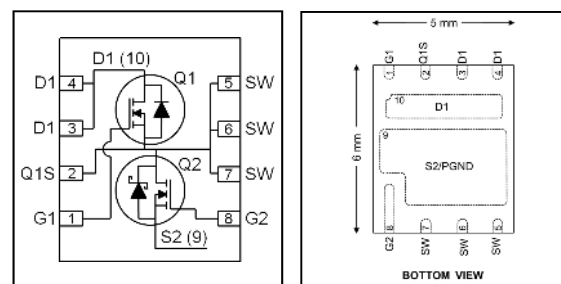


HEXFET® Power MOSFET

	Q1	Q2	
V_{DSS}	25	25	V
R_{DS(on)} max (@V _{GS} = 4.5V)	4.60	1.10	mΩ
Qg (typical)	10	44	nC
I_D (@T _C = 25°C)	45 Ⓣ	45 Ⓣ	A



Applications

- Control and Synchronous MOSFETs for synchronous buck converters



Features

Control and synchronous MOSFETs in one package
Low charge control MOSFET (10nC typical)
Low R _{DS(on)} synchronous MOSFET (<1.10mΩ)
Intrinsic Schottky Diode with Low Forward Voltage on Q2
RoHS Compliant, Halogen-Free
MSL1, Industrial Qualification

results in
⇒

Benefits

Increased power density
Lower switching losses
Lower conduction losses
Lower Switching Losses
Environmentally friendlier
Increased reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH4251DPbF	Dual PQFN 5mm x 6mm	Tape and Reel	4000	IRFH4251DTRPbF

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V _{GS}	Gate-to-Source Voltage	± 20		V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 4.5V	64	188	A
I _D @ T _C = 70°C	Continuous Drain Current, V _{GS} @ 4.5V	51	151	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 4.5V (Source Bonding Technology Limited)	45	45	
I _{DM}	Pulsed Drain Current	120	750	
P _D @ T _C = 25°C	Power Dissipation	31	63	W
P _D @ T _C = 70°C	Power Dissipation	20	40	
	Linear Derating Factor	0.25	0.50	W/°C
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ④	4.0	2.0	°C/W
R _{θJC} (Top)	Junction-to-Case ④	20	12	
R _{θJA}	Junction-to-Ambient ⑤	34	35	
R _{θJA} (<10s)	Junction-to-Ambient ⑤	24	22	

Notes ① through ⑧ are on page 12

Static @ T_J = 25°C (unless otherwise specified)

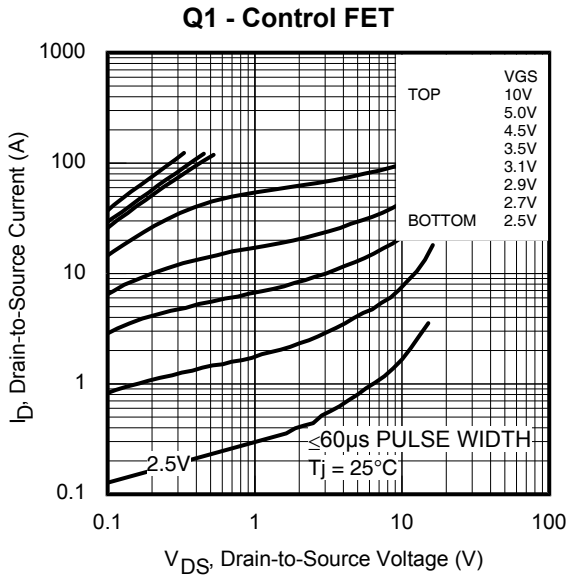
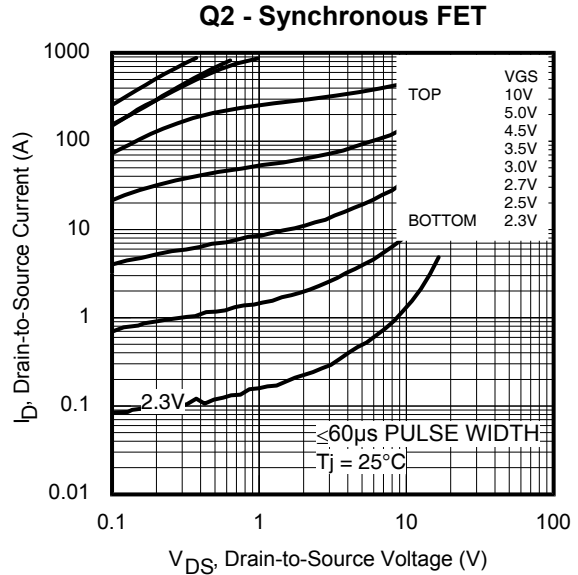
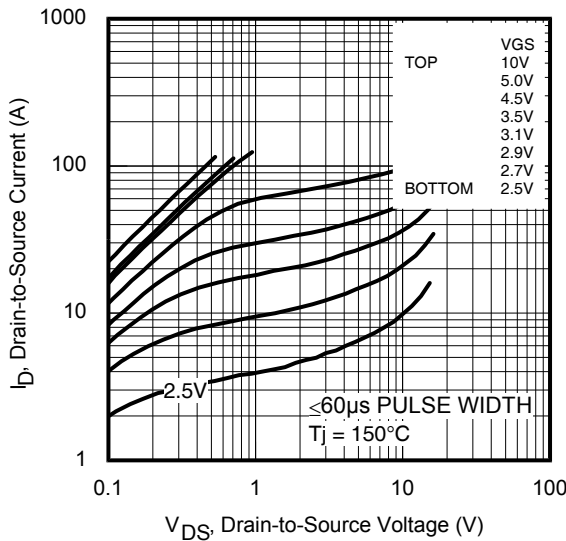
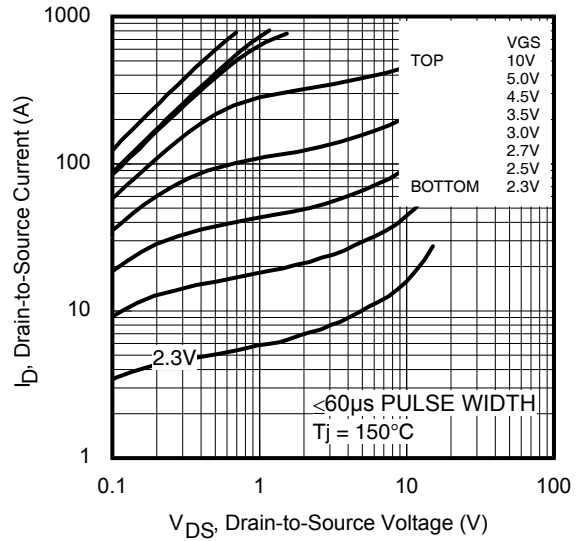
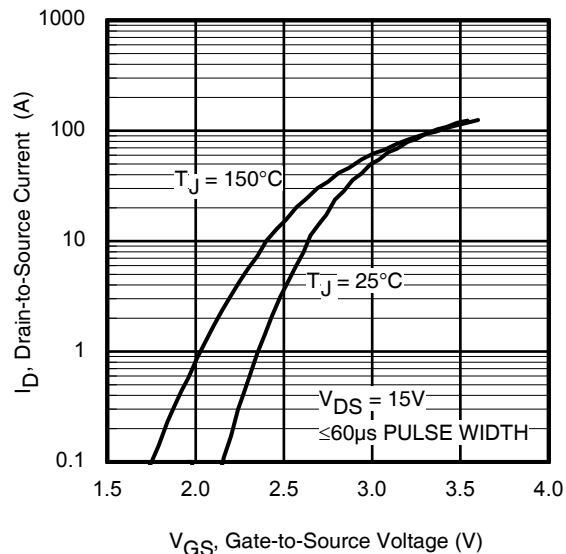
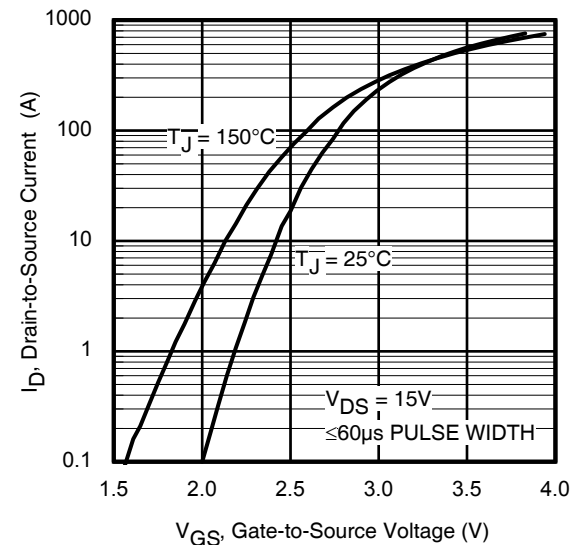
	Parameter		Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	Q1	25	—	—	V	V _{GS} = 0V, I _D = 250μA
		Q2	25	—	—		V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	Q1	—	22	—	mV/°C	Reference to 25°C, I _D = 1.0mA
		Q2	—	20	—		Reference to 25°C, I _D = 10mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	Q1	—	2.50	3.20	mΩ	V _{GS} = 10V, I _D = 30A ③
		Q2	—	0.60	0.85		V _{GS} = 10V, I _D = 30A ③
		Q1	—	3.70	4.60		V _{GS} = 4.5V, I _D = 30A ③
		Q2	—	0.85	1.10		V _{GS} = 4.5V, I _D = 30A ③
V _{GS(th)}	Gate Threshold Voltage	Q1	1.1	1.6	2.1	V	Q1: V _{DS} = V _{GS} , I _D = 35μA
		Q2	1.1	1.6	2.1		Q2: V _{DS} = V _{GS} , I _D = 150μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	Q1	—	-5.7	—	mV/°C	Q1: V _{DS} = V _{GS} , I _D = 35μA
		Q2	—	-10	—		Q2: V _{DS} = V _{GS} , I _D = 150μA
I _{DSS}	Drain-to-Source Leakage Current	Q1	—	—	1.0	μA	V _{DS} = 20V, V _{GS} = 0V
		Q2	—	—	250		V _{DS} = 20V, V _{GS} = 0V
I _{GSS}	Gate-to-Source Forward Leakage	Q1/Q2	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1/Q2	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	Q1	131	—	—	S	V _{DS} = 10V, I _D = 30A
		Q2	161	—	—		V _{DS} = 10V, I _D = 30A
Q _g	Total Gate Charge	Q1	—	10	15	nC	Q1 V _{DS} = 13V V _{GS} = 4.5V, I _D = 30A Q2 V _{DS} = 13V V _{GS} = 4.5V, I _D = 30A
		Q2	—	44	66		
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	Q1	—	2.5	—		
		Q2	—	11	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	Q1	—	1.6	—		
		Q2	—	4.2	—		
Q _{gd}	Gate-to-Drain Charge	Q1	—	3.8	—		
		Q2	—	15	—		
Q _{godr}	Gate Charge Overdrive	Q1	—	2.1	—		
		Q2	—	13.8	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	Q1	—	5.4	—		
		Q2	—	19.2	—		
Q _{oss}	Output Charge	Q1	—	10	—	nC	V _{DS} = 16V, V _{GS} = 0V
		Q2	—	44	—		
R _G	Gate Resistance	Q1	—	2.4	—	Ω	
		Q2	—	0.85	—		
t _{d(on)}	Turn-On Delay Time	Q1	—	10	—	ns	Q1 V _{DS} = 13V V _{GS} = 4.5V I _D = 30A, R _G = 1.8Ω Q2 V _{DS} = 13V V _{GS} = 4.5V I _D = 30A, R _G = 1.8Ω
		Q2	—	24	—		
t _r	Rise Time	Q1	—	61	—		
		Q2	—	105	—		
t _{d(off)}	Turn-Off Delay Time	Q1	—	13	—		
		Q2	—	35	—		
t _f	Fall Time	Q1	—	15	—		
		Q2	—	60	—		
C _{iss}	Input Capacitance	Q1	—	1314	—	pF	V _{GS} = 0V V _{DS} = 13V f = 1.0MHz
		Q2	—	5845	—		
C _{oss}	Output Capacitance	Q1	—	365	—		
		Q2	—	1703	—		
C _{rss}	Reverse Transfer Capacitance	Q1	—	92	—		
		Q2	—	408	—		

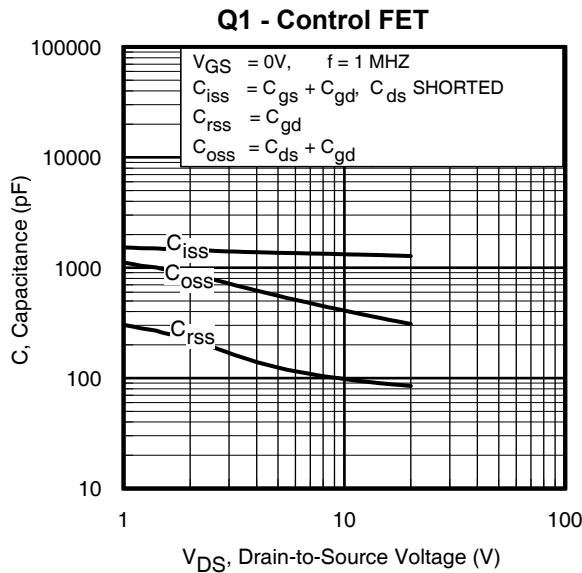
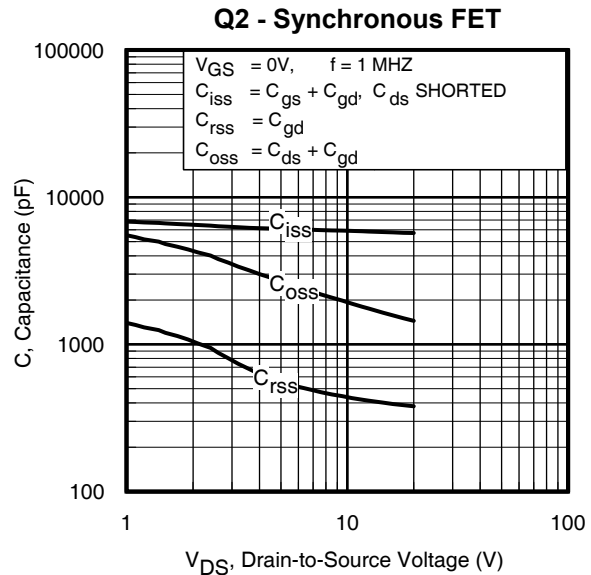
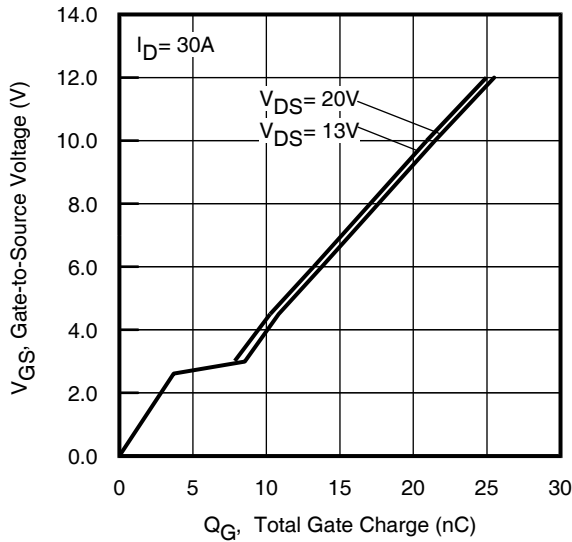
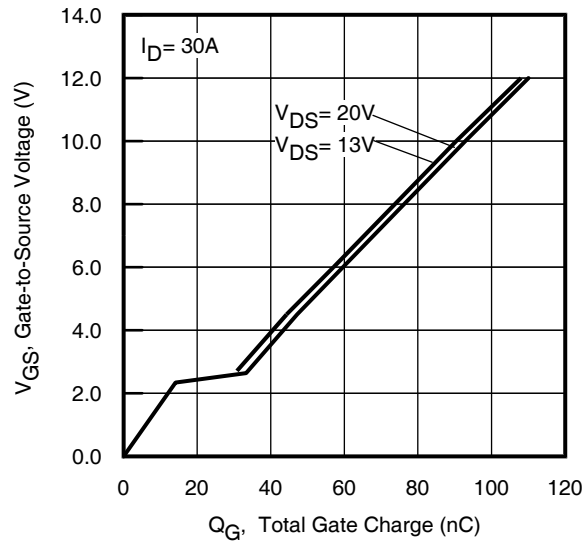
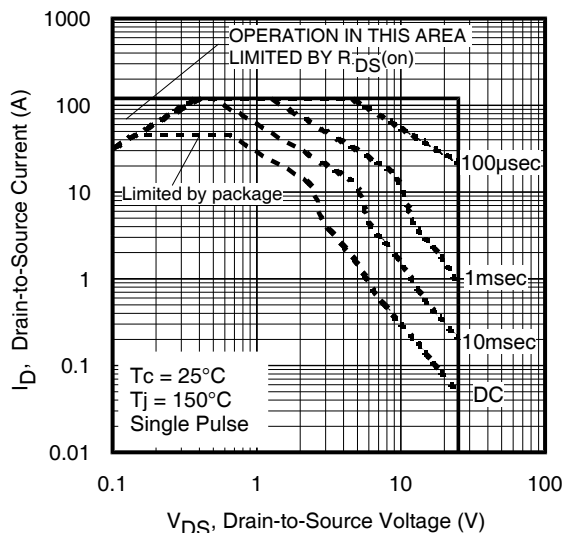
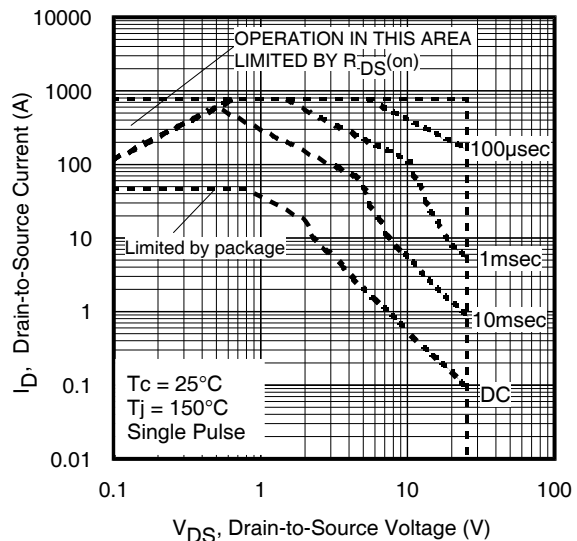
Avalanche Characteristics

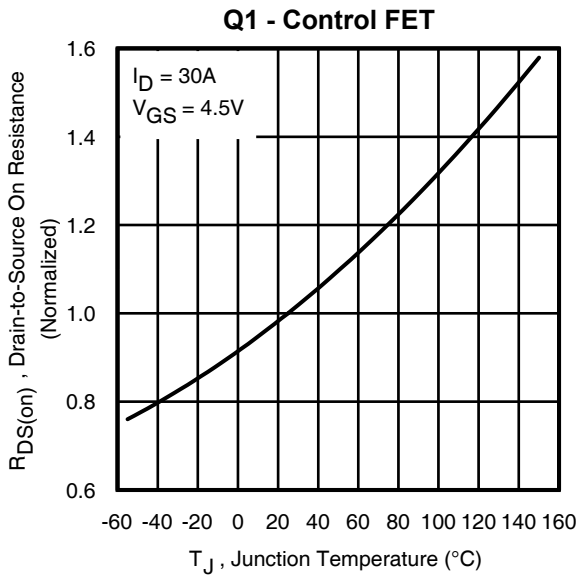
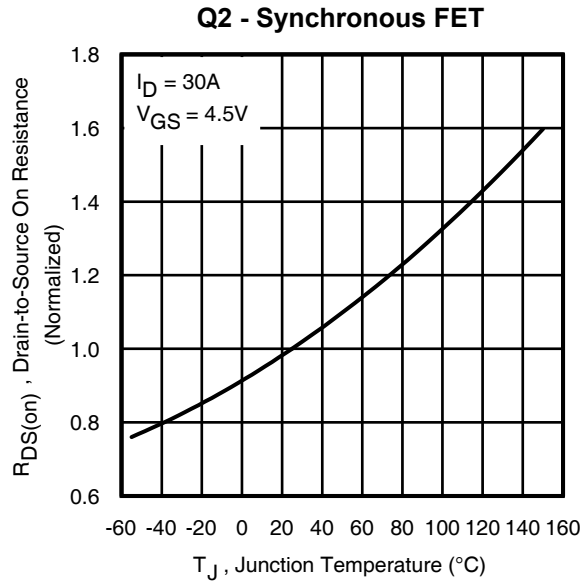
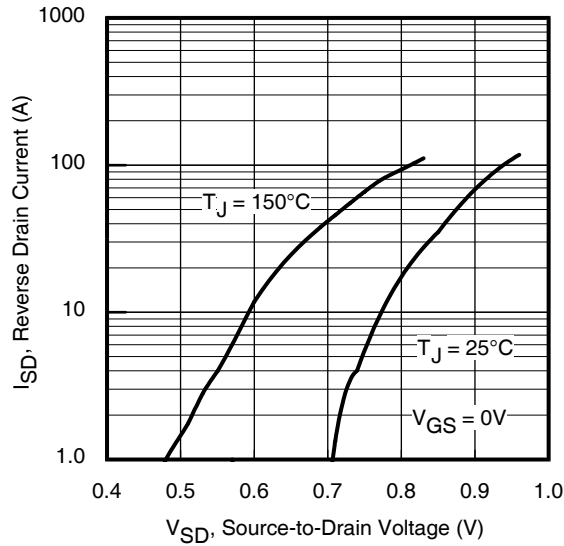
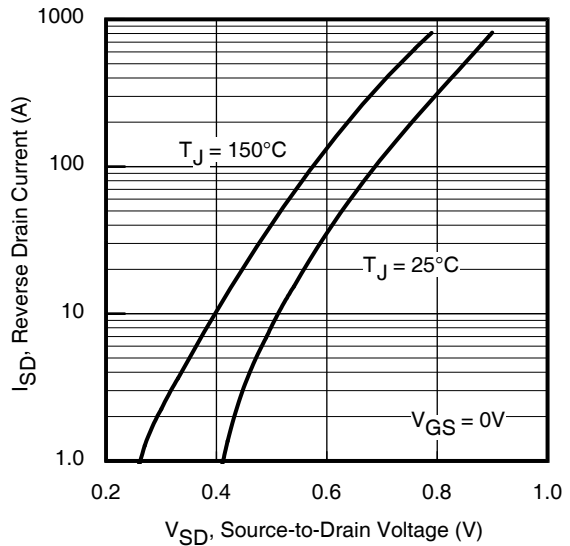
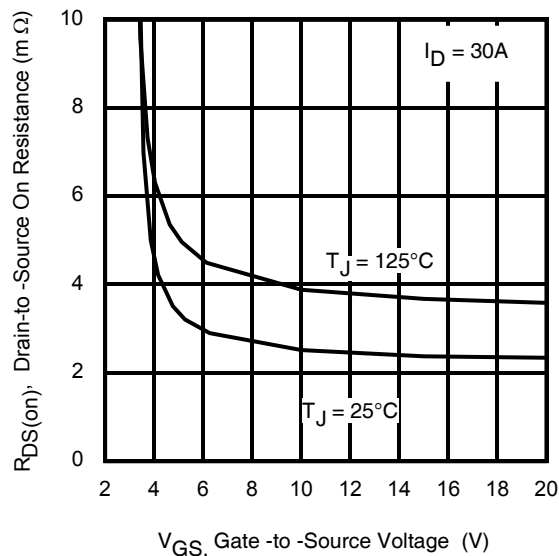
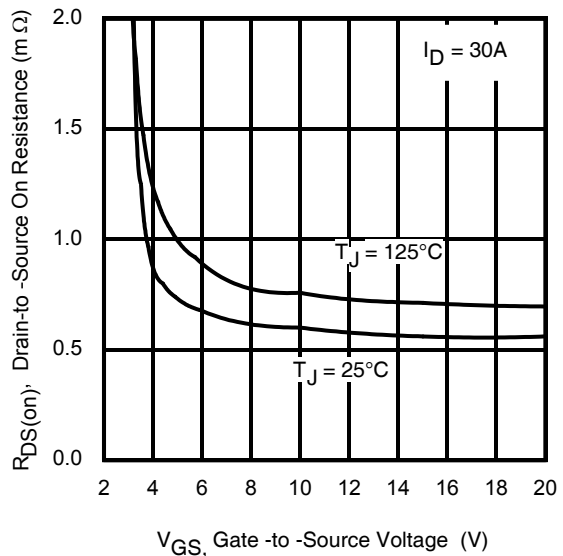
	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	61	1292	mJ
I_{AR}	Avalanche Current ①	—	30	60	A

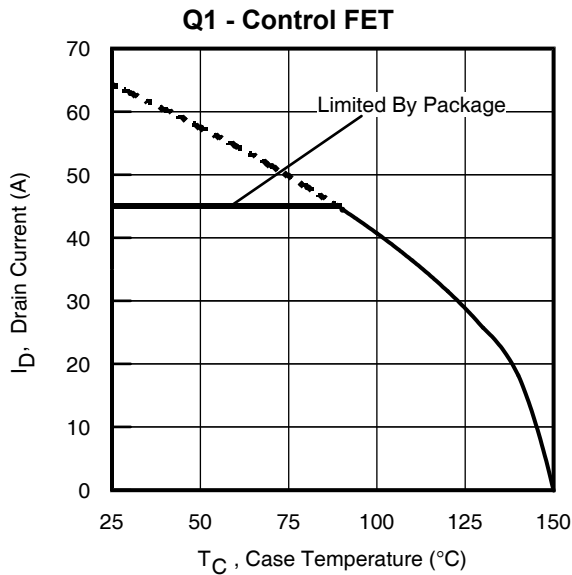
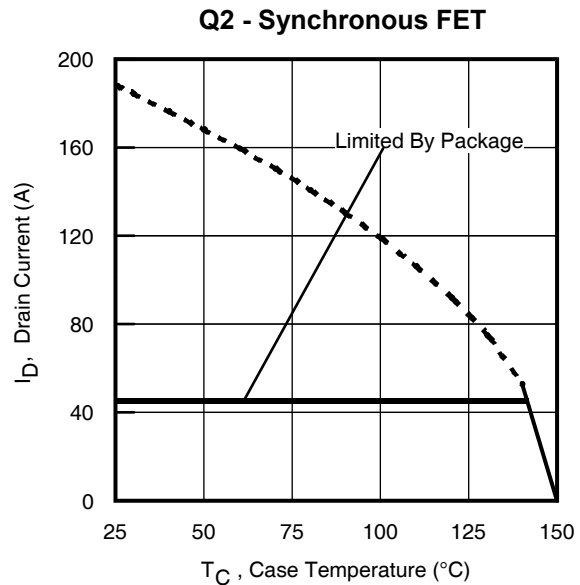
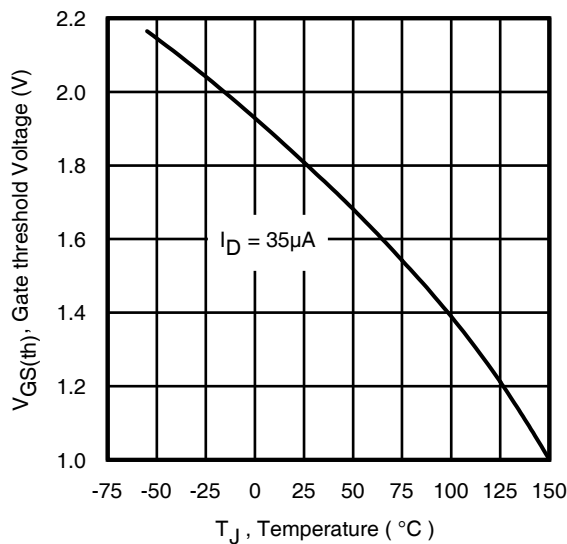
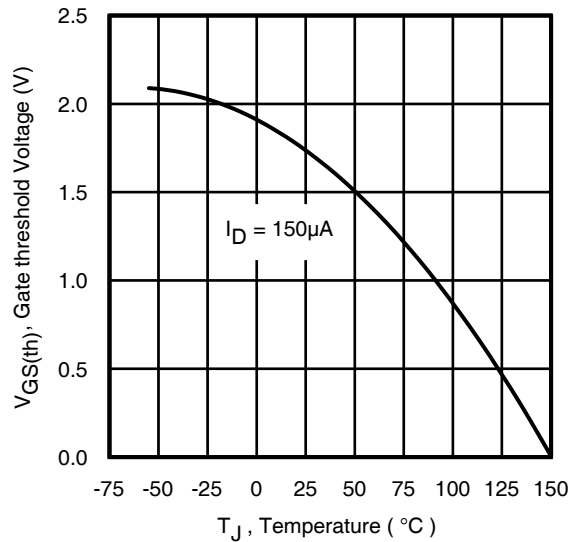
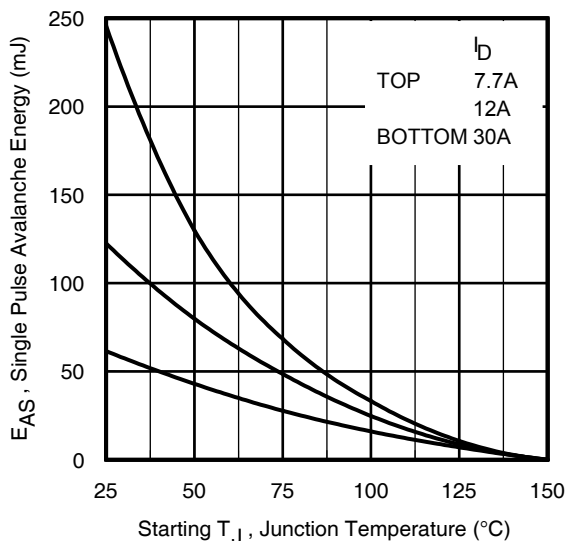
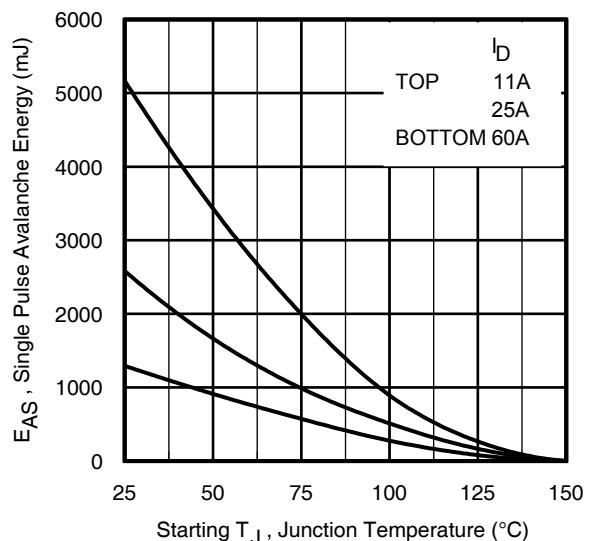
Diode Characteristics

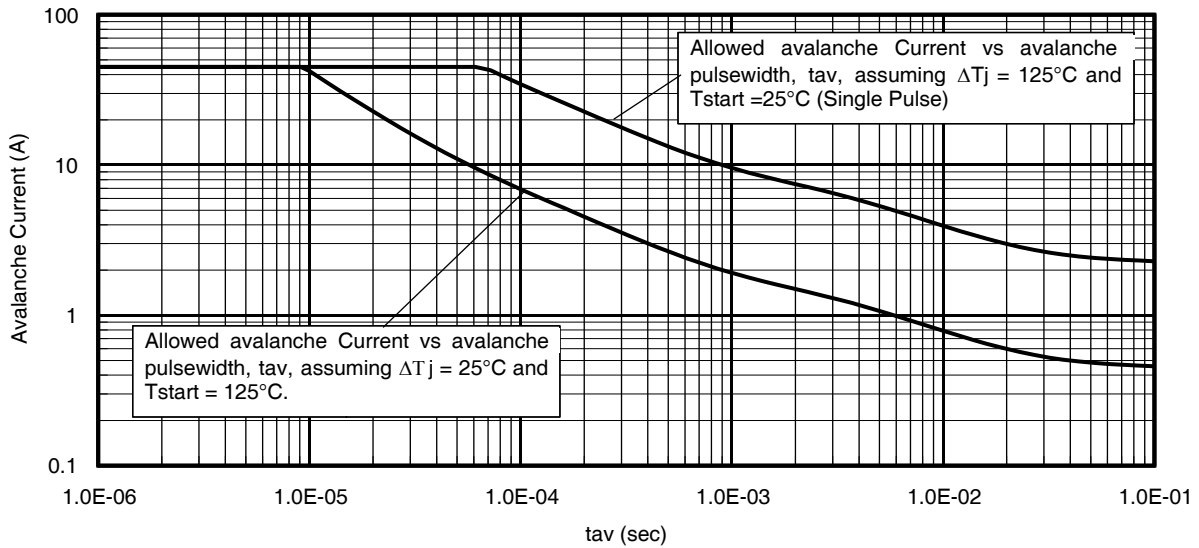
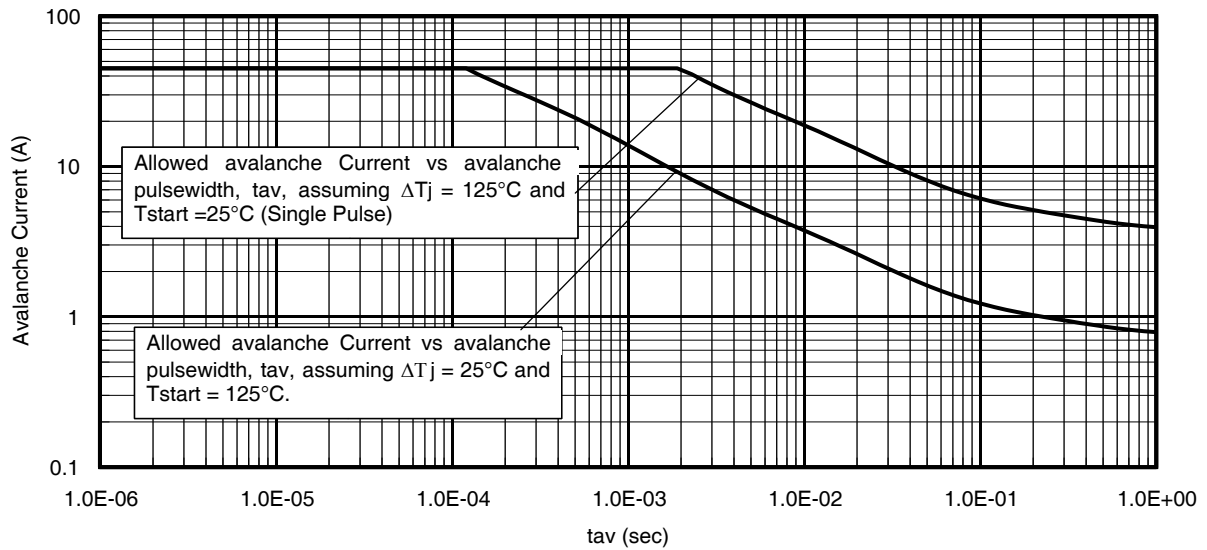
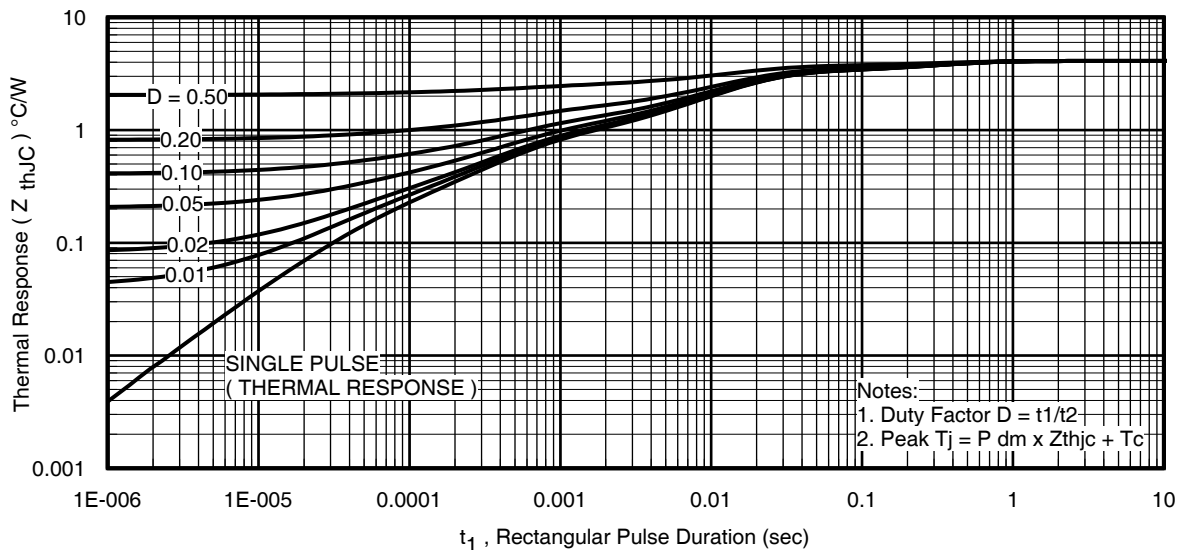
	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	Q1	—	—	45⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
		Q2	—	—	45⑦		
I_{SM}	Pulsed Source Current (Body Diode)	Q1	—	—	120	A	
		Q2	—	—	750⑧		
V_{SD}	Diode Forward Voltage	Q1	—	—	1.0	V	$T_J = 25^\circ\text{C}$, $I_S = 30\text{A}$, $V_{GS} = 0\text{V}$ ③
		Q2	—	—	0.75		$T_J = 25^\circ\text{C}$, $I_S = 30\text{A}$, $V_{GS} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	Q1	—	16	—	ns	$Q1$ $T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$ $V_{DD} = 13\text{V}$, $di/dt = 235\text{A}/\mu\text{s}$ ③
		Q2	—	36	—		
Q_{rr}	Reverse Recovery Charge	Q1	—	13	—	nC	$Q2$ $T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$ $V_{DD} = 13\text{V}$, $di/dt = 190\text{A}/\mu\text{s}$ ③
		Q2	—	67	—		


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Typical Transfer Characteristics


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 11. Maximum Safe Operating Area

Fig 12. Maximum Safe Operating Area


Fig 13. Normalized On-Resistance vs. Temperature

Fig 14. Normalized On-Resistance vs. Temperature

Fig 15. Typical Source-Drain Diode Forward Voltage

Fig 16. Typical Source-Drain Diode Forward Voltage

Fig 17. Typical On-Resistance vs. Gate Voltage

Fig 18. Typical On-Resistance vs. Gate Voltage


Fig 19. Maximum Drain Current vs. Case Temperature

Fig 20. Maximum Drain Current vs. Case Temperature

Fig 21. Threshold Voltage vs. Temperature

Fig 22. Threshold Voltage vs. Temperature

Fig 23. Maximum Avalanche Energy vs. Drain Current

Fig 24. Maximum Avalanche Energy vs. Drain Current


Fig 25. Max Avalanche Current vs. Pulse Width (Q1)

Fig 26. Max Avalanche Current vs. Pulse Width (Q2)

Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)

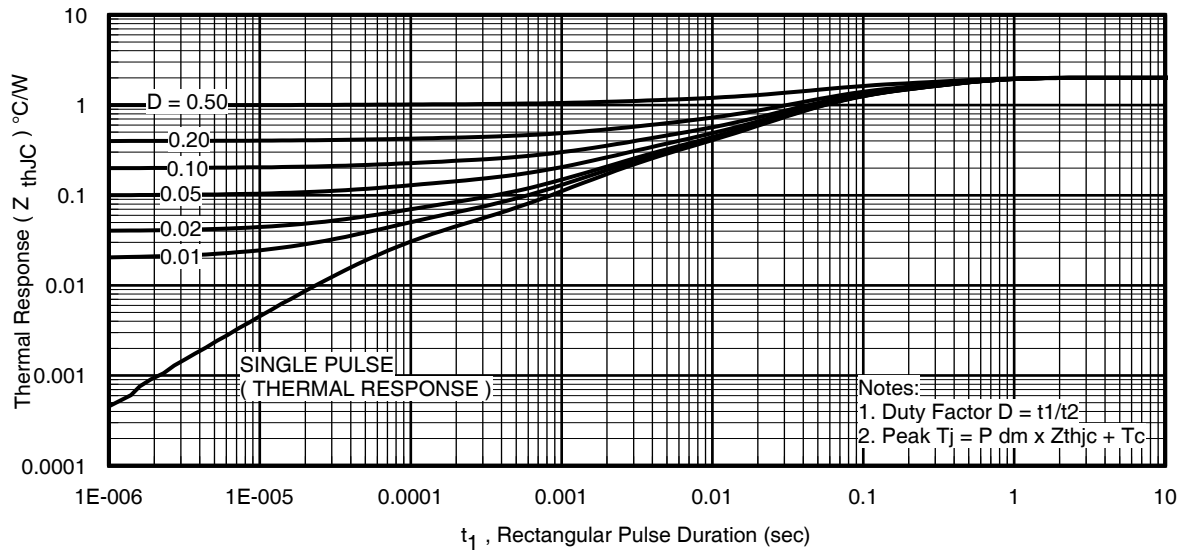
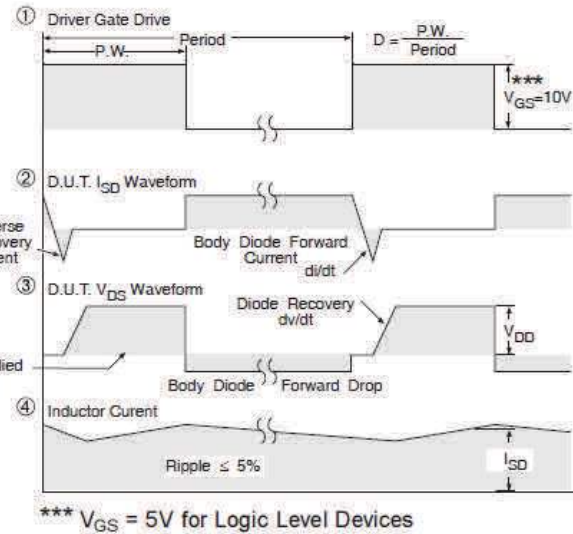
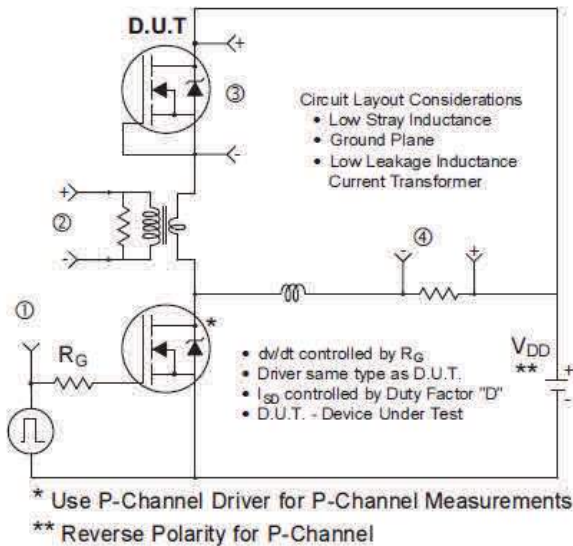
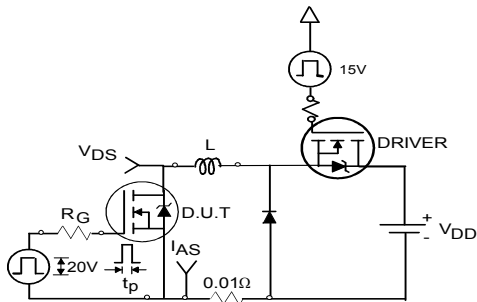
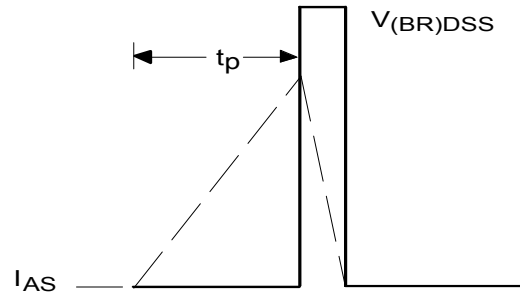
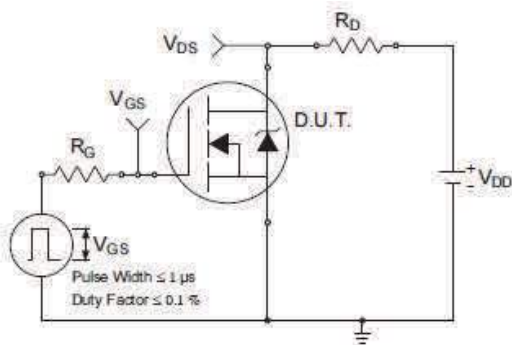
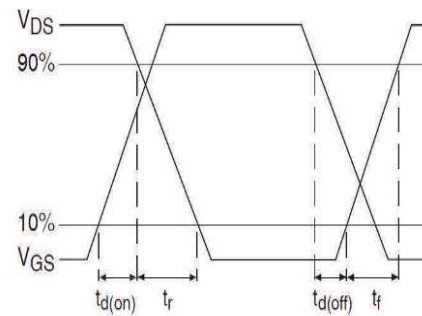
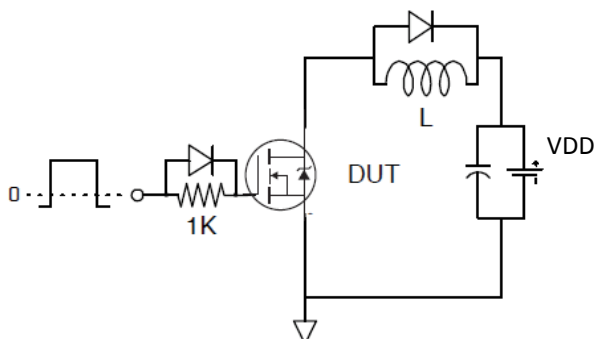
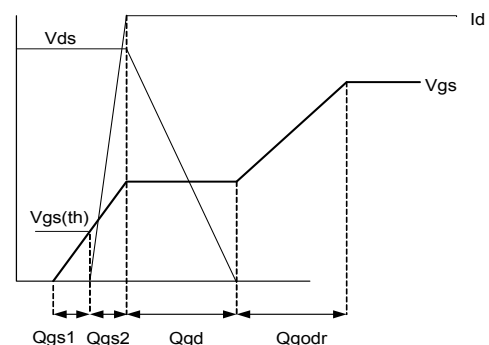
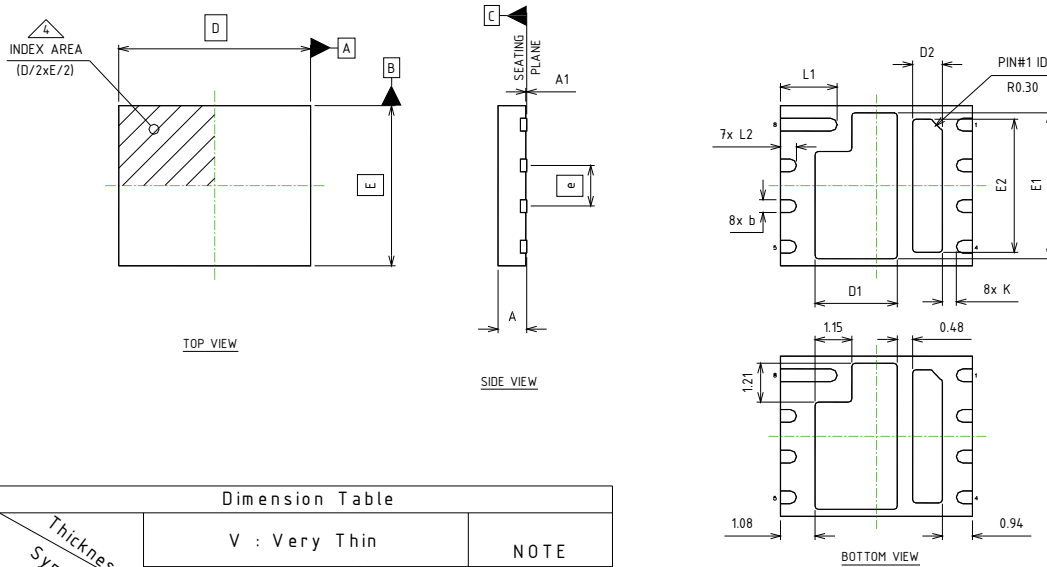


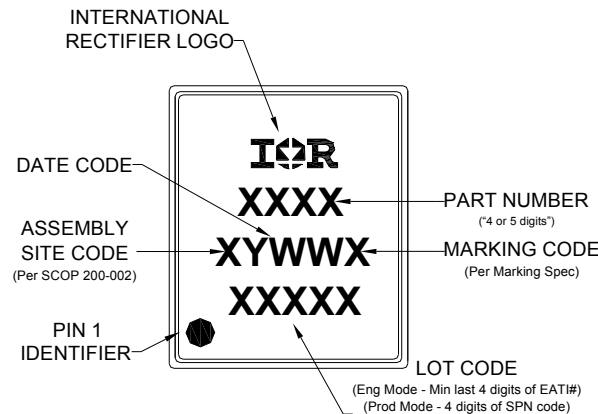
Fig 28. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)


Fig 29. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

Fig 30a. Unclamped Inductive Test Circuit

Fig 30b. Unclamped Inductive Waveforms

Fig 31a. Switching Time Test Circuit

Fig 31b. Switching Time Waveforms

Fig 32a. Gate Charge Test Circuit

Fig 32b. Gate Charge Waveform

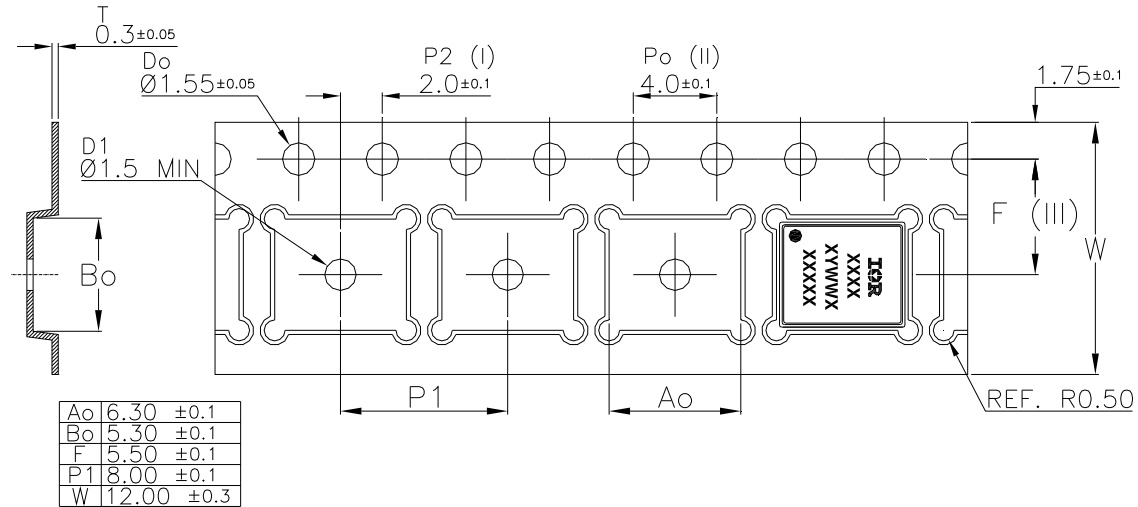
Dual PQFN 5x6 Outline "H" Package Details


Dimension Table				
Thickness Symbol	V : Very Thin			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.30	0.40	0.50	6
D	6.00 BSC			
E	5.00 BSC			
e	1.27 BSC			
D1	2.42	2.57	2.67	
E1	4.41	4.56	4.66	
D2	0.78	0.93	1.03	
E2	4.01	4.16	4.26	
K	0.20	---	---	
L1	1.67	1.77	1.87	
L2	0.40	0.50	0.60	

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>
 For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "H" Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Dual PQFN 5x6 Outline Tape and Reel


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information†

Qualification level	Industrial (per JEDEC JESD47F †† guidelines)	
Moisture Sensitivity Level	DUAL PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$,
Q1: $L = 0.14\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 30\text{A}$;
Q2: $L = 0.72\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 60\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to Q1 = 45A & Q2 = 45A by source bonding technology.
- ⑧ Pulsed drain current is limited to 180A by source bonding technology.

Revision History

Date	Comments
05/28/2013	<ul style="list-style-type: none"> • Updated the schematic drawing, on page 1. • Updated the Features and Benefits table, on page 1. • Updated Vsd for Q2 from 1.0V to 0.75V, on page 3. • Added Tape and Reel drawing, on page 12.
06/10/2013	<ul style="list-style-type: none"> • Updated the MSL level from MSL3 to MSL2, on pages 1 & 12.
08/15/2013	<ul style="list-style-type: none"> • Added “Fast/RFET™” above the part number, on page 1. • Added part marking drawing, on page 11.
01/16/2014	<ul style="list-style-type: none"> • Update the MSL level from MSL2 to MSL1, on page 1 & 12.
5/20/2014	<ul style="list-style-type: none"> • Updated fig. 25 to show the max avalanche plateau at 45A, on page 8. • Corrected fig. 26 to cap the curves at package limitation current of 45A, on page 8.

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