High Speed CMOS Bus Exchange Switches with Active Termination

QS3388

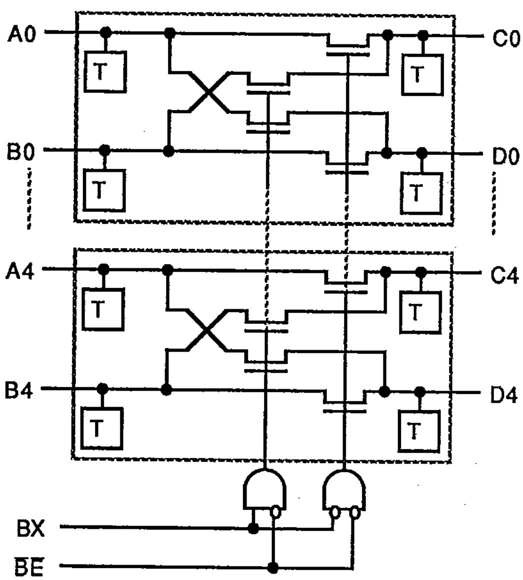
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Active termination drives bus pins to rails when off
- Zero propagation delay
- Undershoot Clamp diodes on all inputs
- Available in 24-pin DIP, ZIP, SOIC and QSOP
- Low power CMOS proprietary technology
- Bus exchange allows nibble swap
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels

DESCRIPTION

The QS3388 provides two sets of ten high-speed CMOS TTL compatible bus switches with active terminators on the bus switch I/O pins. The low on resistance (5Ω) of the 3388 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. When the switches are turned off, a low drive active terminator circuit drives the disconnected pins to Vcc or ground, away from the TTL threshold. This moves undriven buses from the threshold region to a TTL high or low, reducing system noise and power dissipation. The bus enable (BE) signal turns the switches on. The bus exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM

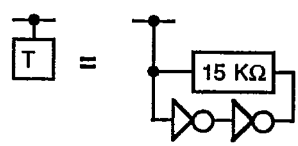


PIN DESCRIPTION

Name	I/O	Function
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

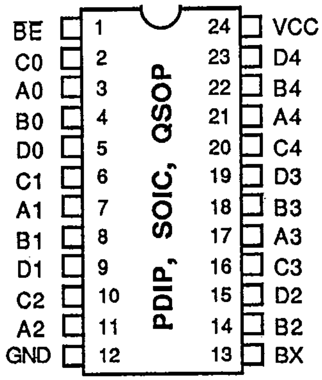
FUNCTION TABLE

$\overline{BE}$	BX	A0-4	B0-4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange



7

PIN CONFIGURATIONS



ALL PINS TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.............................. -0.5V to +7.0V
DC Switch Voltage V_S .... -0.5V to V_{CC} +0.5V
DC Input Voltage V_I .... -0.5V to V_{CC} +0.5V
AC Input Voltage (for a pulse width ≤20 ns).................... -3.0V
DC Input Diode Current with V_I<0.................................. -20 mA
DC Channel Current Max. sink current/pin.......................120 mA
Maximum Power Dissipation...................................... 0.5 watts
T_{STG} Storage Temperature................................ -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC		QSOP		PDIP		Unit
	Typ	Max	Typ	Max	Typ	Max	
Controls	3	4	3	4	4	5	pF
QuickSwitch Channels	7	8	7	8	8	9	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

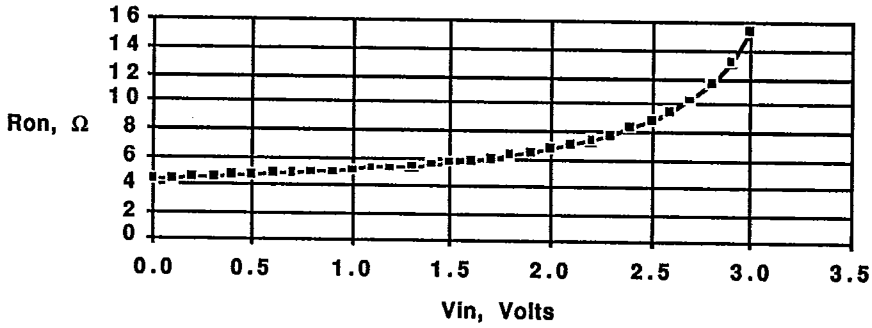
Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%   Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Paramete	Test	Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
|Iin|	Input Leakage Current	Vin = Vcc, 0V	-	-	5	µA
It	Input crnt., Disconnect	Vout = 0.5V, 4.5V ; Vcc=5V		33		µA
Rt	Terminator resistance(6,7)			15		KΩ
|Ios|	Short Circuit Current (2,6)	AB (CD) = 0V, CD (AB) = Vcc		300	-	mA
Vic	Clamp Diode Voltage	Vcc = Min, Iin = -18 mA	-	-0.7	-1.2	Volts
Ron	Switch On Resistance (3)	Vcc = Min, Vin = 0.0 Volts Ion = 30 mA	-	5	7	Ω
		Vcc = Min, Vin = 2.4 Volts Ion = 15 mA	-	10	15	Ω

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
3. Measured by voltage drop between AB and CD pins at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (Aor B, C or D) pins.
4. Each A-D pin has an active terminator. Each active terminator provides current to drive the pin high or low if the input is above or below the TTL threshold of approximately 1.4 volts, respectively. This current is provided by a resistor which is driven to Vcc or Ground, as shown in the block diagram. These terminators provide sufficient drive to overcome leakage currents and drive their corresponding pins away from the threshold region.
5. This parameter is tested at Vout=0.5V and guaranteed by design for Vout=4.5V for Vcc=5.0V.
6. Characterized, not tested.
7. Computed from parameter "It" and the test conditions.

7

On Resistance vs Vin @ 4.75 Vcc



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, Vi = GND or Vcc, f = 0	-	-	1.5	mA
ΔIcc	Pwr Supply Current, per Input High (2)	Vcc = MAX, Input = 3.4 V, f = 0 Per control input	-	-	2.5	mA
Qccd	Dynamic Pwr Supply Current per mHz (3)	Vcc = MAX, ABCD pins open, Control input toggling @ 50% duty cycle	-	-	0.25	mA/ mHz
Ic	Total Power Supply Current (4,5)	Vcc = MAX,ABCD pins at 0.0V, Control inputs toggling @ 50% duty cycle Vih = 3.4V, f clock = 10 mHz	-	-	9.0	mA

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V, control inputs only). A,B,C,D pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A,B,C,D inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
4. Calculated parameter
   Ic= I Quiescent + I Inputs+ I Dynamic
   Ic=Icc+ ΔIccDhNt+ Qccd (fiNi)
   Icc= Quiescent Current
   ΔIcc= Power Supply Current for each TTL High input (Vi=3.4V, control inputs only)
   Dh= Duty Cycle for each TTL input that is High (control inputs only).
   Nt= Number of TTL inputs that are at DH (control inputs only).
   fi= frequency that the inputs are toggled (control inputs only).
5. Note that activity on A,B,C,D inputs do not contribute to Ic if A,B,C,D inputs are between gnd and Vcc. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, Ic will be equal to Icc only regardless of activity on the A and B pins.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%   Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t PLH t PHL	Data Propagation Delay AiBi to CiDi, CiDi to AiBi	3,2		0.25		0.25	ns
t PZH t PZL	Switch Turn On Delay BE to Ai, Bi, Ci, Di		1.5	6.5	1.5	7.5	ns
t PLZ t PHZ	Switch Turn Off Delay BE to Ai, Bi, Ci, Di	2	1.5	5.5	1.5	6.5	ns
t BX	Switch Multiplex Delay BX to Ai, Bi, Ci, Di		1.5	6.5	1.5	7.5	ns
| Qci |	Charge Injection, Typical	4,2		1.5		1.5	pC
| Qdci |	Differential Charge Injection, Typical	5,2		<.5		<.5	pC

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pf load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
5) Measured at switch turn off through bus multiplex, A to C => A to D, B connected to C, load = 50 pF in parallel with 10 meg ohm scope probe, Vin at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.