Inventek Systems

ISM20736S
Embedded
Bluetooth Low Energy SIP Module

Data Sheet

Table of Contents

1 General Description

The Inventek ISM20736S module is an embedded wireless Bluetooth low energy (BLE) connectivity device, based on the Broadcom BCM20736 BLE with integrated M3 Cortex processor SoC chip, RF antenna, matching and decoupling network, and 512 Kb EEPROM. The module provides a number of features and standard peripheral interfaces (see "Summary of Key Features" below), enabling connection to an embedded design. It supports BLE baseband, stack, and several fully qualified profiles embedded in ROM (see "Typical Applications" below), and the option of loading additional profiles into RAM. The ISM20736S adds wireless charging, simultaneous central and peripheral operation. The low cost, small foot print (6.5 mm x 6.5 mm x 1.2 LGA 48 pin package and ease of design-in make it ideal for a range of embedded applications.

Summary of Key Features:

- Bluetooth low energy (BLE)-compliant
- Supports Adaptive Frequency Hopping
- Excellent receiver sensitivity
- On-chip support for 3.0 Bluetooth HCI (H5) and peripheral UARTs
- On-chip support for Serial Peripheral Interfaces (master and slave modes SPI)
- Integrated ARM Cortex-M3 based microprocessor core
- RoHS compliant

Typical Applications:

The module has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4GHz unlicensed industrial, scientific, and medical (ISM) band. The following application profiles are supported in ROM:

- Battery Status
- Blood Pressure Monitor
- Find Me
- Heart Rate Monitor
- Proximity
- Thermometer
- Weight Scale
- Time

Additional profiles that can be supported from RAM include:

- Blood Glucose Monitor
- Temperature Alarm
- Location

2 PART NUMBER DETAIL DESCRIPTION

2.1 Ordering Information

Part Number	Description
ISM20736S	Bluetooth LE Module

3 General Features

- Based on the Broadcom BCM20736 Bluetooth Low Energy 4.0 (WICED SMART™) Baseband/Radio device.
- Integrates Bluetooth SMART embedded stack, and fully qualified application profiles in ROM
- CPU ARM Cortex™-M3 32-bit RISC core.
- Inputs +3.93 V tolerant
- The devices operate from 1.62-3.63 V power supply.
- Power-saving mode allows the design of low-power applications.
- Lead Free Design which is compliant with ROHS requirements.
- FCC/CE Compliance Certified

3.1 Limitations

Inventek Systems products are not authorized for use in safety-critical applications (such as life support) where a failure of the Inventek Systems product would reasonably be expected to cause severe personal injury or death.

3.2 Regulatory Compliance

FCC CE

FCC ID: QDS-BRCM1078
Canada IC: 4324A-BRCM1078
Taiwan NCC ID: CCAF13LP1890T1
Europe (EU) R&TTECE Mark Modular approval.
Japan MIC (RF) ID: 007-AB0221 Modular approval.
LMA (Limited Modular Approval) in a specific host.

There are specific regulatory requirements imposed by regulatory authorities around the world on radio devices. Customers using Broadcom SIP modules are advised to engage with an accredited test lab to determine the overall system level regulatory requirements. Customers may be able to leverage Broadcom's regulatory test reports. Please discuss the process with your test lab, such as FCC ID transfers. Broadcom can provide authorizations as needed

4 Complementary Documents

4.1 Inventek Systems

- FCC Test Report

5 Specifications

5.1 Module Architecture

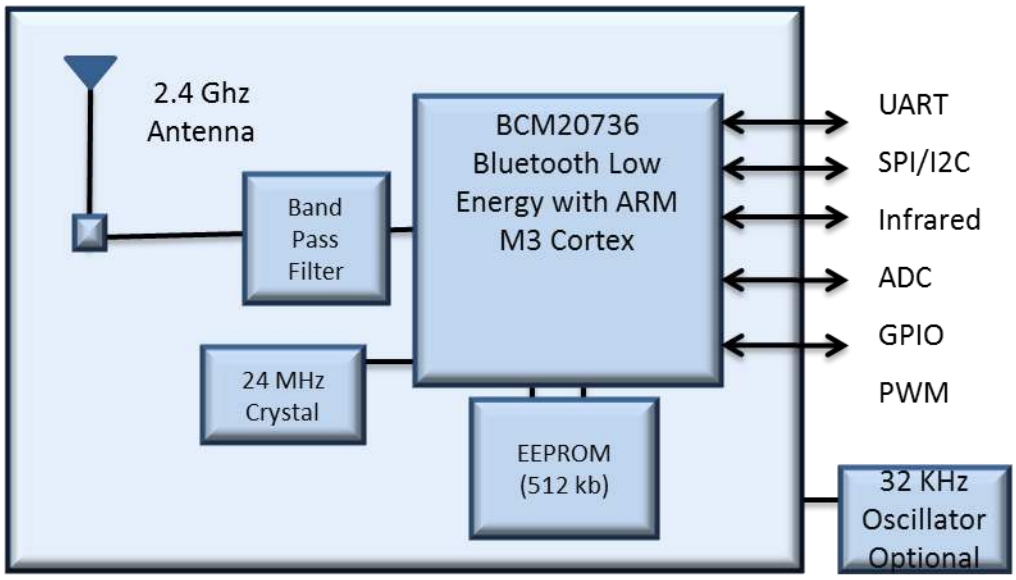


Figure 1 Inventek's ISM20736S Block Diagram

6 Environmental Specifications

Item	Description
Operating Temperature Range	-40 deg. C to +85 deg. C
Storage Temperature Range	-40 deg. C to +125 deg. C
Humidity	95% max non-condensing

7 Hardware Electrical Specifications

7.1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Supply Power	Input Supply Voltage		3.63	V
Voltage Ripple		0	+/-2%	
Vbat		1.62	3.63	V

7.2 Recommended Operating Ratings

Symbol	Min	Typ	Max	Unit
VBAT	1.62	-	3.63	V

7.3 ADC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Number of input channels	-	-	-	9	-	-
Channel switching rate	f_{ch}	-	-	-	133.33	Kch/s
Input Signal range	V_{inp}	-	0	-	3.63	V
Reference settling time	-	Changing refsel	7.5	-	-	us
Input resistance	R_{inp}	Effective, single ended	-	500	-	KΩ
Input capacitance	C_{inp}	-	-	-	5	pF
Conversion rate	f_C	-	5.859	-	187	KHz
Conversion time	T_C	-	5.35	-	170.7	us
Resolution	R	-	-	16	-	bits
Effective number of bits	-	In specified performance range	See section	-	-	-

			9.5			
Absolute voltage measurement error	-	Using on-chip firmware driver	-	±2	-	%
Current	I	$I_{avdd1p2}+I_{avdd3p3}$	-	-	1	mA
Power	P	-	-	1.5	-	mW
Leakage Current	$I_{leakage}$	T=25	-	-	100	nA
Power-up time	$T_{powerup}$	-	-	-	200	us
Integral nonlinearity	INL	In guaranteed performance ranges	-1	-	1	LSB[a]
Differential nonlinearity	DINL	In guaranteed performance ranges	-1	-	1	LSB[a]

[a]. LSBs are expressed at 10 bit level.

8 Power Consumption

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core. There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the ISM20736 runs on the Low Power Oscillator and wakes up after a predefined time period.
- The following power modes are supported:
  - Active mode
  - Idle mode
  - Sleep mode
  - HIDOFF (Deep Sleep) mode

In HIDOFF (Deep Sleep) mode, the ISM20736 baseband and core are powered off -- this mode minimizes chip power consumption and is intended for long periods of inactivity.

8.1.1 Estimated Power Consumption

Operational Mode	Description	Typ.	Max.	Unit
Receive	Receiver and baseband are both operating, 100% — ON	24	28	mA
Transmit	Transmitter and baseband are both operating	24	28	mA
Sleep	Internal LPO is in use	55	60	uA
HIDOFF (DeepSleep)	-	2	2.5	uA

9 Module Pin Out

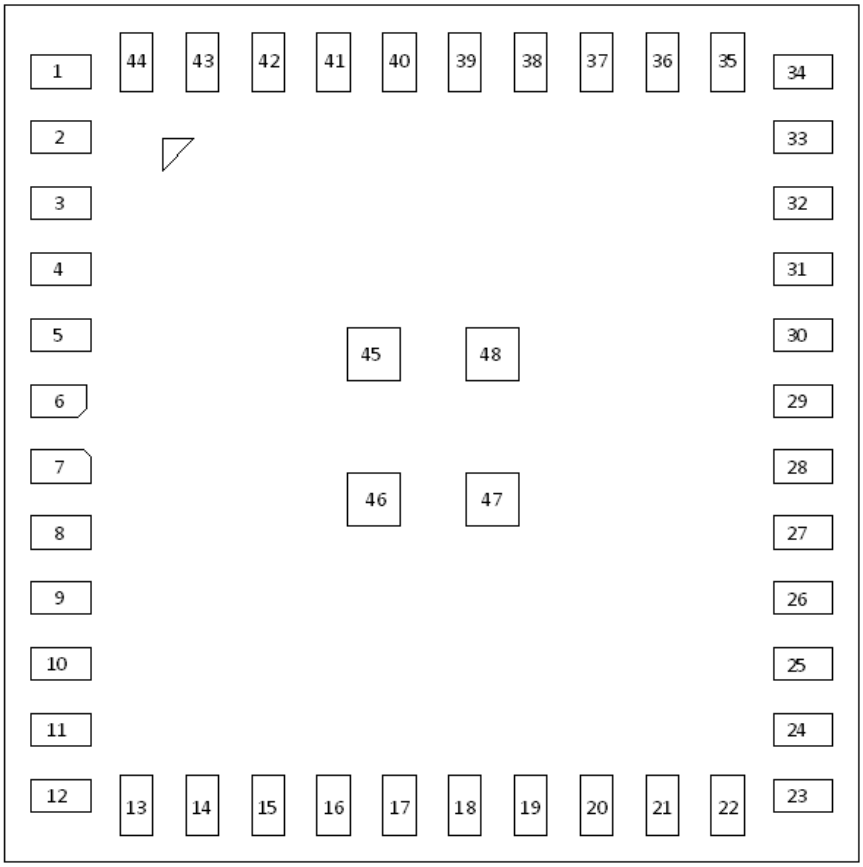


Figure 2 Pin Mapping

9.1 Detailed Pin Description

Pin #	Pin Name	I/O Type	Description
1	GPIO: P27 PWM1	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- SPI_2: MOSI (master and slave) Current: 16 mA
2	GND	GND	GND
3	VBAT	I	Battery Supply Input.
4	GND	GND	GND
5	GND	GND	GND
6	GND	GND	GND
7	GND	GND	GND
8	GND	GND	GND
9	GND	GND	GND
10	NC	-	NC – Leave Floating
11	GND	GND	GND
12	GND	GND	GND
13	GND	GND	GND
14	GND	GND	GND
15	GND	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	UART_RX	I	UART_RX, this pin has been pulled down via 10K ohm inside module.
19	UART_TX	O PU	UART_TX
20	GND	GND	GND
21	SCL	I/O PU	Clock signal for an external I2C device
22	SDA	I/O PU	Data signal for an external I2C device
23	GND	GND	GND

Pin #	Pin Name	I/O Type	Description
24	GND	GND	GND
25	GPIO: P1	I	Default Direction: Input This pin was tied to WP pin of internal EEPROM inside module. After POR State: Input Floating Tied to WP of internal EEPROM, External 10K pullup required
26	TMC	I	Test mode control High: test mode Let it floating if not used. This Pin was connected to GND via 10K internally.
27	RESET_N	I/O PU	Active-low system reset with open-drain output
28	GPIO: P0	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- Peripheral UART: puart_tx 3- SPI_2: MOSI (master and slave) 4- IR_RX 5- 60Hz_main
29	GND	GND	GND

Pin #	Pin Name	I/O Type	Description
30	GPIO: P3	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- Peripheral UART: puart_cts 2- SPI_2: SPI_CLK (master and slave)
31	GPIO: P2	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- Peripheral UART: puart_rx 2- SPI_2: SPI_CS (slave only) 3- SPI_2: SPI_MOSI (master only)
32	GPIO: P4	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- Peripheral UART: puart_rx 2- SPI_2: MOSI (master and slave) 3- IR_TX
33	GPIO: P8	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input
34	GPIO: P33	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- SPI_2: MOSI (slave only) 3- Auxiliary clock output: ACLK1 4- Peripheral UART: puart_rx

Pin #	Pin Name	I/O Type	Description
35	GPIO: P32	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- SPI_2: SPI_CS (slave only) 3- Auxiliary clock output: ACLK0 4- Peripheral UART: puart_tx
36	GPIO: P25	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- SPI_2: MISO (master and slave) 2- Peripheral UART: puart_rx
37	GPIO: P24	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- SPI_2: SPI_CLK (master and slave) 2- Peripheral UART: puart_tx
38	GND	GND	GND
39	GPIO: P13 PWM3	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input
	GPIO: P28 PWM2	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- LED1 3- IR_TX Current: 16mA

Pin #	Pin Name	I/O Type	Description
40	GPIO: P14 PWM2	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input
	GPIO: P38	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- SPI_2: MOSI (master and slave) 3- IR_TX
41	GPIO: P15	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- IR_RX 3- 60 Hz_main
42	GPIO: P26 PWM0	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- SPI_2: SPI_CS (slave only) Current: 16 mA
43	GPIO: P12	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- XTALO32K
	XTALO32K	O	Low-power oscillator (LPO) output. Alternative Function: • P12 • P26

	Pin Name	I/O Type	Description
44	GPIO: P11	I	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- XTALI32K
	XTALI32K	I	Low-power oscillator (LPO) input is used. Alternative Function: • P11 • P27
45	GND	GND	GND
46	GND	GND	GND
47	GND	GND	GND
48	GND	GND	GND

Note:
When pin 43 (XTALO32K) is used, ADC/GPIO:P12 is unavailable. P26 may still be available.
When pin 44 (XTALI32K) is used, ADC/GPIO:P11 is unavailable. P27 may still be available

10 AC Characteristics

10.1.1 UART Timing Specifications

Characteristics	Min	Max	Unit
Delay time, UART_CTS_N low to UART_TXD valid	-	24	Baud out cycles
Setup time, UARTS_CTS_N high before midpoint of stop bit	-	10	ns
Delay time, midpoint of stop bit to UART_RTS_N high	-	2	Baud out cycles

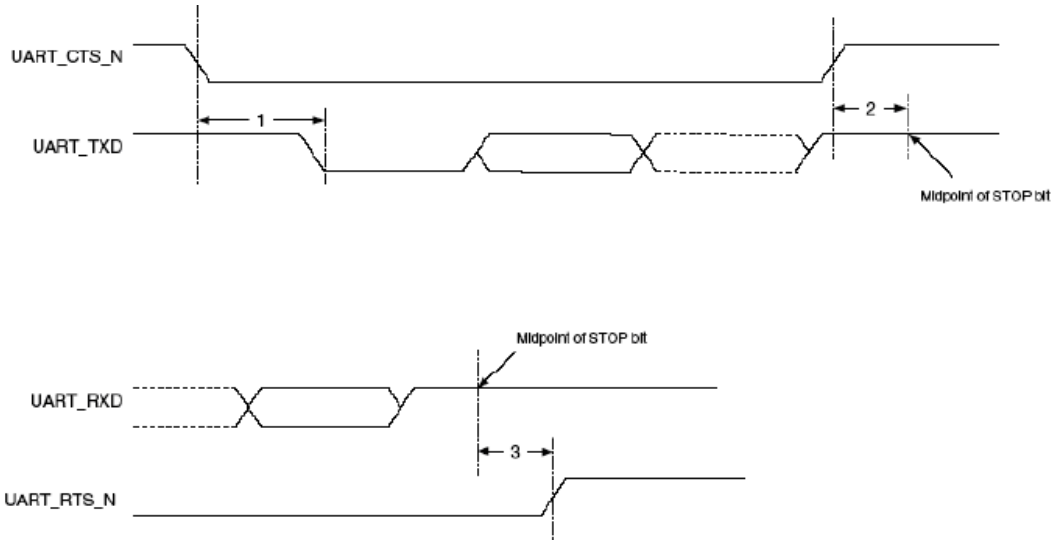


Figure 2 : UART Timing

10.1.2 SPI Timing Specifications

The SPI interface supports clock speeds up to 12 MHz with VDDIO > 2.2V. The supported clock speed is 6 MHz when 2.2V > VDDIO > 1.62V.

Reference	Characteristics	Min	Typ	Max
1	Time from CSN assert to first clock edge	1 SCK	100	∞
2	Master setup time	-	½ SCK	-
3	Master hold time	½ SCK	-	-
4	Slave setup time	-	½ SCK	-
5	Slave hold time	½ SCK	-	-
6	Time from last clock edge to CSN deasserted	SCK	10	100

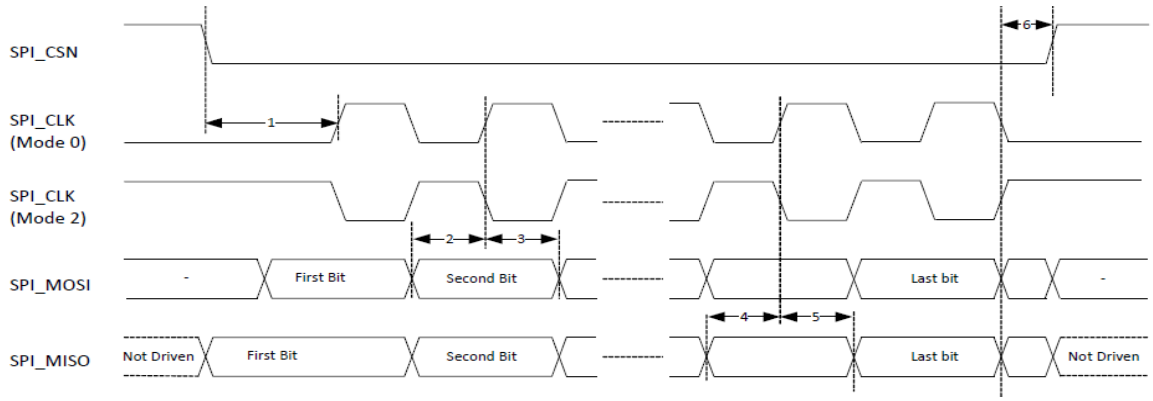


Figure 3: SPI Timing – Mode 0 and 2

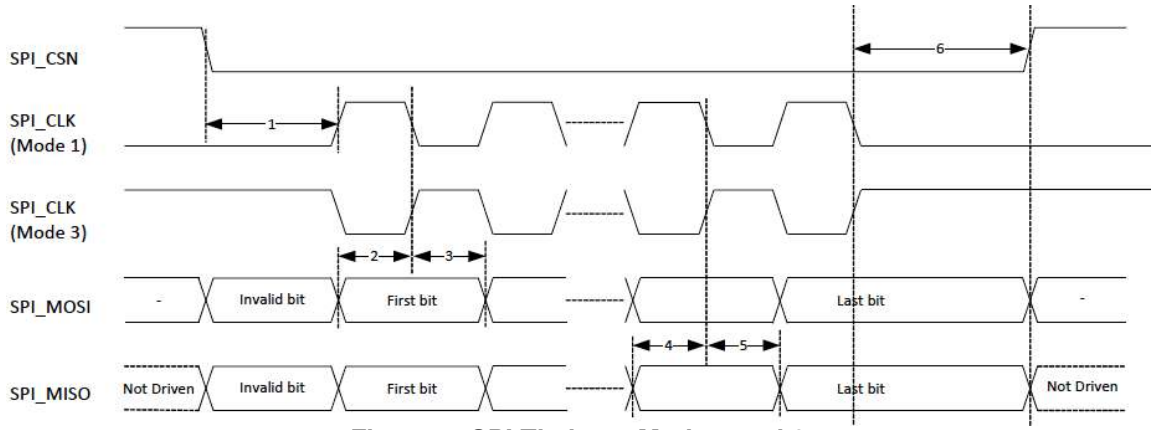


Figure 4: SPI Timing – Mode 1 and 3

10.1.3 BSC Interface Timing

Reference	Characteristics	Min	Max	Unit
1	Clock Frequency	-	100/400/800/1000	KHz
2	START condition setup time	650	-	ns
3	START condition hold time	280	-	ns
4	Clock low time	650	-	ns
5	Clock high time	380	-	ns
6	Data input hold time [a]	0	-	ns
7	Data input setup time	100	-	ns
8	STOP condition setup time	280	-	ns
9	Output valid from clock	-	400	ns
10	Bus free time [b]	650	-	ns

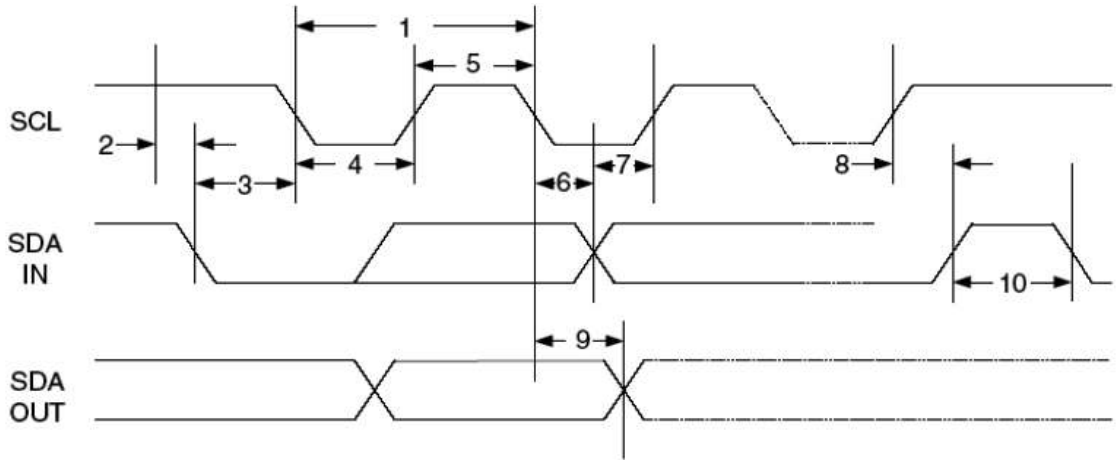


Figure 3 : BSC Interface Timing

11 INTERFACES

11.1 SPI (Serial Peripheral Interface)

The BCM20736 has one independent SPI interface. Each interface has a 16-byte transmit buffer and a 16-byte receive buffer. To support more flexibility for user applications, the BCM20736 has optional I/O ports that can be configured individually and separately for each functional pin, as shown in tables below. The BCM20736 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The BCM20736 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.

11.2 UART

The UART is a standard 2-wire interface (RX and TX) and has adjustable baud rates from 9600 bps to 1 Mbps. The baud rate can be selected via a vendor-specific UART HCI command. The interface supports the Bluetooth 3.0 UART HCI (H5) specification. The default baud rate for H5 is 115.2 Kbaud.

Both high and low baud rates can be supported by running the UART clock at 24 MHz. The ISM20736 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

11.3 I2C

The BCM20736 provides a 2-pin master BSC interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with 12C slave devices. The BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices. The following transfer clock rates are supported by the BSC:

- 100kHz
- 400kHz
- 800 kHz (Not a standard I2C-compatible speed.)
- 1 MHz (Compatibility with high-speed 12C-compatible devices is not guaranteed.)
  The following transfer types are supported by the BSC:
- Read (Up to 16 bytes can be read.)
- Write (Up to 16 bytes can be written.)
- Read-then-Write (Up to 16 bytes can be read and up to 16 bytes can be written.)
- Write-then-Read (Up to 16 bytes can be written and up to 16 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the BCM20736 are required on both the SCL and SDA pins for proper operation.

11.4 GPIO

The ISM20736 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-up and pull-down resistors, and all support a 2 mA drive strength except P26, P27, and P28, which provide a 16 mA drive strength at 3.3V supply.

11.5 ADC

The ISM20736 contains a 16-bit ADC (effective number of bits is 10).
The conversion time is 10 us. There is a built-in reference with supply- or bandgap-based reference modes. The maximum conversion rate is 187 kHz. There is a rail-to-rail input swing.

The ADC input range (V_{inp}) is selectable by firmware control:
- When an input range of 0—3.6V is used, the input impedance is 3 MO.
- When an input range of 0—2.4V is used, the input impedance is 1.84 MO.
- When an input range of 0—1.2V is used, the input impedance is 680 KO.

Mode	ENOB (Typical)	Maximum Sampling Rate (KHz)	Latency (us) [a]
0	13	5.859	171
1	12.6	11.7	85
2	12	46.875	21
3	11.5	93.75	11
4	10	187	5

[a]. Settling time after switching channels.

11.6 PWM

The ISM20736 has internal PWM channels. The following GPIOs can be mapped as PWMs:
- P26
- P14/P28 (Dual bonded, only one of two is available.)
- P13

Each of the PWM channels, PWMO-3, contains the following registers:
- 10-bit initial value register (read/write)
- 10-bit toggle register (read/write)
- 10-bit PWM counter value register (read)

The PWM configuration register is shared among PWMO-3 (read/write). This 12-bit register is used:

- To configure each PWM channel.
- To select the clock of each PWM channel.
- To change the phase of each PWM channel.

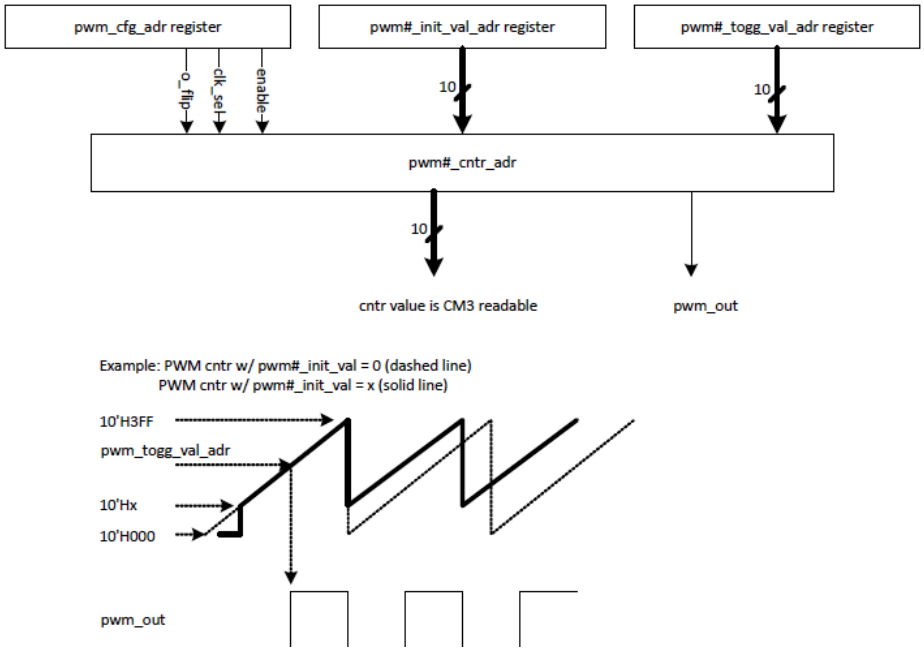


Figure 3: Structure of one PWM channel

11.7 32.768 kHz Oscillator

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Frequency	F_{oscout}	-	-	32.768	-	KHz
Frequency tolerance	-	Crystal dependent	-	100	-	ppm
Start-up time	$T_{startup}$	-	-	-	500	ms
XTAL drive leve	P_{drv}	For crystal selection	0.5	-	-	uW
XTAL series resistance	R_{series}	For crystal selection	-	-	70	KΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	-	-	1.3	pF

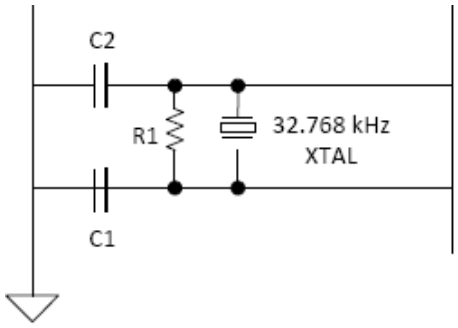


Figure 4: 32 KHz Oscillator Block Diagram

It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 KHz or 32.768 KHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1= 10 MΩ, C1=C2=~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

12 External Reset

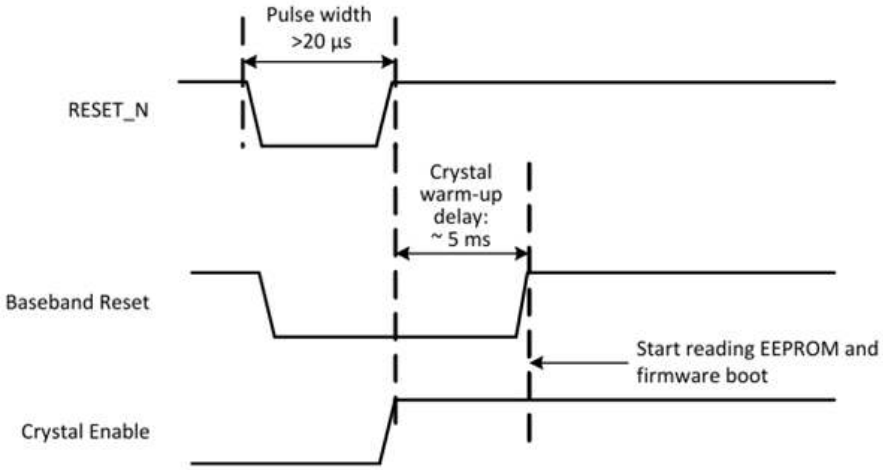


Figure 5: External Reset Timing

13 Bluetooth Low energy Specifications

The ISM20736 Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high performance Bluetooth operation, including:

- Data de-/framing, de-/whitening, HEC, FEC, CRC
- Link key generation
- Independently handles HCI events
- Frequency hopping generator
- E0 encryption
- Link control layer
- Adaptive frequency hopping
- Test mode

The ISM20736 integrated radio transceiver is optimized for operation in 2.4GHz ISM band, and fully meets or exceeds Bluetooth Radio Specification 4.0. It consists of:

- Transmitter
- Digital modulator
- Power Amplifier (PA) that can transmit up to 4 dBm for class 2 operation
- Receiver, featuring extended dynamic range and high-order on-chip filtering
- Digital demodulator and bit synchronizer
- Receiver signal strength indicator
- Local oscillator with internal loop filter, that provides fast frequency hopping (1600 hops/second) across 79 maximum available channels
- Automatic calibration scheme, activating during hop settling and normal operation to compensate for temperature, gain, phase, transceiver analog parts characteristics and process variations
- Internal LDO regulator that provides power to the digital and RF circuits

13.1 Receiver RF Specifications

Parameter	Mode and Conditions	Min	Typ	Max	Unit
Receiver Section [a]					
Frequency Range	-	2402	-	2480	MHz
RX sensitivity (standard)	0.1% BER, 1Mbps	-	-94	-	dBm
Maximum input	-	-10	-	-	dBm
Measurements @ 3V					

[a]. 30.8% PER.
[b]. Desired signal is 3 dB above the reference sensitivity level (defined as -70 dBm).
[c]. Measurement resolution is 10 MHz.
[d]. Measurement resolution is 3 MHz.
[e]. Measurement resolution is 25 MHz.

13.2 Transmitter RF Specifications

Parameter	Min	Typ	Max	Unit
Transmitter Section				
Frequency range	2402	-	2480	MHz
Output power adjustment range	-20	-	4	dBm
Default output power	-	2.0	-	dBm
Output power variation	-	2.5	-	dB
Initial carrier frequency tolerance	-	-	±150	KHz
Frequency Drift				
Frequency drift	-	-	±50	KHz
Drift rate	-	-	20	KHz/50 us
Frequency deviation				
Average deviation in payload (sequence used is 00001111)	225	-	275	KHz
Maximum deviation in payload (sequence used is 10101010)	185	-	-	KHz
Channel spacing	-	2	-	MHz

14 ON BOARD PROCESSOR

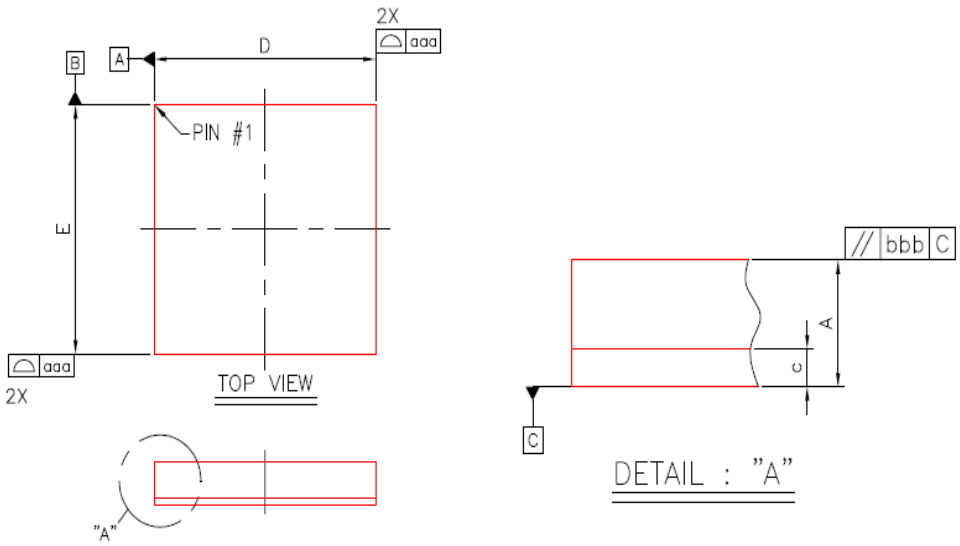
The ISM20736 microprocessor unit executes software from the link control (LC) layer up to the application layer components. The microprocessor is based on an ARM Cortex M3, 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The unit has 320 KB of ROM for program storage and boot-up, 60 KB of RAM for scratch-pad data, and patch RAM code. The internal boot ROM provides power-on reset flexibility, which enables the same device to be used in different HID applications with an external serial EEPROM or with an external serial flash memory. At power-up, the lowest layer of the protocol stack is executed from the internal ROM memory. External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device can also support the integration of user applications.

14.1 EEPROM Interface

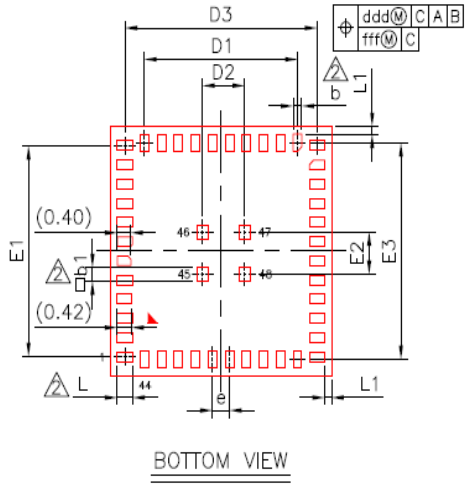
The ISM20736 provides a Broadcom Serial Control (BSC) master interface. The BSC is programmed by the CPU to generate four types of BSC bus transfers: read-only, write-only, combined read/write, and combined write / read. BSC supports both low-speed and fast mode devices. The BSC is compatible with a Philips 12C slave device, except that master arbitration (multiple I2C masters contending for the bus) is not supported. The EEPROM can contain customer application configuration information including: application code, configuration data, patches, pairing information, BD_ADDR, baud rate, SDP service record, and file system information used for code.

15 Mechanical Specification

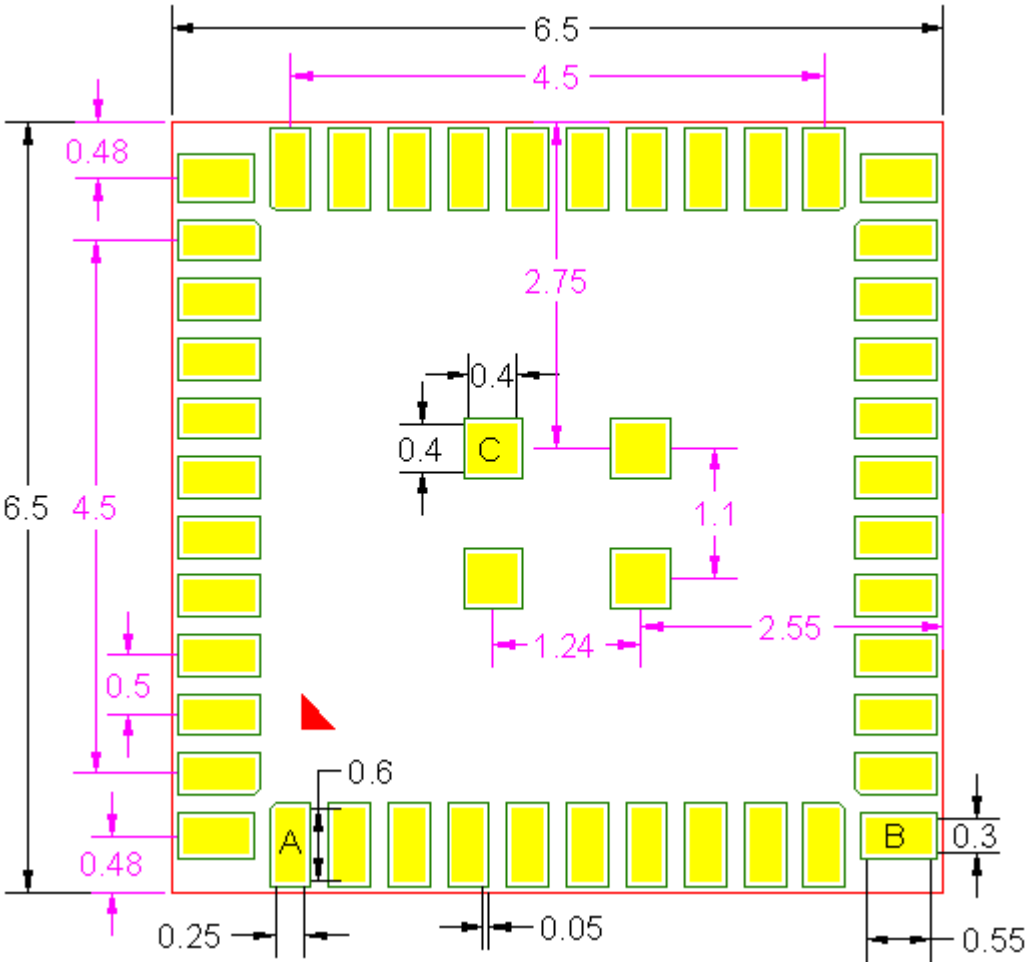
The Physical dimensions of the module are as follow:
6.5 x 6.5 x 1.18 mm (Tolerance +/- 0.1mm)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.18	---	---	0.046
c	0.17	0.20	0.23	0.007	0.008	0.009
D/E	6.40	6.50	6.60	0.252	0.256	0.260
D1	---	4.50	---	---	0.177	---
E1	---	5.50	---	---	0.217	---
D2	---	1.24	---	---	0.049	---
E2	---	1.10	---	---	0.043	---
D3/E3	---	5.65	---	---	0.222	---
e	---	0.50	---	---	0.020	---
b	---	0.25	---	---	0.010	---
L	---	0.45	---	---	0.018	---
b1	---	0.35	---	---	0.014	---
L1	---	0.20	---	---	0.008	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	



16 ISM20736S Footprint



Note:

1. Please use Un-Solder Mask to design the Module Footprint.
2. There are two types pad size in the Module.
   - Type A:
     Pad size: 0.6 x 0.25 mm & Solder Mask Opening: 0.7 x 0.35mm
   - Type B
     Pad size: 0.55 x 0.3mm & Solder Mask Opening: 0.65 x 0.4mm
   - Type C:
     Pad size: 0.4 x 0.4mm & Solder Mask Opening: 0.5 x 0.5 mm

17 Recommend Stencil

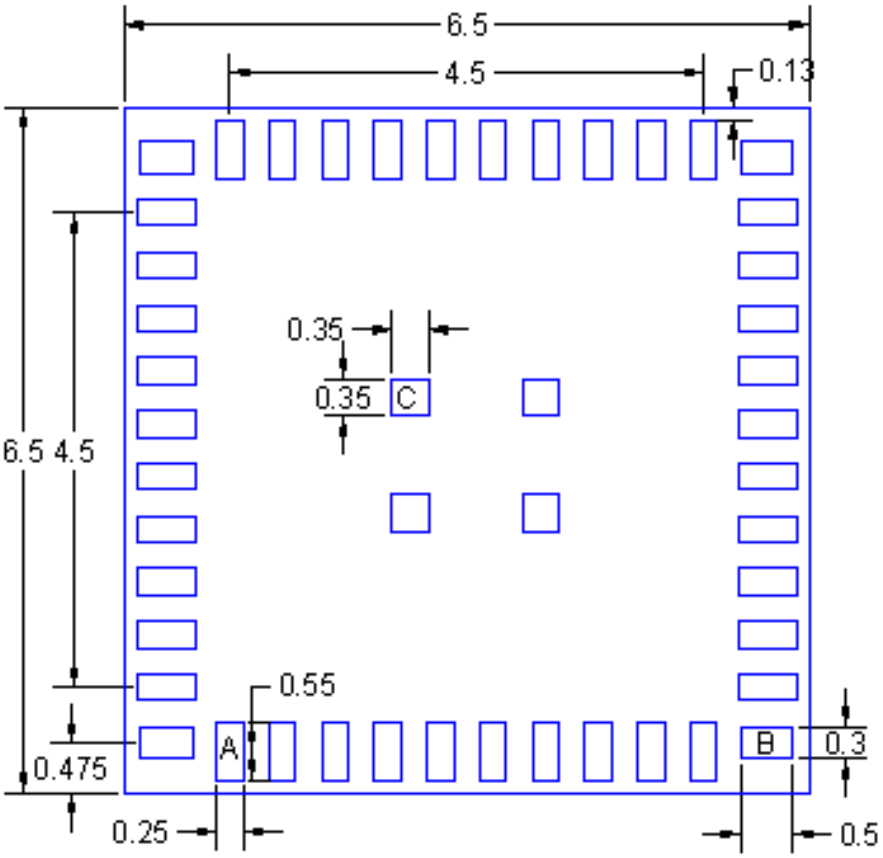


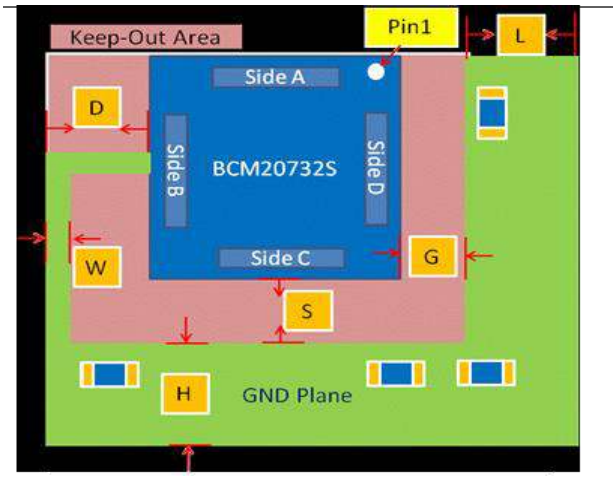
Figure 4: Bottom View

18 PCB Layout Recommendations

The following layout recommendations

- Connect to system ground from side B of the module (pins 13–22).
- An L-shaped ground plane is required for the embedded BLE antenna. Keep the GND continuous. Do not cut off the GND shape to accommodate trace routes.
- If the L-shaped GND plane is located on the top layer of the PCB, do not place components on the ground plane. If this cannot be avoided, move the L-shaped ground plane to another layer.
- Antenna efficiency of 31–41% can be achieved based on the layout and the dimensions listed below. Following these layout recommendations is expected to yield 50+ meters of usable range; deviating from these recommendations may reduce the range of the antenna.
  - D: 4.5 mm (typical)
  - G, H, S: 3 mm (typical)
  - L: 3 mm (minimum)
  - W: 0.4 mm (typical)

- Route signal traces out of the module from side C (between pins 27 and 30) or side B (between pins 16 and 19) of the module. Traces can be overlapped to avoid routing through the keep-out area.
- Do not route traces from side A or side D.



Side A indicates the side of Pin #1 - Pin #12 of the ISM20736S.

- Side B indicates the side of Pin #13 - Pin #22 of the ISM20736S.
- Side C indicates the side of Pin #23 - Pin #34 of the ISM20736S.
- Side D indicates the side of Pin #35 - Pin #44 of the ISM20736S.

L-shaped ground arrangement in the 2nd layer (purple color) and the top-side component placement and trace routing (blue color). We can see that some components and routings are placing in the L-shaped area on the top layer and the “L -shaped” ground is connected to system ground in the 2nd layer.

The clearance area (marked in yellow) and L-shaped GND area (marked in green).

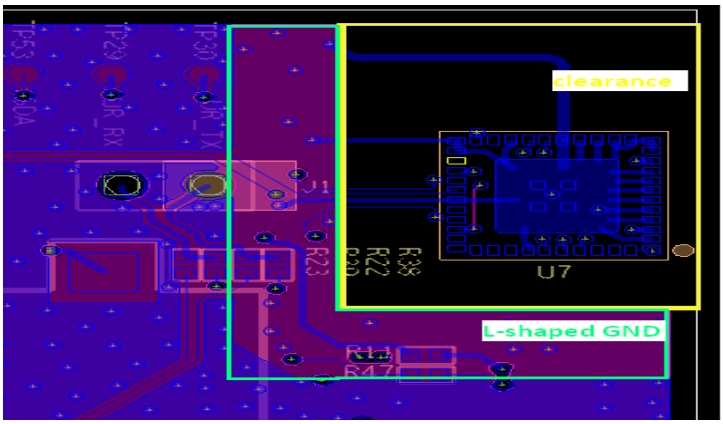


Figure 5: L Shaped Ground (Arranged in 2nd layer only)

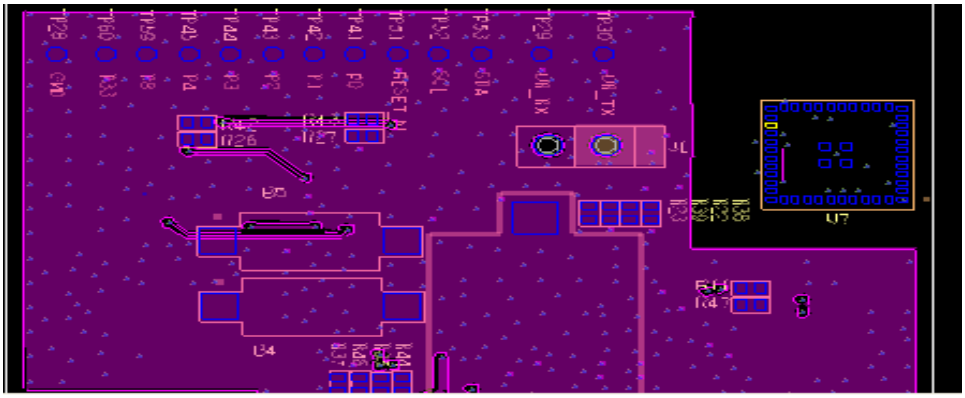


Figure 6 : L Shaped Ground Plane , 2nd layer)

It is also recommended to have a 0.4mm gap between the top of the module and plastic case.

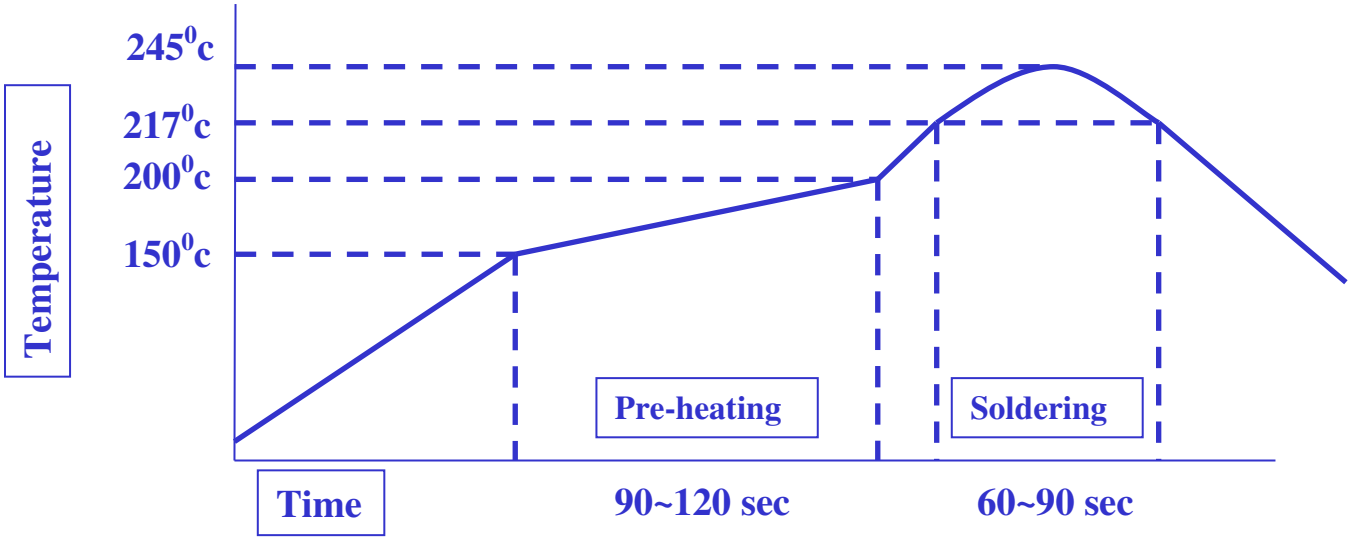
19 PRODUCT COMPLIANCE CONSIDERATIONS

RoHS: Restriction of Hazardous Substances (RoHS) directive has come into force since 1st July 2006 all electronic products sold in the EU must be free of hazardous materials, such as lead. Inventek is fully committed to being one of the first to introduce lead-free GPS products while maintaining backwards compatibility and focusing on a continuously high level of product and manufacturing quality.

EMI/EMC: The Inventek module design embeds EMI/EMC suppression features and accommodations to allow for higher operational reliability in noisier (RF) environments and easier integration compliance in host (OEM) applications.

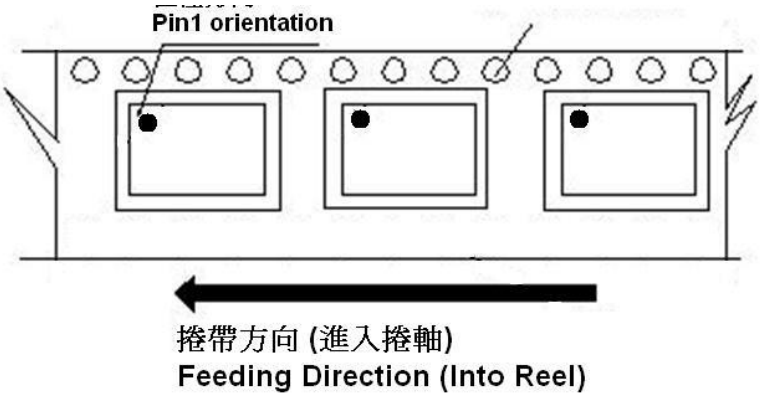
FCC/CE: The module is compliant with FCC/CE.

20 REFLOW PROFILE

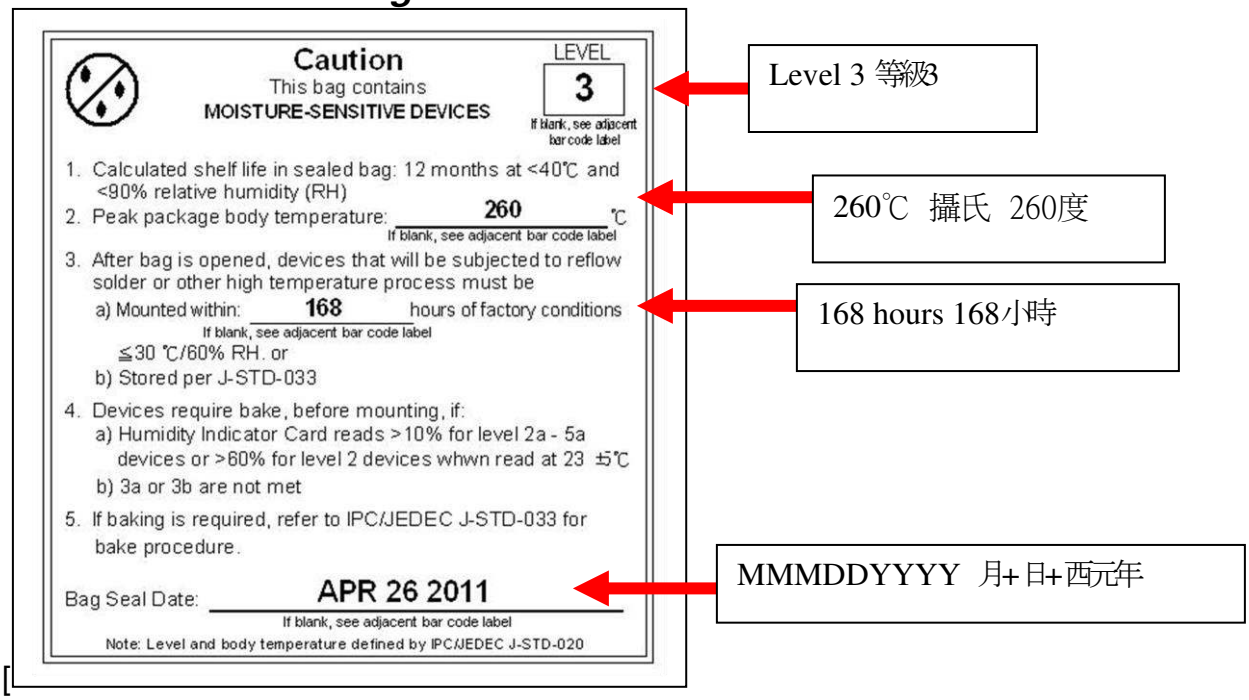


21 PACKAGING INFORMATION

Pin 1 Location in the Tape/Reel



21.1 MSL Level / Storage Condition



22 REVISION CONTROL

Document : ISM20736S	
External Release	

Date	Author	Revision	Comment
4/17/2016	FMT	1.0	Preliminary

23 CONTACT INFORMATION

Inventek Systems
2 Republic Road
Billerica Ma, 01862
Tel: 978-667-1962
Sales@inventeksys.com

www.inventeksys.com

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