TS4621B

High-performance class-G stereo headphone amplifier with I²C volume control

Features

- Power supply range: 2.3 V to 4.8 V
- 0.6 mA/channel quiescent current
- 2.1 mA current consumption with 100 µW/channel (10 dB crest factor)
- 0.006% typical THD+N at 1 kHz
- 100 dB typical PSRR at 217 Hz
- 100 dB of SNR A-weighted at G = 0 dB
- Zero pop and click
- I²C interface for volume control
- Digital volume control range from -60 dB to +4 dB
- Independent right and left channel shutdown control
- Integrated high-efficiency step-down converter
- Low software standby current: 5 µA max
- Output-coupling capacitors removed
- Thermal shutdown
- Flip-chip package: 1.65 mm x 1.65 mm, 400 µm pitch, 16 bumps

Applications

- Cellular phones, smart phones
- Mobile internet devices
- PMP/MP3 players

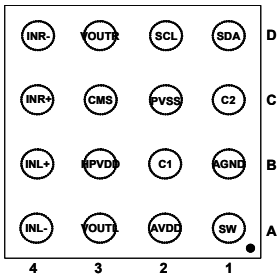
Description

The TS4621B is a class-G stereo headphone driver dedicated to high audio performance, high power efficiency and space-constrained applications.

It is based on the core technology of a low power dissipation amplifier combined with a high-efficiency step-down DC/DC converter for supplying this amplifier.

TS4621BEIJT - flip-chip

Pinout (top view)



Balls are underneath

When powered by a battery, the internal step-down DC/DC converter generates the appropriate voltage to the amplifier depending on the amplitude of the audio signal to supply the headsets. It achieves a total 2.1 mA current consumption at 100 µW output power (10 dB crest factor).

THD+N is 0.02 % maximum at 1 kHz and PSRR is 100 dB at 217 Hz, which ensures a high audio quality of the device in a wide range of environments.

The traditionally bulky output coupling capacitors can be removed.

A dedicated common-mode sense pin removes parasitic ground noise.

The TS4621B is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads.

The TS4621B is packaged in a tiny 16-bump flip-chip package with a pitch of 400 µm.

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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1) during 1ms.	5.5	V
V_{in+},V_{in-}	Input voltage referred to ground	+/- 1.2	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature(2)	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_d	Power dissipation	Internally limited(4)	
ESD	Human body model (HBM)(5) All pins VOUTR, VOUTL vs. AGND	 2 4	kV
	Machine model (MM), min. value(6)	100	V
	Charge device model (CDM) All pins VOUTR, VOUTL	 500 750	V
	IEC61000-4-2 level 4, contact(7) IEC61000-4-2 level 4, air discharge(7)	+/- 8 +/- 15	kV
	Lead temperature (soldering, 10 sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. Thermal shutdown is activated when maximum junction temperature is reached.
3. The device is protected from over-temperature by a thermal shutdown mechanism, active at 150° C.
4. Exceeding the power derating curves for long periods may provoke abnormal operation.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. The measurement is performed on an evaluation board, with ESD protection EMIF02-AV01F3.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.3 to 4.8	V
HPVDD	internal step-down DC output voltages High rail voltage Low rail voltage	 1.9 1.2	V
SDA, SCL	Input voltage range	GND to V_{cc}	V
R_L	Load resistor	≥ 16	Ω
C_L	Load capacitor Serial resistor of 12 Ω minimum, $R_L \geq 16$ Ω	 0.8 to 100	nF
T_{oper}	Operating free air temperature range	-40 to +85	°C
R_{thja}	Flip-chip thermal resistance junction to ambient	90	°C/W

2 Typical application schematics

Figure 1. Typical application schematics for the TS4621B

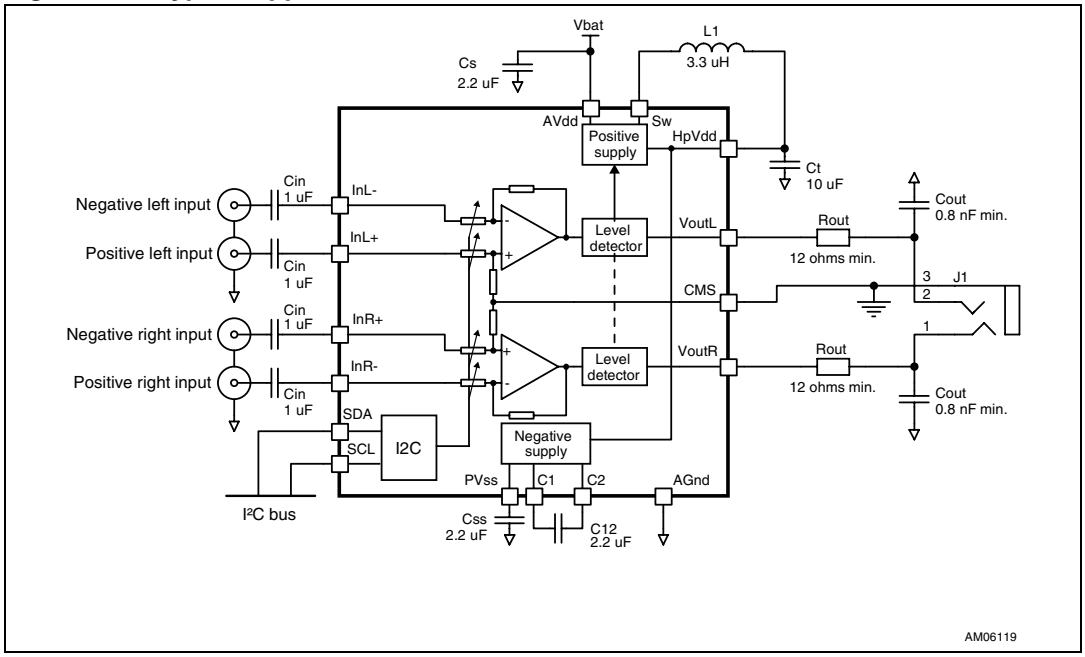


Table 3. TS4621B pin description

Pin number	Pin name	Pin definition
A1	SW	Switching node of the buck converter
A2	AVDD	Analog supply voltage, connect to battery
A3	VOUTL	Output signal for left audio channel
A4	INL-	Negative input signal for left audio channel
B1	AGND	Device ground
B2	C1	Flying capacitor terminal for internal negative supply generator
B3	HPVDD	Buck converter output, power supply for amplifier
B4	INL+	Positive input signal for left audio channel
C1	C2	Flying capacitor terminal for internal negative supply generator
C2	PVSS	Negative supply generator output
C3	CMS	Common mode sense, to be connected as close as possible to the ground of headphone/line out plug
C4	INR+	Positive input signal for right audio channel
D1	SDA	I²C data signal, up to V_{CC} tolerant input
D2	SCL	I²C clock signal, up to V_{CC} tolerant input
D3	VOUTR	Output signal for right audio channel
D4	INR-	Negative input signal for right audio channel

Table 4. TS4621B component description(1)

Component	Value	Description
Cs	2.2 µF	Decoupling capacitors for V_{CC}. A 2.2 µF capacitor is sufficient for proper decoupling of the TS4621B. An X5R dielectric and 10 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when V_{CC} = 4.8 V. Must be placed as close as possible to the TS4621B to minimize parasitic inductance and resistance.
C12	2.2 µF	Capacitor for internal negative power supply operation. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V. Must be placed as close as possible to the TS4621B to minimize parasitic inductance and resistance.
C_{SS}	2.2 µF	Filtering capacitor for internal negative power supply. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V.
C_{in}	$Cin = \frac{1}{2 \times \pi \times Rin \times Fc}$	Input coupling capacitor that forms with Rin ≈ Rindiff/2 a first-order high-pass filter with a -3 dB cutoff frequency Fc. For example, at maximum gain G = 4 dB, Rin = 12.5 kΩ, C_{in} = 1 µF, therefore Fc = 13 Hz.
C_{out}	0.8 to 100 nF	Output capacitor of 0.8 nF minimum to 100 nF maximum. This capacitor is mandatory for operation of the TS4621B.
R_{out}	12 Ω min.	Output resistor in-series with the TS4621B output. This 12 Ω minimum resistor is mandatory for operation of the TS4621B.
L1	3.3 µH	Inductor for internal DC/DC step-down converter. References of inductors: refer to *Section 4.4.1* for more information.
C_t	10 µF	Tank capacitor for internal DC/DC step-down converter. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V. Refer to *Section 4.4.2* for more information.

1. Refer to *Section 4.4* for a complete description of each component.

3 Electrical characteristics

Table 5. Electrical characteristics of the I²C interface for V_{CC} = +3.6 V, AGND = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage on SDA, SCL pins			0.6	V
V_{IH}	High level input voltage on SDA, SCL pins	1.2			V
V_{OL}	Low level output voltage, SDA pin, I_{sink} = 3mA			0.4	V
I_{in}	Input current on SDA, SCL		$\frac{V_{SDA, SCL}}{600k\Omega}$	10	µA

Table 6. Electrical characteristics of the amplifier for V_{CC} = +3.6 V, AGND = 0 V, R_L= 32 Ω + 15 Ω, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Quiescent supply current, no input signal, both channels enabled		1.2	1.5	mA
I_s	Supply current, with input modulation, both channels enabled, HPVDD = 1.2 V, output power per channel, F=1kHz Pout = 100 µW at 3 dB crest factor Pout = 500 µW at 3 dB crest factor Pout = 1 mW at 3 dB crest factor Pout = 100 µW at 10 dB crest factor Pout = 500 µW at 10 dB crest factor Pout = 1 mW at 10 dB crest factor		 2.3 3.7 4.7 2.1 3.1 3.9	 3.5 5 6.5	mA
I_{STBY}	Standby current, no input signal, I²C CR1 = 01h V_{SDA} = 0 V, V_{SCL} = 0 V		0.6	5	µA
V_{in}	Input differential voltage range(1)			1	V_{rms}
V_{oo}	Output offset voltage No input signal	-500		+500	µV
V_{out}	Maximum output voltage, in-phase signals R_L = 16 Ω, THD+N = 1% max, f = 1 kHz R_L = 47 Ω, THD+N = 1% max, f = 1 kHz R_L = 10 kΩ, R_s = 15 Ω, C_L = 1 nF, THD+N = 1% max, f = 1 kHz	 0.6 1.0 1.0	 0.8 1.1 1.3		V_{rms}
THD+N	Total harmonic distortion + noise, G = 0 dB V_{out} = 700 mVrms, F = 1 kHz V_{out} = 700 mVrms, 20 Hz < F < 20 kHz		 0.006 0.05	0.02	%
PSRR	Power supply rejection ratio(1), V_{ripple} = 200 mV_{pp}, grounded inputs F = 217 Hz, G = 0 dB, R_L ≥16 Ω F = 10 kHz, G = 0 dB, R_L ≥16 Ω	 90	 100 70		dB

Table 6. Electrical characteristics of the amplifier for V_{CC} = +3.6 V, AGND = 0 V, R_L= 32 Ω + 15 Ω, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
CMRR	Common mode rejection ratio F = 1 kHz, G = 0 dB, V_{ic} = 200 mV_{pp} F = 20 Hz to 20 kHz, G = 0 dB, V_{ic} = 200 mV_{pp}		 65 45		dB
Crosstalk	Channel separation R_L = 32 Ω + 15 Ω , G = 0 dB, F = 1 kHz, P_o = 10 mW R_L = 10 kΩ, G = 0 dB, F = 1 kHz, V_{out} = 1 Vrms	 60 80	 100 110		dB
SNR	Signal-to-noise ratio, A-weighted, V_{out} = 1 V_{rms}, THD+N < 1%, F = 1 kHz(1) G = +4 dB G = +0 dB	 99 100			dB
ONoise	Output noise voltage, A-weighted (1) G = +4 dB G = +0 dB		9	 11 9	µVrms
G	Gain range with gain (dB) = 20 x log[(V_{out}L/R)/(InL/R+ - InL/R-)]	-60		+4	dB
Mute	InL/R+ - InL/R- = 1 V_{rms}			-80	dB
-	Gain step size error	-0.5		+0.5	step-size
-	Gain error (G = +4 dB)	-0.45		+0.42	dB
R_{indiff}	Differential input impedance	25	34		kΩ
	Input impedance during wake-up phase (referred to ground)		2		kΩ
Z_{out}	Output impedance when CR1 = 00h (negative supply is ON and amplifier output stages are OFF)(1) F < 40 kHz F = 6 MHz F = 36 MHz	 10 500 75			 kΩ Ω Ω
t_{wu}	Wake-up time(2)		12	16	ms
t_{stby}	Standby time		100		µs
t_{atk}	Attack time. Setup time between low rail and high rail voltages of internal step-down DC/DC converter		100		µs
t_{dcy}	Decay time		50		ms

1. Guaranteed by design and parameter correlation.
2. Refer to the application information in *Section 4.2 on page 30*.

Table 7. Timing characteristics of the I²C interface for I²C interface signals over recommended operating conditions (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	Frequency, SCL			400	kHz
$t_{d(H)}$	Pulse duration, SCL high	0.6			µs
$t_{d(L)}$	Pulse duration, SCL low	1.3			µs
t_{st1}	Setup time, SDA to SCL	100			ns
t_{h1}	Hold time, SCL to SDA	0			ns
t_f	Bus free time between stop and start condition	1.3			µs
t_{st2}	Setup time, SCL to start condition	0.6			µs
t_{h2}	Hold time, start condition to SCL	0.6			µs
t_{st3}	Setup time, SCL to stop condition	0.6			µs

Figure 2. SCL and SDA timing diagram

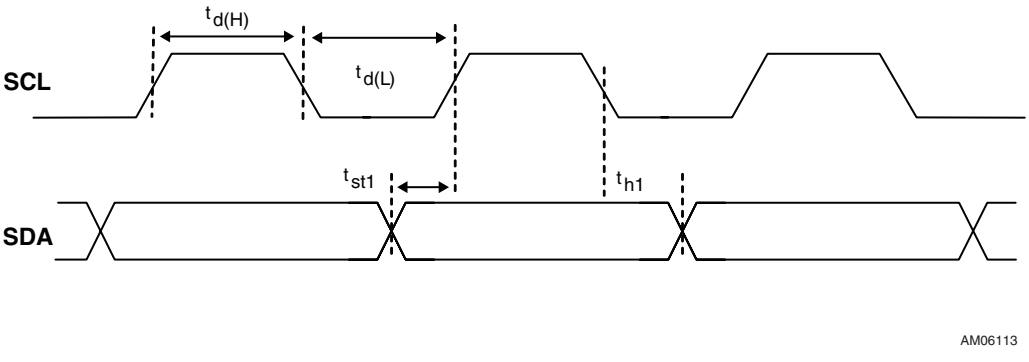


Figure 3. Start and stop condition timing diagram

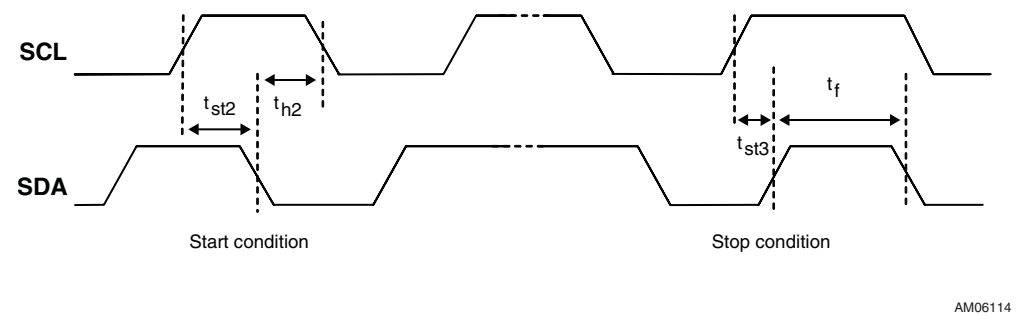


Figure 4. Current consumption vs. power supply voltage

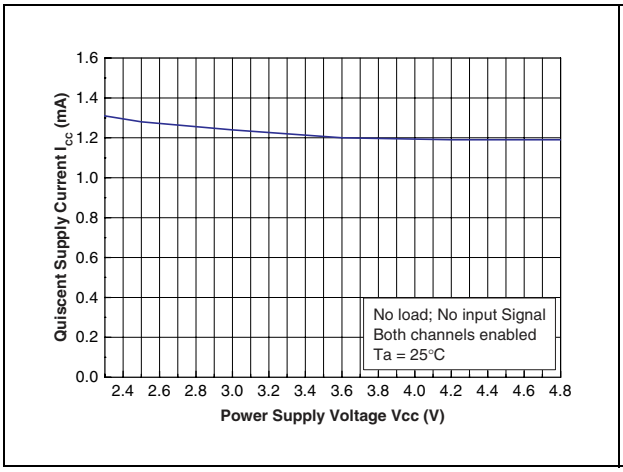


Figure 5. Standby current consumption vs. power supply voltage

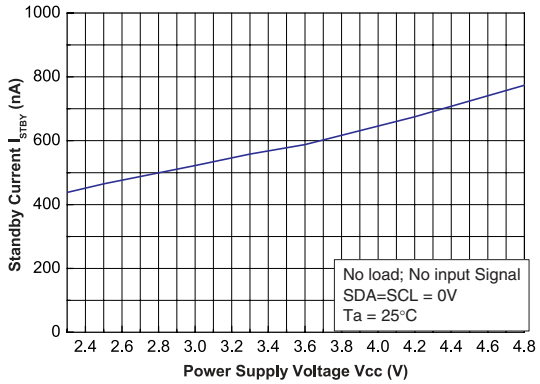


Figure 6. Maximum output power vs. load in-phase

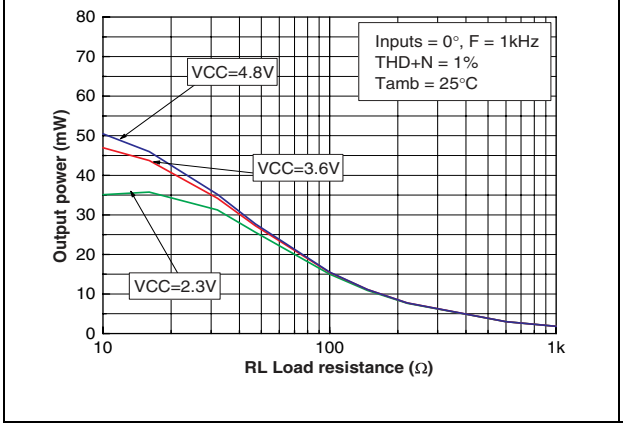


Figure 7. Maximum output power vs. load out-of-phase

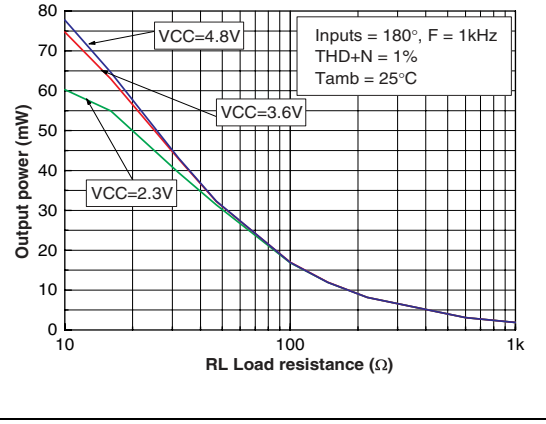


Figure 8. Maximum output power vs. power supply voltage, RL = 16 Ω

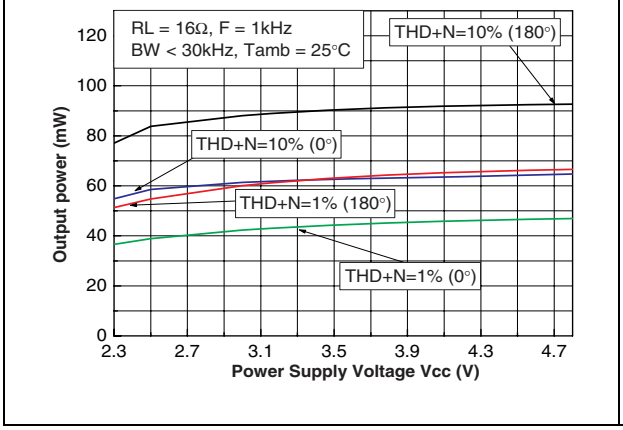


Figure 9. Maximum output power vs. power supply voltage, RL = 32 Ω

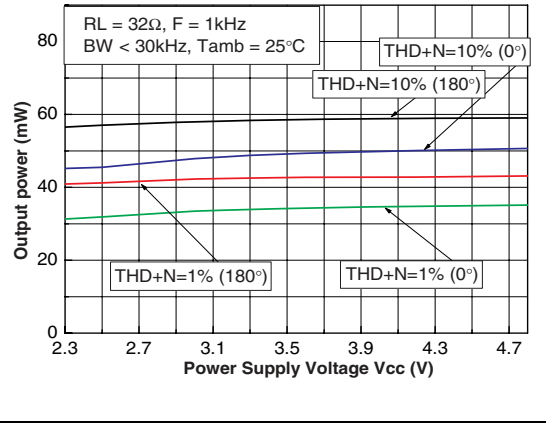


Figure 10. Maximum output power vs. power supply voltage, RL = 47 Ω

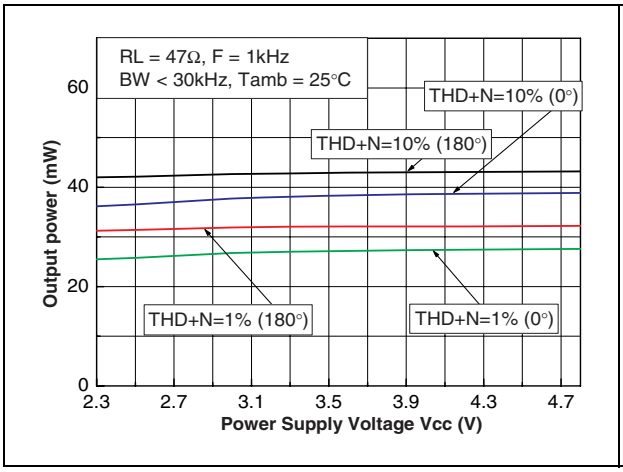


Figure 11. Maximum output voltage vs. power supply voltage, in-phase

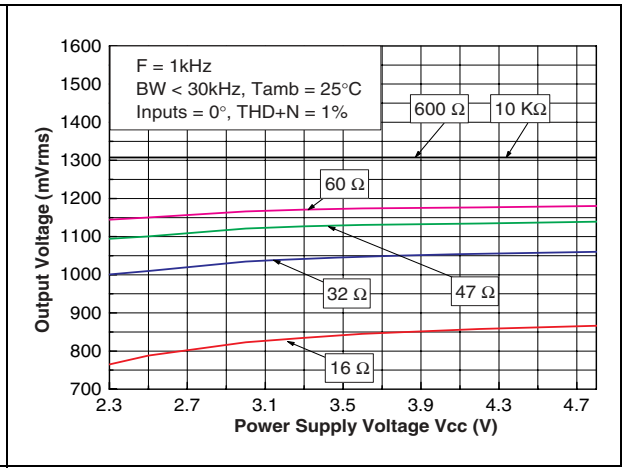


Figure 12. Maximum output voltage vs. power supply voltage, out-of-phase

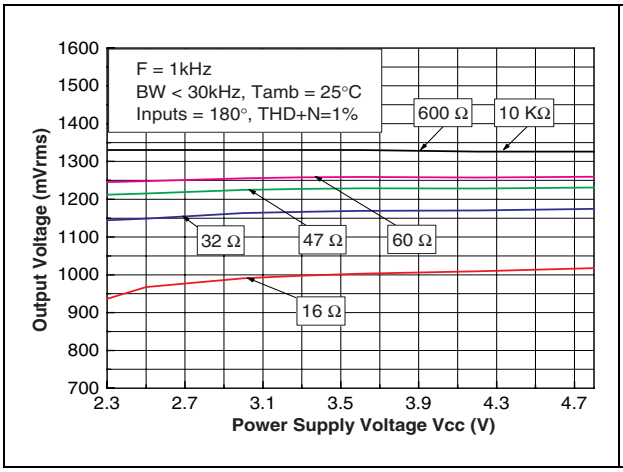


Figure 13. Current consumption vs. total output power, RL = 16 Ω

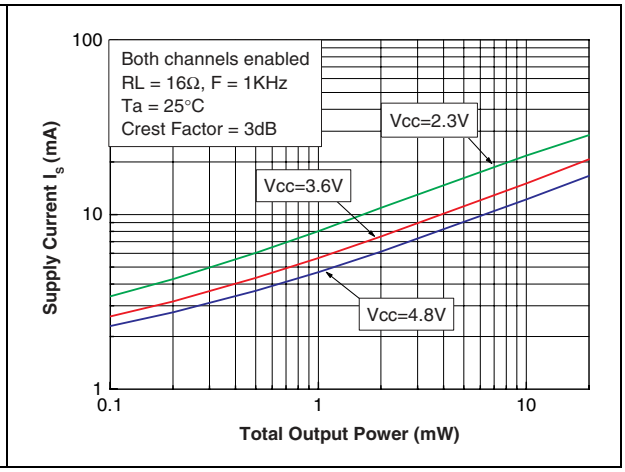


Figure 14. Current consumption vs. total output power, RL = 32 Ω

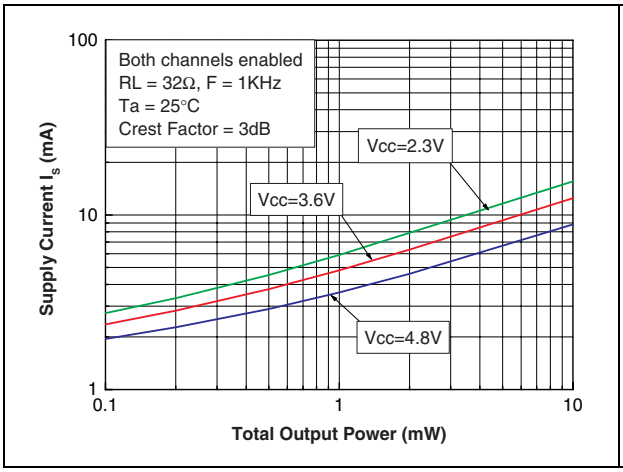


Figure 15. Current consumption vs. total output power, RL = 47 Ω

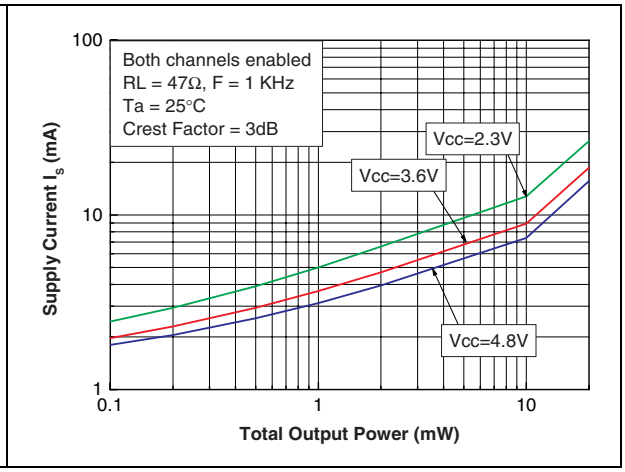


Figure 16. Current consumption vs. total output power

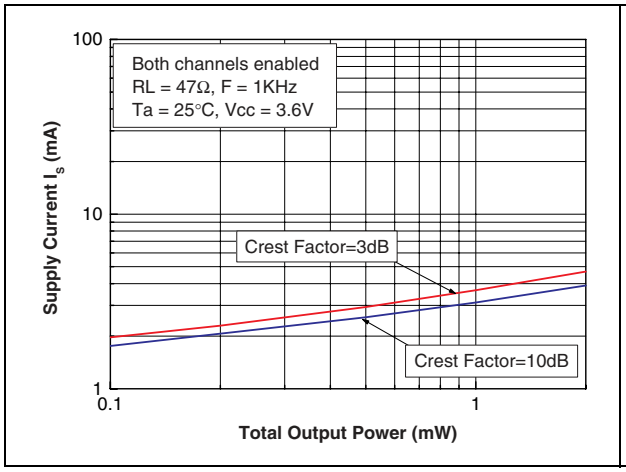


Figure 17. Power dissipation vs. total output power

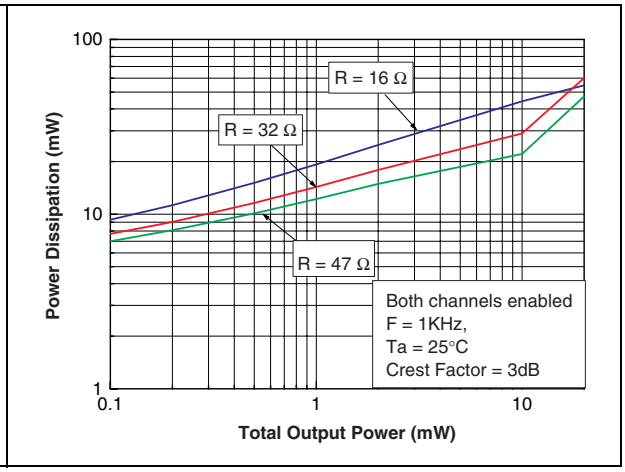


Figure 18. Output impedance vs. frequency in HiZ mode

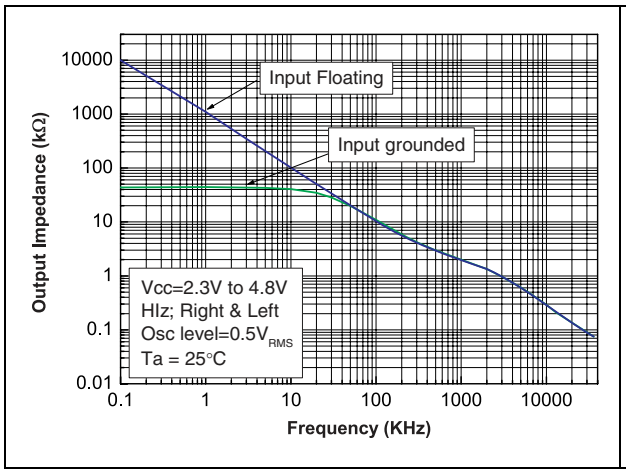


Figure 19. Differential input impedance vs. gain

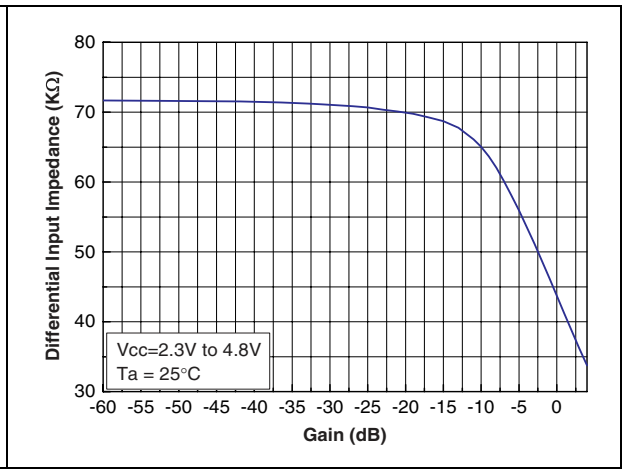


Figure 20. THD+N vs. output power RL = 16 Ω, in-phase, V_{CC} = 2.5 V

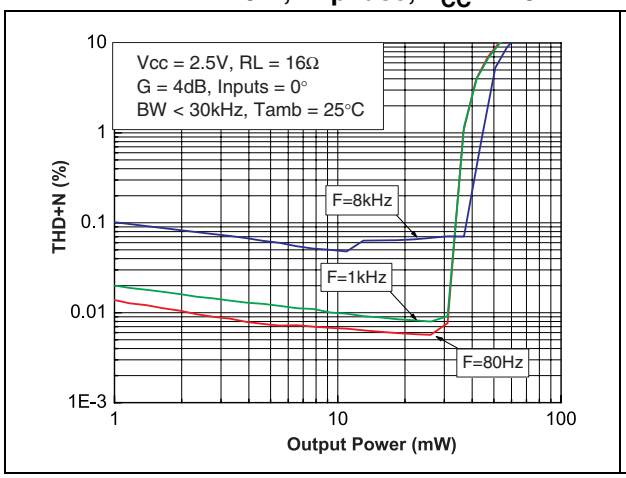


Figure 21. THD+N vs. output power RL = 16 Ω, out-of-phase, V_{CC} = 2.5 V

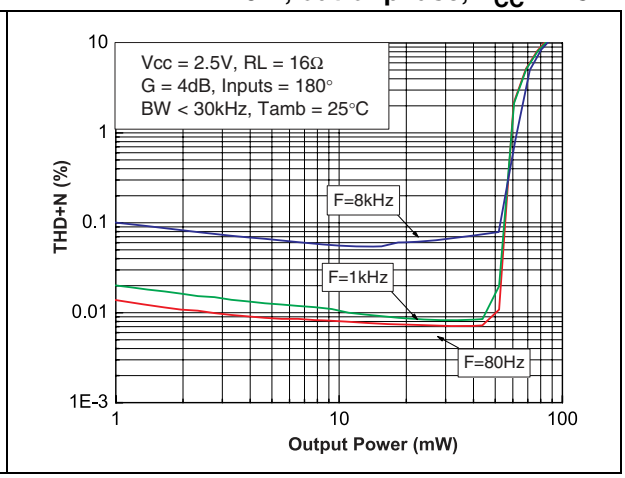


Figure 22. THD+N vs. output power RL = 16 Ω, in-phase, V_{CC} = 3.6 V

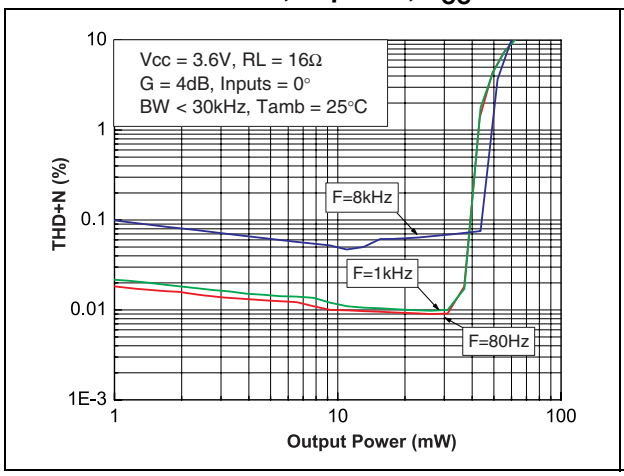


Figure 23. THD+N vs. output power RL = 16 Ω, out-of-phase, V_{CC} = 3.6 V

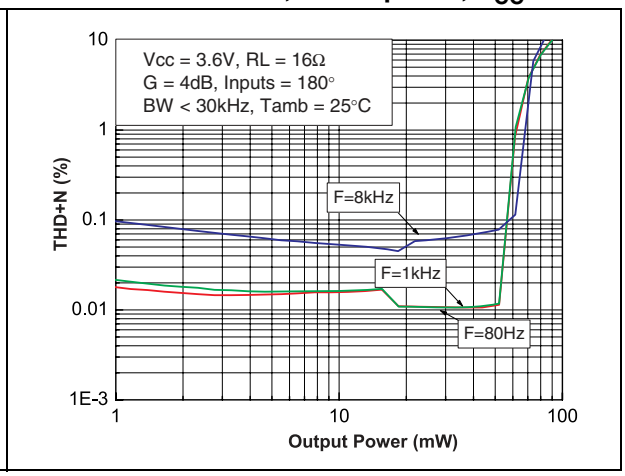


Figure 24. THD+N vs. output power RL = 16 Ω, in-phase, V_{CC} = 4.8 V

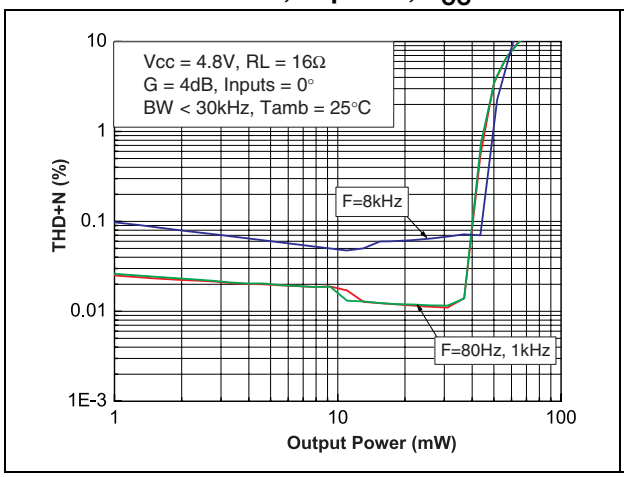


Figure 25. THD+N vs. output power RL = 16 Ω, out-of-phase, V_{CC} = 4.8 V

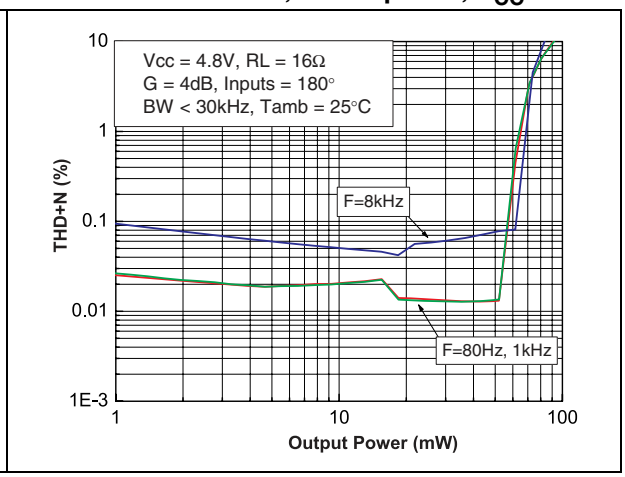


Figure 26. THD+N vs. output power RL = 32 Ω, in-phase, V_{CC} = 2.5 V

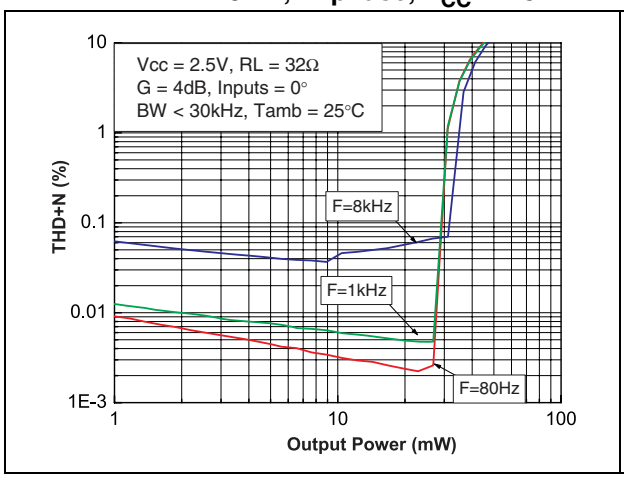


Figure 27. THD+N vs. output power RL = 32 Ω, out-of-phase, V_{CC} = 2.5 V

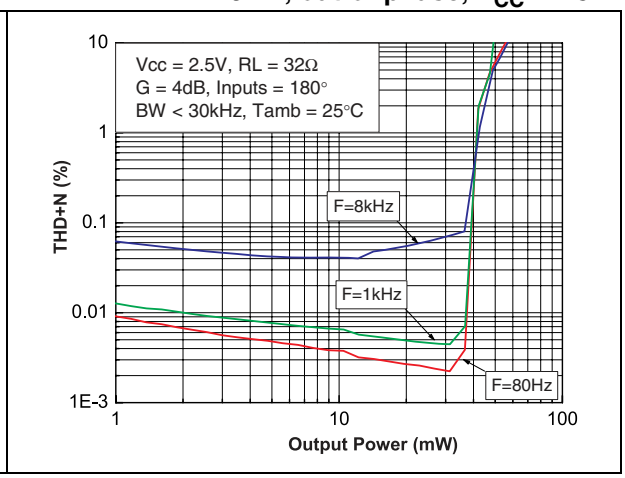


Figure 28. THD+N vs. output power RL = 32 Ω, in-phase, V_{CC} = 3.6 V

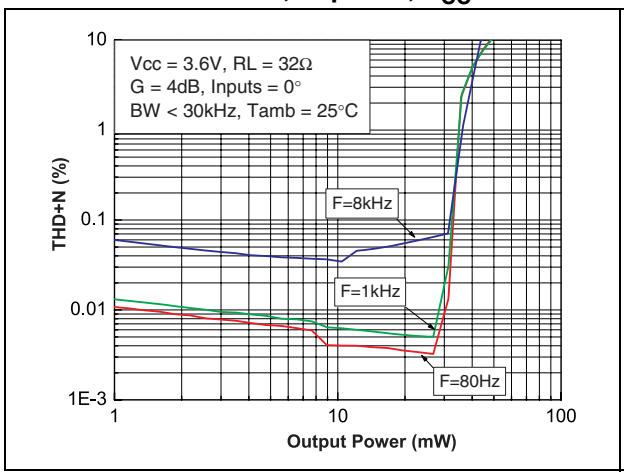


Figure 29. THD+N vs. output power RL = 32 Ω, out-of-phase, V_{CC} = 3.6 V

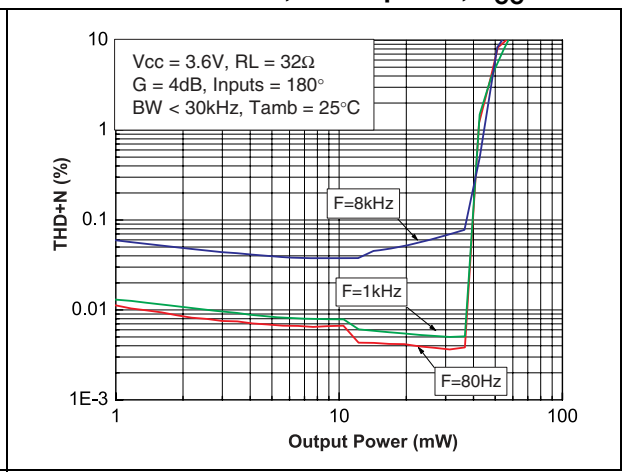


Figure 30. THD+N vs. output power RL = 32 Ω, in-phase, V_{CC} = 4.8 V

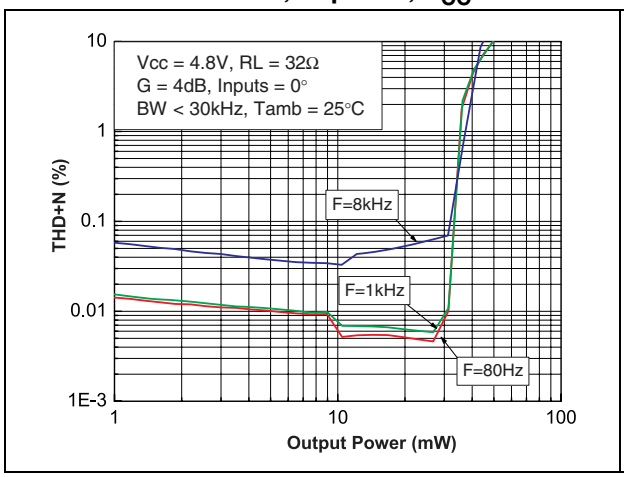


Figure 31. THD+N vs. output power RL = 32 Ω, out-of-phase, V_{CC} = 4.8 V

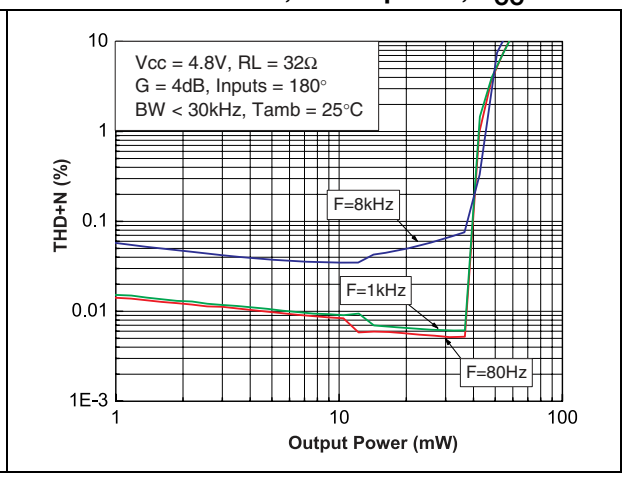


Figure 32. THD+N vs. output power RL = 47 Ω, in-phase, V_{CC} = 2.5 V

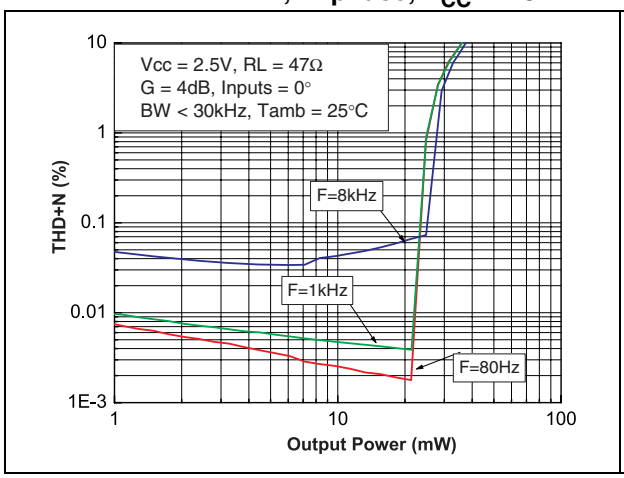


Figure 33. THD+N vs. output power RL = 47 Ω, out-of-phase, V_{CC} = 2.5 V

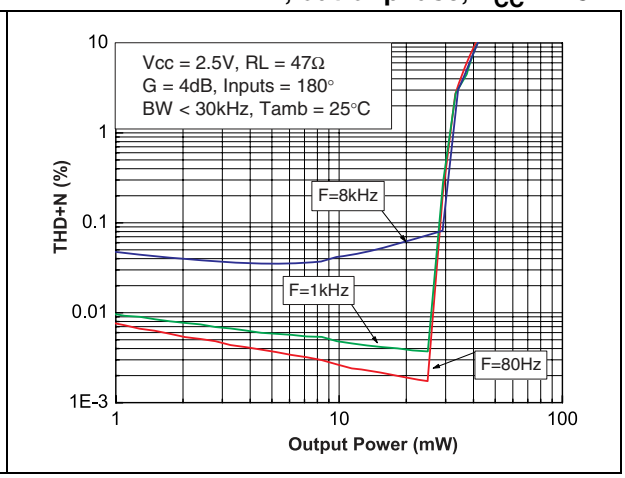


Figure 34. THD+N vs. output power RL = 47 Ω, in-phase, V_{CC} = 3.6 V

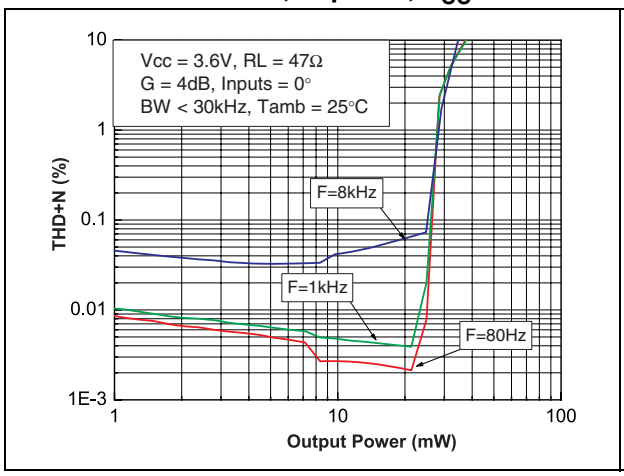


Figure 35. THD+N vs. output power RL = 47 Ω, out-of-phase, V_{CC} = 3.6 V

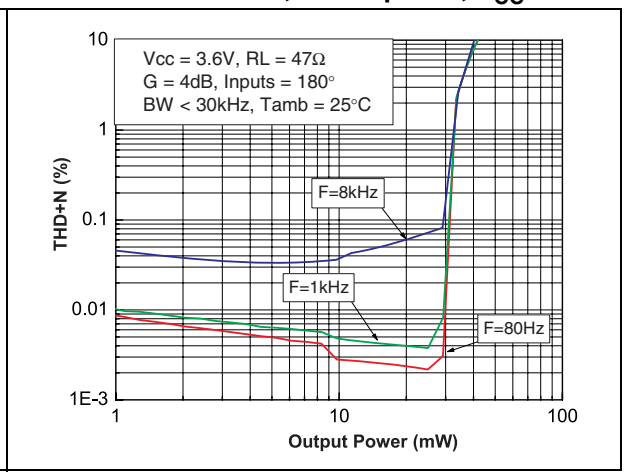


Figure 36. THD+N vs. output power RL = 47 Ω, in-phase, V_{CC} = 4.8 V

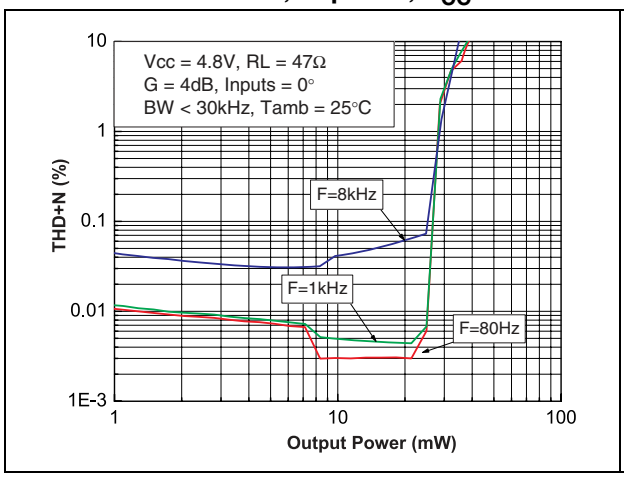


Figure 37. THD+N vs. output power RL = 47 Ω, out-of-phase, V_{CC} = 4.8 V

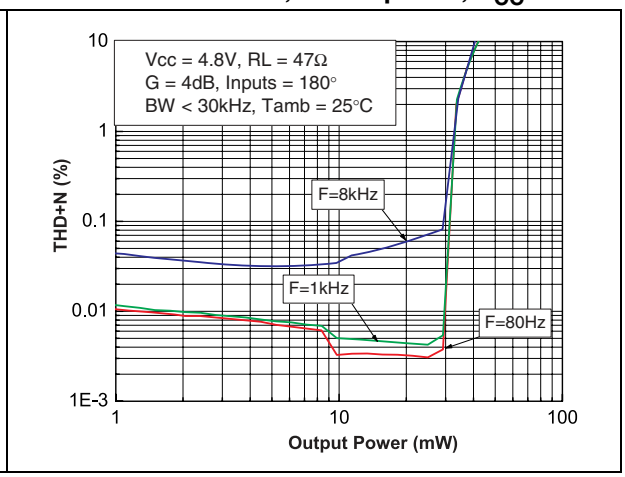


Figure 38. THD+N vs. frequency RL = 16 Ω, in-phase, V_{CC} = 2.5 V

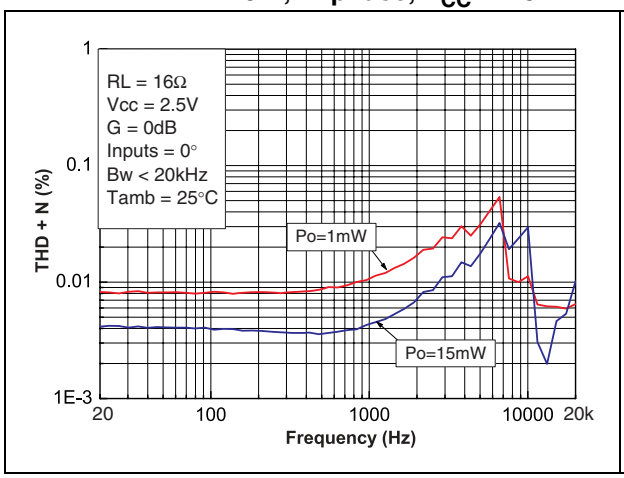


Figure 39. THD+N vs. frequency RL = 16 Ω, out-of-phase, V_{CC} = 2.5 V

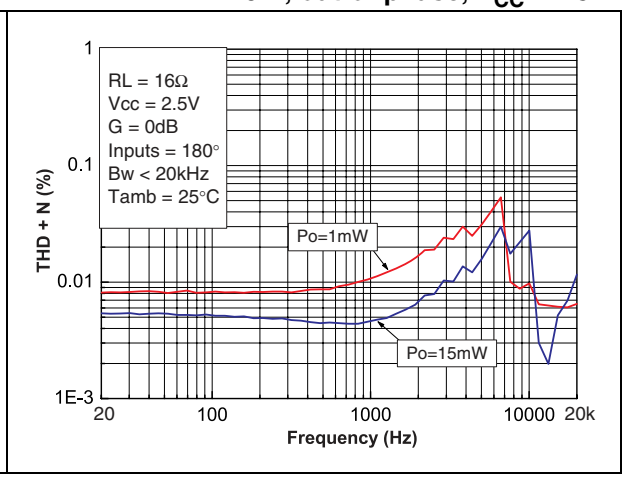


Figure 40. THD+N vs. frequency RL = 16 Ω, in-phase, V_{CC} = 3.6 V

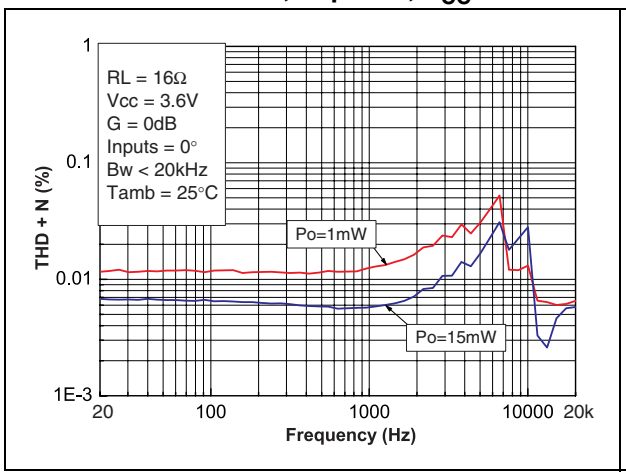


Figure 41. THD+N vs. frequency RL = 16 Ω, out-of-phase, V_{CC} = 3.6 V

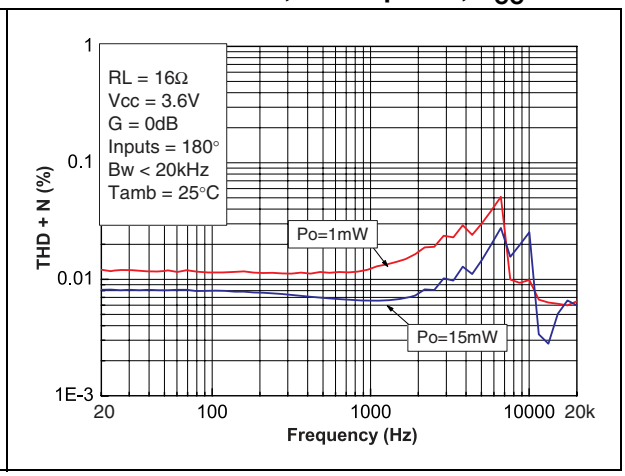


Figure 42. THD+N vs. frequency RL = 16 Ω, in-phase, V_{CC} = 4.8 V

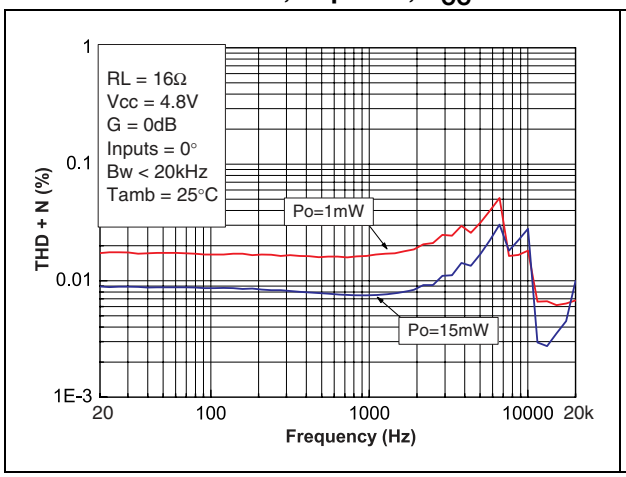


Figure 43. THD+N vs. frequency RL = 16 Ω, out-of-phase, V_{CC} = 4.8 V

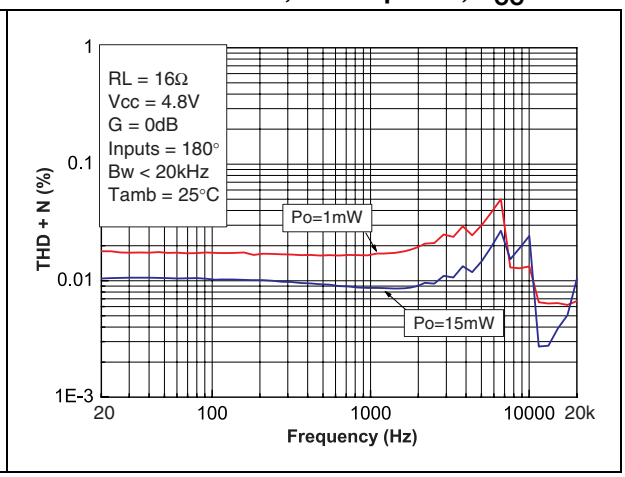


Figure 44. THD+N vs. frequency RL = 32 Ω, in-phase, V_{CC} = 2.5 V

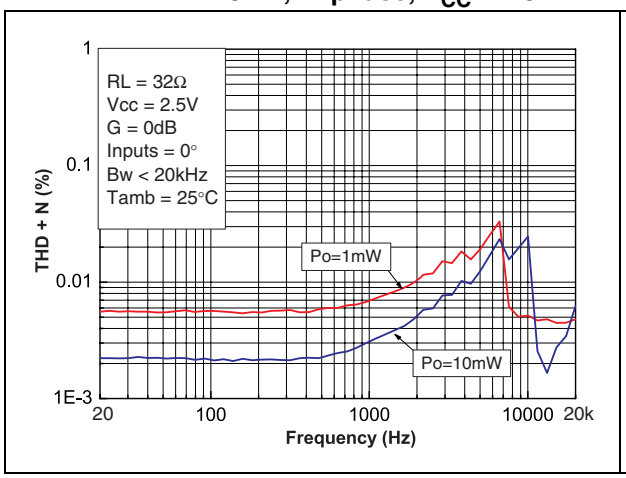


Figure 45. THD+N vs. frequency RL = 32 Ω, out-of-phase, V_{CC} = 2.5 V

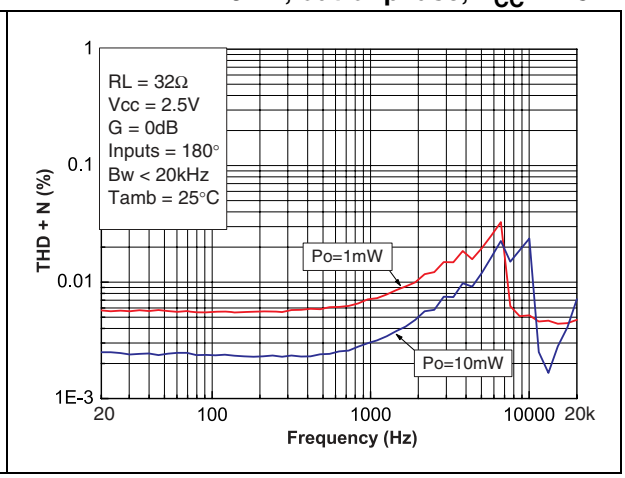


Figure 46. THD+N vs. frequency RL = 32 Ω, in-phase, V_{CC} = 3.6 V

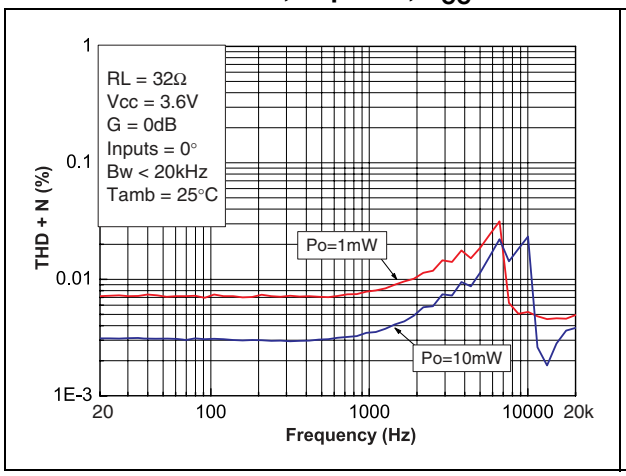


Figure 47. THD+N vs. frequency RL = 32 Ω, out-of-phase, V_{CC} = 3.6 V

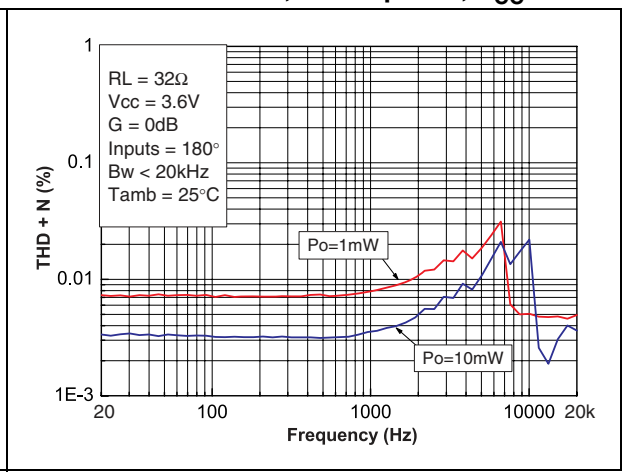


Figure 48. THD+N vs. frequency RL = 32 Ω, in-phase, V_{CC} = 4.8 V

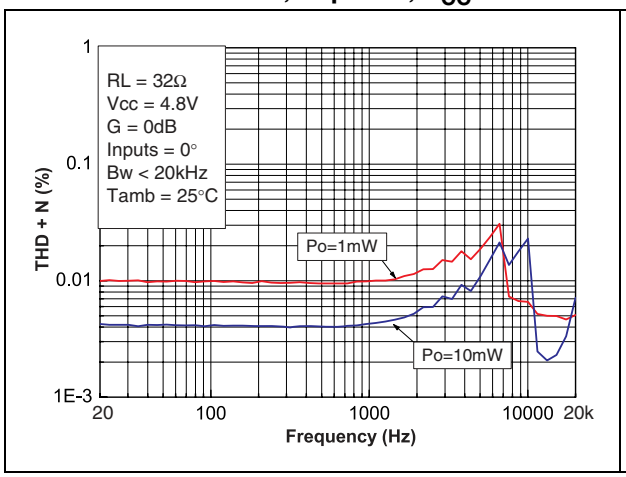


Figure 49. THD+N vs. frequency RL = 32 Ω, out-of-phase, V_{CC} = 4.8 V

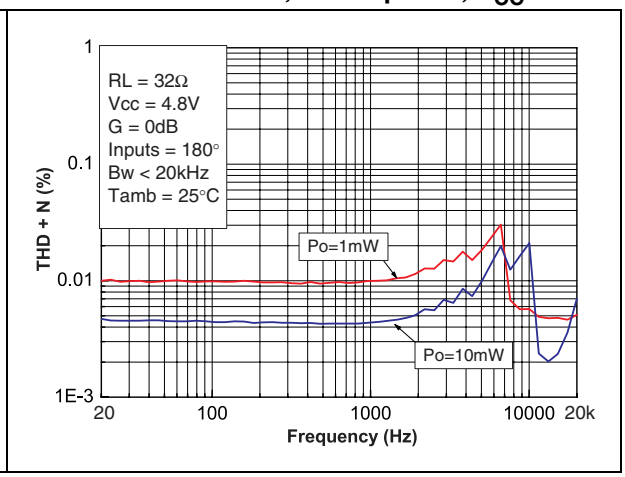


Figure 50. THD+N vs. frequency RL = 47 Ω, in-phase, V_{CC} = 2.5 V

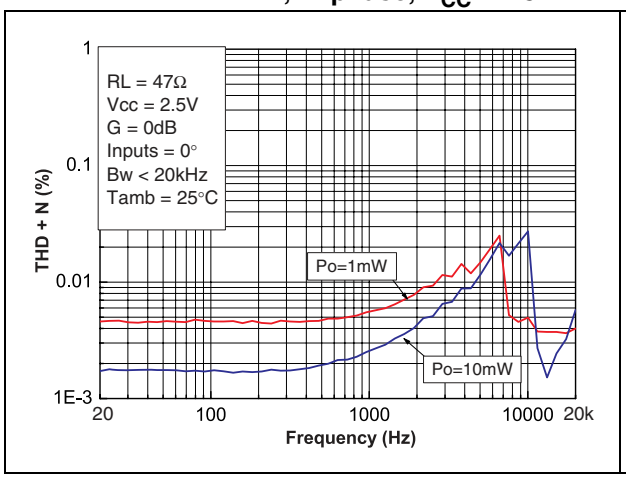


Figure 51. THD+N vs. frequency RL = 47 Ω, out-of-phase, V_{CC} = 2.5 V

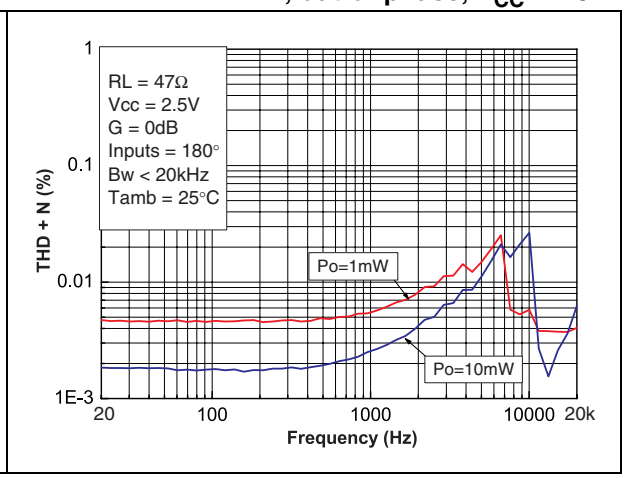


Figure 52. THD+N vs. frequency RL = 47 Ω, in-phase, V_{CC} = 3.6 V

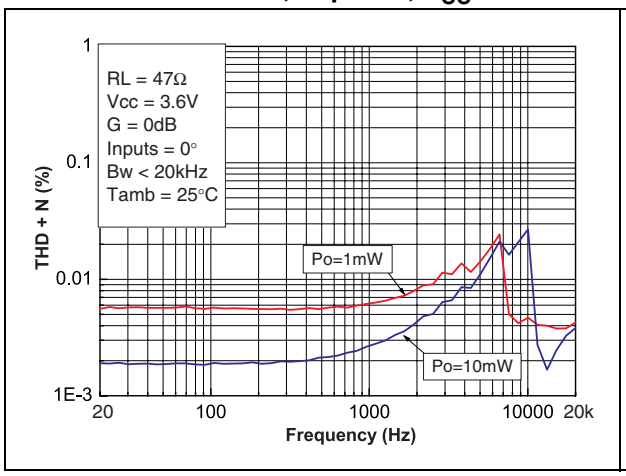


Figure 53. THD+N vs. frequency RL = 47 Ω, out-of-phase, V_{CC} = 3.6 V

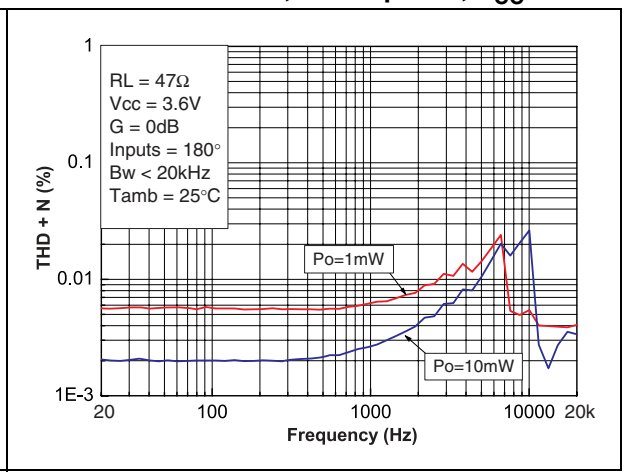


Figure 54. THD+N vs. frequency RL = 47 Ω, in-phase, V_{CC} = 4.8 V

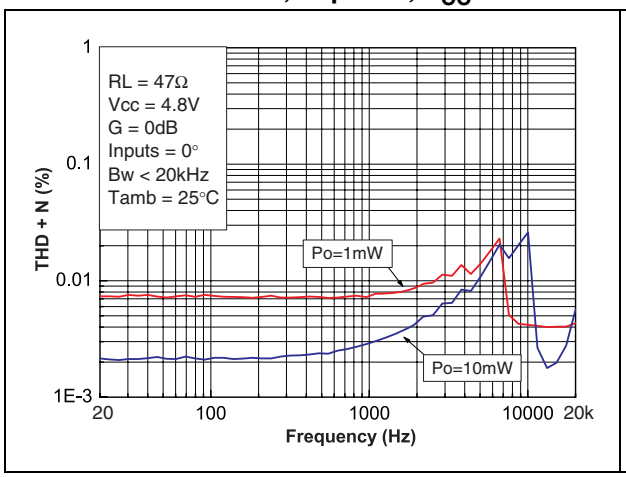


Figure 55. THD+N vs. frequency RL = 47 Ω, out-of-phase, V_{CC} = 4.8 V

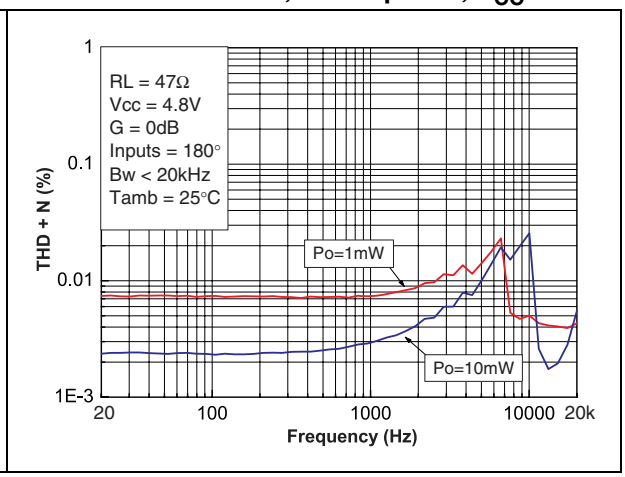


Figure 56. THD+N vs. frequency RL = 10 kΩ

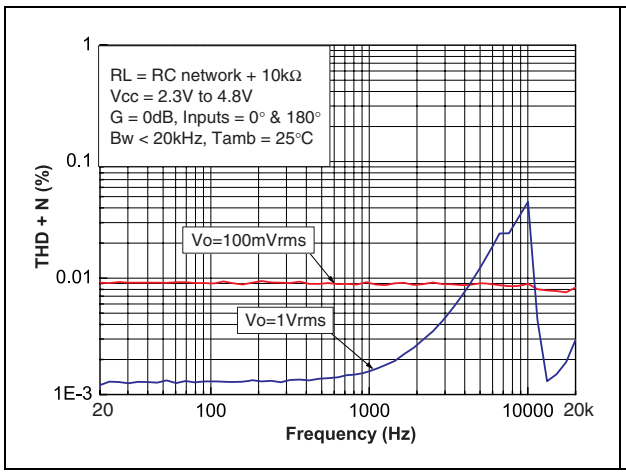


Figure 57. THD+N vs. frequency RL = 600 Ω

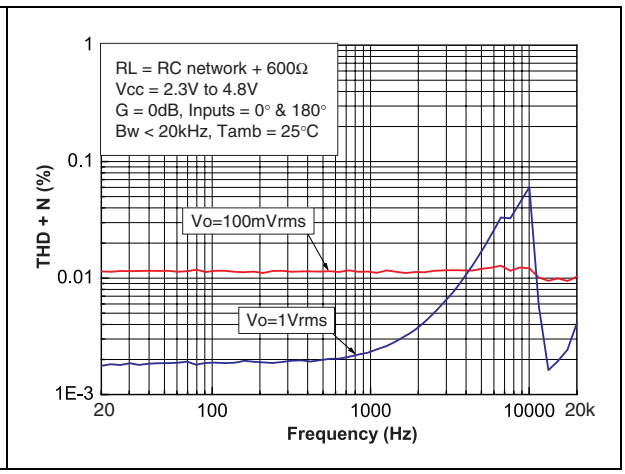


Figure 58. THD+N vs. output voltage RL = 10 kΩ

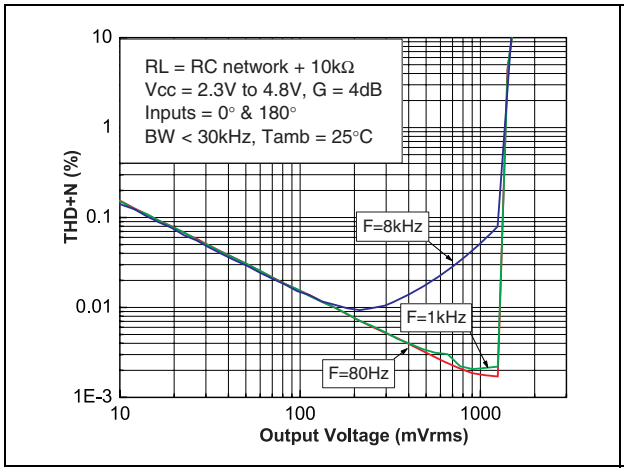


Figure 59. THD+N vs. output voltage RL = 600 Ω

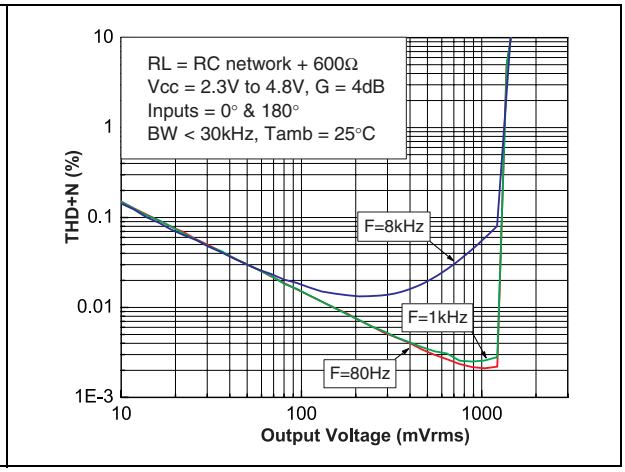


Figure 60. THD+N vs. input voltage, HiZ left and right

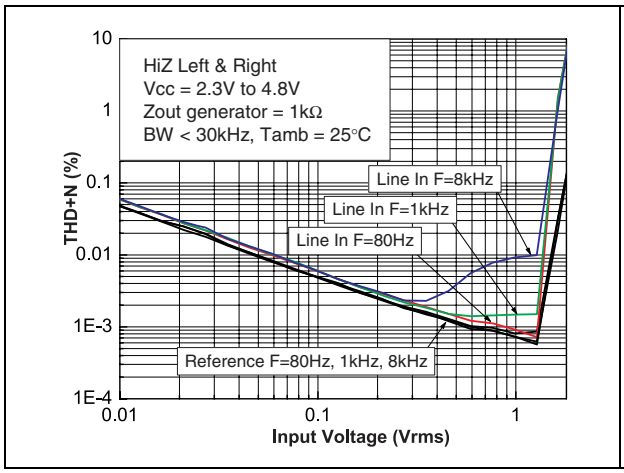


Figure 61. CMRR vs. frequency

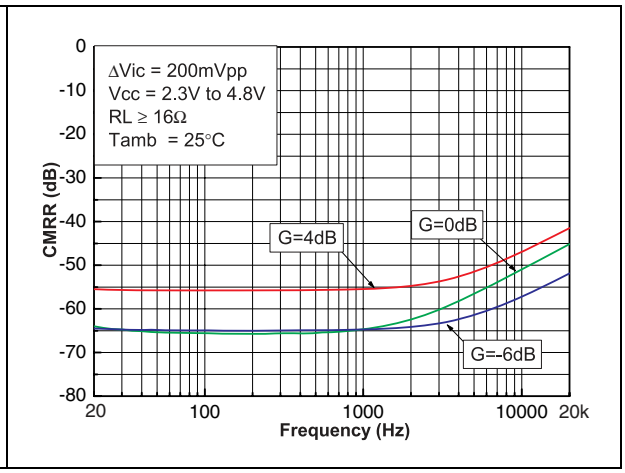


Figure 62. PSRR vs. frequency V_{CC} = 2.5 V

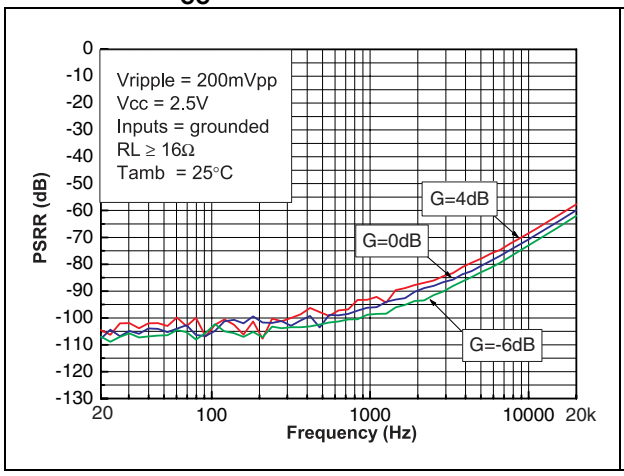


Figure 63. PSRR vs. frequency V_{CC} = 3.6 V

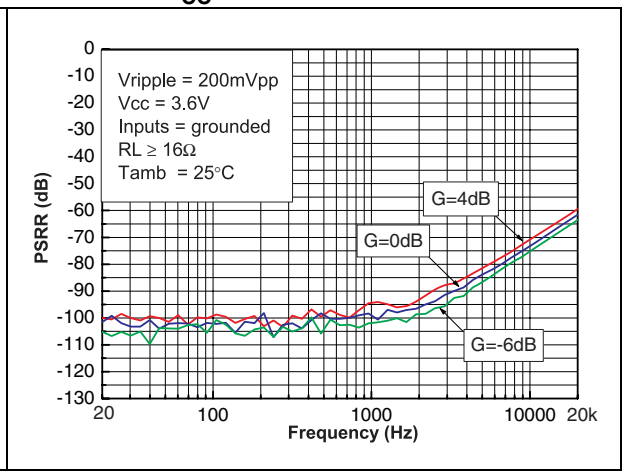


Figure 64. PSRR vs. frequency V_{CC} = 4.8 V

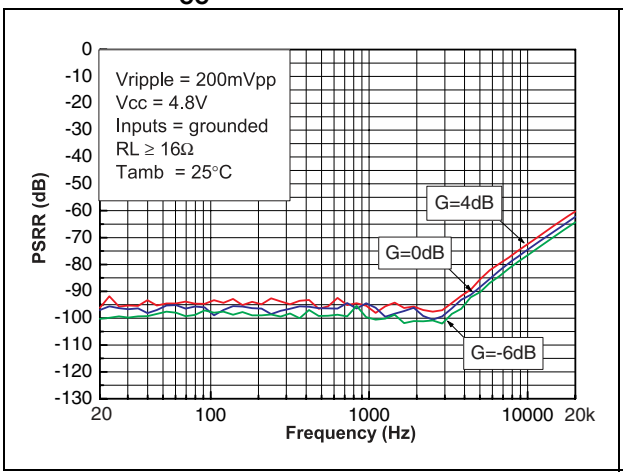


Figure 65. Output signal spectrum

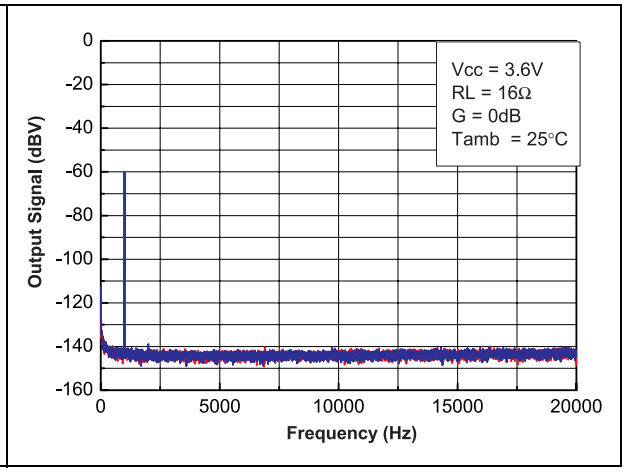


Figure 66. Crosstalk vs. frequency RL = 16 Ω

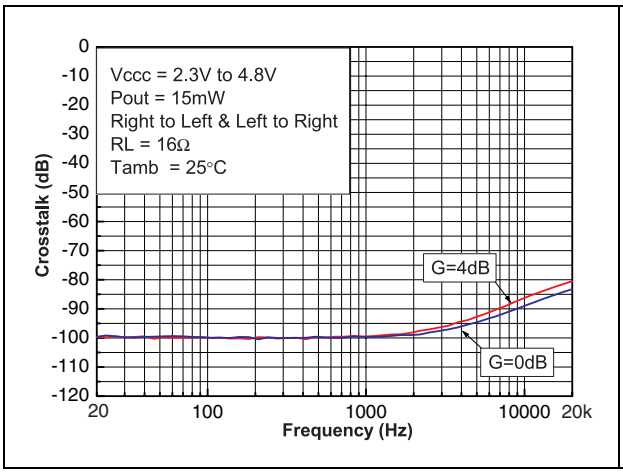


Figure 67. Crosstalk vs. frequency RL = 32 Ω

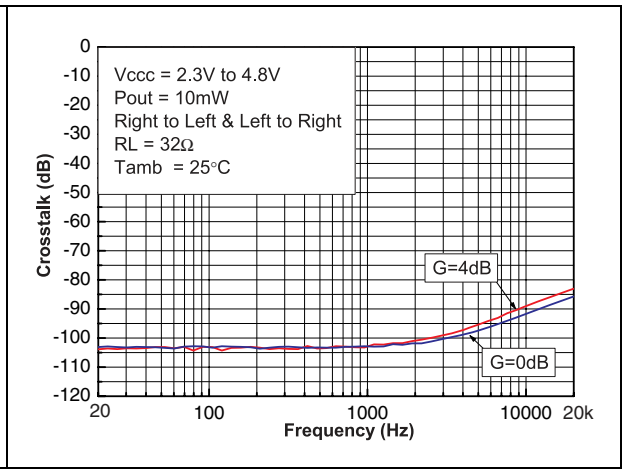


Figure 68. Crosstalk vs. frequency RL = 47 Ω

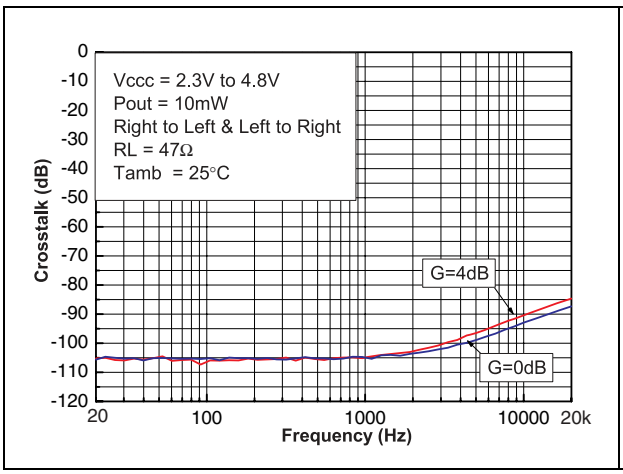


Figure 69. Crosstalk vs. frequency RL = 10 kΩ

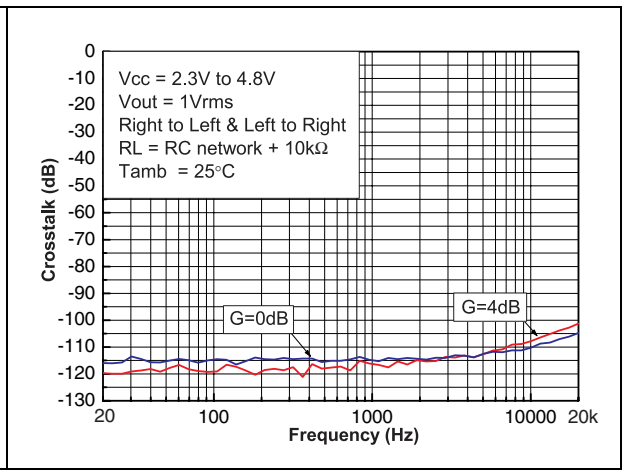


Figure 70. Wake-up time

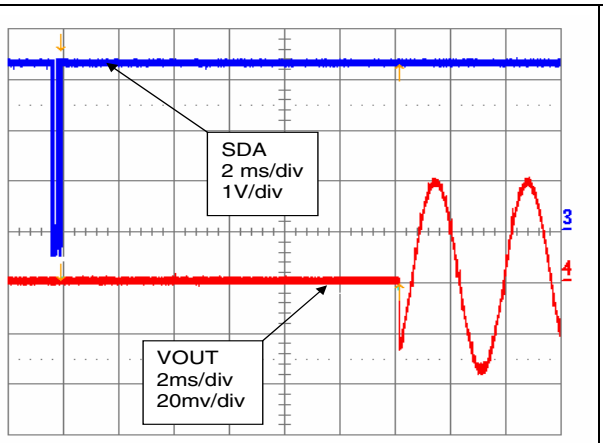
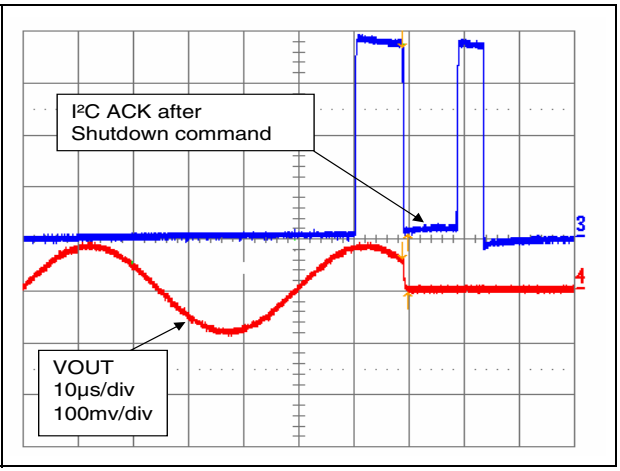


Figure 71. Shutdown time



4 Application information

4.1 I²C bus interface

In compliance with the I²C protocol, the TS4621B uses a serial bus to control the chip's functions with the clock (SCL) and data (SDA) wires. These two lines are bi-directional (open collector) and require an external pull-up resistor (typically 10 kΩ). The maximum clock frequency in fast mode specified by the I²C standard is 400 kHz, which the TS4621B supports. In this application, the TS4621B is always the slave device and the controlling microcontroller MCU is the master device.

The slave address of the TS4621B is 1100 000x (C0h).

Table 8 summarizes the pin descriptions for the I²C bus interface.

Table 8. Pin description of the I²C bus interface

Pin	Functional description
SDA	Serial data pin
SCL	Clock input pin

4.1.1 I²C bus operation

The host MCU can write to the TS4621B control register to control the TS4621B, and read from the control register to obtain a configuration from the TS4621B. The TS4621B is addressed by the byte consisting of the 7-bit slave address and the R/$\overline{W}$ bit.

Table 9. First byte after the START message for addressing the device

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	0	0	0	0	X

There are four control registers (*Table 10*) named CR1 to CR4. In read mode, all the control registers can be accessed. In write mode, only CR1, CR2 and CR3 can be addressed.

Table 10. Summary of control registers

Description	Register address	D7	D6	D5	D4	D3	D2	D1	D0
CR1	1	HP_EN_L	HP_EN_R	0	0	SC_L	SC_R	T_SH	SWS
CR2 volume control	2	Mute_L	Mute_R	Volume control					0
CR3	3	0	0	0	0	0	0	HiZ_L	HiZ_R
CR4 identification	4	0	1	0	0	0	0	0	0

Table 11. Control registers at power-up

Description	Register address	D7	D6	D5	D4	D3	D2	D1	D0
CR1	1	0	0	0	0	0	0	0	1
CR2	2	1	1	0	0	0	0	0	0
CR3	3	0	0	0	0	0	0	0	0
CR4	4	0	1	0	0	0	0	0	0

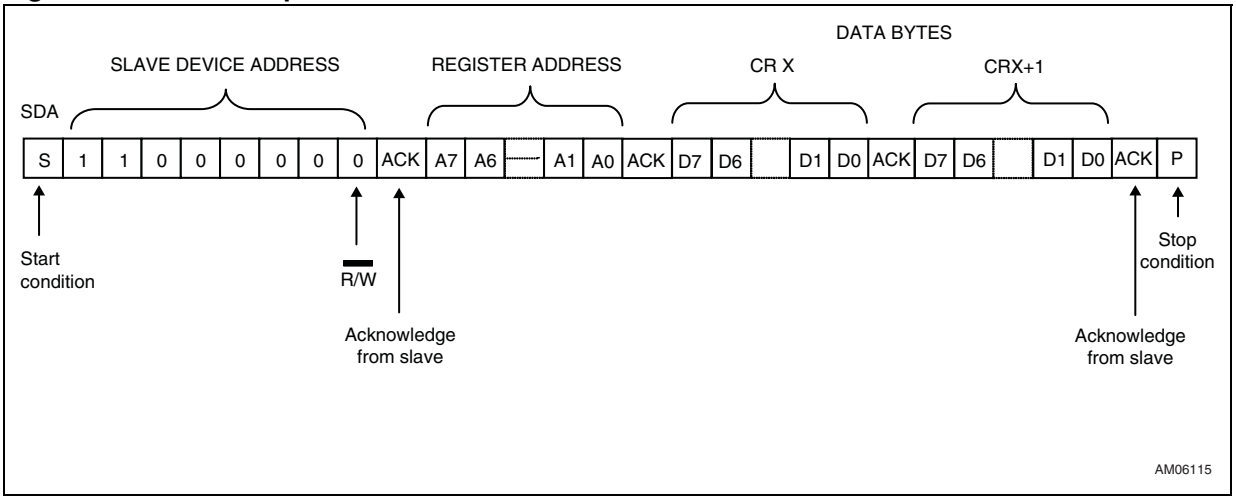
Writing to the control registers

To write data to the TS4621B, after the "start" message the MCU must:

- send the I²C 7-bit slave address and a low level for the R/$\overline{W}$ bit.
- send the register address to write to.
- send the data bytes (control register settings).

All bytes are sent MSB first. The transfer of written data ends with a "stop" message. When transmitting several data bytes, the data can be written without having to repeat the "start" message or send the byte with the slave address. If several bytes are transmitted, they will be written repeatedly to CR1, CR2 and CR3.

Figure 72. I²C write operations



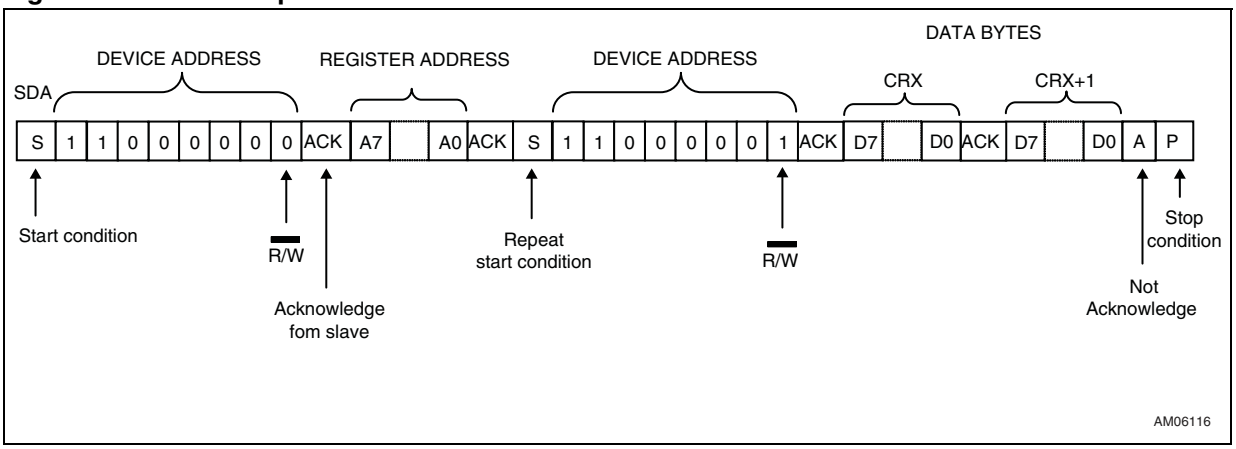
Reading from the control registers

To read data from the TS4621B, after the "start" message the MCU must:

- send the I²C 7-bit slave address and a low level for the R/$\overline{W}$ bit.
- send the register address to read.
- send the I²C 7-bit slave address and a high level for the R/$\overline{W}$ bit.
- receive the data (control register value).

All bytes are read MSB first. The transfer of read data ends with a "stop" message. When transmitting several data bytes, the data can be read without having to repeat the "start" message or send the byte with the slave address. If several bytes are transmitted, they are read repeatedly from CR1, CR2, CR3 and CR4.

Figure 73. I²C read operations1



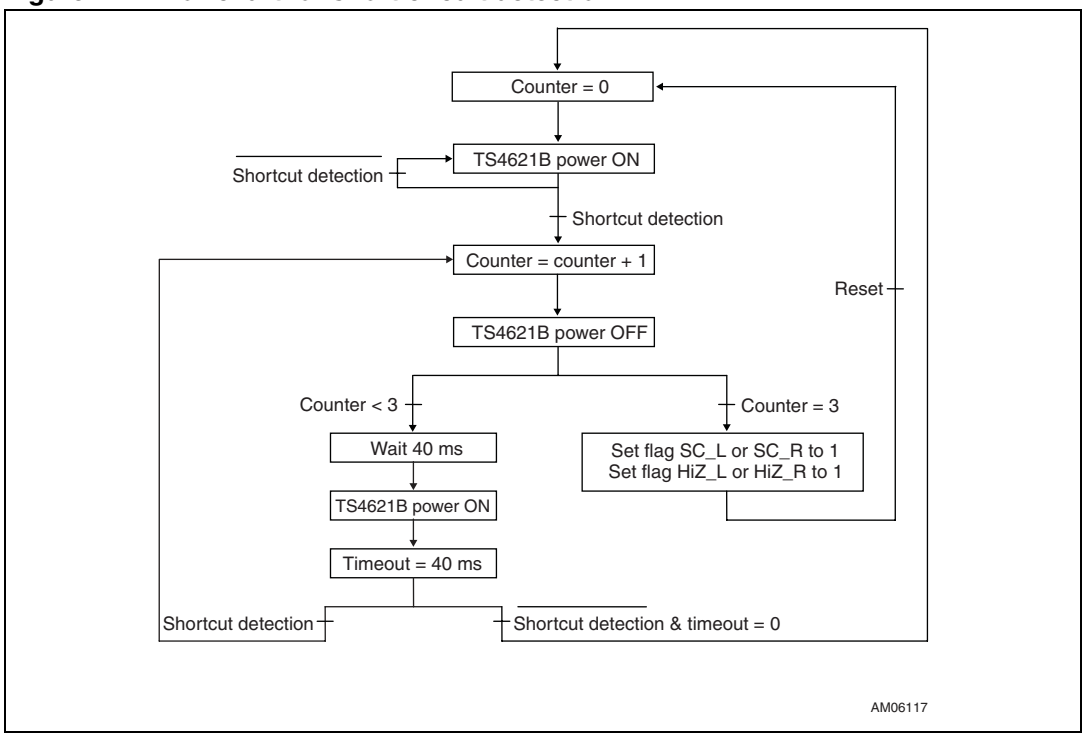
4.1.2 Control register CR1 - address 1

Amplifier output short-circuit detection: bits SC_L and SC_R

The amplifier's outputs are protected from short-circuits that might accidentally occur during manipulation of the device. In a typical application, if a short-circuit arises on the jack plug, there will be no detection because of the serial resistor present on the amplifier output, thus the output current threshold will not be reached.

To be active, the detection has to occur directly on the amplifier's output with a signal modulation on the inputs of the TS4621B. This detection is depicted in *Figure 74*.

Figure 74. Flowchart for short-circuit detection



If a short-circuit is detected three consecutive times on one channel, a flag is raised in the I²C read register CR1.

- SC_L: equals 0 during normal operation, equals 1 when a short-circuit is detected on the left channel.
- SC_R: equals 0 during normal operation, equals 1 when a short-circuit is detected on the right channel.

The corresponding channel's output stage is then set to high impedance mode. An I²C read command allows the reading of the SC_L and SC_R flags but does not reset them. An I²C write command has to be sent to CR1 to reset the flags to 0 and restore normal operation.

Thermal shutdown protection: bit T_SH

A thermal shutdown protection is implemented to protect the device from overheating. If the temperature rises above the thermal junction of 150°C, the device is put into standby mode and a flag is raised in the read register CR1.

- T_SH: equals 0 during normal operation, equals 1 when a thermal shutdown is detected.

When the temperature decreases to safe levels, the circuit switches back to normal operation and the corresponding flag is cleared.

Software shutdown: bit SWS

When SWS equals 1, the device is set to I²C software shutdown. When SWS equals 0, the negative supply and buck converters are activated.

Channel activation: bits HP_EN_L and HP_EN_R

When HP_EN_L or HP_EN_R equals 1, the corresponding amplifier channel is enabled.

4.1.3 Control register CR2 - address 2

Table 12. Volume control register CR2 - address 2

Volume control range: -60 dB to +4 dB												
D5	D4	D3	D2	D1	Gain (in dB)		D5	D4	D3	D2	D1	Gain (in dB)
0	0	0	0	0	-60 dB		1	0	0	0	0	-11 dB
0	0	0	0	1	-54 dB		1	0	0	0	1	-10 dB
0	0	0	1	0	-50.5 dB		1	0	0	1	0	-9 dB
0	0	0	1	1	-47 dB		1	0	0	1	1	-8 dB
0	0	1	0	0	-43 dB		1	0	1	0	0	-7 dB
0	0	1	0	1	-39 dB		1	0	1	0	1	-6 dB
0	0	1	1	0	-35 dB		1	0	1	1	0	-5 dB
0	0	1	1	1	-31 dB		1	0	1	1	1	-4 dB
0	1	0	0	0	-27 dB		1	1	0	0	0	-3 dB
0	1	0	0	1	-25 dB		1	1	0	0	1	-2 dB
0	1	0	1	0	-23 dB		1	1	0	1	0	-1 dB
0	1	0	1	1	-21 dB		1	1	0	1	1	0 dB
0	1	1	0	0	-19 dB		1	1	1	0	0	+1 dB
0	1	1	0	1	-17 dB		1	1	1	0	1	+2 dB
0	1	1	1	0	-15 dB		1	1	1	1	0	+3 dB
0	1	1	1	1	-13 dB		1	1	1	1	1	+4 dB

Mute function: bits MUTE_L and MUTE_R

In the volume register, MUTE_L and MUTE_R are dedicated to enabling the mute function, independently of the channel. When MUTE_L and MUTE_R are set to 1, the mute function is enabled on the corresponding channel and the gain is set to -80 dB. When MUTE_L and MUTE_R are set to 0, the I²C gain level is applied to the channel.

4.1.4 Control register CR3 - address 3

High output impedance mode: bits HiZ_L and HiZ_R

The TS4621B features a high-output impedance mode used, for example, to share the headphone jack with the audio and composite video signal.

To set this mode, you must set the HIZ bit to 1 for the targeted output in the CR3 register.

At this time, the considered output is in high-impedance mode with the following characteristics:

- Maximum input voltage = -1.8 to +1.8 V
- Output impedance = input impedance detected by the video driver. For an example, refer to *Chapter 3: Electrical characteristics on page 10* or *Figure 18*.

4.1.5 Summary of output impedance

Table 13. Summary table for output impedance vs. output mode

SWS	HiZ	HP_EN	Output impedance	Maximum voltage allowed on output pin
1	0	0	20 to 40 Ω	Less than ± 100 mV
1	0	1	20 to 40 Ω	Less than ± 100 mV
1	1	0	about 10 kΩ	-0.3 V to AVdd
1	1	1	about 10 kΩ	-0.3 V to AVdd
0	0	0	20 to 40 Ω	Less than ± 100 mV
0	0	1	Less than 1 Ω	Not applicable
0	1	0	See *Figure 18*	-1.8 to +1.8 V
0	1	1	See *Figure 18*	-1.8 to +1.8 V

4.2 Wake-up and standby time definition

The wake-up time of the TS4621B is guaranteed at 12 ms typical (refer to *Chapter 3: Electrical characteristics*). However, since the TS4621B is activated with an I^2C bus, the wake-up start procedure is as follows.

1. The master sends a start bit.
2. The master sends the device address.
3. The slave (TS4621B) answers by an acknowledge bit.
4. The master sends the register address.
5. The slave (TS4621B) answers by an acknowledge bit.
6. The master sends the output mode configuration (CR1).
7. If the TS4621B was previously in standby mode, the wake-up starts on the falling edge of the eighth clock signal (SCL) corresponding to the CR1 byte.
8. After 12 ms (de-pop sequence time), the TS4621B outputs are operational.

The standby time is guaranteed as 100 µs typical (refer to *Chapter 3*). However, since the TS4621B is de-activated with an I^2C bus, the standby time operates as follows.

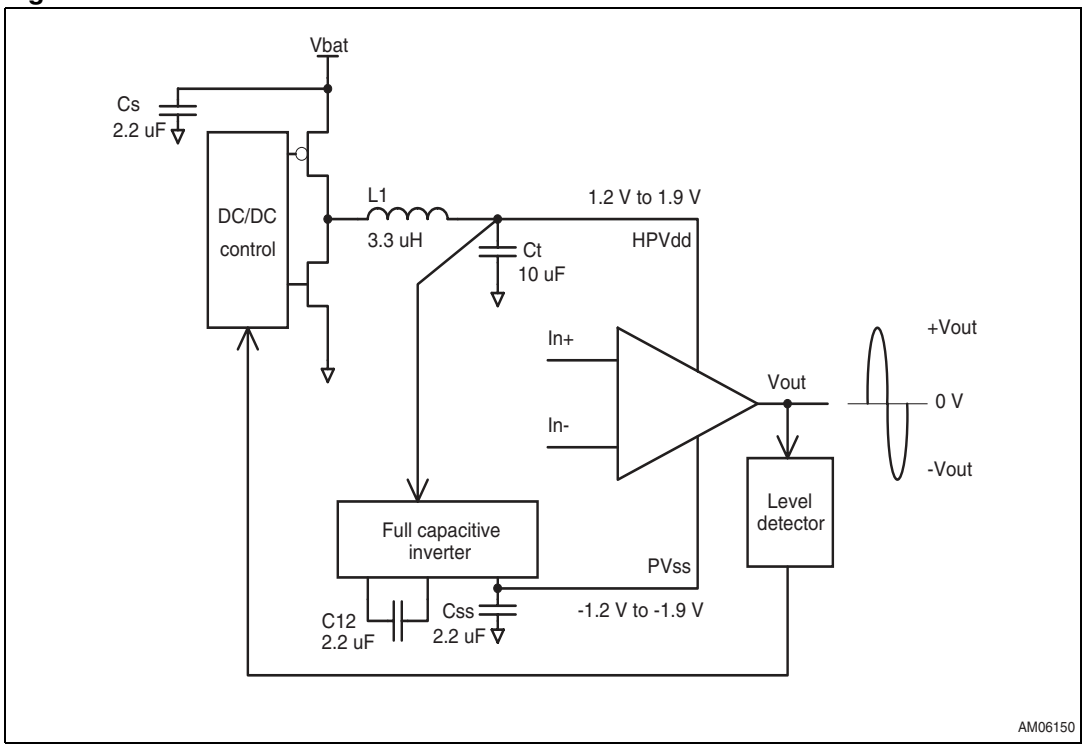
1. The master sends a start bit.
2. The master sends the device address.
3. The slave (TS4621B) answers by an acknowledge bit.
4. The master sends the register address.
5. The slave (TS4621B) answers by an acknowledge bit.
6. The master sends the output mode configuration (CR1), which corresponds, in this case, to standby mode.
7. The standby time starts on the falling edge of the eighth clock signal (SCL) corresponding to the CR1 byte.
8. After 100 µs, the TS4621B is in standby mode.

4.3 Overview of the class-G, 2-level headphone amplifier

The TS4621B uses what is referred to as *class-G operating mode*. This mode is a combination of the class-AB biasing technique and an adaptive power supply. For this device, the power supply uses two levels: ±1.2 V and ±1.9 V.

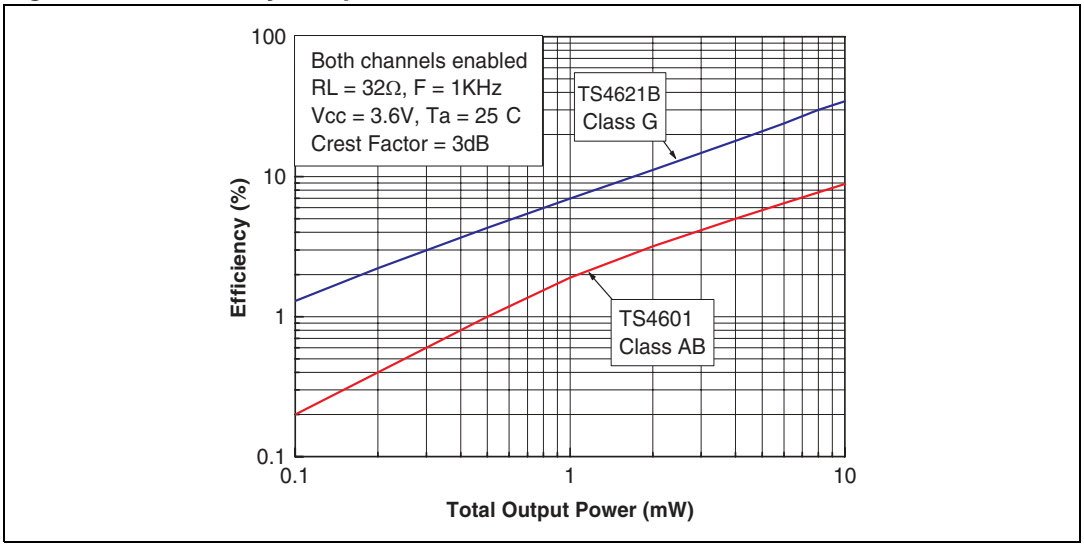
To create the ±1.2 V and ±1.9 V levels, the device uses an internal high-efficiency step-down converter linked with a fully capacitive inverter from AVdd. Thanks to these internally-generated symmetrical power supply voltages, the output of the amplifier can be biased at 0 V, thus eliminating the classical bulky DC blocking output capacitors (typically more than 100 µF).

Figure 75. TS4621B architecture



When an audio signal is playing with the TS4621B, the class-G feature adjusts in real time the internal power supply voltage in order to achieve the best efficiency possible. In addition, thanks to the fast transient response of the internal DC/DC converters, the switching between ±1.2 V and ±1.9 V can be achieved without audio clipping. Moreover, the out-of-audio band DC/DC switching frequency keeps the audio quality at a high level (distortion, noise, etc…).

Figure 76. Efficiency comparison

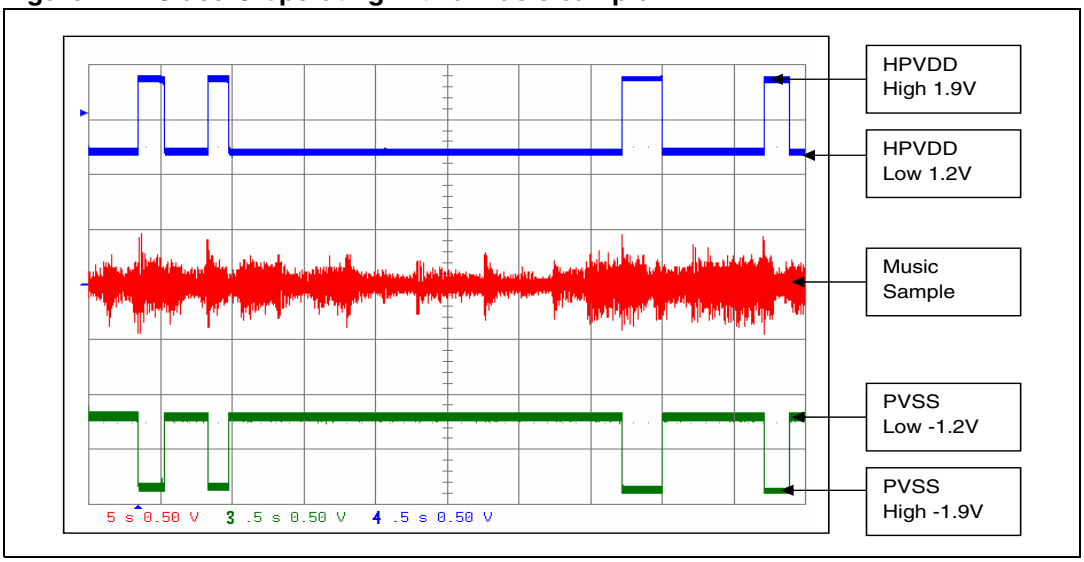


Most audio signals have a crest factor higher than 6 dB (10 dB on average), which means that most of the time the music level is low. In this case, the setting of the internal DC/DC converters is low (1.2 V) and in this way, helps to minimize the power dissipation.

When the audio signal amplitude increases due to a peak or louder music, the setting of the internal DC/DC converters increases to 1.9 V, automatically increasing the output dynamic range. This 1.9 V value remains until the end of the decay time.

Figure 77 shows a music sample played at high levels.

Figure 77. Class-G operating with a music sample



Note: HPVDD/PVSS voltages are created internally by DC/DC converters. To avoid destruction of the TS4621B power amplifier, do not connect any external power supply on these pins.

4.4 External component selection

The TS4621B requires few external passive components to operate correctly. Each component is described in the following sections.

4.4.1 Step-down inductor selection (L1)

The TS4621B needs one inductor for the internal step-down DC/DC converter. This inductor must fit the following constraints:

- Typical value: 2.2 µH to 3.3 µH (3.3 µH is recommended).
- Maximum current in operating mode: 400 mA
- Minimum inductor value at maximum current: 1.5 µH
- Maximum inductor value at zero current: 4.3 µH
- DC resistance: from 50 mΩ up to 450 mΩ

Table 14 shows the part number that should be used according to the inductor value.

Table 14. Recommended inductor

Manufacturer	Part number	Value
Murata	LQM21PN3R3NGRD	3.3 µH
	LQM2MPN3R3G0L	3.3 µH
	LQM2MPN2R2G0L	2.2 µH
FDK	MIPSZ2012D3R3	3.3 µH
	MIPSZ2012D2R2	2.2 µH

4.4.2 Step-down output capacitor selection (Ct)

For the internal DC/DC step-down converter, the TS4621B needs one output capacitor.

The three criteria for selecting the output capacitor are the range value of the capacitor including self tolerance, DC variation and the minimum ESR value, which is mandatory to avoid oscillation of the converter. Therefore the following constraints must be observed.

- Typical capacitor value: 10 µF at DC = 0 V
- Maximum capacitor value: 12 µF at DC = 0 V
- Minimum capacitor value: 4.8 µF at DC = 2 V
- Voltage range across this capacitor: from 1.1 V to 2 V
- Minimum DC ESR value: 5 mΩ

A ceramic capacitor in a 0603-type package is also recommended because of its close placement to the TS4621B, which makes it easier to minimize parasitic inductance and resistance that have a negative impact on the audio performance.

Table 15. Recommended capacitor

Manufacturer	Part number	Value
Murata	GRM188R60J106ME47	10 µF, 6.3 V, X5R
	GRM188R60J106ME84	10 µF, 6.3 V, X5R
	GRM188R61E106ME73	10 µF, 25 V, X5R

4.4.3 Full capacitive inverter capacitors selection (C12 and Css)

Two capacitors (C12 and Css) are needed for this internal DC/DC inverter.

The three criteria for selecting theses capacitors are the range value of the capacitor including self tolerance, DC variation and the minimum ESR to minimize power losses.

- Typical capacitor value: 2.2 µF +/-20 %
- Voltage across these capacitors: from 1.1 V to 2 V
- Minimum capacitor value: 1 µF

Again, a ceramic capacitor in a 0603 or 0402-type package is also recommended because of their close placement to the TS4621B, which makes it easier to minimize parasitic inductance and resistance that have a negative impact on the audio performance.

4.4.4 Power supply decoupling capacitor selection (Cs)

A 2.2 µF decoupling capacitor with low ESR is recommended for positive power supply decoupling. Packages such as the 0402 or 0603 are also recommended because of their close placement to the TS4621B, which makes it easier to minimize parasitic inductance. It is advised to choose a X5R dielectric for capacitor tolerance, and a 10 V DC rating voltage for 4.8 V operations (or a 6.3 V DC rating voltage for 3.6 V operations), to take into consideration the $\Delta C/\Delta V$ variation of this type of ceramic capacitor.

An important parameter is the rated voltage of the capacitor. A 2.2 µF/6.3 V capacitor used at 4.8 V DC typically loses about 40 % of its value. In fact, with a 4.8 V power supply voltage, the decoupling value is about 1.3 µF instead of 2.2 µF. Because the decoupling capacitor influences the THD+N in the medium-to-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply's AMR value (5.5 V). This is why, for a 2.2 µF value, we recommend a 2.2 µF/10 V, a 4.7 µF/6.3 V or a ceramic capacitor with a low DC bias variation rated at 6.3 V.

4.4.5 Input coupling capacitor selection (Cin)

Cin input coupling capacitors are mandatory for the TS4621B's operation. They block any DC component coming from the audio signal source.

Cin with Rin form a first-order high-pass filter and the -3 dB cutoff frequency is:

$$FC(-3dB) = \frac{1}{2 \times \pi \times Rin \times Cin}$$

Rin is the single-ended input impedance that can be approximated at about Rindiff/2.

Rin also depends on the gain setting. *Figure 19* provides the differential input impedance vs. gain. One can also see that Rindiff is minimum for the maximum gain setting (that is, 4 dB).

Therefore, in most cases, Rin should be set to 4 dB to calculate the minimum input capacitor Cin.

Example:

At maximum gain G = 4 dB, Rindiff/2 = kΩ/2 = 17 kΩ. However, to take into consideration the worst case, one has to use Rindiff/2 = 25 kΩ/2 = 12.5 kΩ.

In this case and for a -3 dB cutoff frequency of 20 Hz, Cin = 0.64 µF. The closest normalized value is 0.68 µF but a 1 µF capacitor is more suitable to take into consideration the capacitor tolerance +/-20 %.

If the aim is to have the 20 Hz at -1 dB, the capacitor has to be multiplied by 1.96. As such, Cin = 0.64 x 1.96 = 1.25 µF. The closest normalized value would be 1.5 µF or 2.2 µF.

4.4.6 Low-pass output filter (Rout and Cout) and IEC 61000-4-2 ESD protection

The TS4621B is designed to operate with a passive first-order low-pass filter (as shown in *Figure 1.*). This low-pass filter is mandatory to ensure correct operation of the TS4621B over the volume range and output capacitance range vs. load.

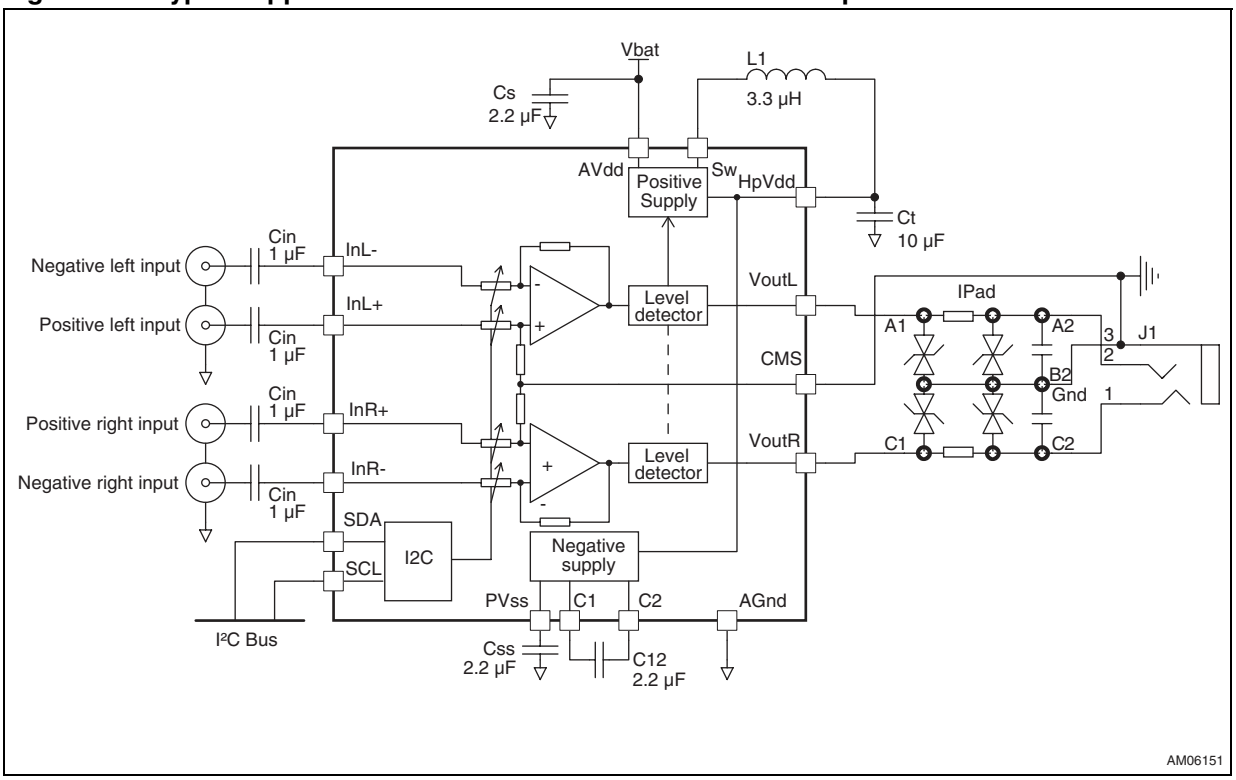
Rout must have a value of 12 Ω minimum and Cout a value of 0.8 nF minimum up to 100 nF maximum. Values of 12 Ω and 1 nF are a good starting point for a design to be able to drive a classic headphone (16 Ω, 32 Ω, 60 Ω) and the line-in of any Hi-fi system or sound card. The cutoff frequency of this filter (12 Ω and 1 nF) is approximately 13 MHz and clearly above the audio band.

However, this output RC filter is also a part of the IEC 61000-4-2 ESD protection. In most cases, this RC filter is designed with transient absorbers and the final solution can be a discrete solution or an integrated solution. ST Microelectronics' portfolio has many integrated solutions for ESD, but one dedicated to headphone amplifiers in particular: IPAD[(a)] reference EMIF02-AV01F3.

To fit the IEC 61000-4-2 standard, this audio line IPAD can be added to the output of the TS4621B as shown in *Figure 78*.

a. Copyright STMicroelectronics.

Figure 78. Typical application schematic with IEC 61000-4-2 ESD protection



By adding this ESD protection, the TS4621B complies with the IEC 61000-4-2 level 4 standard on jack pins. Our demonstration board has been tested using the same conditions as those outlined in the IEC 61000-4-2 standard. Results may differ depending on the layout of the PCB.

- 15 kV (air discharge)
- 8 kV (contact discharge)

This IPAD has an internal series resistor Rout = 15 Ω +/-20 % and an output capacitor Cout = 3.2 nF +/-25 %.

4.4.7 Integrated input low-pass filter

The TS4621B has an integrated internal first-order low-pass filter with a -3 dB cutoff frequency set at 65 kHz and independent of the volume position. This integrated filter is present on each input and filters any out-of-band audio noise coming from the audio source.

4.5 Single-ended input configuration

The TS4621B can be used in a single-ended input configuration. InR- and InL- or InR+ and InL+ can be shorted to ground through input capacitors. All Cin capacitors must have the same value to keep the same PSRR performance as in a differential input configuration. *Figure 79* and *Figure 80* show how to connect the TS4621B. Note the ground connection of each input. To avoid PSRR issues resulting from any ground noise, this connection must be done on the ground of the audio source and not on the ground of the TS4621B itself.

Figure 79. Single-ended input configuration1

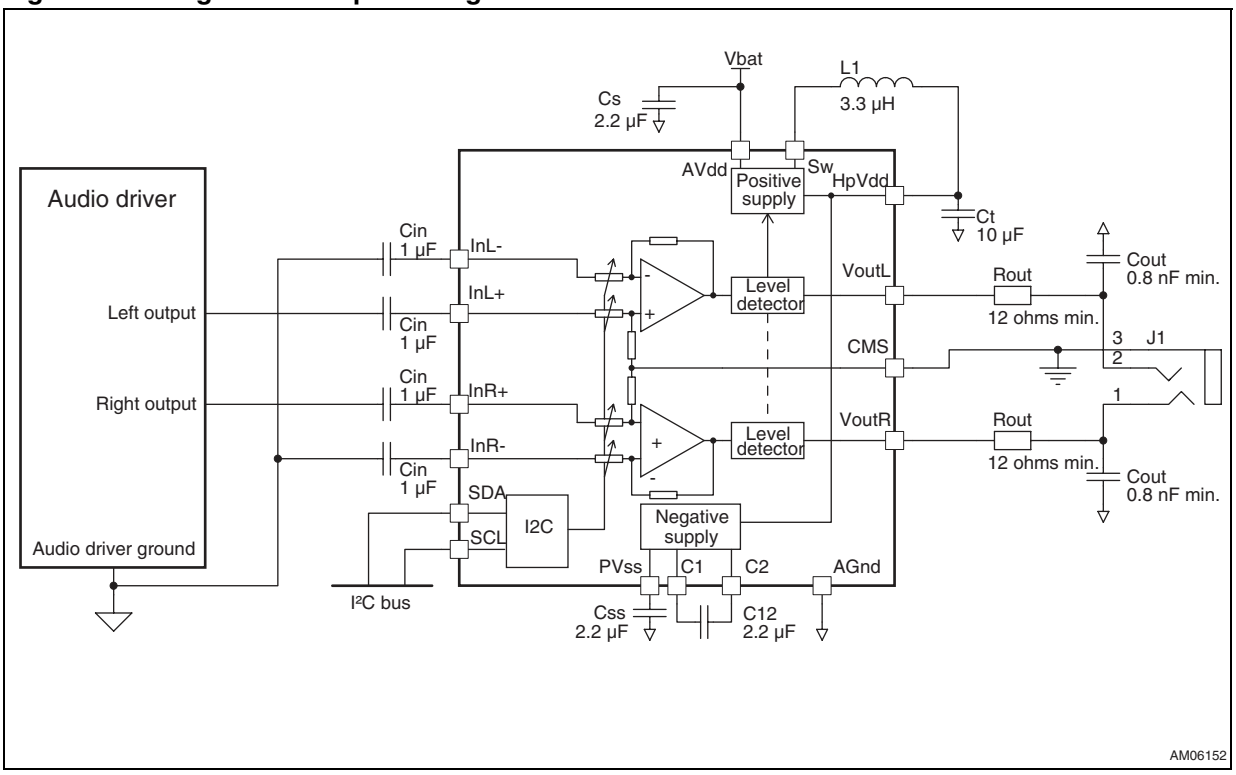
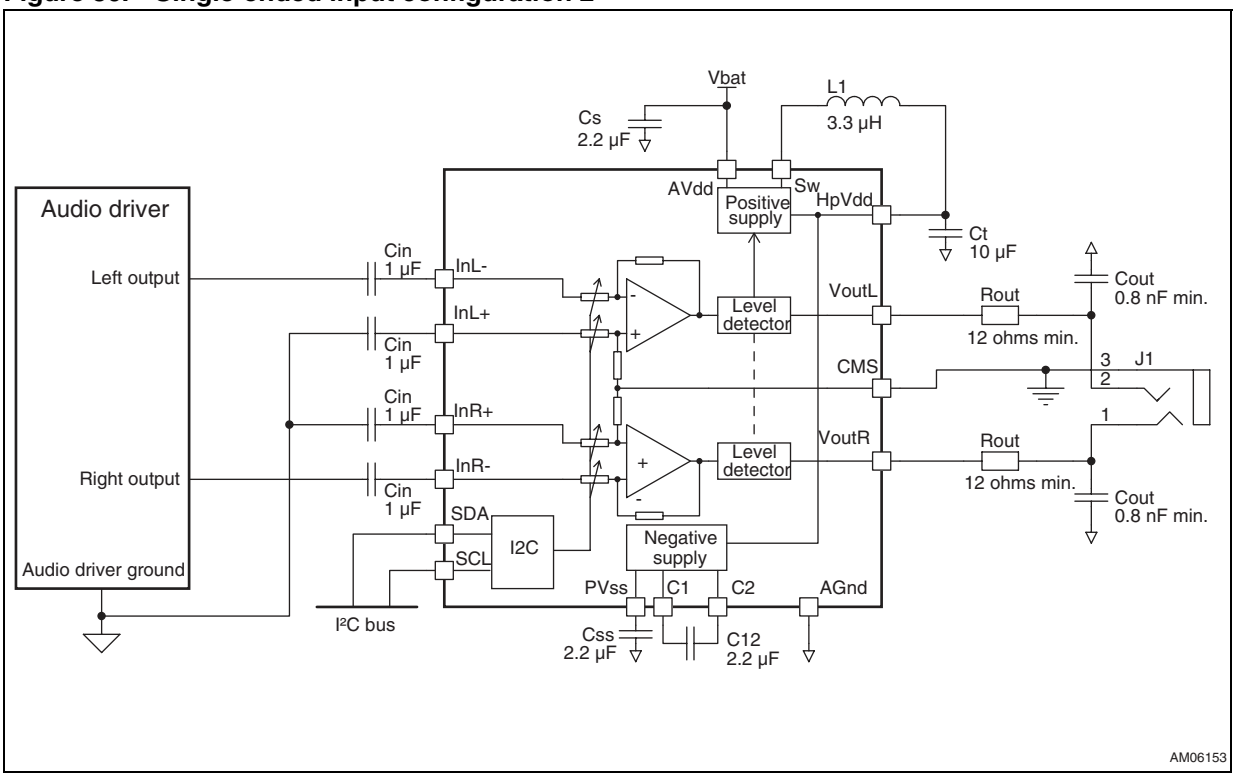


Figure 80. Single-ended input configuration 2



The gain range in these configurations remains unchanged and is given by:

$$VoutLR = VinLR \times Gain$$

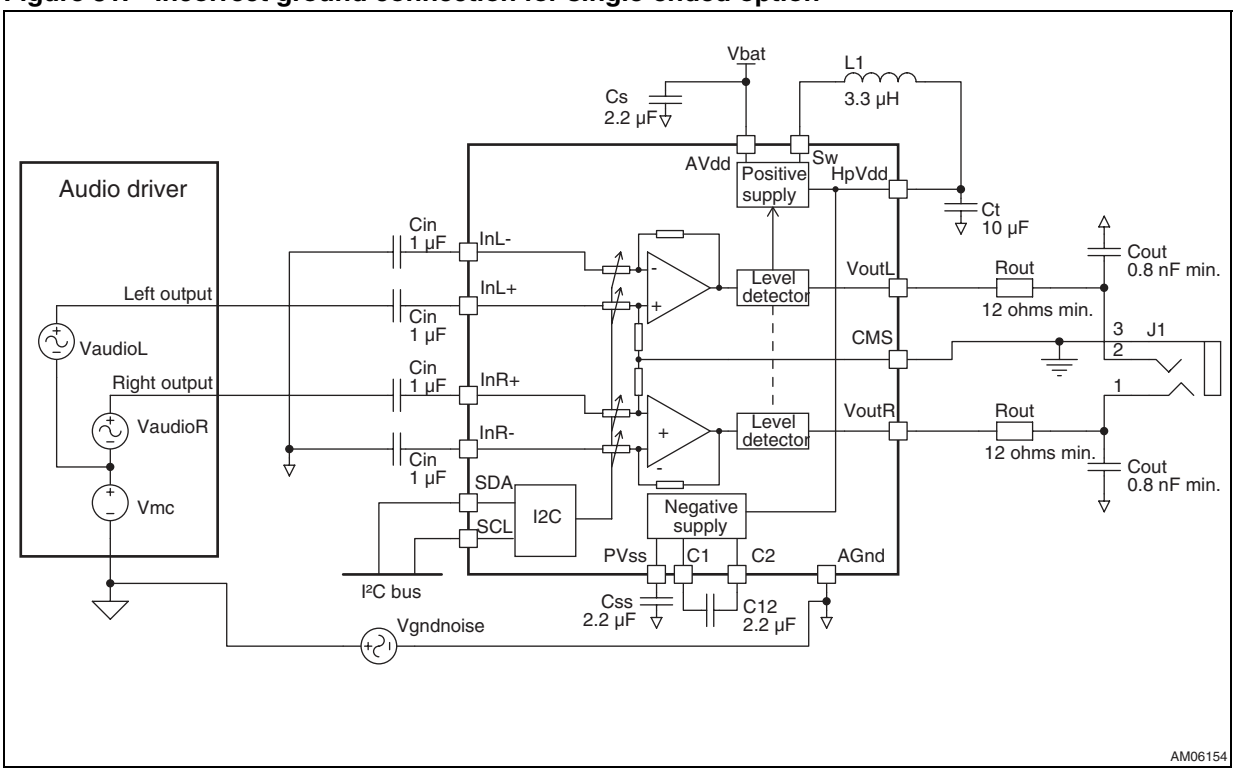
With reference to *Figure 80.*, note that the absolute phase in the audio band is 180°.

4.5.1 Layout recommendations for single-ended operation

The connection location of each input that has to be set to ground is extremely important.

Incorrect connection location

Figure 81. Incorrect ground connection for single-ended option



If these inputs are connected to AGnd (the ground of the TS4621B class-G), the output voltage can be expressed by the following simplified equation from an AC point of view.

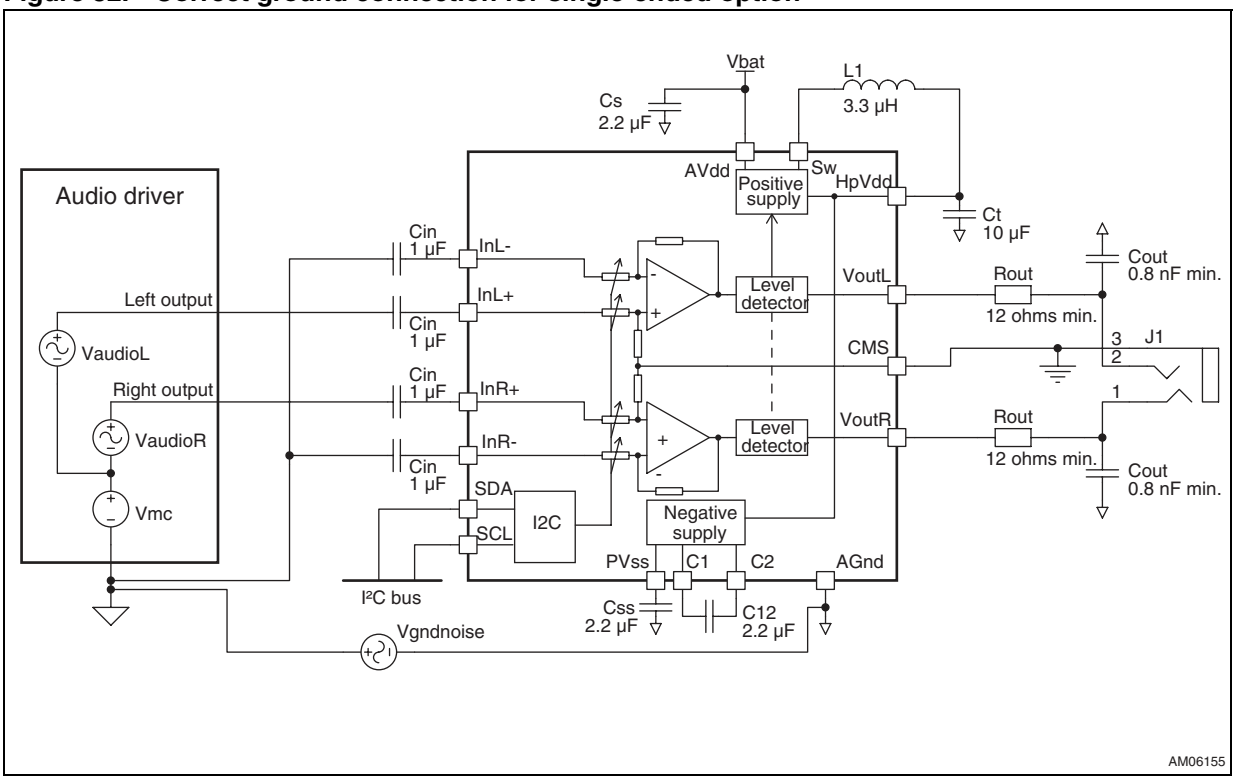
Vout = Av x (Vaudio + Vmc + Vgndnoise) + Vbatnoise x PSRR (1)

As shown in Equation (1), any ground noise and any parasitic AC voltage on Vmc is directly multiplied by the gain of the amplifier. If Vmc can be totally controlled by the design of the audio source device (no parasitic AC voltage), it is not necessarily the case for Vgndnoise. This noise can be significantly reduced by an adequate low impedance ground plane, but not totally eliminated. In practice, only ten millivolts in the right frequency range are enough to produce an audible parasitic sound in the headphone with a volume level as low as -20 dB.

Correct connection location

As shown in *Figure 82*, the best option is to route the single-ended signal in parallel with the AC ground line of the other input. The AC grounded terminal must be routed in parallel to the audio signal and grounded with the ground of the audio source.

Figure 82. Correct ground connection for single-ended option



In this configuration, the AC output voltage is:

Vout = Av x (Vaudio + Vmc) + Vgndnoise x CMRR + Vbatnoise x PSRR (2)

In equation (2), the ground noise is attenuated by the performance of the CMRR. In practice, 50 dB of CMRR and ten millivolts for ground noise gives an output of approximately 30 µV, which is normally too low to be perceptible in the headphone. If Vmc is also totally controlled by the design of the audio source, equation (2) becomes:

Vout = Av x Vaudio + Vbatnoise x PSRR (3)

Like in differential mode, the main contributor for audio signal degradation is the AC noise voltage on Vbat. Thanks to the TS4621B's very high PSRR that can attenuate GSM burst noise, equation (3) becomes:

Vout = Av x Vaudio (4)

4.6 Startup phase

The TS4621B uses different techniques to reduce the DC current consumption and offer a pop-and-click performance close to none.

4.6.1 Auto zero technology

During the start-up phase, the differential output voltage is sensed and adjusted to 0 V (+/-500 µV) to avoid any pop noise when the amplifier becomes operational. This also helps to minimize extra current consumption due to the load (Icc-extra = VoutDC / Rload).

4.6.2 Input impedance

The TS4621B requires input coupling capacitors. The usual lowest frequency used for the headphone is close to 20 Hz. This frequency means a constant time for a first-order high-pass filter of approximately 1 / (2 x Pi x 20) = 8 ms.

To achieve 95 % of the capacitor's charge, it is necessary to wait 3 x 8 ms = 24 ms, which is out of range for a device with a fast start-up time.

Because of the mismatching of all input capacitors and input resistors, if it is decided to start the TS4621B at a time of 8 ms, a voltage difference at the inputs (multiplied by the gain) can create a voltage step on the output and consequently a pop noise.

To avoid this issue during the starting phase, the TS4621B accelerates the charging of the input capacitors by reducing the input impedance to 2 kΩ.

In such a case, for a 1 µF capacitor the 95 % charge is reached in 6 ms. As the start-up time of TS4621B is 12 ms, there remains sufficient time to fully charge the input capacitors and as such eliminate any pop noise.

4.7 Layout recommendations

Particular attention must be given to the correct layout of the PCB traces and wires between the amplifier, load and power supply (in most cases, the battery of the cellular phone).

The power and ground traces are critical since they must provide adequate energy and grounding for all circuits. Good practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

A track with a width of at least 200 µm for a copper thickness of 18 µm is recommended for bringing energy to the amplifier from the battery.

Proper grounding guidelines help improve audio performances, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. It is also recommended to use a large-area and multi-via ground plane to minimize parasitic impedance.

A multi-layer PCB board allows double or multiple ground planes to be implemented. Most of the time, the top and bottom layers are used as ground planes and provide shielding for tracks routed on the intermediate layers. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

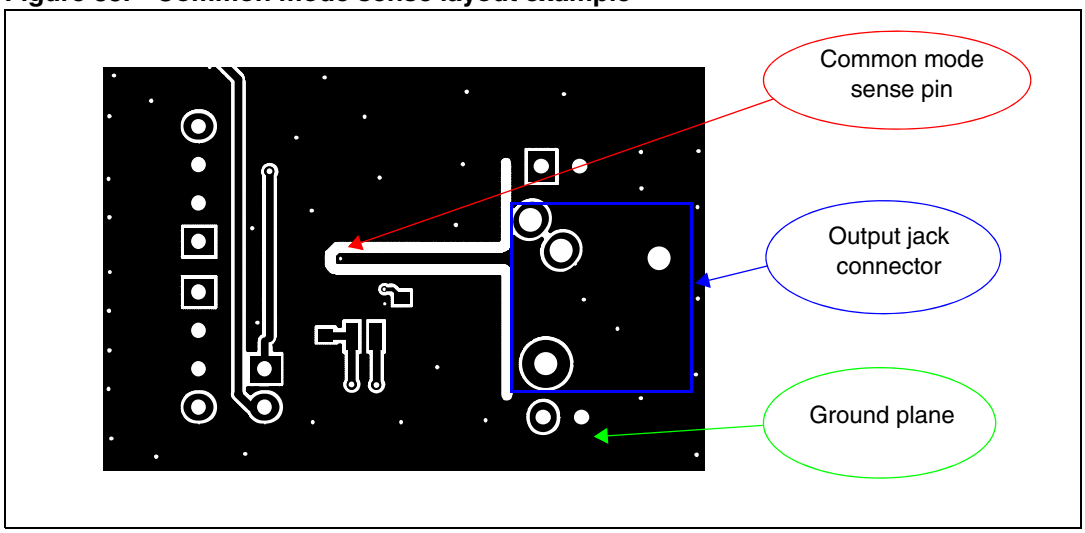
The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize the trace resistances.

4.7.1 Common mode sense layout

The TS4621B implements a common-mode sense pin to correct any voltage differences that might occur between the return of the headphone jack and the AGND of the device that can create parasitic noise in the headphone and/or line out.

The solution to strongly reduce and practically eliminate this noise consists in connecting the headphone jack ground to the CMS pin. This pin senses the difference of potential (voltage noise) between the TS4621B ground and the headphone ground. Thanks to the frequency response and the attenuation of the common-mode sense pin, this noise is removed from the TS4621B outputs.

Figure 83. Common mode sense layout example



4.8 Demonstration board

A demonstration board is available at *www.st.com* with the order code STEVAL-CCA025V1. The following figures show the demonstration board schematics and associated PCB layouts.

Figure 84. Demonstration board schematic

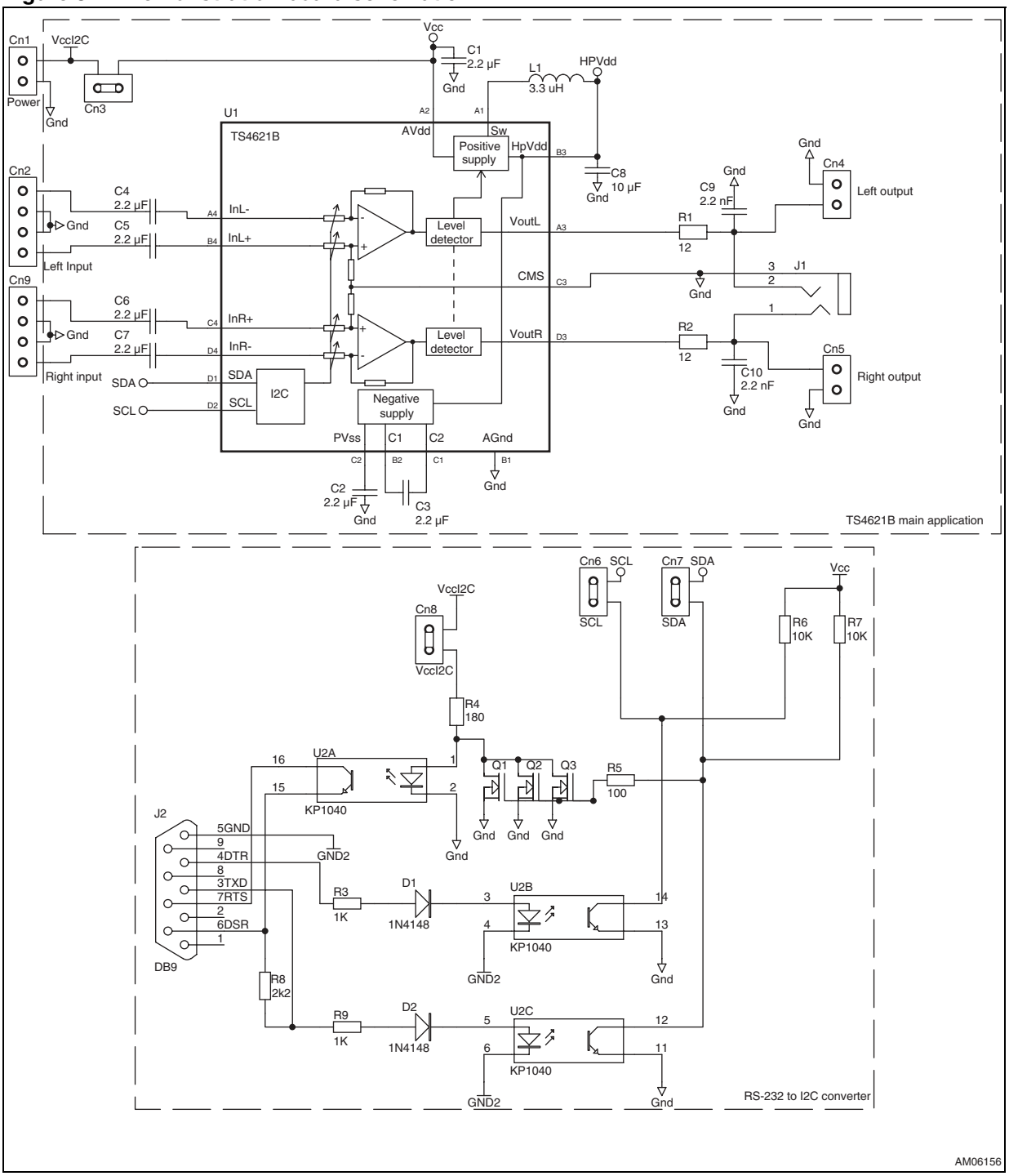


Figure 85. Copper layers

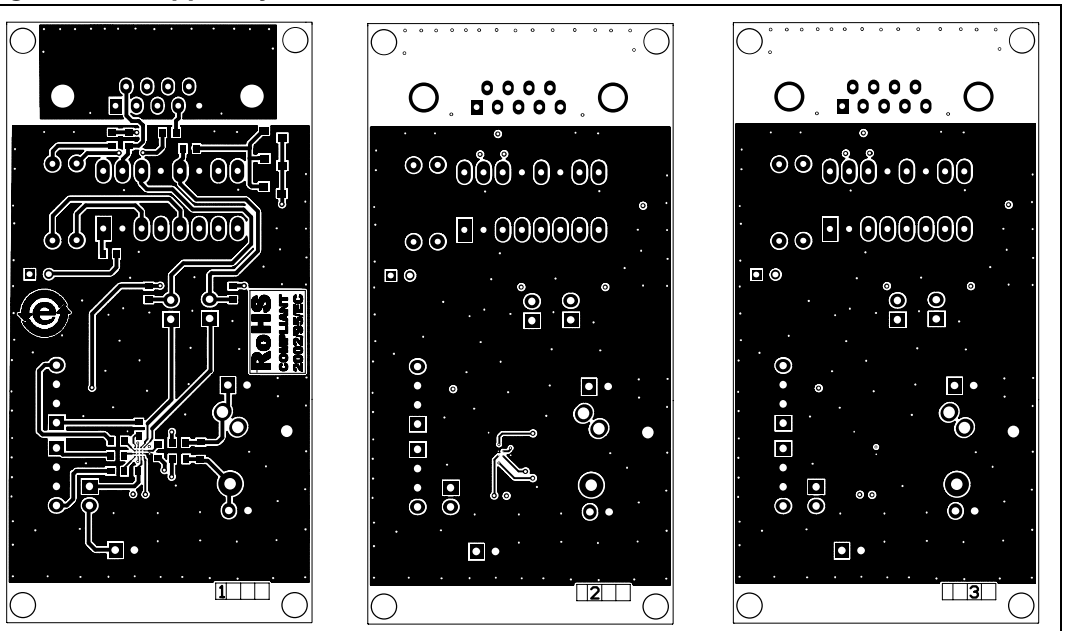
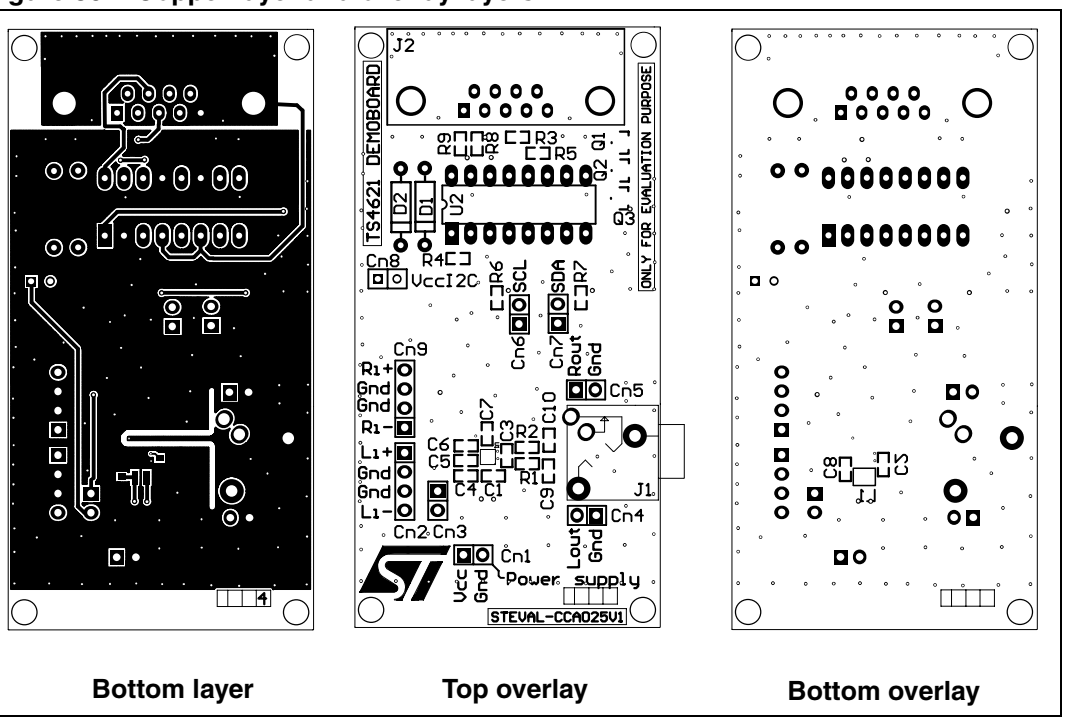


Figure 86. Copper layer and overlay layers



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 87. TS4621B footprint recommendation

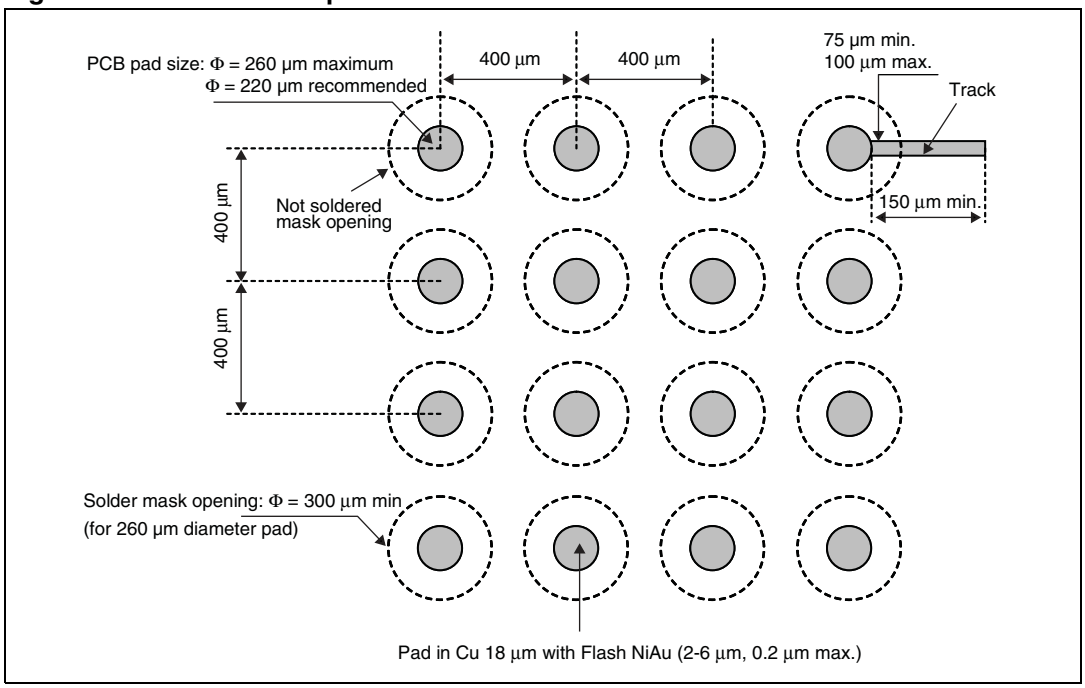


Figure 88. Pinout

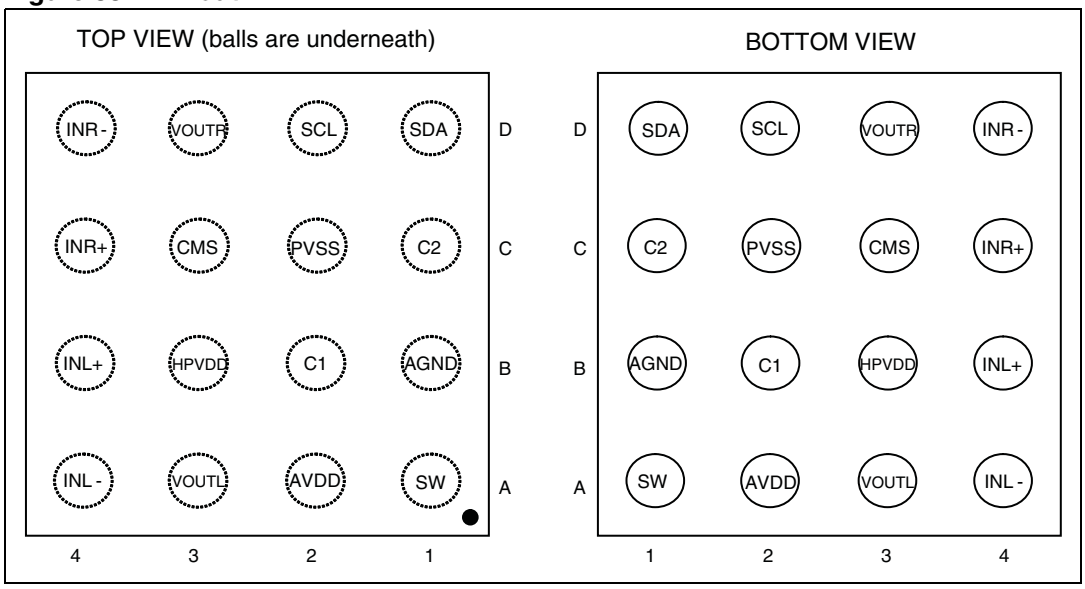


Figure 89. Marking (top view)

- Logo: ST
- Symbol for lead-free: E
- Part number: 21
- X digit: Assembly code
- Date code: YWW
- The dot marks pin A1

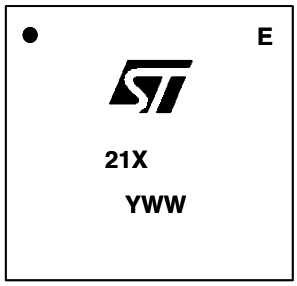
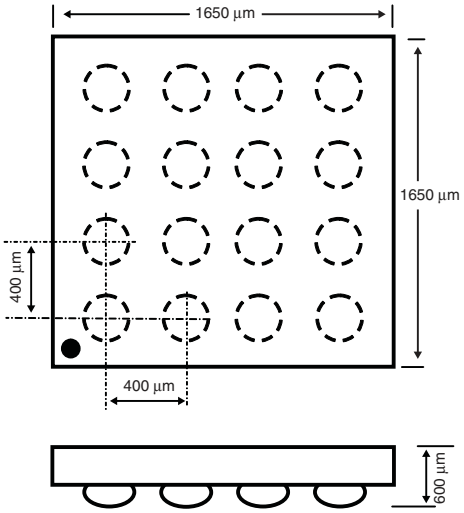
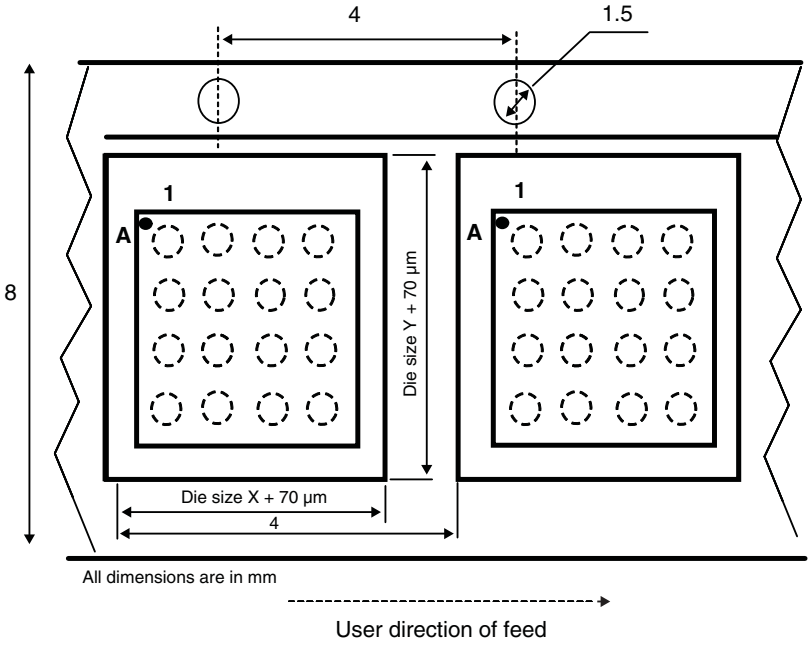


Figure 90. Flip-chip - 16 bumps



- Die size: 1.65 mm x 1.65 mm ± 30 µm
- Die height (including bumps): 600 µm ±55 µm
- Bump diameter: 250 µm ±40 µm
- Bump height: 205 µm ±35 µm
- Die height: 395 µm ±20 µm
- Pitch: 400 µm ±40 µm
- Coplanarity: 50 µm max

Figure 91. Device orientation in tape pocket



6 Ordering information

Table 16. Order codes

Order code	Temperature range	Package	Packing	Marking
TS4621BEIJT	-40°C to +85°C	Flip-chip	Tape & reel	21

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
06-Sep-2011	1	Initial release.
12-Sep-2011	2	Updated *Table 10: Summary of control registers on page 25* Updated *Section 4.1.2: Control register CR1 - address 1 on page 27*

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