TPD8S009 8-Channel ESD Protection for DisplayPort and HDMI

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV Contact Discharge
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8 / 20 µs)
- I/O Capacitance: 0.8 pF (Typical)
- Low Leakage Current: 10 nA (Typical)
- Supports High-Speed Differential Data Rates (3-dB Bandwidth > 4 GHz)
- I_{off} Feature
- Industrial Temperature Range: –40°C to +85°C
- Easy Straight-Through Routing Package for HDMI and DisplayPort Connectors

2 Applications

- End Equipment
  - Set-Top Boxes
  - Laptops and Desktops
  - Projectors
  - Video Surveillance
- Interfaces
  - DisplayPort 1.1
  - HDMI 1.4
  - DVI

3 Description

The TPD8S009 device is an eight-channel TVS diode array for ESD protection. The TPD8S009 is rated to dissipate contact ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4), with ±8-kV contact discharge ESD protection. The low capacitance (0.8 pF) of this device, coupled with the excellent matching between differential signal pairs enables this device to provide transient voltage suppression circuit protection for high-speed idfferential data rates (3-dB bandwidth > 4 GHz).

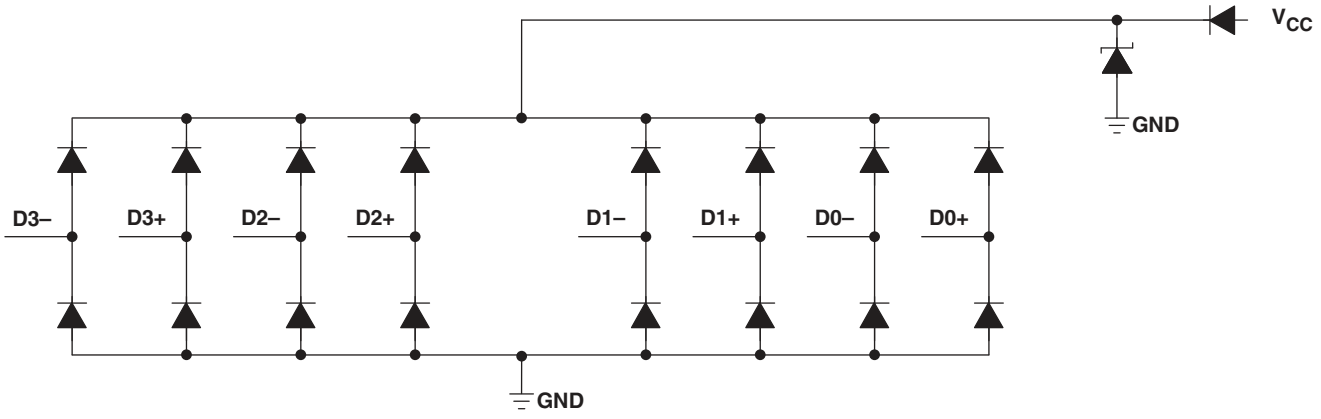
The TPD8S009 is offered in a 8-pin SON package. This package offers easy design and layout, as the package matches exactly with the HDMI and DisplayPort high-speed pinout.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD8S009	SON (15)	2.50 mm × 6.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Internal Schematic



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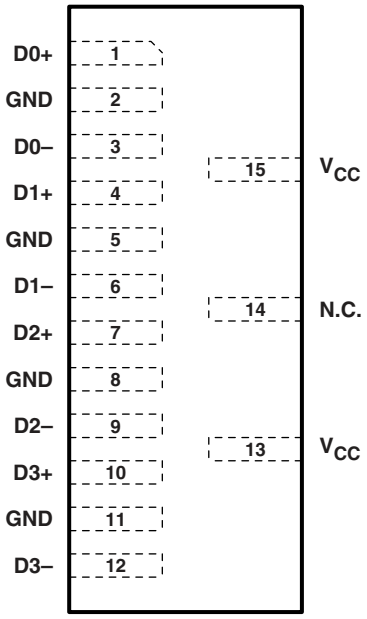
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2008) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted *Ordering Information* table	1
• Removed Lead temperature from *Absolute Maximum Ratings*	4

5 Pin Configuration and Functions

DSM Package
15-Pin SON
Top View



N.C. – Not internally connected

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	D0+	ESD port	High-speed ESD clamp provides ESD protection to the high-speed display port/HDMI differential data lines.
3	D0–		
4	D1+		
6	D1–		
7	D2+		
9	D2–		
10	D3+		
12	D3–		
2	GND	GND	Ground
5			
8			
11			
14	N.C.	No connect	No internal signal connection
13	V_{CC}	Supply	I/O supply
15			

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	IO signal voltage	0	V_{CC}	V
T_A	Characterized free-air operating temperature	–40	85	°C
P_{PP}	Peak pulse power (t_p = 8/20 µs)		25	W
I_{PP}	Peak pulse current (t_p = 8/20 µs)		2.5	A
T_{stg}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		IEC 61000-4-2 Contact Discharge	±8000	
		IEC 61000-4-2 Air-Gap Discharge	±9000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPD8S009 DSM (SON) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	405.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	284.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	284.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse standoff voltage	Any IO pin to ground				5.5	V
V_{BR}	Breakdown voltage	I_{IO} = 1 mA	Any IO pin to ground	9			V
I_{IO}	IO port current	V_{IO} = 3.3 V, V_{CC} = 5 V	Any IO pin		0.01	0.1	µA
I_{off}	Current from IO port to supply pins	V_{IO} = 3.3 V, V_{CC} = 5 V	Any IO pin		0.01	0.1	µA
V_D	Diode forward voltage	I_{IO} = 8 mA	Lower clamp diode	0.6	0.8	0.95	V
R_{DYN}	Dynamic resistance	I = 1 A	Any IO pin		1.1		Ω
C_{IO}	IO capacitance	V_{CC} = 5 V, V_{IO} = 2.5 V	Any IO pin		0.8		pF
I_{CC}	Operating supply current	V_{IO} = Open, V_{CC} = 5 V	V_{CC} pin		0.1	1	µA

6.6 Typical Characteristics

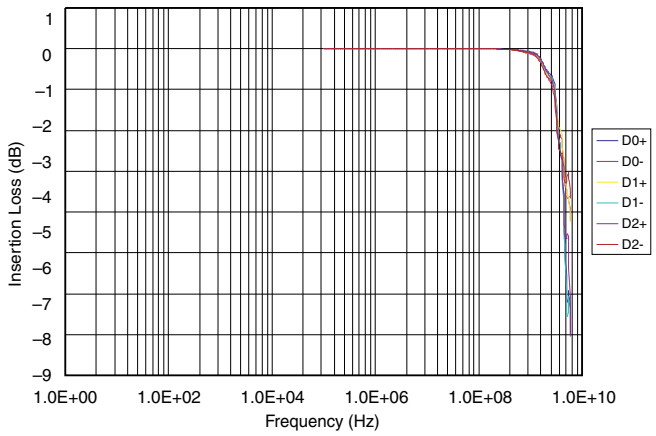


Figure 1. Insertion Loss vs Frequency

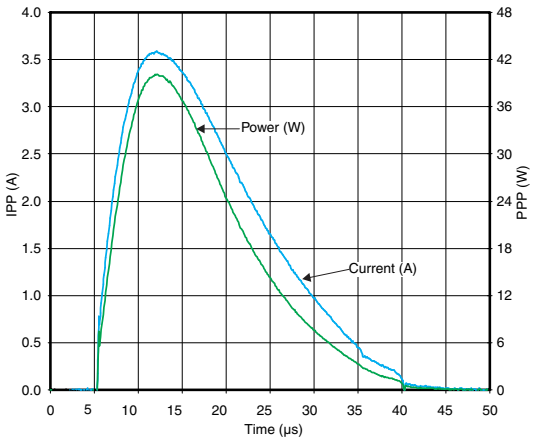


Figure 2. Peak Pulse Waveforms

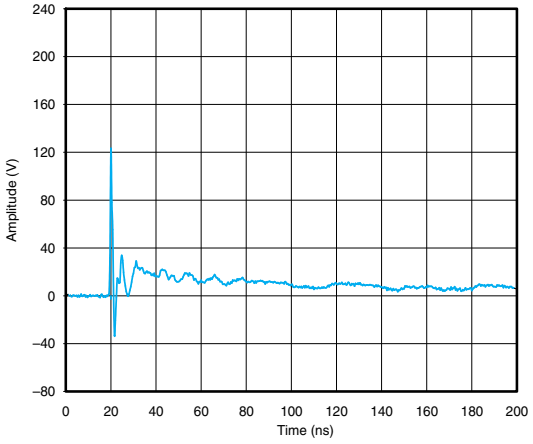


Figure 3. IEC Clamping Waveforms (8-kV Contact)

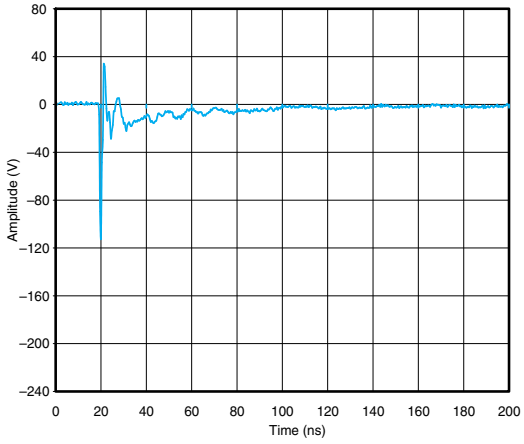


Figure 4. Figure 3. IEC Clamping Waveforms (–8-kV Contact)

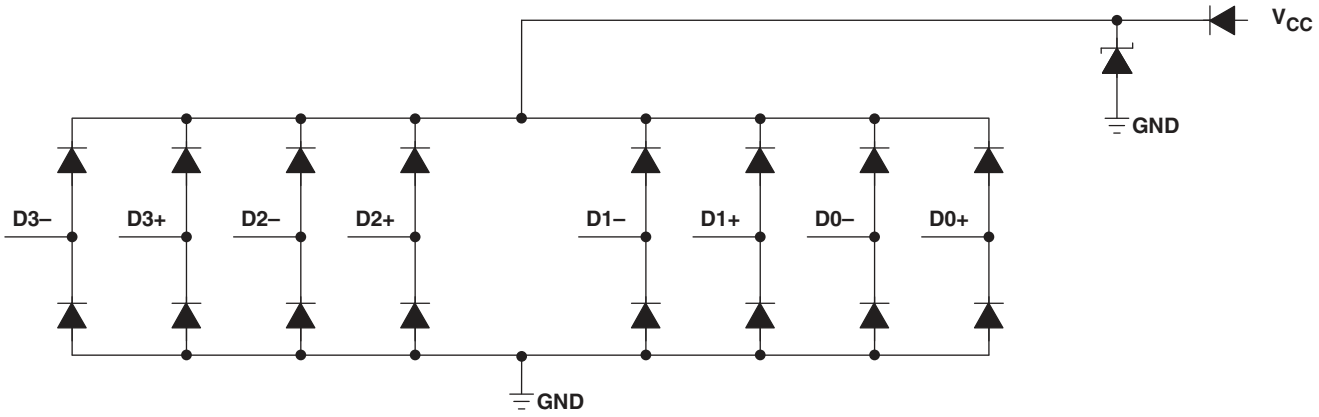
7 Detailed Description

7.1 Overview

The TPD8S009 is an eight-channel TVS diode array for ESD protection. TPD8S009 is rated to dissipate contact ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4), with ±8-kV contact discharge ESD protection. The low capacitance (0.8 pF) of this device, coupled with the excellent matching between differential signal pairs enables this device to provide transient voltage suppression circuit protection for high-speed idfferential data rates (3-dB bandwidth > 4 GHz).

The TPD8S009 offers an optional V_{CC} supply pin which can be connected to system supply plane. There is a blocking diode at the V_{CC} pin to enable the I_{off} feature for the TPD8S009. The TPD8S009 can handle live signal at the signal pins when the V_{CC} pin is connected to 0 V. The V_{CC} pin allows all the internal circuit nodes of the TPD8S009 to be at known potential during start-up time. However, connecting the optional V_{CC} pin to board supply plane doesn't affect the system level ESD performance of the TPD8S009.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±8-kV contact and ±9-kV air. An ESD and surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 25 W (8/20-µs waveform). An ESD and surge clamp diverts this current to ground.

7.3.3 I/O Capacitance

The capacitance between each I/O pin to ground is 0.8 pF (typical). This device can support data rates up to 3.4 Gbps.

7.3.4 Low Leakage Current

The I/O pins feature a low leakage current of 10 nA (typical) with an IO bias of 3.3 V and V_{CC} bias of 5 V.

7.3.5 Supports High-Speed Differential Data Rates

The I/O pins low capacitance of 0.8 pF (typical) gives them a typical –3-dB bandwidth > 4 GHz. This allows the TPD8S009 to protect interfaces with high-speed signals like HDMI 1.4.

Feature Description (continued)

7.3.6 I_{off} Feature

The TPD8S009 offers an optional V_{CC} supply pin which can be connected to system supply plane. There is a blocking diode at the V_{CC} pin which makes it so the TPD4S009 can handle live signal at the D+, D– pins when the V_{CC} pin is connected to 0 V. This is the I_{off} feature, which is crucial for HDMI, as a live signal can be put on the IO pins when the system is powered off.

7.3.7 Industrial Temperature Range

This device features an industrial operating range of –40°C to +85°C.

7.3.8 Easy Straight Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout. Flow-through routing also allows the PCB designer to optimize the signal integrity of any high-speed signals being protected.

7.4 Device Functional Modes

TPD8S009 is a passive-integrated circuit that activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6 V) are present upon the circuit being protected. During ESD events, voltages as high as ±9 kV can be directed to ground and V_{CC} through the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD8S009 (usually within 10's of nano-seconds) the device reverts back to a high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

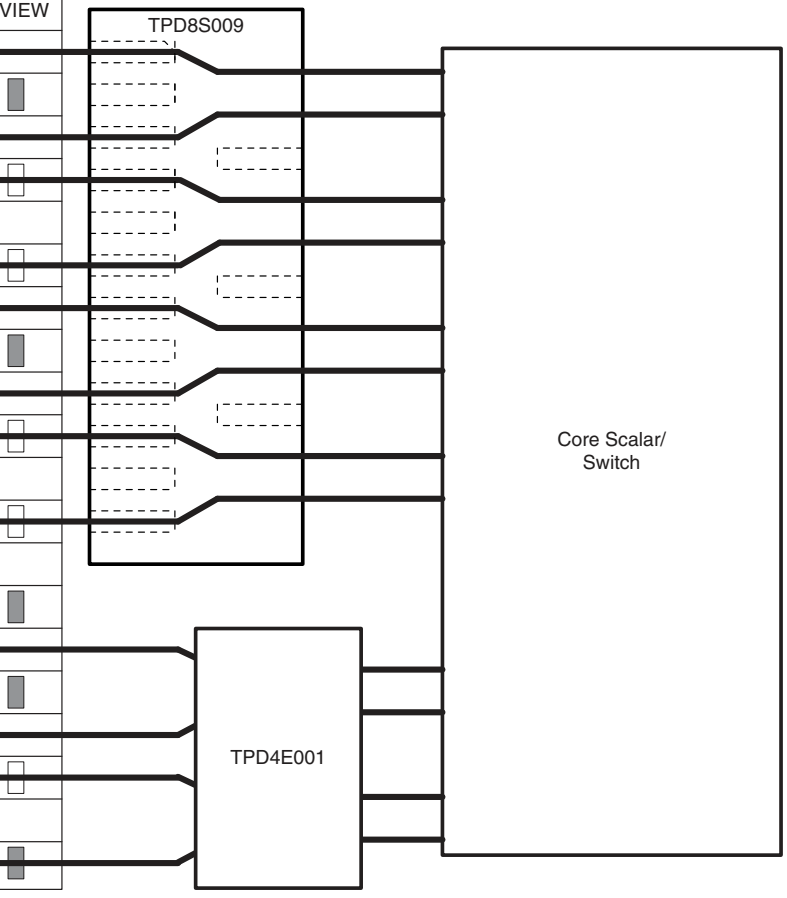
8.1 Application Information

The TPD8S009 can provide system-level ESD protection to the high-speed differential lines of the HDMI or display ports. The flow-through package offers flexibility for board routing with traces up to 15-mm wide. Figure 5 shows the board-layout scheme for the four differential pair lines. The special pin configuration of the TPD8S009 matches the HDMI or DisplayPort pin assignments. It allows the differential signal pairs to couple together after they touch the ESD ports (pins 1–3, 4–6, 7–9, and 10–12) of the TPD8S009.

The TPD4E001 is recommended for ESD protection of slow-speed control lines.

8.2 Typical Application

PIN NO.	SIGNAL TYPE	PIN NAME	MATING ROW CONTACT LOCATION	VERTICALLY OPPOSED CONNECTOR FRONT VIEW
1	Out	ML Lane 0(p)	Top	
2	GND	GND	Bottom	
3	Out	ML Lane 0(n)	Top	
4	Out	ML Lane 1(p)	Bottom	
8	GND	GND	Top	
6	Out	ML Lane 1(n)	Bottom	
7	Out	ML Lane 2(p)	Top	
8	GND	GND	Bottom	
9	Out	ML Lane 2(n)	Top	
10	Out	ML Lane 3(p)	Bottom	
11	GND	GND	Top	
12	Out	ML Lane 3(n)	Bottom	
13	GND	GND	Top	
14	GND	GND	Bottom	
15	I/O	Aux CH (p)	Top	
16	GND	GND	Bottom	
17	I/O	Aux CH (n)	Top	
18	In	Hot Plug Detect	Bottom	
19	PWR Out	Return DP PWR	Top	
20	PWR RIN	DP PWR	Bottom	



Display Port Connector

TPD8S009 and TPD4E001 provide complete ESD protection for display or HDMI interface

Figure 5. Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For this design example, one TPD8S009 devices, and one TPD4E001 are being used in an HDMI 1.4 application. This provides a complete port protection scheme.

Given the HDMI 1.4 application, the following parameters are shown in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on high-speed TMDS pins	0 V to 3.6 V
Operating Frequency	1.7 GHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range on High Speed TMDS Pins

TPD8S009 has 8 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 8 I/O channels protect which signal lines. The package is also designed to easily lay out on an HDMI connector, eliminating any tricky routing issues. Any I/O supports a signal range of 0 to 5.5 V. Therefore, this device supports the HDMI 1.4 signal swing.

8.2.2.2 Bandwidth on High-Speed TMDS Pins

Each pin of the TPD8S009 has a typical –3-dB bandwidth of 4GHz. Therefore, this device can handle HDMI 1.4 data rate of 3.4 Gbps with operating frequency of 1.7 GHz.

8.2.3 Application Curves

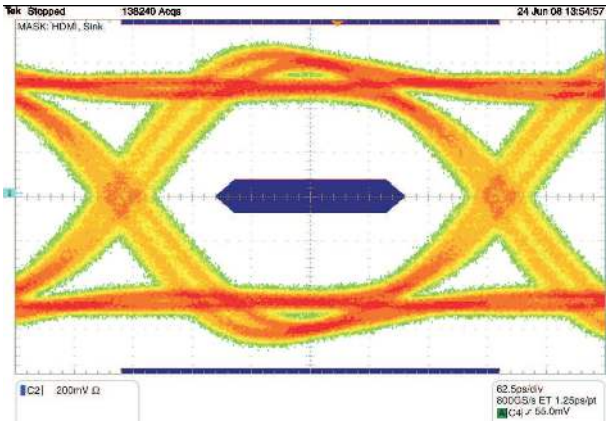


Figure 6. Eye Diagram Without TPD8S009 (2.5-Gbps Data Rate)

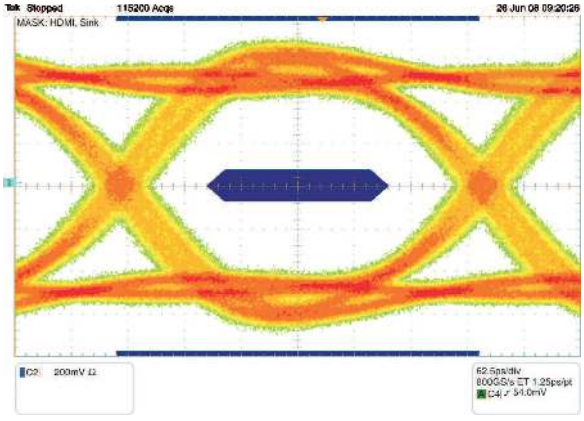


Figure 7. Eye Diagram With TPD8S009 (2.5-Gbps Data Rate)

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Take care to make sure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

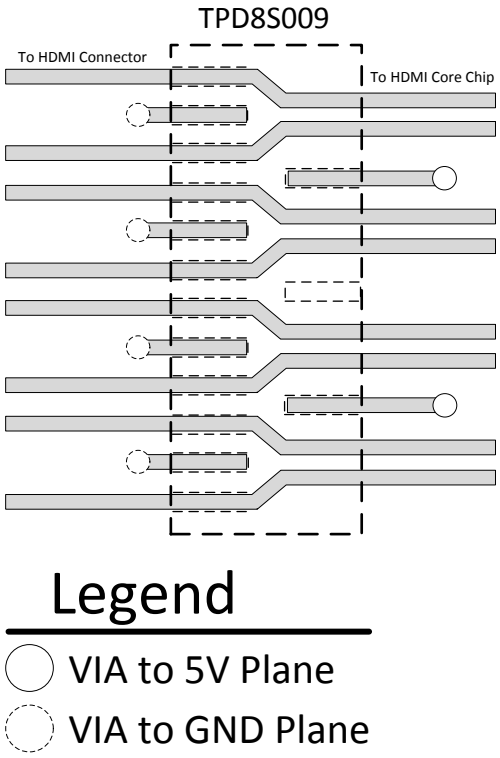


Figure 8. Typical Layout for HDMI Connector

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD8S009DSMR	ACTIVE	SON	DSM	15	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PK009	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

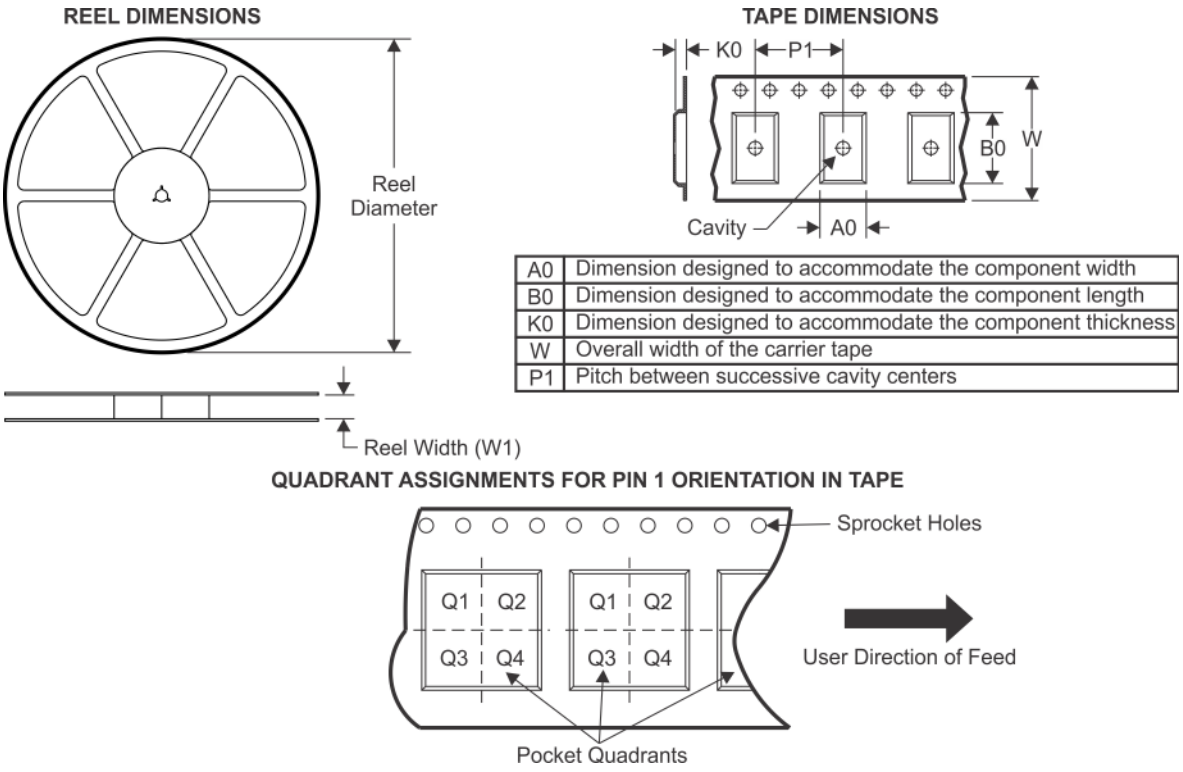
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

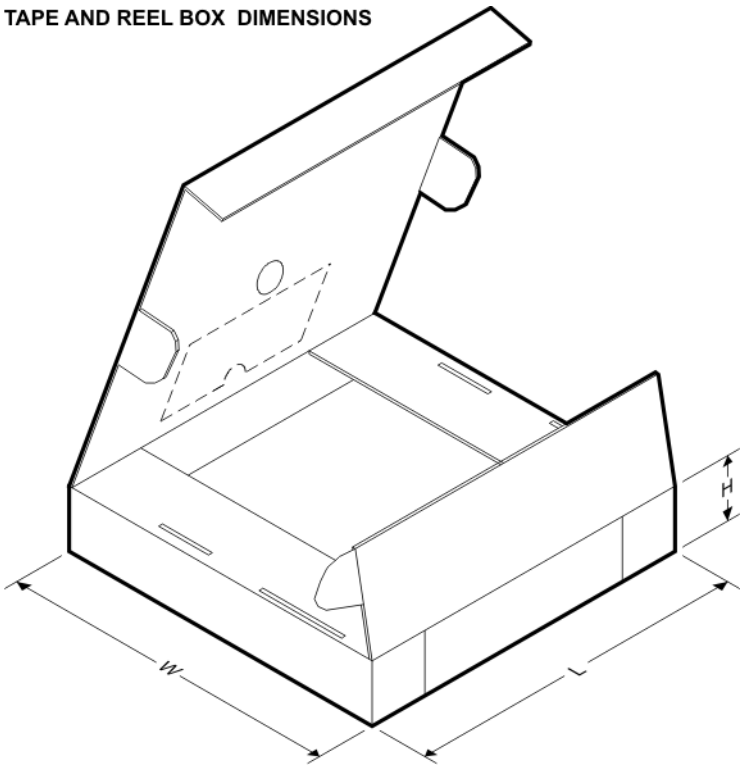


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD8S009DSMR	SON	DSM	15	3000	180.0	12.4	2.75	6.75	0.95	4.0	12.0	Q1

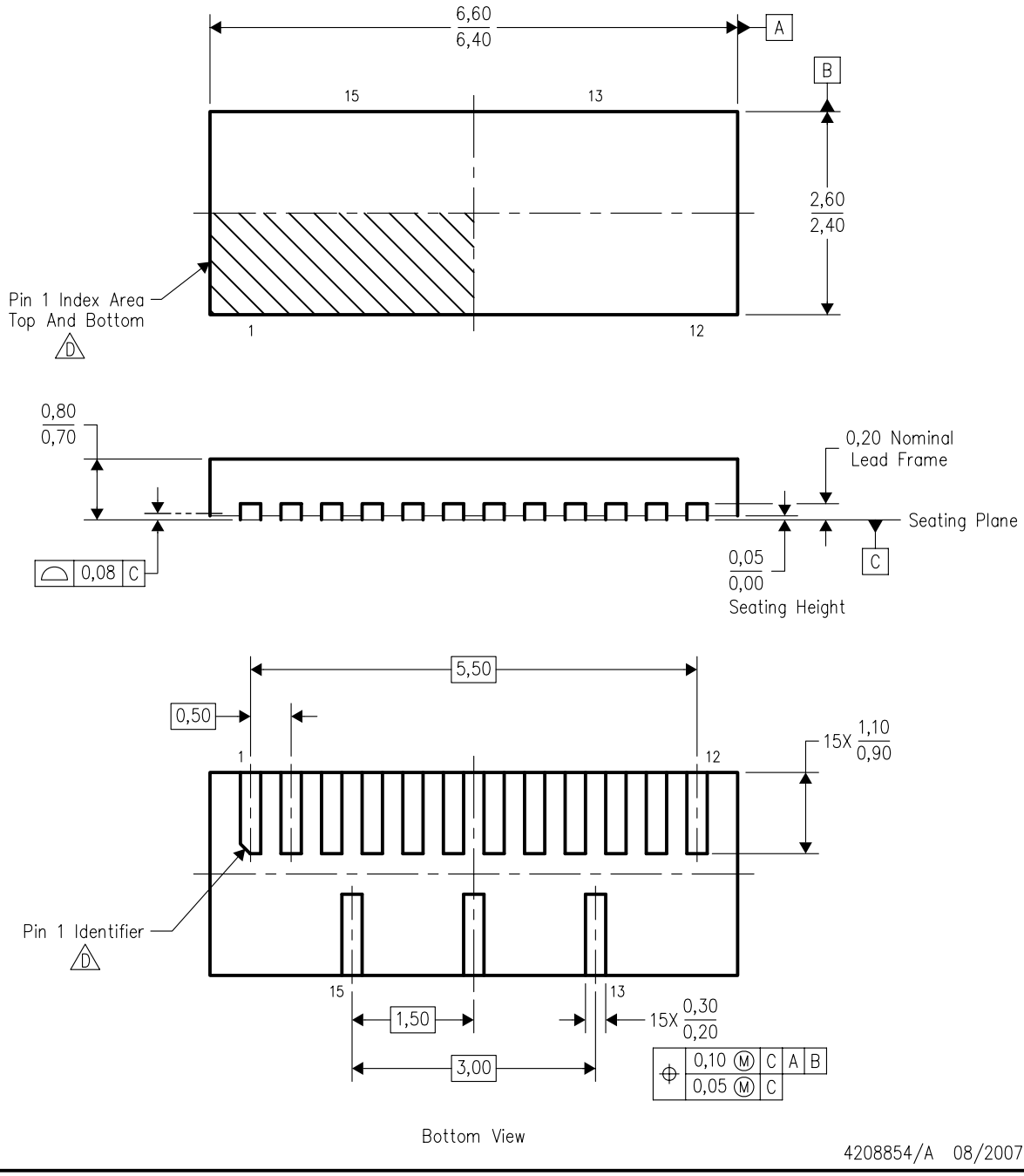
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

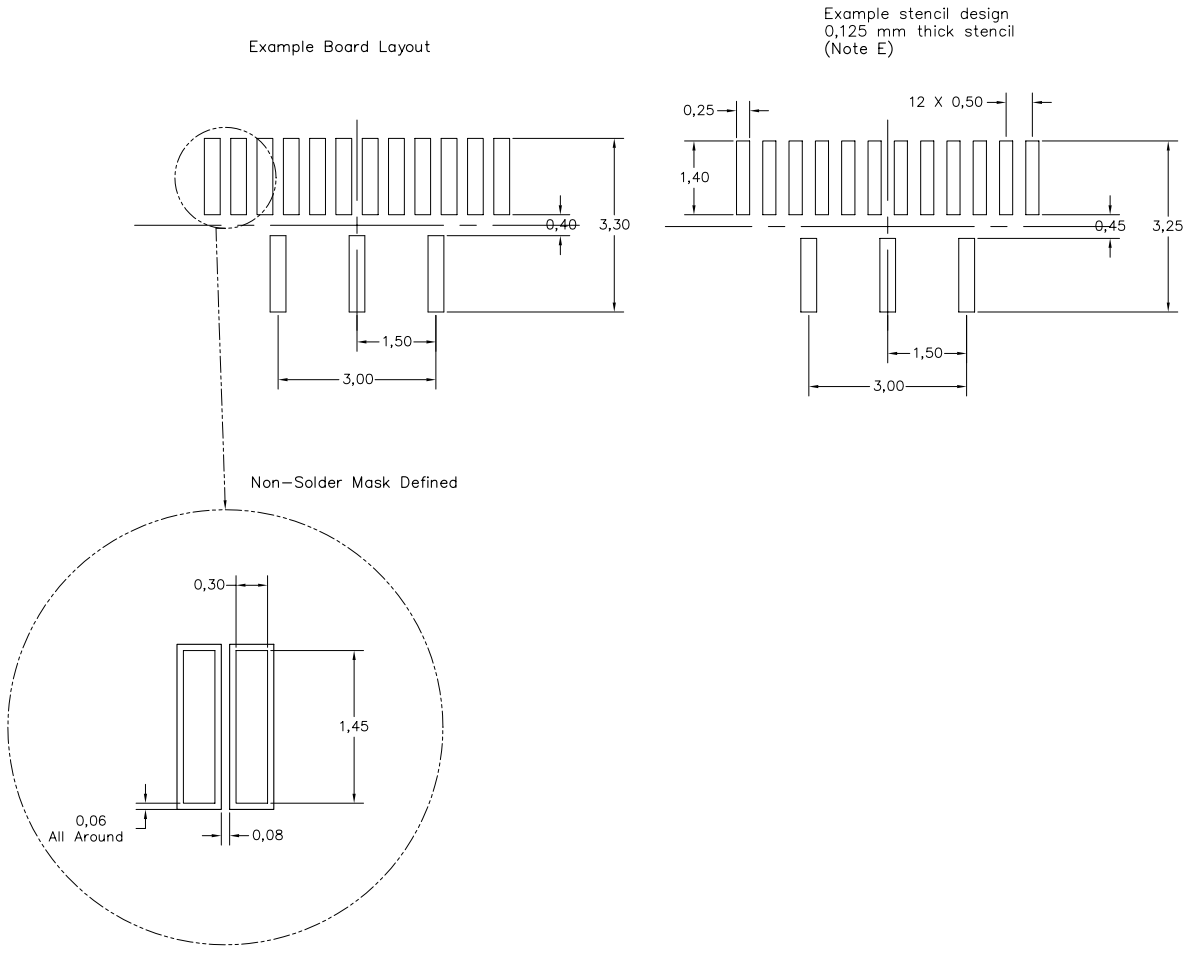
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD8S009DSMR	SON	DSM	15	3000	200.0	183.0	25.0

DSM (R–PDSO–N15) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

DSM (R–PDSO–N15)



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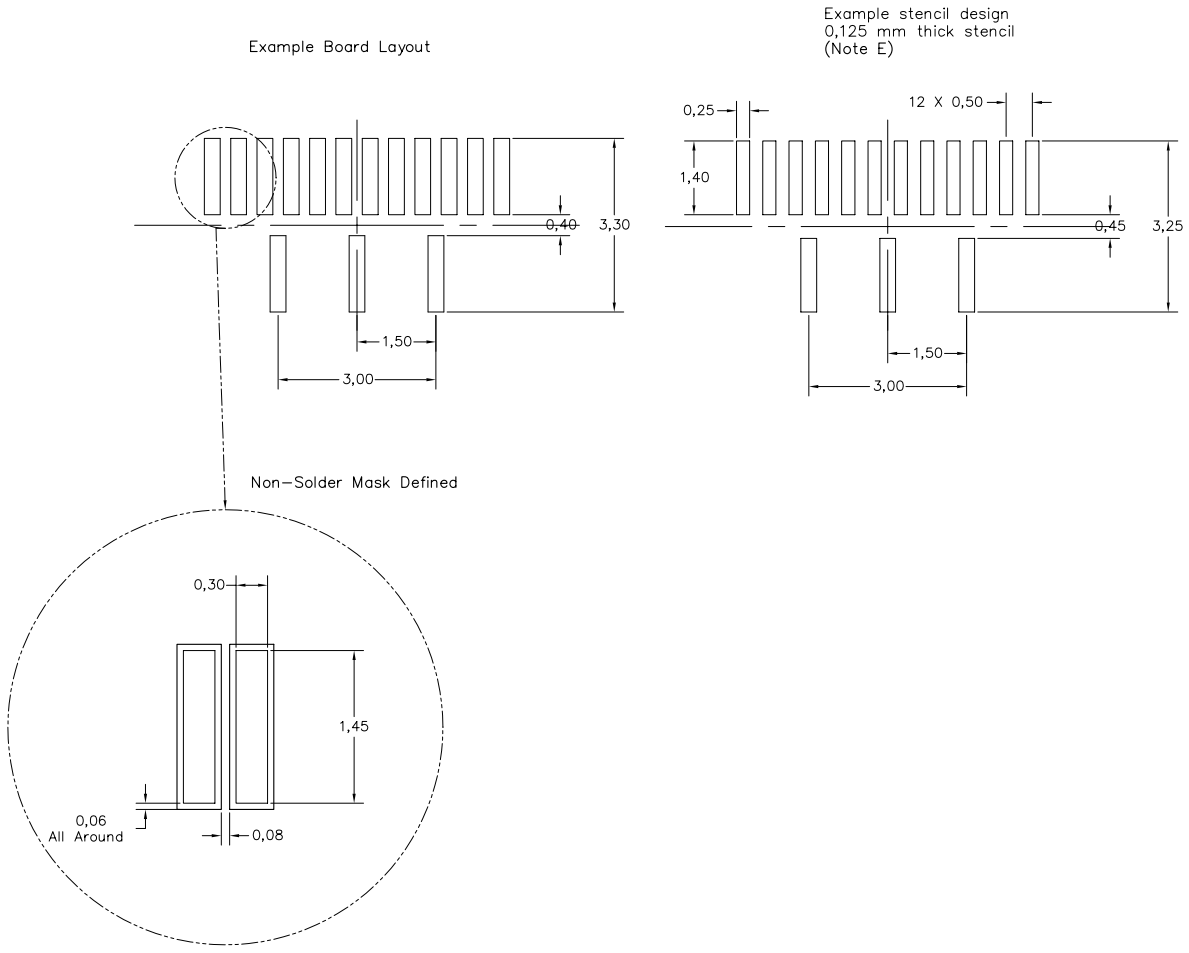
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DSM (R–PDSO–N15)



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