



Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16240T/AT/CT/ET IDT54/74FCT162240T/AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
 - Extended commercial range of -40°C to +85°C
 - Vcc = 5V $\pm 10\%$
- **Features for FCT16240T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162240T/AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

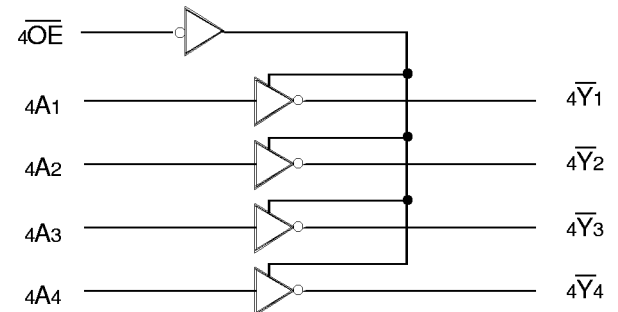
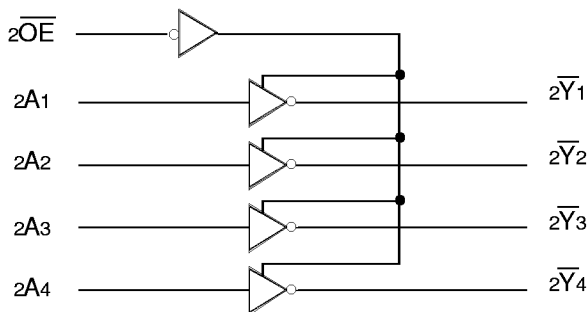
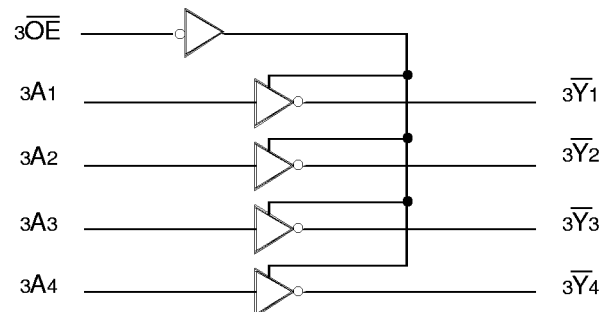
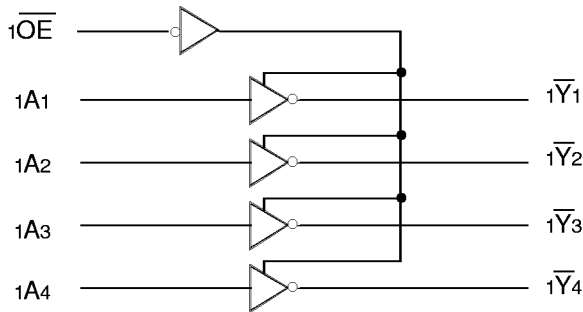
DESCRIPTION:

The FCT16240T/AT/CT/ET and FCT162240T/AT/CT/ET 16-bit buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. The flow-through organization of signal pins simplifies layout. The three-state controls are designed to operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The FCT16240T/AT/CT/ET are ideally suited for driving high capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162240T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times— reducing the need for external series terminating resistors. The FCT162240T/AT/CT/ET are plug-in replacements for FCT16240T/AT/CT/ET and 54/74ABT16240 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



2541 drw 01

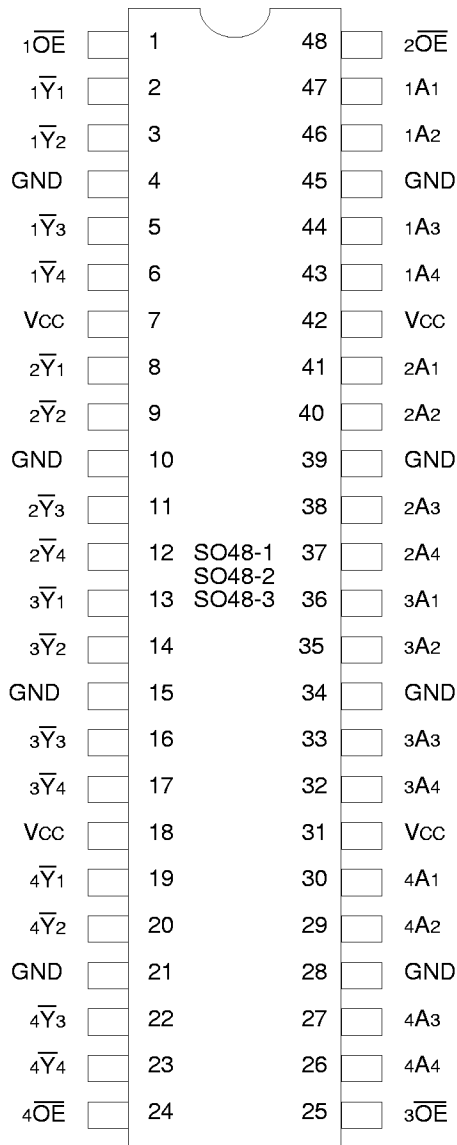
2541 drw 02

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MILITARY AND INDUSTRIAL TEMPERATURE RANGES

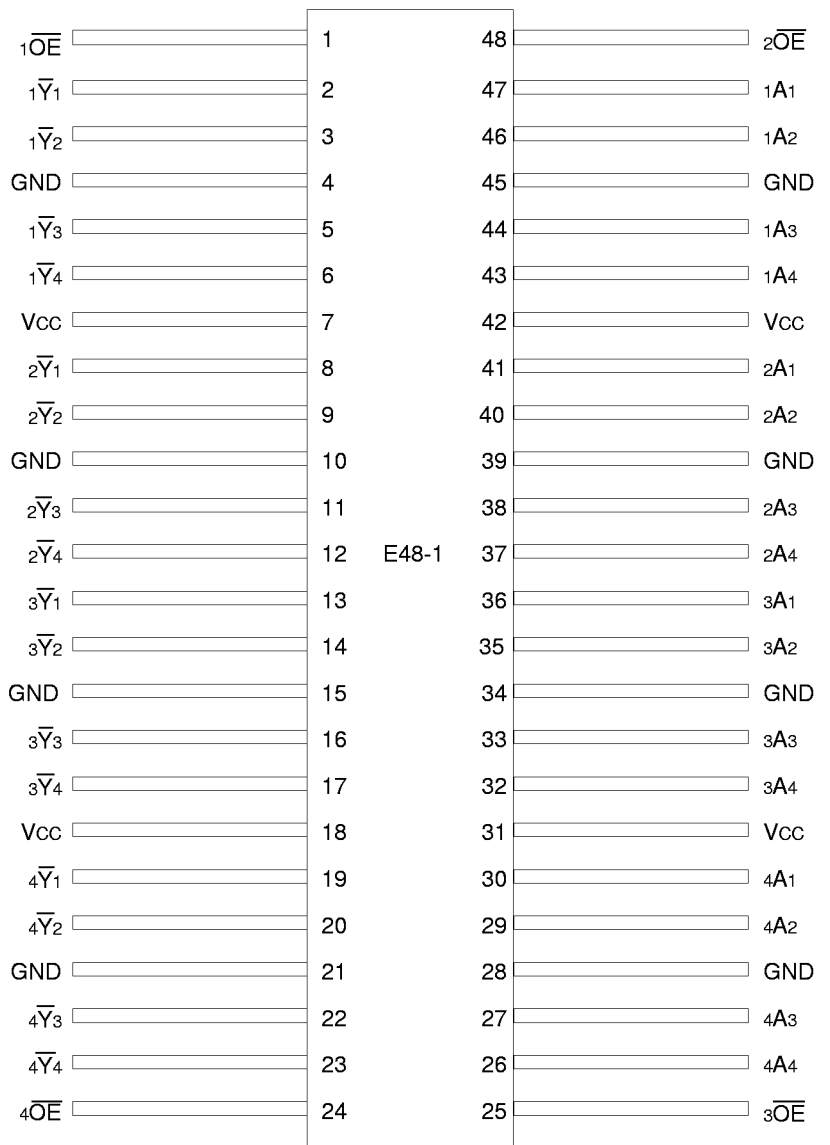
FEBRUARY 1997

PIN CONFIGURATIONS



**SSOP/
TSSOP/TVSOP
TOP VIEW**

2541 drw 03



**CERPACK
TOP VIEW**

2541drw 04

PIN DESCRIPTION

Pin Names	Description
\overline{xOE}	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs
$x\overline{Y}x$	3-State Outputs

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FUNCTION TABLE⁽¹⁾

Inputs		Outputs
\overline{xOE}	xAx	$x\overline{Y}x$
L	L	H
L	H	L
H	X	Z

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NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
$V_{TERM(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
$V_{TERM(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	3.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	3.5	8.0	pF

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NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾		—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾	$V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾		—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$ $V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾	-80	-140	-250	mA
V_H	Input Hysteresis	—	—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}	—	5	500	μA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT16240T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I_O	Output Drive Current	$V_{CC} = \text{Max.}$, $V_O = 2.5\text{V}$ ⁽³⁾	-50	—	-180	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}$ ⁽⁴⁾	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	—	0.2	0.55	V	
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$	—	—	± 1	μA	

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OUTPUT DRIVE CHARACTERISTICS FOR FCT162240T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾	60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾	-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16240T/162240T				FCT16240AT/162240AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xAx to xȲx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition ⁽¹⁾	FCT16240CT/162240CT				FCT16240ET/162240ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xAx to xȲx	CL = 50pF RL = 500Ω	1.5	4.3	1.5	4.7	1.5	3.2	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

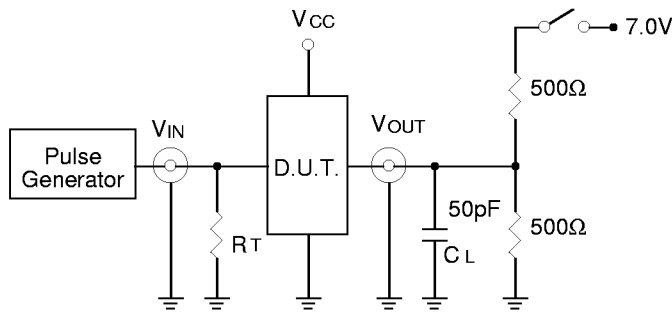
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

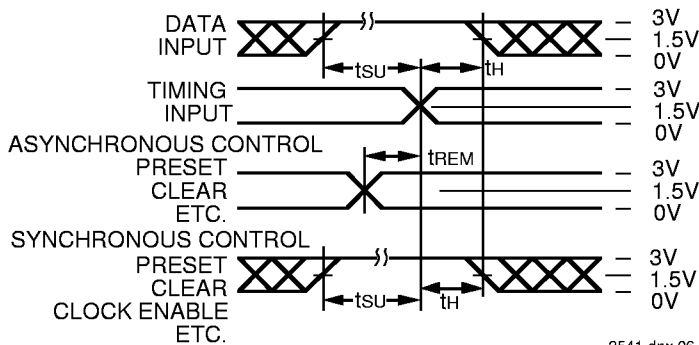
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

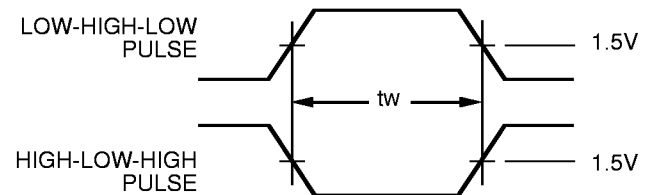
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SET-UP, HOLD AND RELEASE TIMES



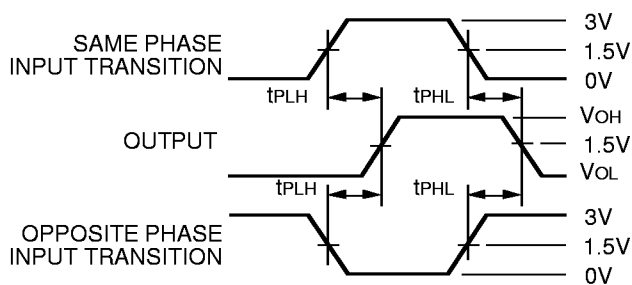
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PULSE WIDTH



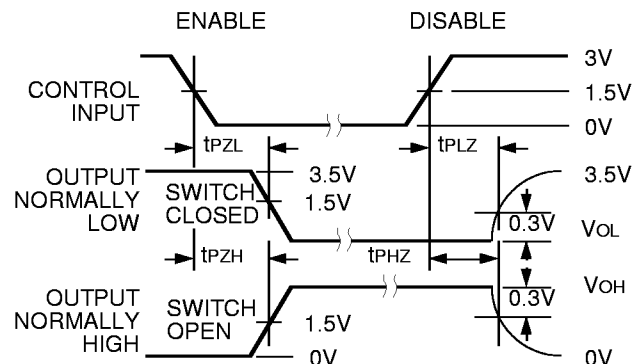
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X	
Temp. Range	Device Type	Package	Process			
					Blank B	Commercial MIL-STD-883, Class B
					PV PA PF E	Shrink Small Outline Package (SO48-1) Thin Shrink Small Outline Package (SO48-2) Thin Very Small Outline Package (SO48-3) CERPACK (E48-1)
					16240T 16240AT 16240CT 16240ET 162240T 162240AT 162240CT 162240ET	Inverting 16-Bit Buffer/Line Driver
					54 74	-55°C to +125°C -40°C to +85°C

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