



256K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Fast access time : 55ns
- Low power consumption:
Operating current : 20/18mA (TYP.)
Standby current : 2 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Lead free and green package available**
- Package : 32-pin 8mm x 20mm TSOP-I
32-pin 8mm x 13.4mm STSOP
32-pin 450 mil SOP
32-pin 600 mil P-DIP
36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

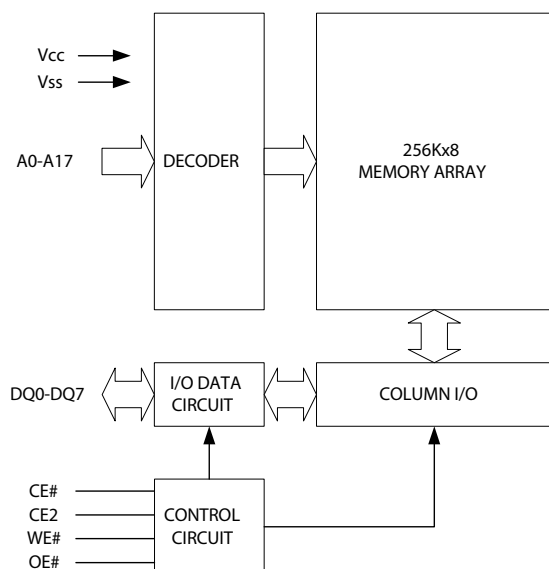
The AS6C2008A is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C2008A is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C2008A operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(Isb1,TYP.)	Operating(Icc,TYP.)
AS6C2008A(LLI)	-40 ~ 85°C	2.7 ~ 5.5V	55ns	2 μ A(LL)	20/18mA

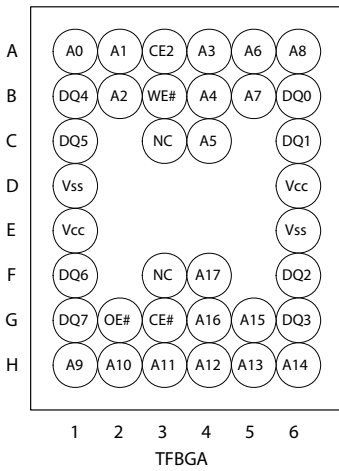
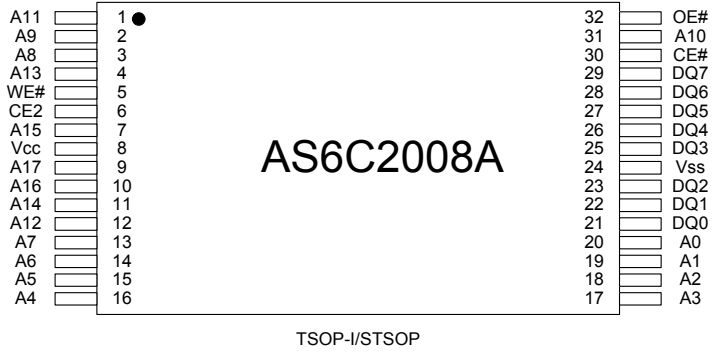
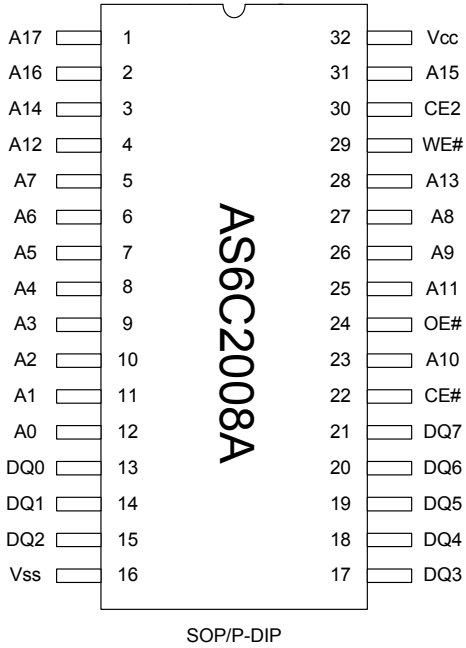
FUNCTIONAL BLOCK DIAGRAM**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



256K X 8 BIT LOW POWER CMOS SRAM

PIN CONFIGURATION





256K X 8 BIT LOW POWER CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{cc} relative to V _{ss}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{ss}	V _{T2}	-0.5 to V _{cc} +0.5	V
Operating Temperature	T _A	-40 to 85(I grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{SOLDER}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{cc} , I _{cc1}
Read	L	H	L	H	D _{OUT}	I _{cc} , I _{cc1}
Write	L	H	X	L	D _{IN}	I _{cc} , I _{cc1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



256K X 8 BIT LOW POWER CMOS SRAM

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}		2.7	3.0	5.5	V
Input High Voltage	V _{IH} ¹		0.7* V _{CC}	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ²		- 0.2	-	0.6	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	2.7	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min., I _{I/O} = 0mA CE# = 0.2V and CE2 = V _{CC} -0.2V other pins at 0.2V or V _{CC} -0.2V	- 55	20	60	mA
			- 70	18	50	mA
	I _{CC1}	Cycle time = 1μs, I _{I/O} = 0mA CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V, other pins at 0.2V or V _{CC} -0.2V	-	4	10	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V other pins at 0.2V or V _{CC} -0.2V	-	2	50	μA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -2mA/4mA



256K X 8 BIT LOW POWER CMOS SRAM

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	AS6C2008A-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	ns
Address Access Time	t _{AA}	-	55	ns
Chip Enable Access Time	t _{ACE}	-	55	ns
Output Enable Access Time	t _{OE}	-	30	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	ns
Output Hold from Address Change	t _{OH}	10	-	ns

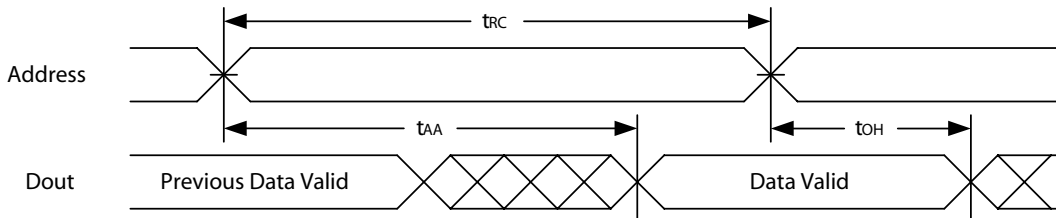
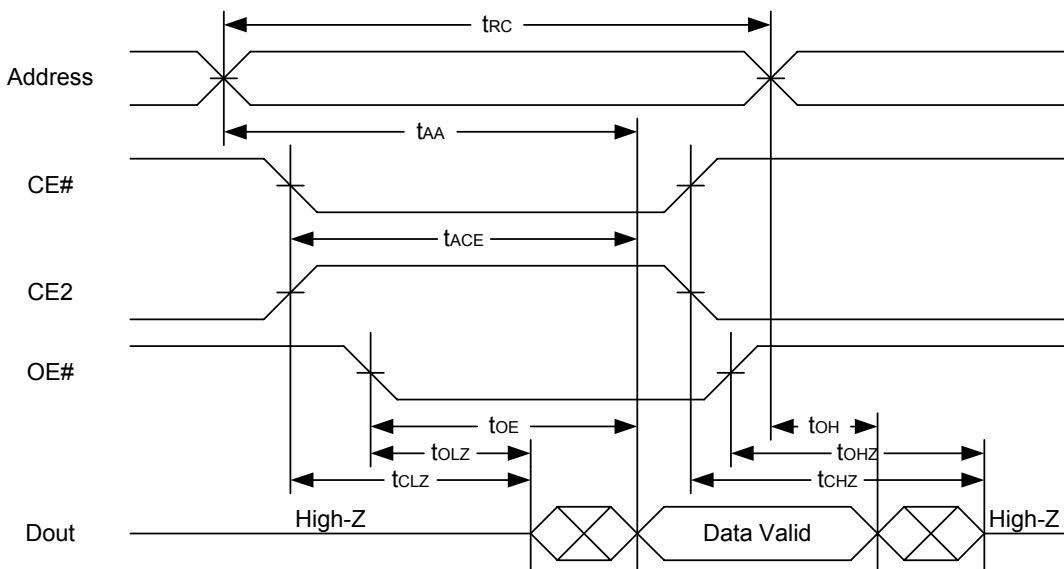
(2) WRITE CYCLE

PARAMETER	SYM.	AS6C2008A-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	ns
Address Valid to End of Write	t _{AW}	50	-	ns
Chip Enable to End of Write	t _{CW}	50	-	ns
Address Set-up Time	t _{AS}	0	-	ns
Write Pulse Width	t _{WP}	45	-	ns
Write Recovery Time	t _{WR}	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	ns

*These parameters are guaranteed by device characterization, but not production tested.



256K X 8 BIT LOW POWER CMOS SRAM

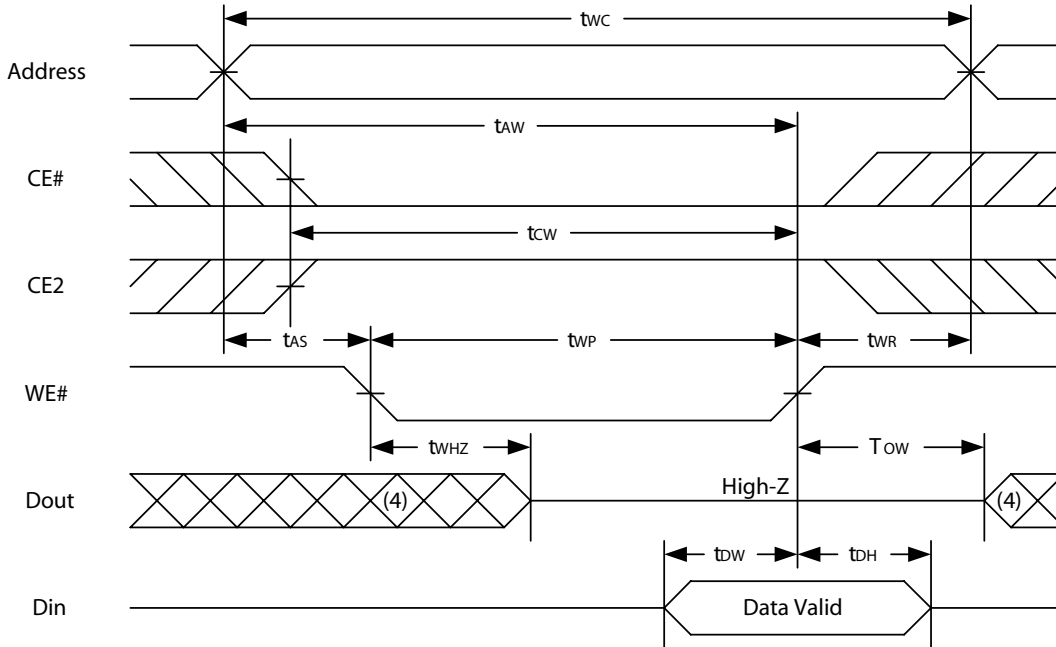
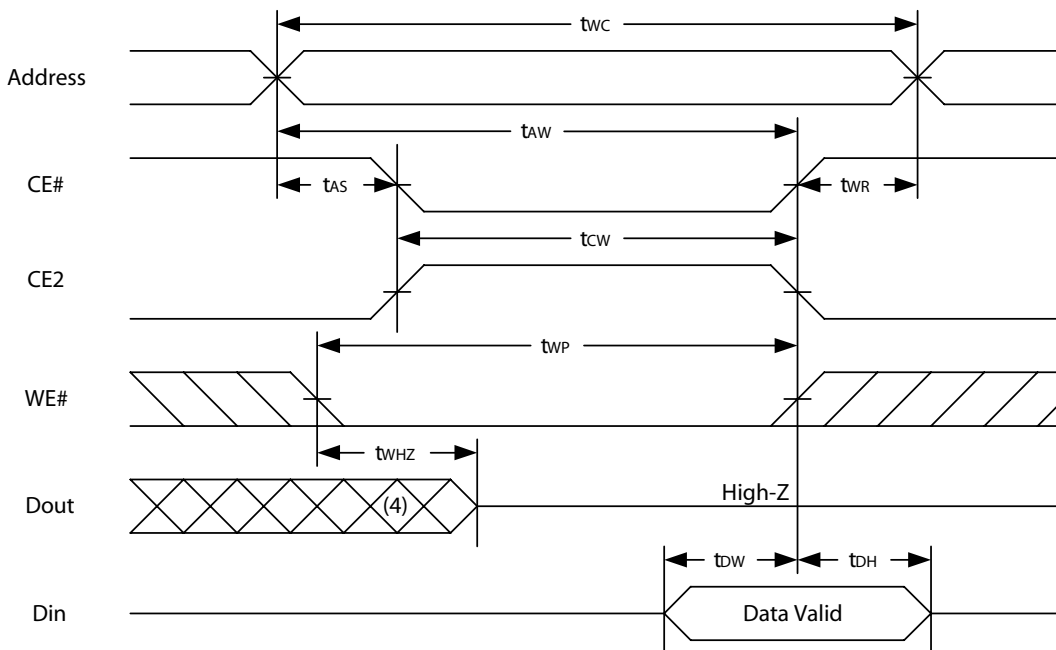
TIMING WAVEFORMS**READ CYCLE 1 (Address Controlled) (1,2)****READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)**

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OZH} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OZH} is less than t_{OLZ} .



256K X 8 BIT LOW POWER CMOS SRAM

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)****Notes :**

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#-low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

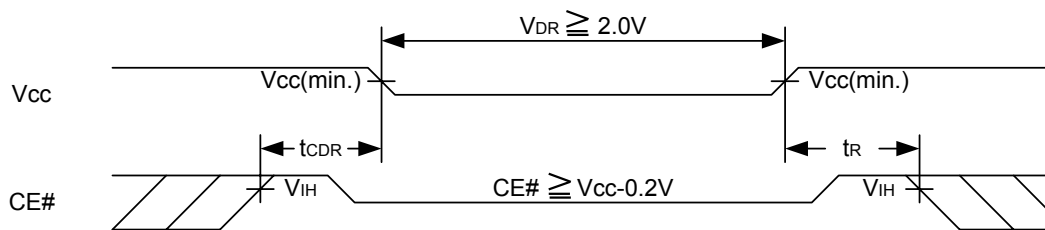
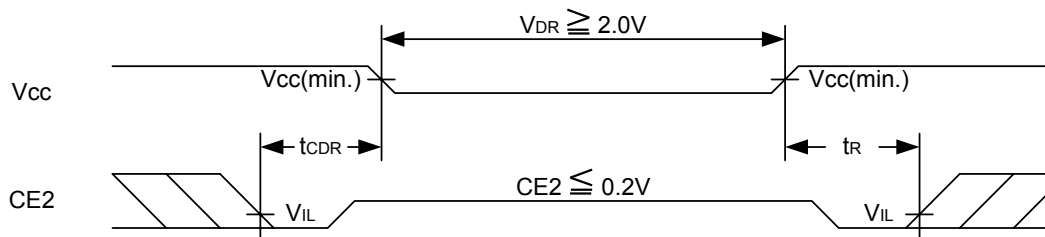


256K X 8 BIT LOW POWER CMOS SRAM

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$	2.0	-	5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 2.0V$ $CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ other pins at 0.2V or $V_{CC}-0.2V$	-	0.5	20	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

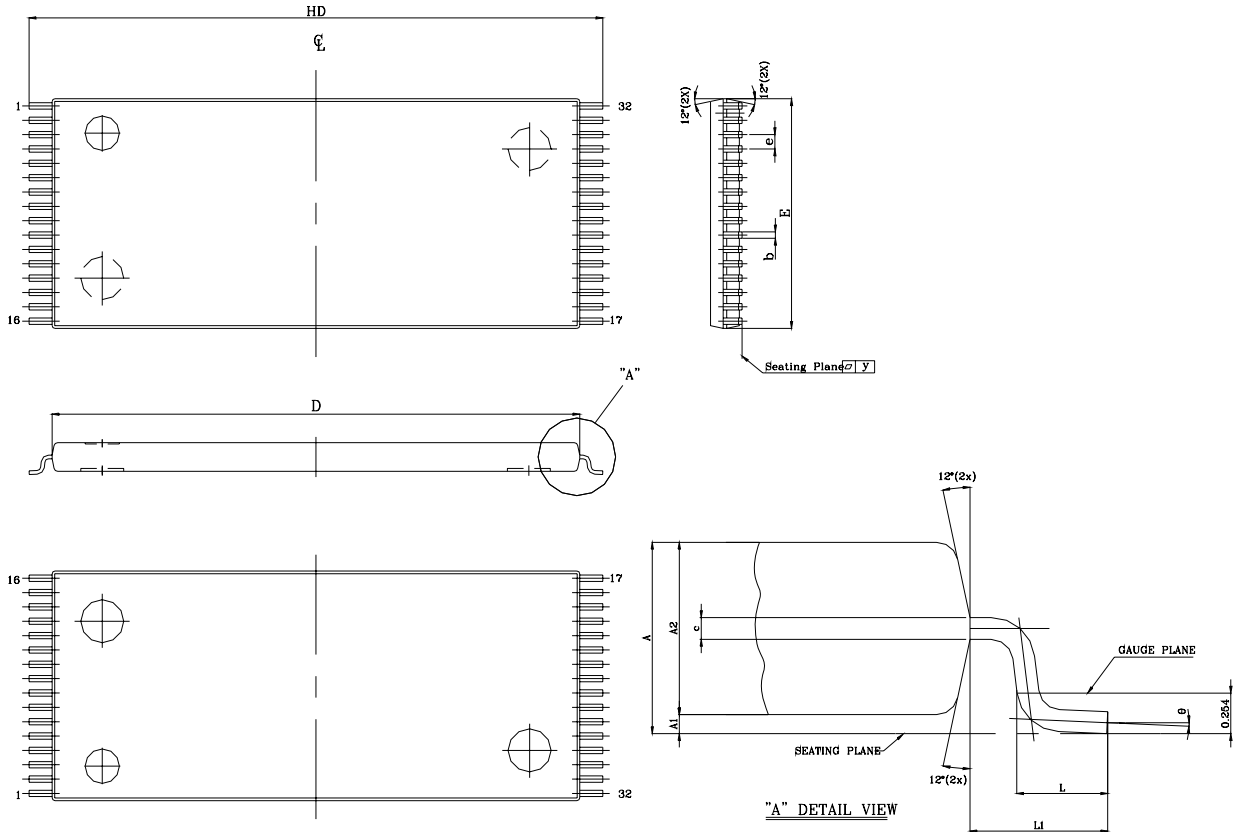
DATA RETENTION WAVEFORM**Low Vcc Data Retention Waveform (1) (CE# controlled)****Low Vcc Data Retention Waveform (2) (CE2 controlled)**



256K X 8 BIT LOW POWER CMOS SRAM

PACKAGE OUTLINE DIMENSION

32 pin 8mm x 20mm TSOP-I Package Outline Dimension

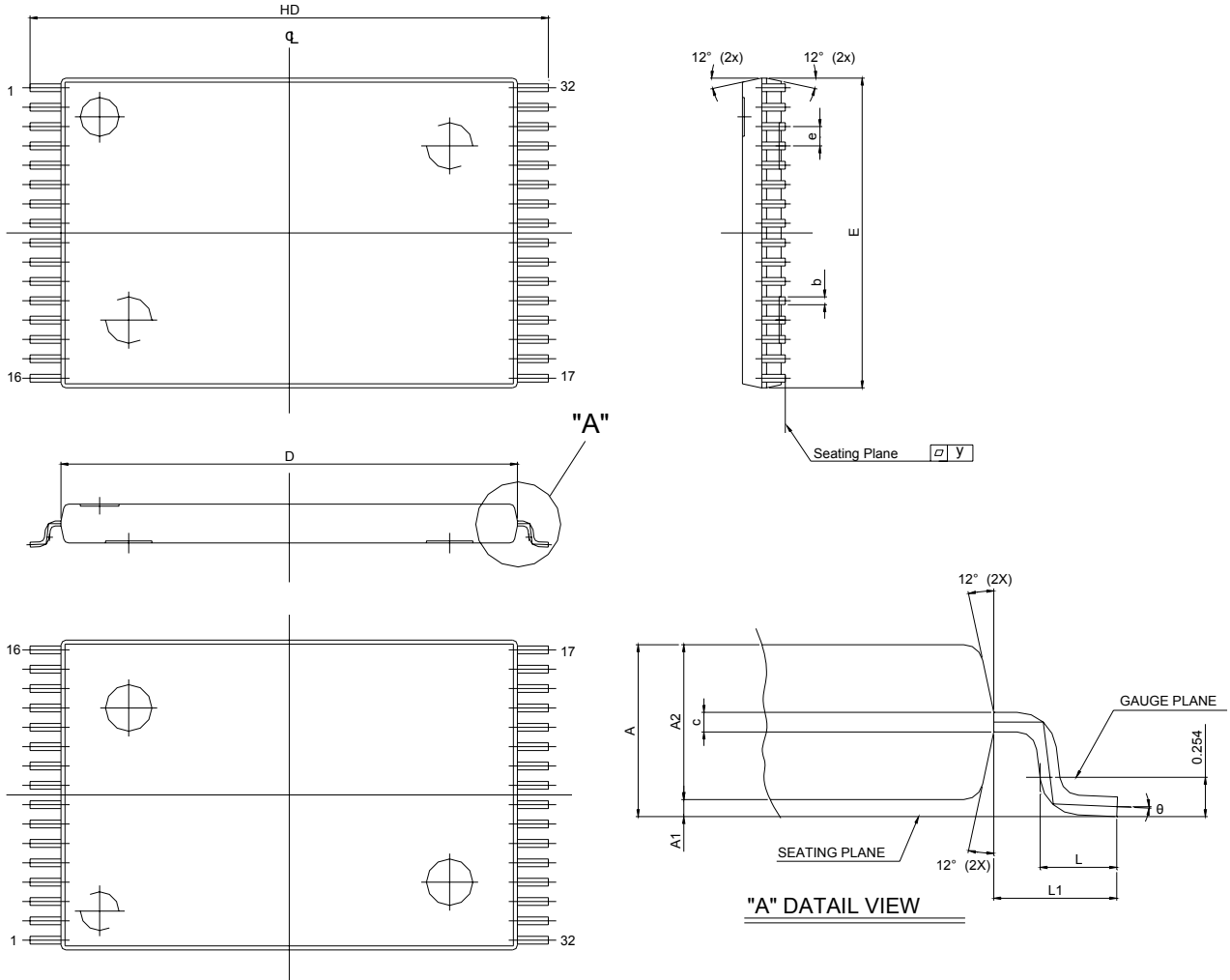


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 \pm 0.002	0.10 \pm 0.05
A2		0.039 \pm 0.002	1.00 \pm 0.05
b		0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c		0.005 (TYP)	0.127 (TYP)
D		0.724 \pm 0.004	18.40 \pm 0.10
E		0.315 \pm 0.004	8.00 \pm 0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 \pm 0.008	20.00 \pm 0.20
L		0.0197 \pm 0.004	0.50 \pm 0.10
L1		0.0315 \pm 0.004	0.08 \pm 0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0 $^\circ$ ~ 5 $^\circ$	0 $^\circ$ ~ 5 $^\circ$



256K X 8 BIT LOW POWER CMOS SRAM

32 pin 8mm x 13.4mm STSOP Package Outline Dimension

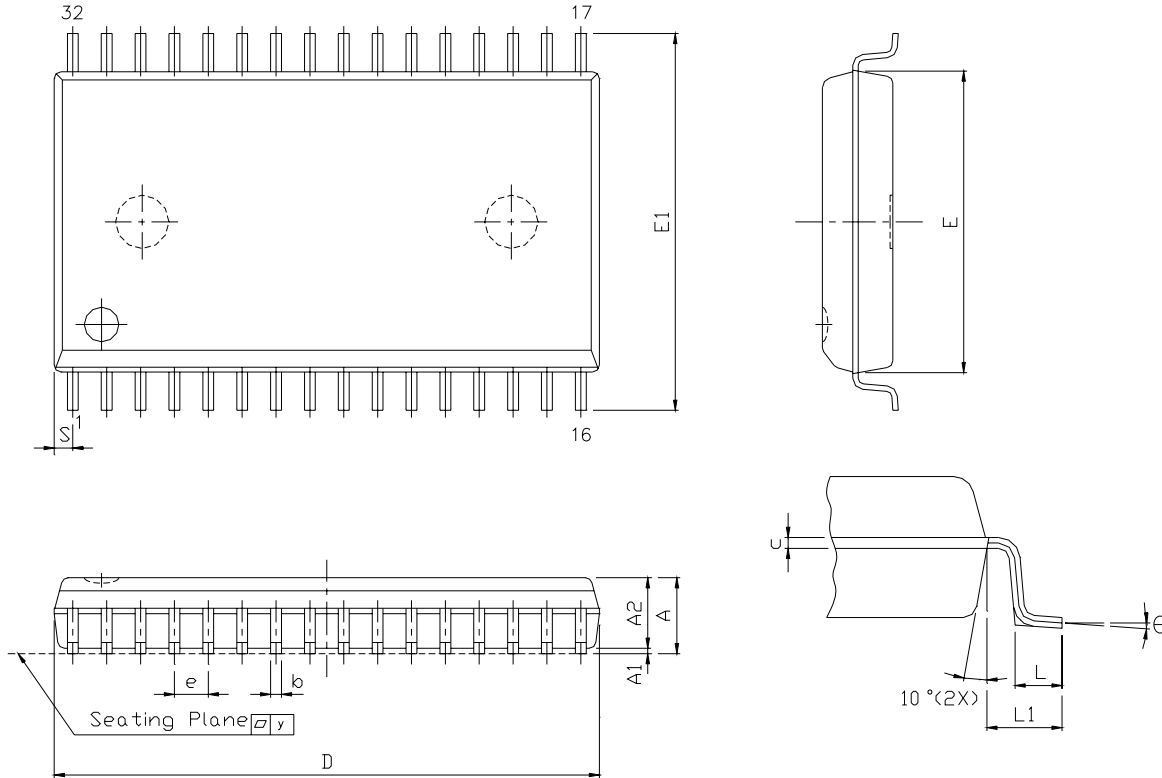


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.005 ±0.002	0.130 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 ±0.01	0.20±0.025
c		0.005 (TYP)	0.127 (TYP)
D		0.465 ±0.004	11.80 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.8 ±0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°



256K X 8 BIT LOW POWER CMOS SRAM

32 pin 450 mil SOP Package Outline Dimension

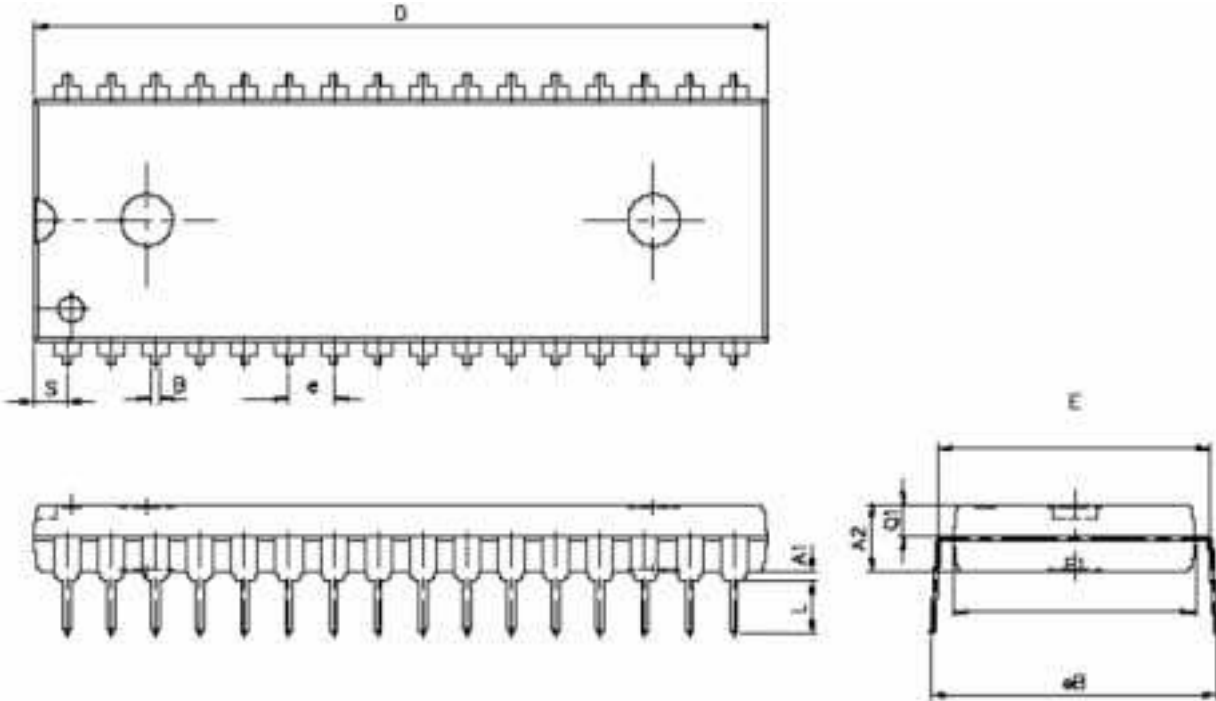


SYMBOL	UNIT	INCH.(BASE)	MM(REF)
A		0.118 (MAX)	2.997 (MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.111(MAX)	2.82(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445 ±0.005	11.303 ±0.127
E1		0.555 ±0.012	14.097 ±0.305
e		0.050(TYP)	1.270(TYP)
L		0.0347 ±0.008	0.881 ±0.203
L1		0.055 ±0.008	1.397 ±0.203
S		0.026(MAX)	0.660 (MAX)
y		0.004(MAX)	0.101(MAX)
θ		0° -10°	0° -10°



256K X 8 BIT LOW POWER CMOS SRAM

32 pin 600 mil P-DIP Package Outline Dimension



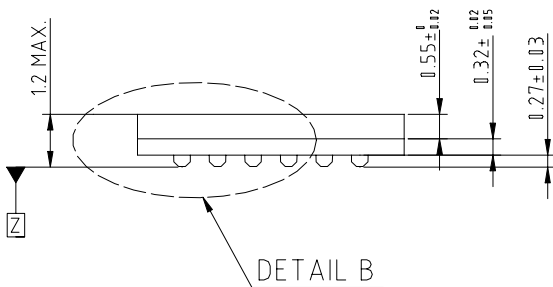
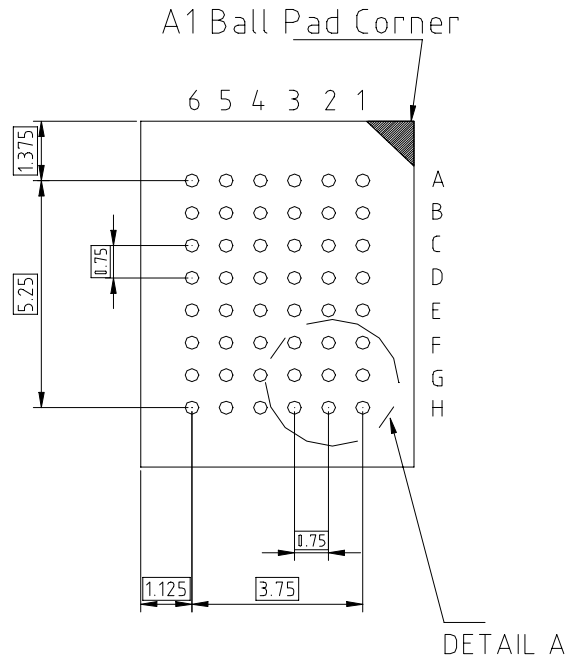
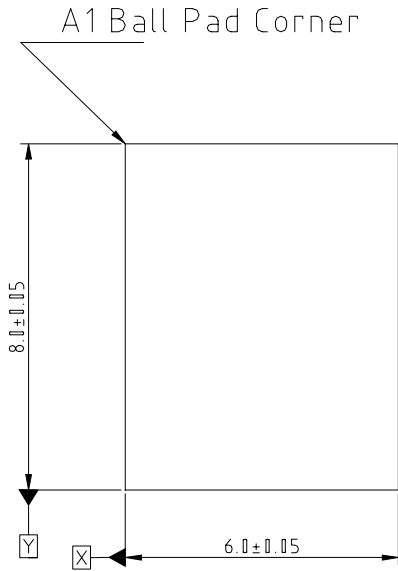
SYM.	UNIT	INCH(BASE)	MM(REF)
A1		0.001 (MIN)	0.254 (MIN)
A2		0.150 ± 0.005	3.810 ± 0.127
B		0.018 ± 0.005	0.457 ± 0.127
D		1.650 ± 0.005	41.910 ± 0.127
E		0.600 ± 0.010	15.240 ± 0.254
E1		0.544 ± 0.004	13.818 ± 0.102
e		0.100 (TYP)	2.540 (TYP)
eB		0.640 ± 0.020	16.256 ± 0.508.
L		0.130 ± 0.010	3.302 ± 0.254
S		0.075 ± 0.010	1.905 ± 0.254
Q1		0.070 ± 0.005	1.778 ± 0.127

Note : D/E1/S dimension do not include mold flash.

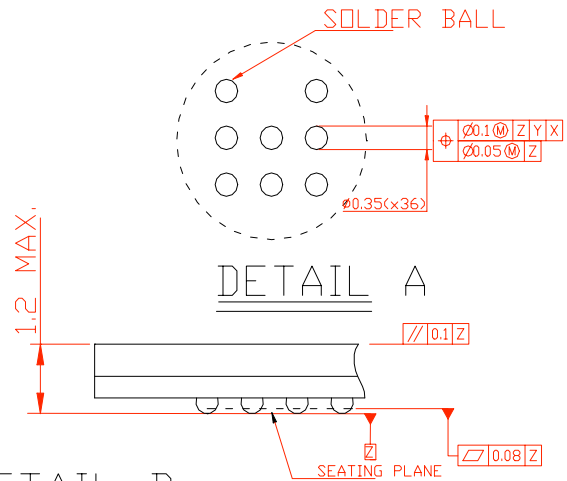


256K X 8 BIT LOW POWER CMOS SRAM

36 ball 6mm x 8mm TFBGA Package Outline Dimension



SIDE VIEW



DETAIL B



256K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C2008A-55SIN	256K x 8	2.7 - 5.5V	32pin 450mil SOP	Industrial ~ -40 F - 85 F	55
AS6C2008A-55STIN	256K x 8	2.7 - 5.5V	32pin sTSOP(8 x 13.4mm)	Industrial ~ -40 F - 85 F	55
AS6C2008A-55TIN	256K x 8	2.7 - 5.5V	32pin TSOP- 1(8 x 20 mm)	Industrial ~ -40 F - 85 F	55
AS6C2008A-55BIN	256K x 8	2.7 - 5.5V	36ball TFBGA(6 x 8mm)	Industrial ~ -40 F - 85 F	55

PART NUMBERING SYSTEM

AS6C	2008	-55	X	X	N
low power SRAM prefix	Device Number 20 = 2M 08 = x8	Access Time	Package Option S = 32pin 450 mil SOP ST = 32pin sTSOP(8 x 13.4) T = 32pin TSOP - 1(8 x 20mm)	Temperature Range I = Industrial (-40 to + 85 C)	N = Lead Free RoHS compliant part



256K X 8 BIT LOW POWER CMOS SRAM



Alliance Memory, Inc
511 Taylor Way,
San Carlos, CA 94070, USA
Phone: 650-610-6800
Fax: 650-620-9211

www.alliancememory.com

Copyright © Alliance Memory

All Rights Reserved

© Copyright 2007 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at anytime, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as expressly agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.