



# STP16NS25 STP16NS25FP

N-CHANNEL 250V - 0.23Ω - 16A TO-220 / TO-220FP  
MESH OVERLAY™ MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP16NS25	250 V	< 0.28 Ω	16 A
STP16NS25FP	250 V	< 0.28 Ω	16 A

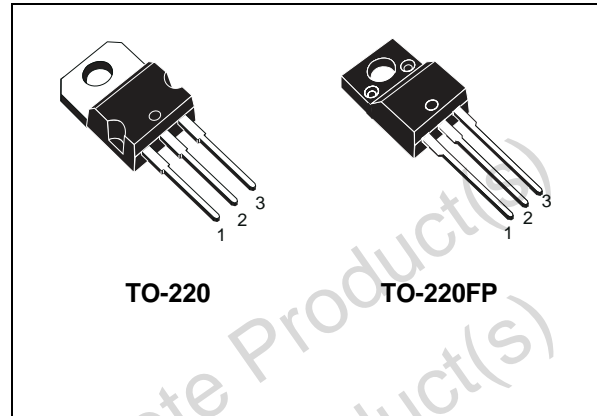
- TYPICAL R<sub>DS(on)</sub> = 0.23 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED

## DESCRIPTION

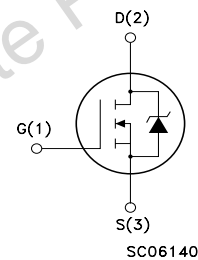
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performance. The new patented STrip layout coupled with the Company's proprietary edge termination structure, makes it suitable in converters for lighting applications.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-DC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT
- IDEAL FOR MONITOR'S B+ FUNCTION



## INTERNAL SCHEMATIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP16NS25	STP16NS25FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	250		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	250		V
V <sub>GS</sub>	Gate-source Voltage	± 20		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	16	16(*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	11	11(*)	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	64	64(*)	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	140	40	W
	Derating Factor	1	0.33	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5		V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2500	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature			

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 16A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>jMAX</sub>  
(\*) Limited only by maximum temperature allowed

## STP16NS25 - STP16NS25FP

### THERMAL DATA

		TO-220	TO-220FP	°C/W
Rthj-case	Thermal Resistance Junction-case Max	0.9	3	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	16	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	600	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	250			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8 A		0.23	0.28	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 8 A		15		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		1270		pF
C <sub>oss</sub>	Output Capacitance			190		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			74		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 125\text{ V}$ , $I_D = 8\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		14.5		ns
$t_r$	Rise Time			26		ns
$Q_g$	Total Gate Charge	$V_{DD} = 200\text{ V}$ , $I_D = 16\text{ A}$ , $V_{GS} = 10\text{ V}$		59	83	nC
$Q_{gs}$	Gate-Source Charge			7.9		nC
$Q_{gd}$	Gate-Drain Charge			22.3		nC

**SWITCHING OFF**

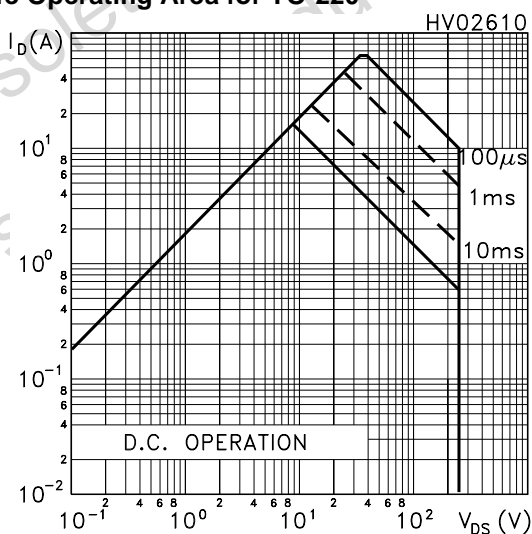
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(Voff)}$	Turn-off- Delay Time	$V_{DD} = 125\text{ V}$ , $I_D = 8\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		72		ns
$t_f$	Fall Time			32		ns
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{clamp} = 200\text{ V}$ , $I_D = 16\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		24		ns
$t_f$	Fall Time			28		ns
$t_c$	Cross-over Time			56		ns

**SOURCE DRAIN DIODE**

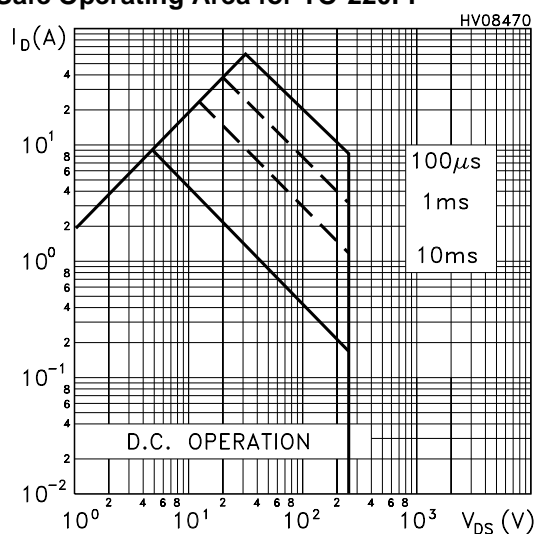
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				16	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				64	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 16\text{ A}$ , $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ , $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		270		ns
$Q_{rr}$	Reverse Recovery Charge			1.5		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			11.4		A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

**Safe Operating Area for TO-220**

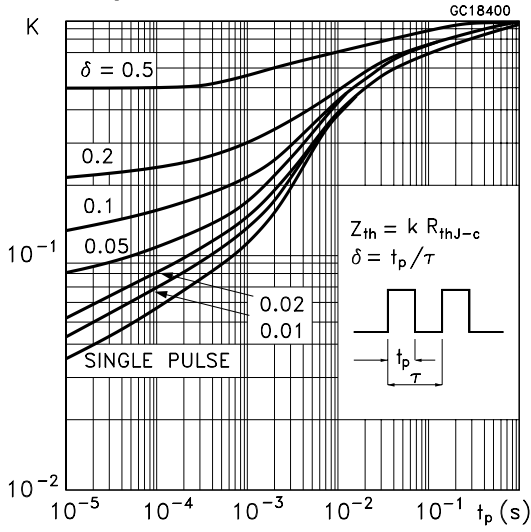


**Safe Operating Area for TO-220FP**

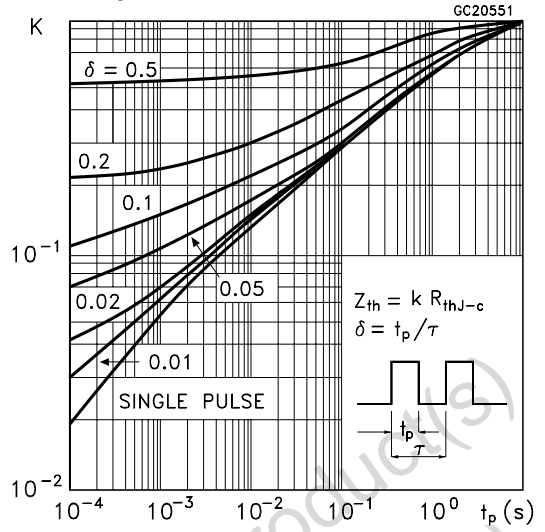


**STP16NS25 - STP16NS25FP**

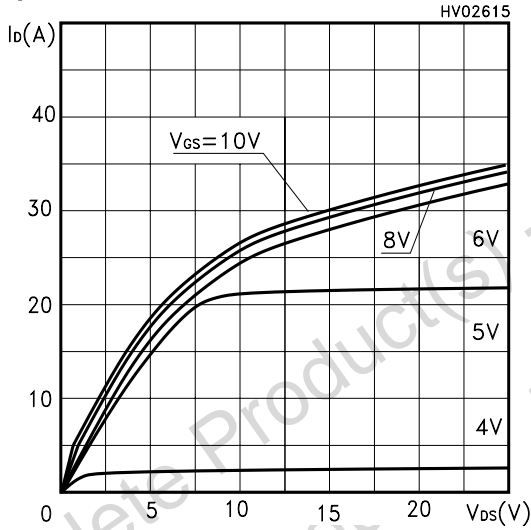
**Thermal Impedance for TO-220**



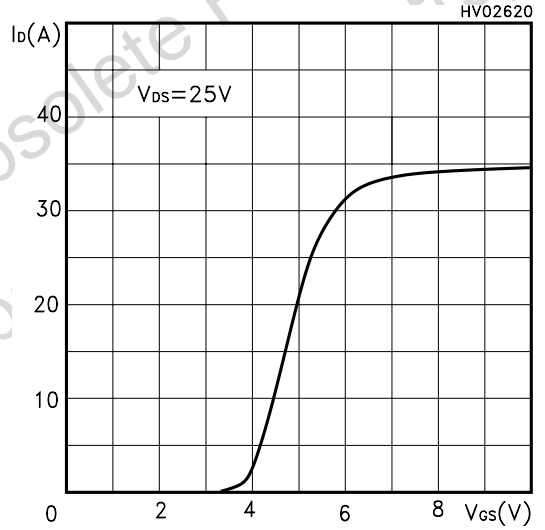
**Thermal Impedance for TO-220FP**



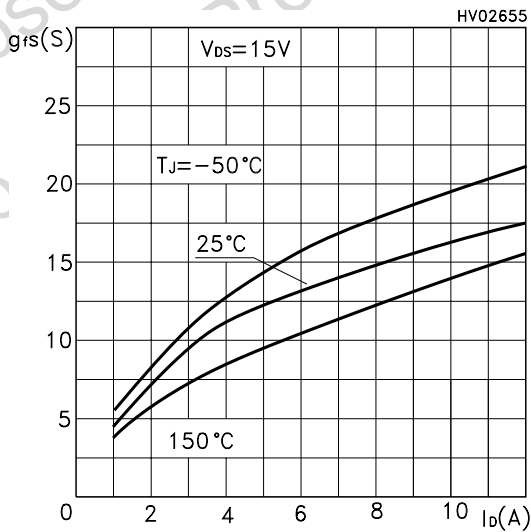
**Output Characteristics**



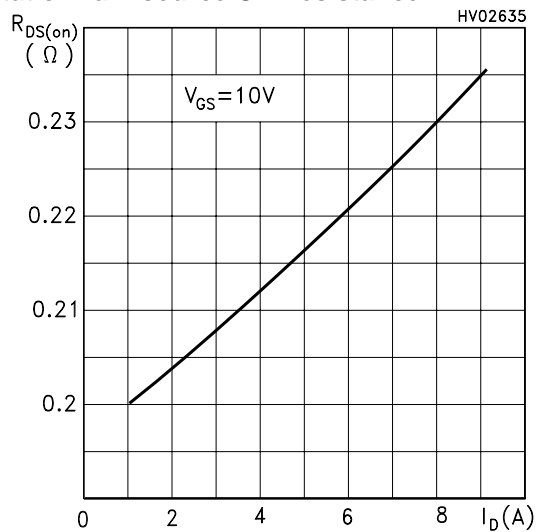
**Transfer Characteristics**



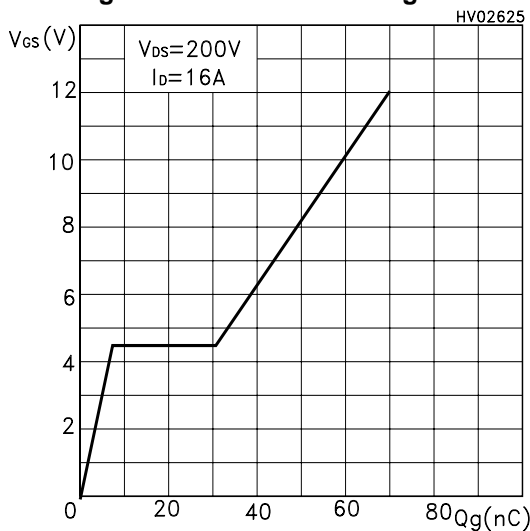
**Transconductance**



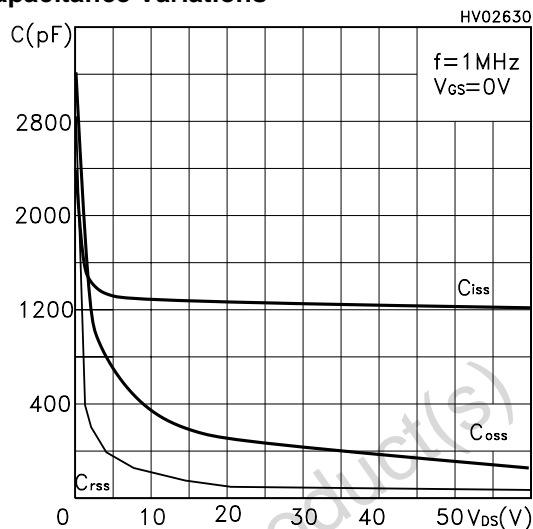
**Static Drain-source On Resistance**



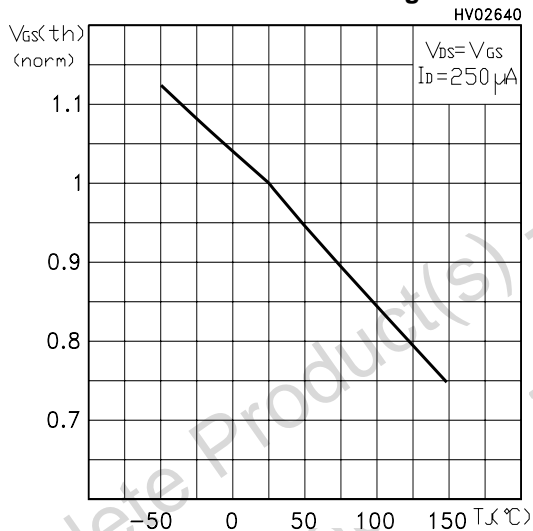
Gate Charge vs Gate-source Voltage



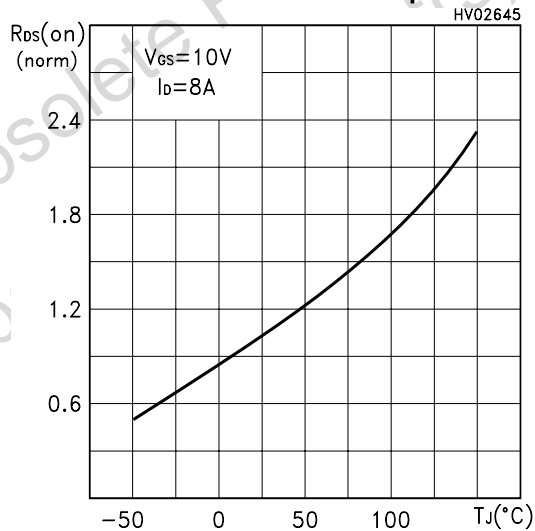
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

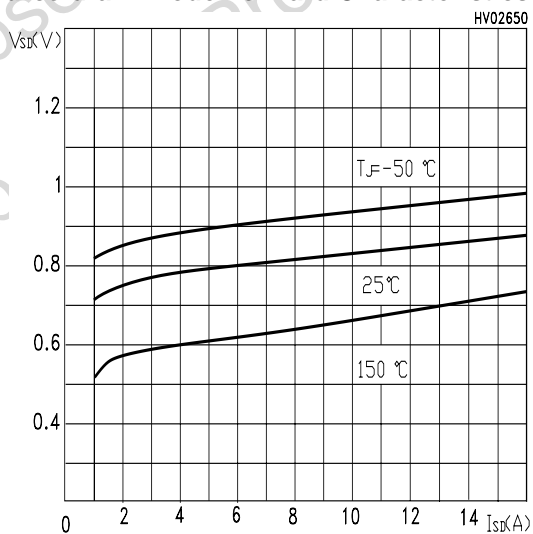


Fig. 1: Unclamped Inductive Load Test Circuit

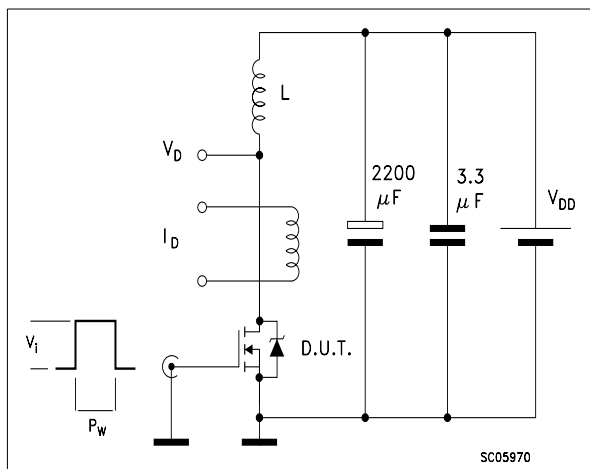


Fig. 2: Unclamped Inductive Waveform

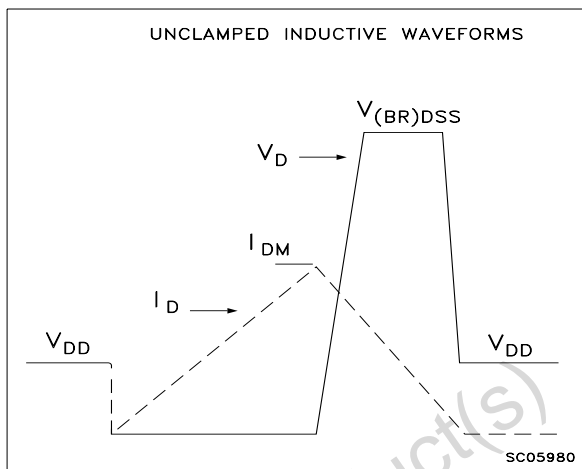


Fig. 3: Switching Times Test Circuit For Resistive Load

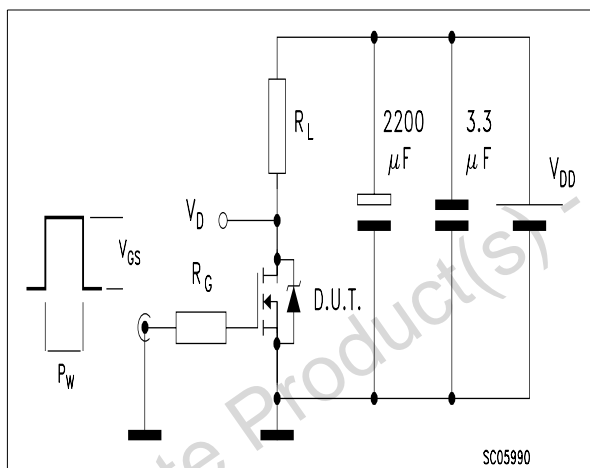


Fig. 4: Gate Charge test Circuit

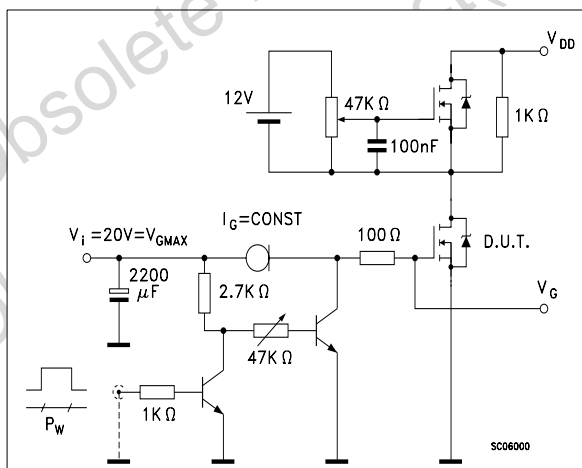
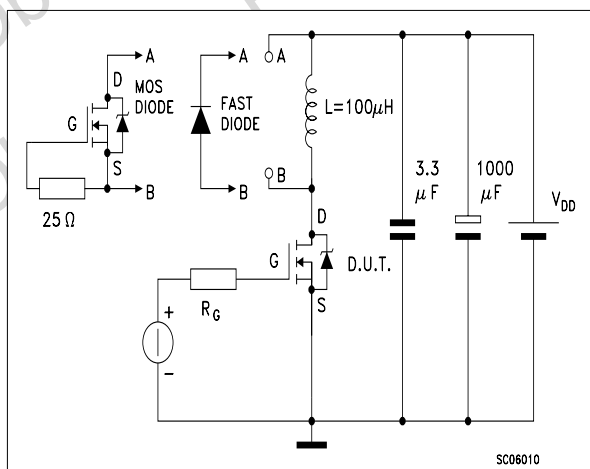
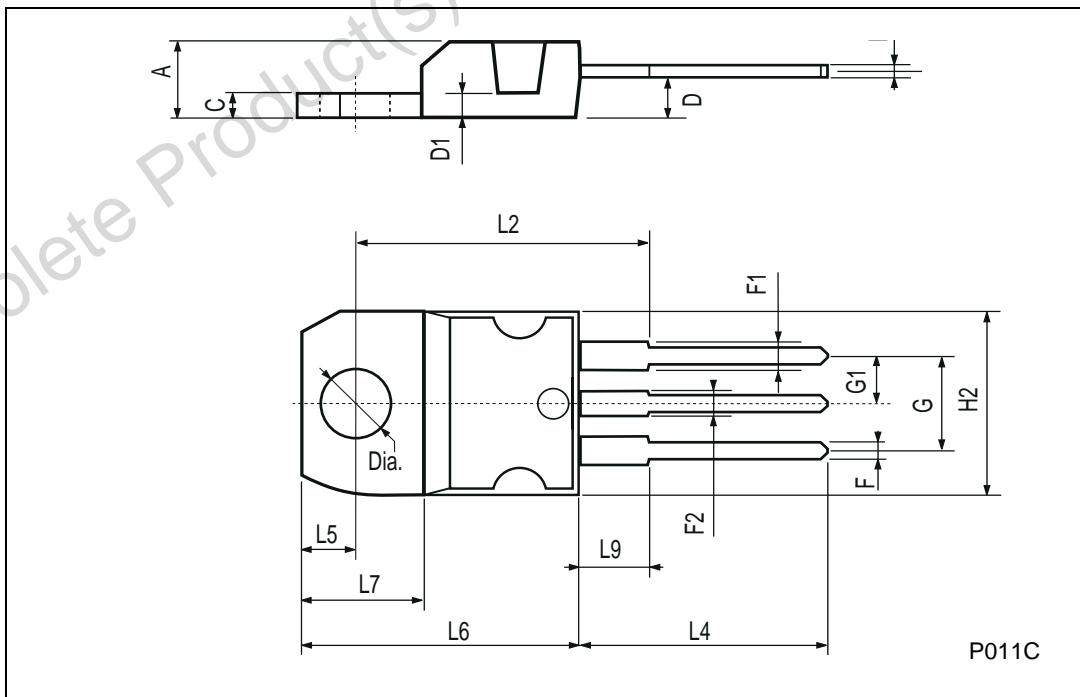


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



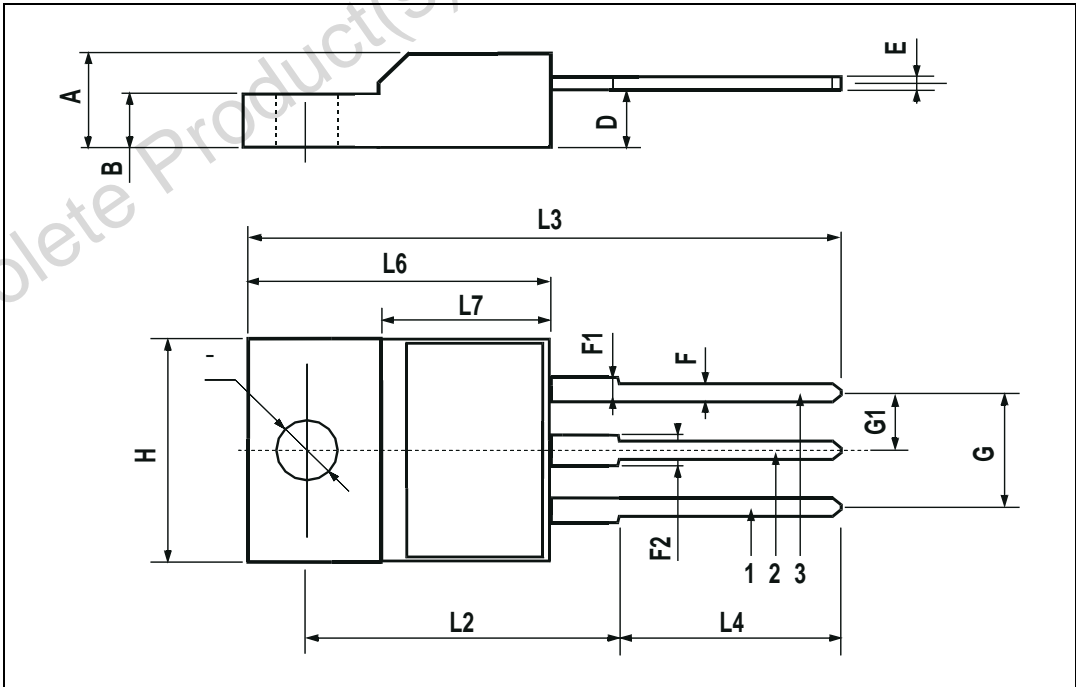
**TO-220 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



**TO-220FP MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126





Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>