![Texas Instruments]

# LP295x Adjustable Micropower Voltage Regulators with Shutdown

## 1 Features

- Wide Input Range: Up to 30 V
- Rated Output Current of 100 mA
- Low Dropout: 380 mV (Typ) at 100 mA
- Low Quiescent Current: 75 µA (Typ)
- Tight Line Regulation: 0.03% (Typ)
- Tight Load Regulation: 0.04% (Typ)
- High $V_O$ Accuracy
  - 1.4% at 25°C
  - 2% Over Temperature
- Can Be Used as a Regulator or Reference
- Stable With Low ESR (>12 mΩ) Capacitors
- Current- and Thermal-Limiting Features
- LP2950 Only (3-Pin Package)
  - Fixed-Output Voltages of 5 V, 3.3 V, and 3 V
- LP2951 Only (8-Pin Package)
  - Fixed- or Adjustable-Output Voltages:
    5 V/ADJ, 3.3 V/ADJ, and 3 V/ADJ
  - Low-Voltage Error Signal on Falling Output
  - Shutdown Capability
  - Remote Sense Capability for Optimal Output Regulation and Accuracy

## 2 Applications

- Applications with High-Voltage Input
- Power Supplies

## 3 Description

The LP2950 and LP2951 devices are bipolar, low-dropout voltage regulators that can accommodate a wide input supply-voltage range of up to 30 V. The easy-to-use, 3-pin LP2950 is available in fixed-output voltages of 5 V, 3.3 V, and 3 V. However, the 8-pin LP2951 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and $V_{TAP}$ pins together, the LP2951 outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and $V_{TAP}$ pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LP2950 | TO-92 (3) | 4.83 mm x 4.83 mm |
| LP2951 | SOIC (8) | 4.90 mm x 3.90 mm |
|  | SON (8) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
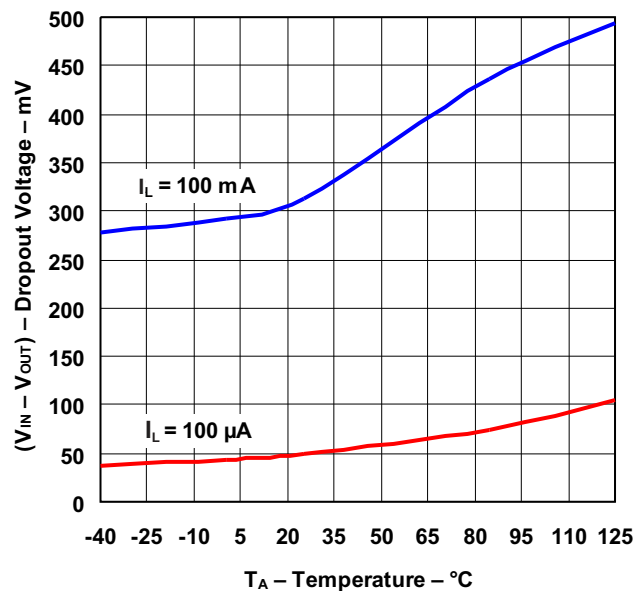
### Dropout Voltage vs Temperature

# Table of Contents

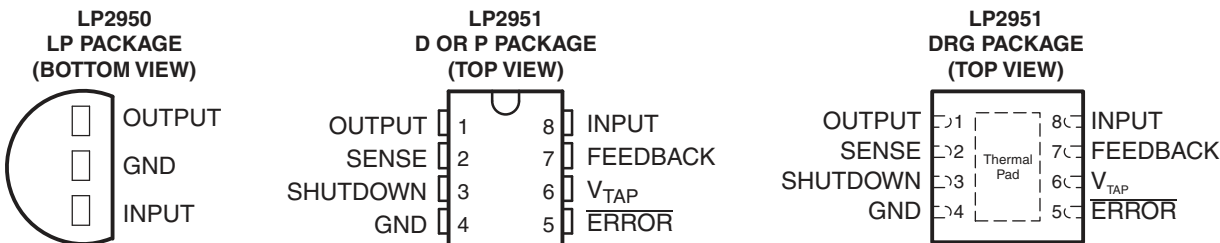# 4 Revision History

**Changes from Revision H (March 2012) to Revision I**                                                                    **Page**

- Added *Applications*, *Device Information* table, *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ...... 1
- Removed *Ordering Information* table. ........................................................................................................................ 1

# 5 Pin Configuration and Functions

**LP2950**
**LP PACKAGE**
**(BOTTOM VIEW)**

OUTPUT
GND
INPUT

**LP2951**
**D OR P PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| OUTPUT | 1 | 8 | INPUT |
| SENSE | 2 | 7 | FEEDBACK |
| SHUTDOWN | 3 | 6 | $V_{TAP}$ |
| GND | 4 | 5 | $\overline{ERROR}$ |

**LP2951**
**DRG PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| OUTPUT | 1 | 8 | INPUT |
| SENSE | 2 | 7 | FEEDBACK |
| SHUTDOWN | 3 | 6 | $V_{TAP}$ |
| GND | 4 | 5 | $\overline{ERROR}$ |

Thermal Pad

**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | LP2950 | LP2951 | | |
| $\overline{ERROR}$ | — | 5 | O | Active-low open-collector error output. Goes low when $V_{OUT}$ drops by 6% of its nominal value. |
| FEEDBACK | — | 7 | I | Determines the output voltage. Connect to $V_{TAP}$ (with OUTPUT tied to SENSE) to output the fixed voltage corresponding to the part version, or connect to a resistor divider to adjust the output voltage. |
| GND | 2 | 4 | — | Ground |
| INPUT | 3 | 8 | I | Supply input |
| OUTPUT | 1 | 1 | O | Voltage output. |
| SENSE | — | 2 | I | Senses the output voltage. Connect to OUTPUT (with FEEDBACK tied to $V_{TAP}$) to output the voltage corresponding to the part version. |
| SHUTDOWN | — | 3 | I | Active-high input. Shuts down the device. |
| $V_{TAP}$ | — | 6 | O | Tie to FEEDBACK to output the fixed voltage corresponding to the part version. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Continuous input voltage range | –0.3 | 30 | V |
| $V_{SHDN}$ | SHUTDOWN input voltage range | –1.5 | 30 | V |
| $V_{ERROR}$ | ERROR comparator output voltage range[2] | –1.5 | 30 | V |
| $V_{FDBK}$ | FEEDBACK input voltage range[2] [3] | –1.5 | 30 | V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) May exceed input supply voltage
(3) If load is returned to a negative power supply, the output must be diode clamped to GND.

## 6.2 Handling Ratings

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | 0 | 2500 | V |
|  |  | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | 0 | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage | See [1] | 30 | V |
| $T_J$ | Operating virtual junction temperature | –40 | 125 | °C |

(1) Minimum $V_{IN}$ is the greater of:
    (a) 2 V (25°C), 2.3 V (over temperature), or
    (b) $V_{OUT(MAX)}$ + Dropout (Max) at rated $I_L$

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LP2950 | LP2951 | | | UNIT |
|---|---|---|---|---|---|---|
| | | LP | D | P | DRG | |
| | | 3 PINS | 8 PINS | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 140 | 97 | 84.6 | 52.44 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

$V_{IN} = V_{OUT}$ (nominal) + 1 V, $I_L$ = 100 µA, $C_L$ = 1 µF (5-V versions) or $C_L$ = 2.2 µF (3-V and 3.3-V versions),
8-pin version: FEEDBACK tied to $V_{TAP}$, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

| PARAMETER | | TEST CONDITIONS | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **3-V VERSION (LP295x-30)** | | | | | | | |
| $V_{OUT}$ | Output voltage | $I_L$ = 100 µA | 25°C | 2.970 | 3 | 3.030 | V |
| | | | −40°C to 125°C | 2.940 | 3 | 3.060 | |
| **3.3-V VERSION (LP295x-33)** | | | | | | | |
| $V_{OUT}$ | Output voltage | $I_L$ = 100 µA | 25°C | 3.267 | 3.3 | 3.333 | V |
| | | | −40°C to 125°C | 3.234 | 3.3 | 3.366 | |
| **5-V VERSION (LP295x-50)** | | | | | | | |
| $V_{OUT}$ | Output voltage | $I_L$ = 100 µA | 25°C | 4.950 | 5 | 5.050 | V |
| | | | −40°C to 125°C | 4.900 | 5 | 5.100 | |
| **ALL VOLTAGE OPTIONS** | | | | | | | |
| | Output voltage temperature coefficient[1] | $I_L$ = 100 µA | −40°C to 125°C | | 20 | 100 | ppm/°C |
| | Line regulation[2] | $V_{IN}$ = [$V_{OUT(NOM)}$ + 1 V] to 30 V | 25°C | | 0.03 | 0.2 | %/V |
| | | | −40°C to 125°C | | | 0.4 | |
| | Load regulation[2] | $I_L$ = 100 µA to 100 mA | 25°C | | 0.04% | 0.2% | — |
| | | | −40°C to 125°C | | | 0.3% | |
| $V_{IN} − V_{OUT}$ | Dropout voltage[3] | $I_L$ = 100 µA | 25°C | | 50 | 80 | mV |
| | | | −40°C to 125°C | | | 150 | |
| | | $I_L$ = 100 mA | 25°C | | 380 | 450 | |
| | | | −40°C to 125°C | | | 600 | |
| $I_{GND}$ | GND current | $I_L$ = 100 µA | 25°C | | 75 | 120 | µA |
| | | | −40°C to 125°C | | | 140 | |
| | | $I_L$ = 100 mA | 25°C | | 8 | 12 | mA |
| | | | −40°C to 125°C | | | 14 | |
| | Dropout ground current | $V_{IN}$ = $V_{OUT(NOM)}$ − 0.5 V, $I_L$ = 100 µA | 25°C | | 110 | 170 | µA |
| | | | −40°C to 125°C | | | 200 | |
| | Current limit | $V_{OUT}$ = 0 V | 25°C | | 160 | 200 | mA |
| | | | −40°C to 125°C | | | 220 | |
| | Thermal regulation[4] | $I_L$ = 100 µA | 25°C | | 0.05 | 0.2 | %/W |
| | Output noise (RMS), 10 Hz to 100 kHz | $C_L$ = 1 µF (5 V only) | 25°C | | 430 | | µV |
| | | $C_L$ = 200 µF | | | 160 | | |
| | | LP2951-50: $C_L$ = 3.3 µF, $C_{Bypass}$ = 0.01 µF between pins 1 and 7 | | | 100 | | |

(1)  Output or reference voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(2)  Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(3)  Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV, below the value measured at 1-V differential. The minimum input supply voltage of 2 V (2.3 V over temperature) must be observed.
(4)  Thermal regulation is defined as the change in output voltage at a time (T) after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50-mA load pulse at $V_{IN}$ = 30 V, $V_{OUT}$ = 5 V (1.25-W pulse) for t = 10 ms.

## Electrical Characteristics (continued)

$V_{IN}$ = $V_{OUT}$ (nominal) + 1 V, $I_L$ = 100 µA, $C_L$ = 1 µF (5-V versions) or $C_L$ = 2.2 µF (3-V and 3.3-V versions),
8-pin version: FEEDBACK tied to $V_{TAP}$, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

| PARAMETER | TEST CONDITIONS | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **(LP2951-xx) 8-PIN VERSION ONLY ADJ** | | | | | | |
| Reference voltage | | 25°C | 1.218 | 1.235 | 1.252 | V |
| | | −40°C to 125°C | 1.212 | | 1.257 | |
| | $V_{OUT}$ = $V_{REF}$ to ($V_{IN}$ − 1 V), $V_{IN}$ = 2.3 V to 30 V, $I_L$ = 100 µA to 100 mA | −40°C to 125°C | 1.200 | | 1.272 | |
| Reference voltage temperature coefficient[1] | | 25°C | | 20 | | ppm/°C |
| FEEDBACK bias current | | 25°C | | 20 | 40 | nA |
| | | −40°C to 125°C | | | 60 | |
| FEEDBACK bias current temperature coefficient | | 25°C | | 0.1 | | nA/°C |
| **ERROR COMPARATOR** | | | | | | |
| Output leakage current | $V_{OUT}$ = 30 V | 25°C | | 0.01 | 1 | µA |
| | | −40°C to 125°C | | | 2 | |
| Output low voltage | $V_{IN}$ = $V_{OUT(NOM)}$ − 0.5 V, $I_{OL}$ = 400 µA | 25°C | | 150 | 250 | mV |
| | | −40°C to 125°C | | | 400 | |
| Upper threshold voltage (ERROR output high)[5] | | 25°C | 40 | 60 | | mV |
| | | −40°C to 125°C | 25 | | | |
| Lower threshold voltage (ERROR output low)[5] | | 25°C | | 75 | 95 | mV |
| | | −40°C to 125°C | | | 140 | |
| Hysteresis[5] | | 25°C | | 15 | | mV |
| **SHUTDOWN INPUT** | | | | | | |
| Input logic voltage | Low (regulator ON) | −40°C to 125°C | | | 0.7 | V |
| | High (regulator OFF) | | 2 | | | |
| SHUTDOWN input current | SHUTDOWN = 2.4 V | 25°C | | 30 | 50 | µA |
| | | −40°C to 125°C | | | 100 | |
| | SHUTDOWN = 30 V | 25°C | | 450 | 600 | |
| | | −40°C to 125°C | | | 750 | |
| Regulator output current in shutdown | $V_{SHUTDOWN}$ ≥ 2 V, $V_{IN}$ ≤ 30 V, $V_{OUT}$ = 0, FEEDBACK tied to $V_{TAP}$ | 25°C | | 3 | 10 | µA |
| | | −40°C to 125°C | | | 20 | |

(5) Comparator thresholds are expressed in terms of a voltage differential equal to the nominal reference voltage (measured at $V_{IN}$ − $V_{OUT}$ = 1 V) minus FEEDBACK terminal voltage. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = $V_{OUT}$/$V_{REF}$ = (R1 + R2)/R2. For example, at a programmed output voltage of 5 V, the ERROR output is specified to go low when the output drops by 95 mV × 5 V/1.235 V = 384 mV. Thresholds remain constant as a percentage of $V_{OUT}$ (as $V_{OUT}$ is varied), with the low-output warning occurring at 6% below nominal (typ) and 7.7% (max).

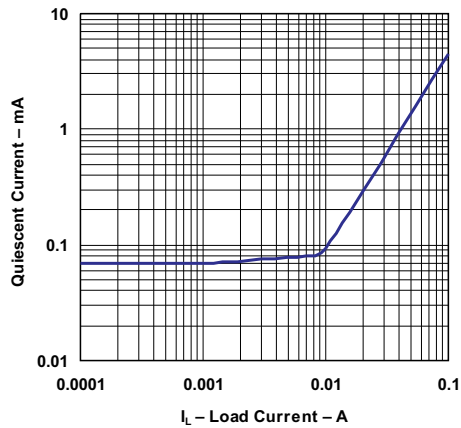Product Folder Links: *LP2950  LP2951*

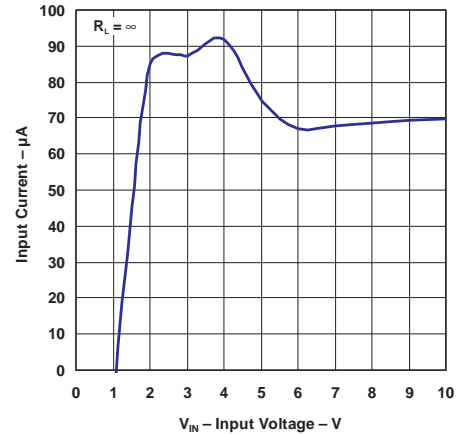## 6.6 Typical Characteristics



Figure 1. Quiescent Current vs Load Current



Figure 2. Input Current vs Input Voltage ($R_L$ = OPEN)



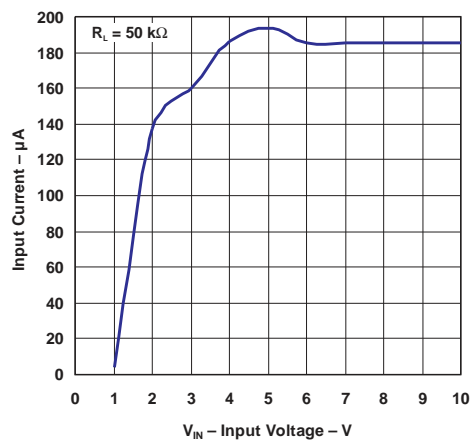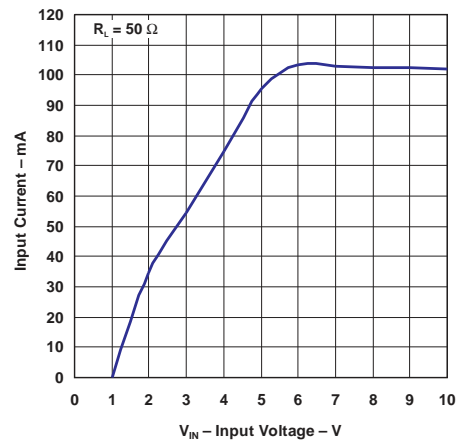Figure 3. Input Current vs Input Voltage ($R_L$ = 50 kΩ)



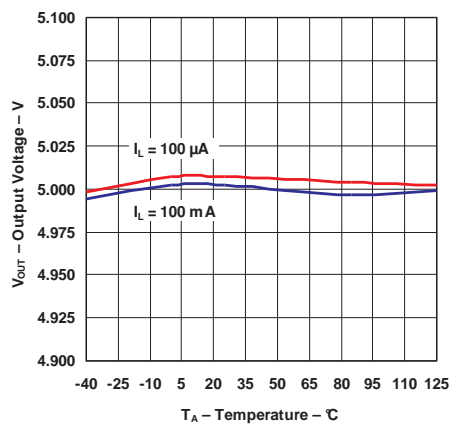Figure 4. Input Current vs Input Voltage ($R_L$ = 50 Ω)
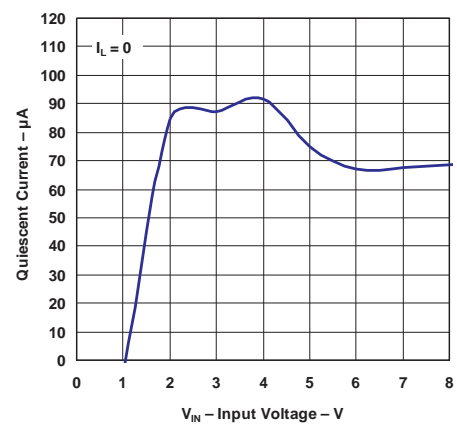


Figure 5. Output Voltage vs Temperature



Figure 6. Quiescent Current vs Input Voltage ($I_L$ = 0)
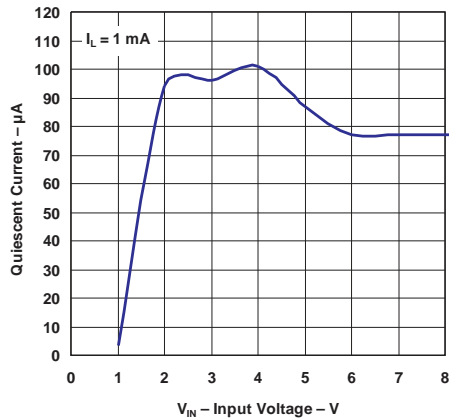
## Typical Characteristics (continued)



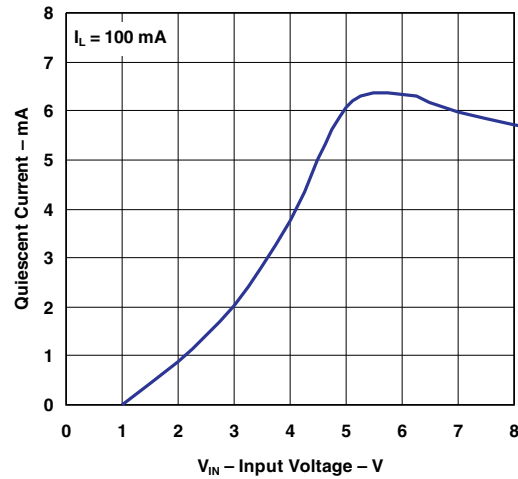Figure 7. Quiescent Current vs Input Voltage ($I_L$ = 1 mA)



Figure 8. Quiescent Current vs Input Voltage ($I_L$ = 100 mA)
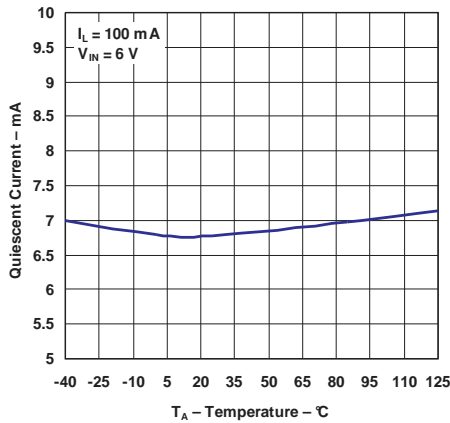


Figure 9. Quiescent Current vs Temperature ($I_L$ = 100 mA)

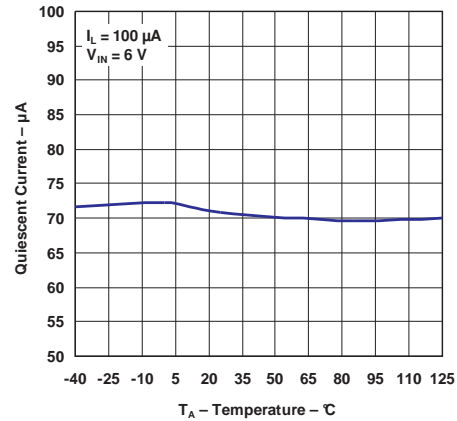

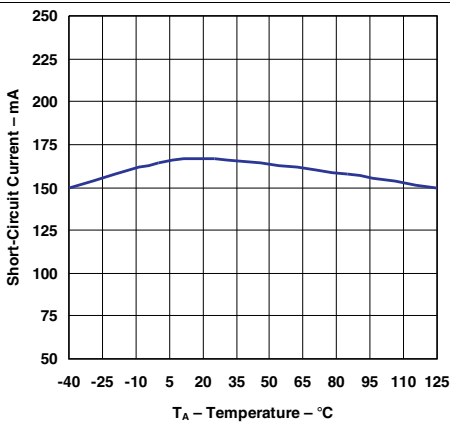Figure 10. Quiescent Current vs Temperature ($I_L$ = 100 µA)
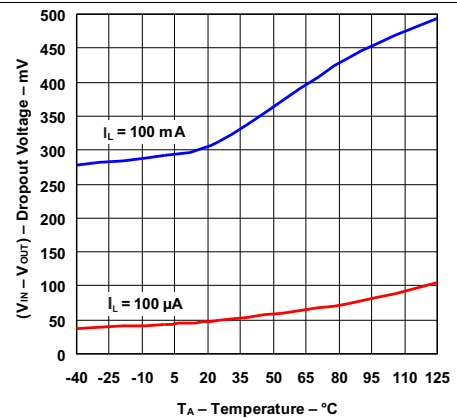


Figure 11. Short-circuit Current vs Temperature



Figure 12. Dropout Voltage vs Temperature

Product Folder Links: *LP2950  LP2951*

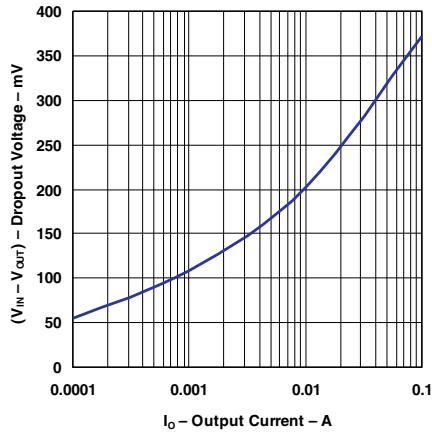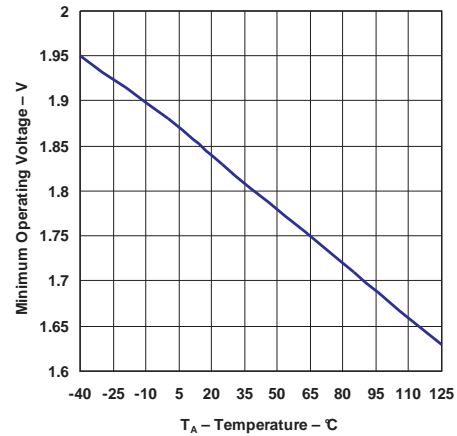## Typical Characteristics (continued)


Figure 13. Dropout Voltage vs Dropout Current

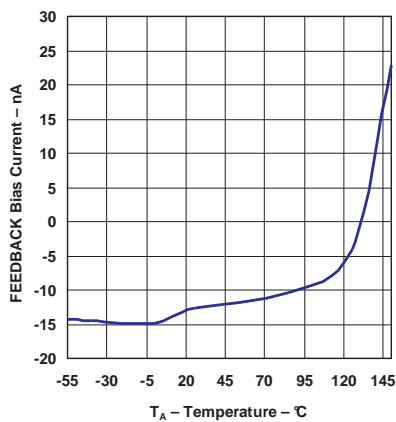
Figure 14. LP2951 Minimum Operating Voltage vs Temperature


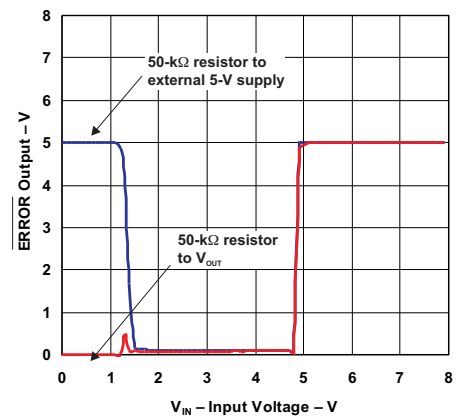Figure 15. LP2951 FEEDBACK Bias Current vs Temperature

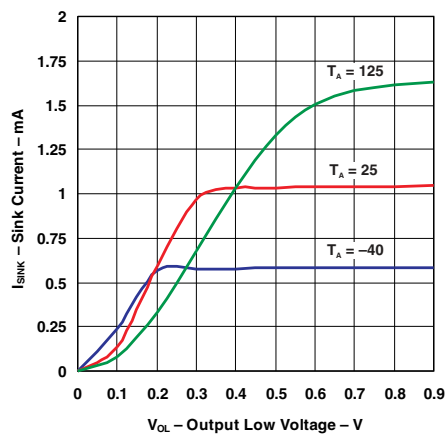
Figure 16. LP2951 ERROR Comparator Output vs Input Voltage


Figure 17. LP2951 ERROR Comparator Sink Current vs Output Low Voltage
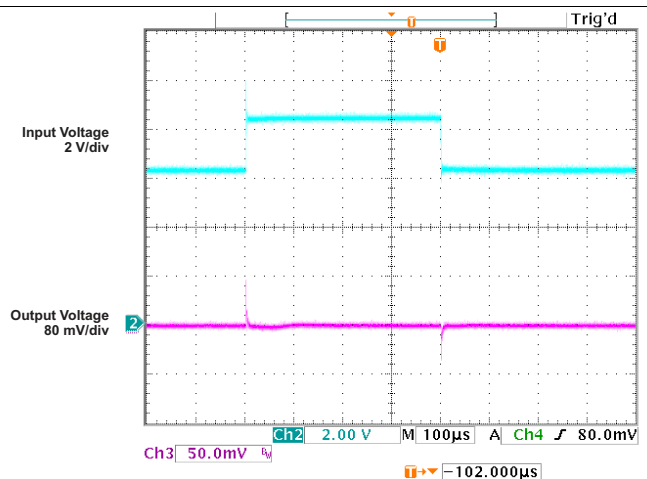

Figure 18. Line Transient Response vs Time

Product Folder Links: LP2950  LP2951

# Typical Characteristics (continued)
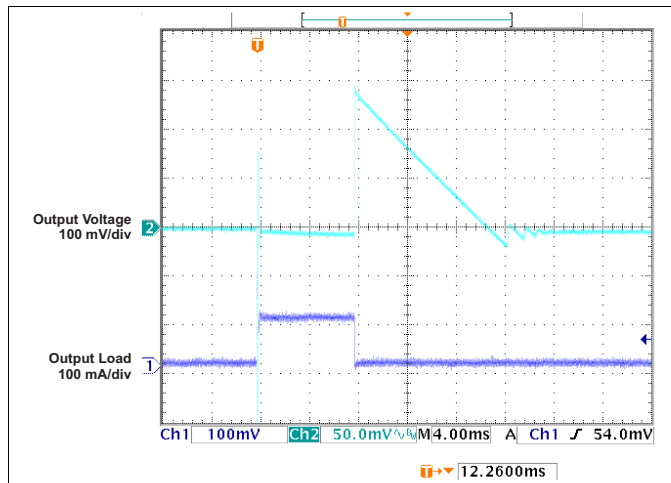


**Figure 19. Load Transient Response vs Time (V$_{OUT}$ = 5 V, C$_L$ = 10 µF)**
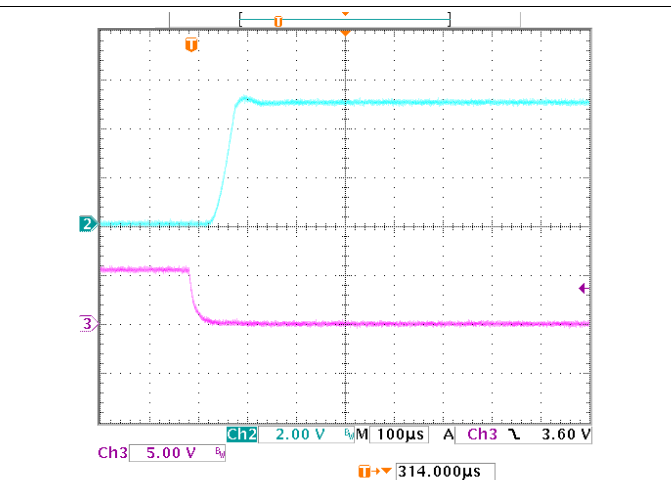


**Figure 20. Enable Transient Response vs Time (I$_L$ = 1 mA, C$_L$ = 1 µF)**
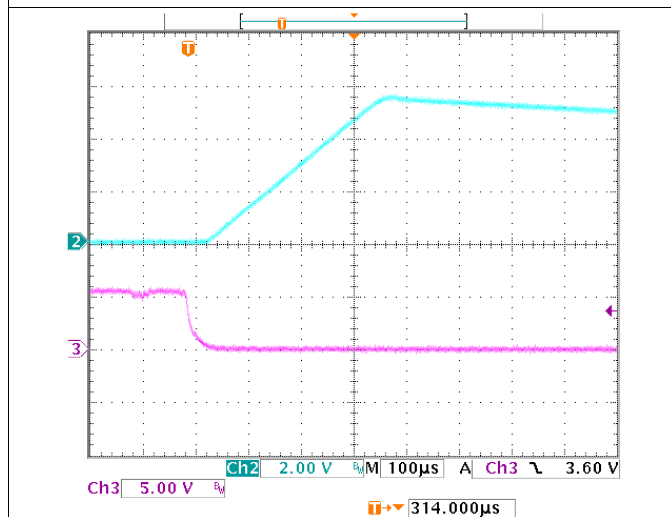


**Figure 21. Enable Transient Response vs Time (I$_L$ = 1 mA, C$_L$ = 10 µF)**
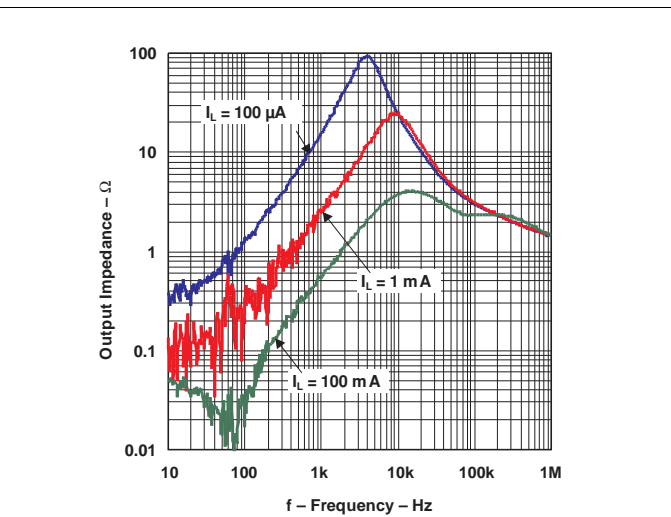


**Figure 22. Output Impedance vs Frequency**
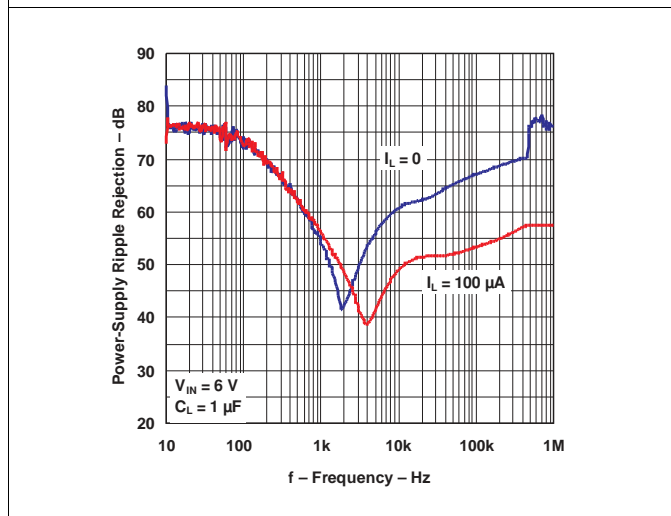


**Figure 23. Ripple Rejection vs Frequency**
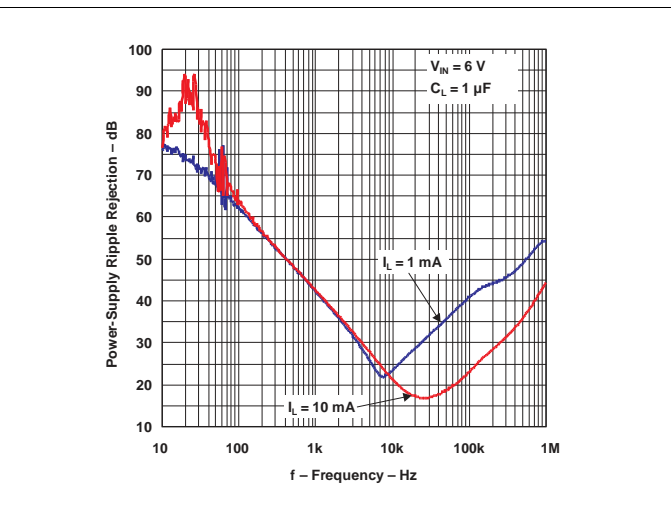


**Figure 24. Output Impedance vs Frequency**

Product Folder Links: *LP2950  LP2951*

## Typical Characteristics (continued)
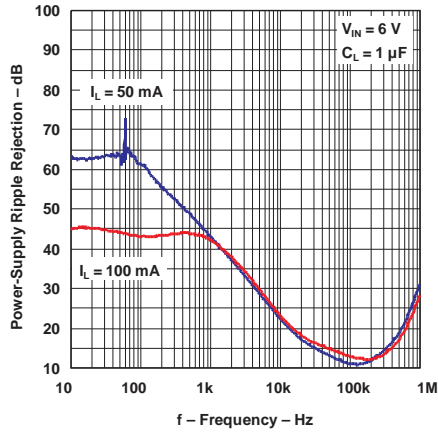


**Figure 25. Output Impedance vs Frequency**
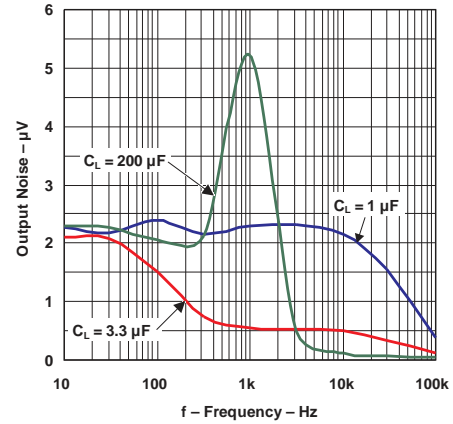


**Figure 26. LP2951 Output Noise vs Frequency**
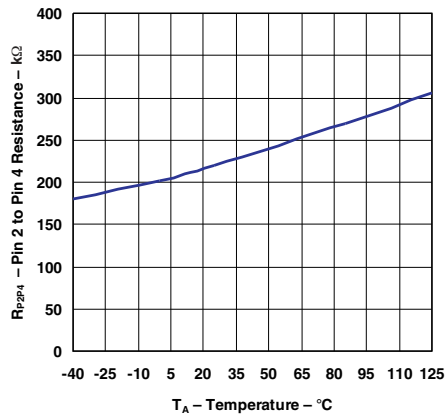


**Figure 27. LP2951 Divider Resistance vs Temperature**
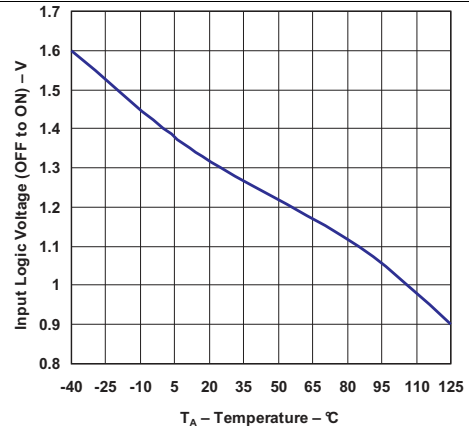


**Figure 28. Shutdown Threshold Voltage (Off to On) vs Temperature**
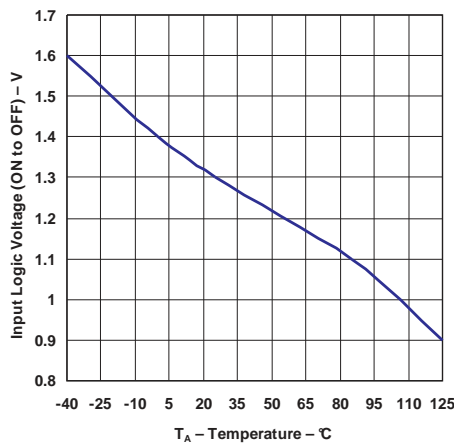


**Figure 29. Shutdown Threshold Voltage (On to Off) vs Temperature**
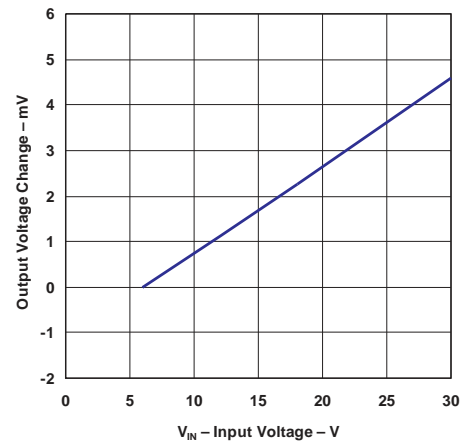


**Figure 30. Line Regulation vs Input Voltage**

# 7 Detailed Description

## 7.1 Overview

The LP2950 and LP2951 devices are bipolar, low-dropout voltage regulators that can accommodate a wide input supply-voltage range of up to 30 V. The easy-to-use, 3-pin LP2950 is available in fixed-output voltages of 5 V, 3.3 V, and 3 V. However, the 8-pin LP2951 device is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and $V_{TAP}$ pins together, the LP2951 device outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and $V_{TAP}$ pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

The 8-pin LP2951 device also offers additional functionality that makes it particularly suitable for battery-powered applications. For example, a logic-compatible shutdown feature allows the regulator to be put in standby mode for power savings. In addition, there is a built-in supervisor reset function in which the $\overline{ERROR}$ output goes low when $V_{OUT}$ drops by 6% of its nominal value for whatever reasons – due to a drop in $V_{IN}$, current limiting, or thermal shutdown.

The LP2950 and LP2951 devices are designed to minimize all error contributions to the output voltage. With a tight output tolerance (0.5% at 25°C), a very low output voltage temperature coefficient (20 ppm typical), extremely good line and load regulation (0.3% and 0.4% typical), and remote sensing capability, the parts can be used as either low-power voltage references or 100-mA regulators.

## 7.2 LP2950 Functional Block Diagram
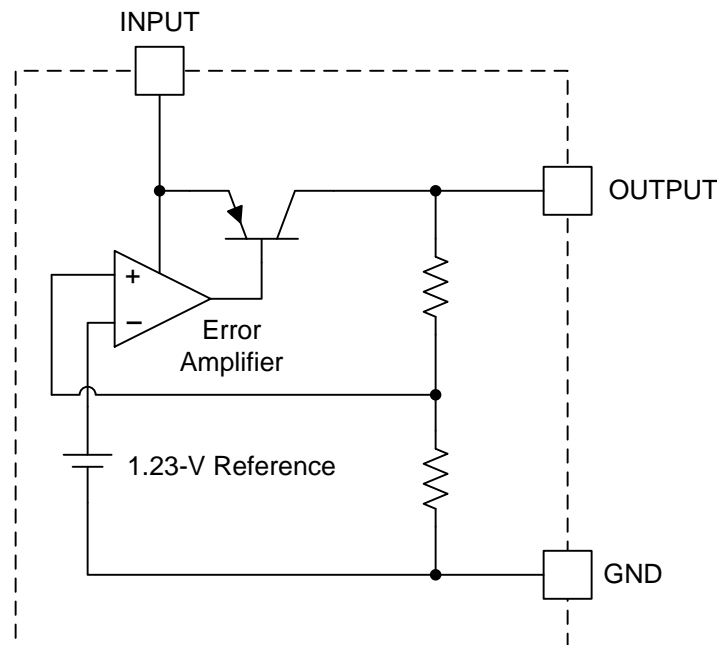
## 7.3 LP2951 Functional Block Diagram
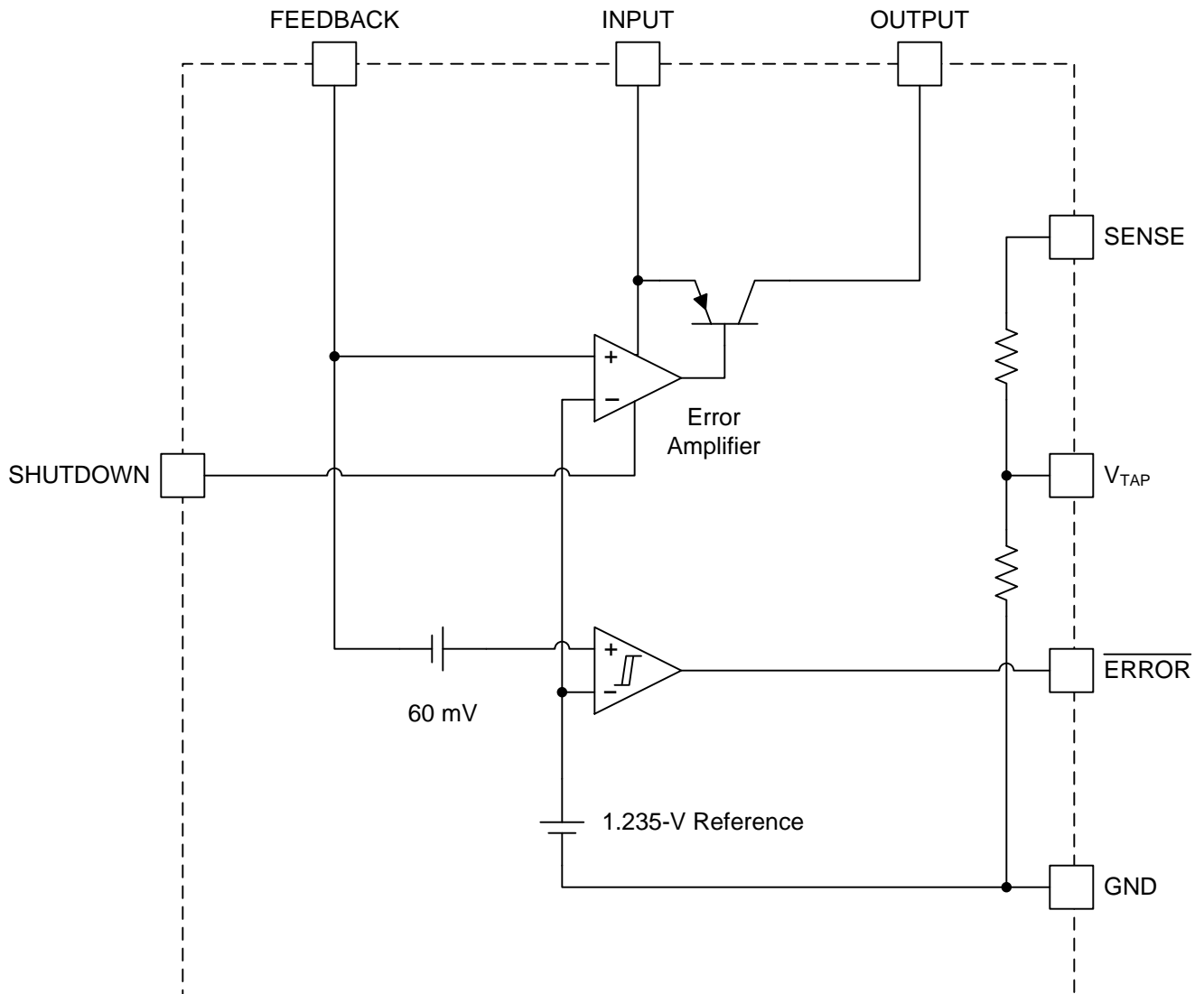
## 7.4 Feature Description

### 7.4.1 $\overline{ERROR}$ Function (LP2951 Only)

The LP2951 device has a low-voltage detection comparator that outputs a logic low when the output voltage drops by ≈6% from its nominal value, and outputs a logic high when $V_{OUT}$ has reached ≈95% of its nominal value. This 95% of nominal figure is obtained by dividing the built-in offset of ≈60 mV by the 1.235-V bandgap reference, and remains independent of the programmed output voltage. For example, the trip-point threshold ($\overline{ERROR}$ output goes high) typically is 4.75 V for a 5-V output and 11.4 V for a 12-V output. Typically, there is a hysteresis of 15 mV between the thresholds for high and low $\overline{ERROR}$ output.

A timing diagram is shown in Figure 31 for $\overline{ERROR}$ vs $V_{OUT}$ (5 V), as $V_{IN}$ is ramped up and down. $\overline{ERROR}$ becomes valid (low) when $V_{IN} \approx 1.3$ V. When $V_{IN} \approx 5$ V, $V_{OUT} = 4.75$ V, causing $\overline{ERROR}$ to go high. Because the dropout voltage is load dependent, the output trip-point threshold is reached at different values of $V_{IN}$, depending on the load current. For instance, at higher load current, $\overline{ERROR}$ goes high at a slightly higher value of $V_{IN}$, and vice versa for lower load current. The output-voltage trip point remains at ~4.75 V, regardless of the load. Note that when $V_{IN} \leq 1.3$ V, the $\overline{ERROR}$ comparator output is turned off and pulled high to its pullup voltage. If $V_{OUT}$ is used as the pullup voltage, rather than an external 5-V source, $\overline{ERROR}$ typically is ~1.2 V. In this condition, an equal resistor divider (10 kΩ is suitable) can be tied to $\overline{ERROR}$ to divide down the voltage to a valid logic low during any fault condition, while still enabling a logic high during normal operation.
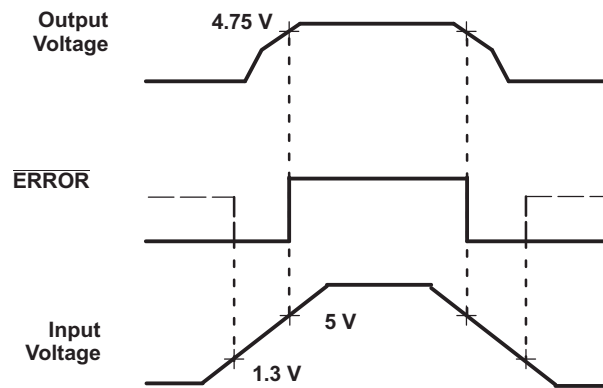


**Figure 31. $\overline{ERROR}$ Output Timing**

Because the $\overline{ERROR}$ comparator has an open-collector output, an external pullup resistor is required to pull the output up to $V_{OUT}$ or another supply voltage (up to 30 V). The output of the comparator is rated to sink up to 400 µA. A suitable range of values for the pullup resistor is from 100 kΩ to 1 MΩ. If $\overline{ERROR}$ is not used, it can be left open.

## Feature Description (continued)

### 7.4.2 Programming Output Voltage (LP2951 Only)

A unique feature of the LP2951 device is its ability to output either a fixed voltage or an adjustable voltage, depending on the external pin connections. To output the internally programmed fixed voltage, tie the SENSE pin to the OUTPUT pin and the FEEDBACK pin to the $V_{TAP}$ pin. Alternatively, a user-programmable voltage ranging from the internal 1.235-V reference to a 30-V max can be set by using an external resistor divider pair. The resistor divider is tied to $V_{OUT}$, and the divided-down voltage is tied directly to FEEDBACK for comparison against the internal 1.235-V reference. To satisfy the steady-state condition in which its two inputs are equal, the error amplifier drives the output to equal Equation 1:

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right) - I_{FB} R_1$$

(1)

Where:

$V_{REF}$ = 1.235 V applied across R2 (see Figure 32)

$I_{FB}$ = FEEDBACK bias current, typically 20 nA

A minimum regulator output current of 1 µA must be maintained. Thus, in an application where a no-load condition is expected (for example, CMOS circuits in standby), this 1-µA minimum current must be provided by the resistor pair, effectively imposing a maximum value of R2 = 1.2 MΩ (1.235 V/1.2 MΩ ≠ 1 µA).

$I_{FB}$ = 20 nA introduces an error of ≠0.02% in $V_{OUT}$. This can be offset by trimming R1. Alternatively, increasing the divider current makes $I_{FB}$ less significant, thus, reducing its error contribution. For instance, using R2 = 100 kΩ reduces the error contribution of $I_{FB}$ to 0.17% by increasing the divider current to ≠12 µA. This increase in the divider current still is small compared to the 600-µA typical quiescent current of the LP2951 under no load.
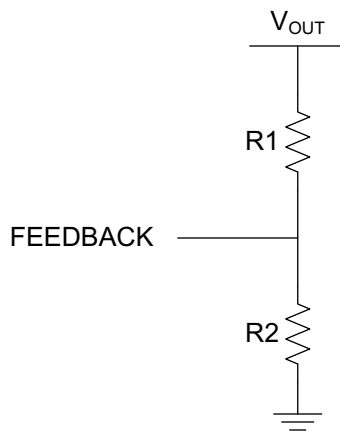


**Figure 32. Adjusting the Feedback on the LP2951**

## 7.5 Device Functional Modes

### 7.5.1 Shutdown Mode

These devices can be placed in shutdown mode with a logic high at the SHUTDOWN pin. Return the logic level low to restore operation or tie SHUTDOWN to ground if the feature is not being used.

# 8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LP295x devices are used as low-dropout regulators with a wide range of input voltages.

## 8.2 Typical Application
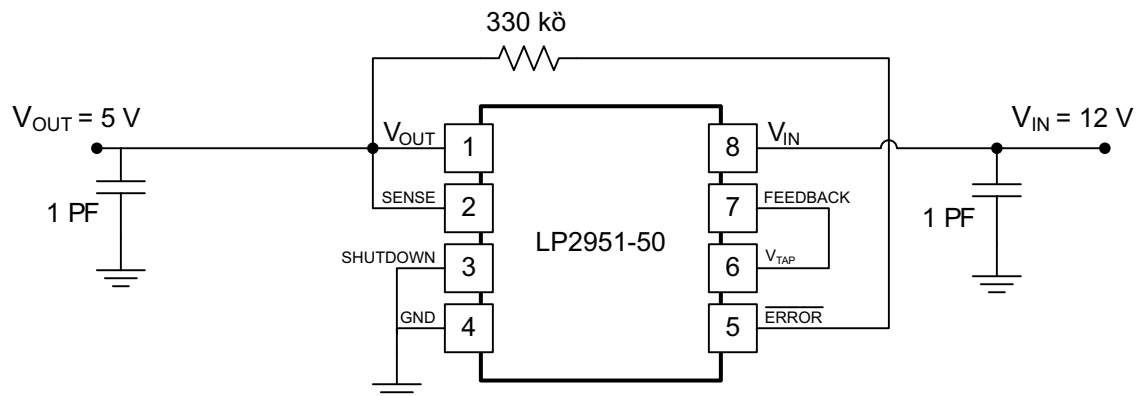


**Figure 33. 12-V to 5-V Converter**

### 8.2.1 Design Requirements

#### 8.2.1.1 Input Capacitor ($C_{IN}$)

A 1-μF (tantalum, ceramic, or aluminum) electrolytic capacitor should be placed locally at the input of the LP2950 or LP2951 device if there is, or will be, significant impedance between the ac filter capacitor and the input; for example, if a battery is used as the input or if the ac filter capacitor is located more than 10 in away. There are no ESR requirements for this capacitor, and the capacitance can be increased without limit.

#### 8.2.1.2 Output Capacitor ($C_{OUT}$)

As with most PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

## Typical Application  (continued)

### 8.2.2  Detailed Design Procedure

#### 8.2.2.1  Capacitance Value

For $V_{OUT} \geq 5$ V, a minimum of 1 µF is required. For lower $V_{OUT}$, the regulator's loop gain is running closer to unity gain and, thus, has lower phase margins. Consequently, a larger capacitance is needed for stability. For $V_{OUT} = 3$ V or 3.3 V, a minimum of 2.2 µF is recommended. For worst case, $V_{OUT} = 1.23$ V (using the ADJ version), a minimum of 3.3 µF is recommended. $C_{OUT}$ can be increased without limit and only improves the regulator stability and transient response. Regardless of its value, the output capacitor should have a resonant frequency greater than 500 kHz.

The minimum capacitance values given above are for maximum load current of 100 mA. If the maximum expected load current is less than 100 mA, then lower values of $C_{OUT}$ can be used. For instance, if $I_{OUT} < 10$ mA, then only 0.33 µF is required for $C_{OUT}$. For $I_{OUT} < 1$ mA, 0.1 µF is sufficient for stability requirements. Thus, for a worst-case condition of 100-mA load and $V_{OUT} = V_{REF} = 1.235$ V (representing the highest load current and lowest loop gain), a minimum $C_{OUT}$ of 3.3 µF is recommended.

For the LP2950/51, no load stability is inherent in the design — a desirable feature in CMOS circuits that are put in standby (such as RAM keep-alive applications). If the LP2951 is used with external resistors to set the output voltage, a minimum load current of 1 µA is recommended through the resistor divider.

#### 8.2.2.2  Capacitor Types

Most tantalum or aluminum electrolytics are suitable for use at the input. Film-type capacitors also work but at higher cost. When operating at low temperature, care should be taken with aluminum electrolytics, as their electrolytes often freeze at –30°C. For this reason, solid tantalum capacitors should be used at temperatures below –25°C.

Ceramic capacitors can be used, but due to their low ESR (as low as 5 mΩ to 10 mΩ), they may not meet the minimum ESR requirement previously discussed. If a ceramic capacitor is used, a series resistor between 0.1 Ω to 2 Ω must be added to meet the minimum ESR requirement. In addition, ceramic capacitors have one glaring disadvantage that must be taken into account — a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥ 2.2 µF) can lose more than half of its capacitance as temperature rises from 25°C to 85°C. Thus, a 2.2-µF capacitor at 25°C drops well below the minimum $C_{OUT}$ required for stability as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2 µF required for stability for the entire operating temperature range.

#### 8.2.2.3  $C_{BYPASS}$: Noise and Stability Improvement

In the LP2951 device, an external FEEDBACK pin directly connected to the error amplifier noninverting input can allow stray capacitance to cause instability by shunting the error amplifier feedback to GND, especially at high frequencies. This is worsened if high-value external resistors are used to set the output voltage, because a high resistance allows the stray capacitance to play a more significant role; i.e., a larger RC time delay is introduced between the output of the error amplifier and its FEEDBACK input, leading to more phase shift and lower phase margin. A solution is to add a 100-pF bypass capacitor ($C_{BYPASS}$) between OUTPUT and FEEDBACK; because $C_{BYPASS}$ is in parallel with R1, it lowers the impedance seen at FEEDBACK at high frequencies, in effect offsetting the effect of the parasitic capacitance by providing more feedback at higher frequencies. More feedback forces the error amplifier to work at a lower loop gain, so $C_{OUT}$ should be increased to a minimum of 3.3 µF to improve the regulator's phase margin.

$C_{BYPASS}$ can be also used to reduce output noise in the LP2951 device. This bypass capacitor reduces the closed loop gain of the error amplifier at the high frequency, so noise no longer scales with the output voltage. This improvement is more noticeable with higher output voltages, where loop gain reduction is greatest. A suitable $C_{BYPASS}$ is calculated as shown in Equation 2:

$$f_{(CBYPASS)} \simeq 200\,\text{Hz} \rightarrow C_{(BYPASS)} = \frac{1}{2\pi \times R1 \times 200\,\text{Hz}}$$

(2)

On the 3-pin LP2950 device, noise reduction can be achieved by increasing the output capacitor, which causes the regulator bandwidth to be reduced, thus eliminating high-frequency noise. However, this method is relatively inefficient, as increasing $C_{OUT}$ from 1 µF to 220 µF only reduces the regulator's output noise from 430 µV to 160 µV (over a 100-kHz bandwidth).

## Typical Application (continued)

### 8.2.2.4 ESR Range

The regulator control loop relies on the ESR of the output capacitor to provide a zero to add sufficient phase margin to ensure unconditional regulator stability; this requires the closed-loop gain to intersect the open-loop response in a region where the open-loop gain rolls off at 20 dB/decade. This ensures that the phase is always less than 180° (phase margin greater than 0°) at unity gain. Thus, a minimum-maximum range for the ESR must be observed.

The upper limit of this ESR range is established by the fact that an ESR that is too high could result in the zero occurring too soon, causing the gain to roll off too slowly. This, in turn, allows a third pole to appear before unity gain and introduces enough phase shift to cause instability. This typically limits the maximum ESR to approximately 5 Ω.

Conversely, the lower limit of the ESR range is tied to the fact that an ESR that is too low shifts the zero too far out, past unity gain, which allows the gain to roll off at 40 dB/decade at unity gain, resulting in a phase shift of greater than 180°. Typically, this limits the minimum ESR to approximately 20 mΩ to 30 mΩ.

For specific ESR requirements, see *Typical Characteristics*.

### 8.2.3 Application Curves



**Figure 34. Load Transient Response vs Time (V$_{OUT}$ = 5 V, C$_L$ = 1 µF)**

Product Folder Links: *LP2950  LP2951*
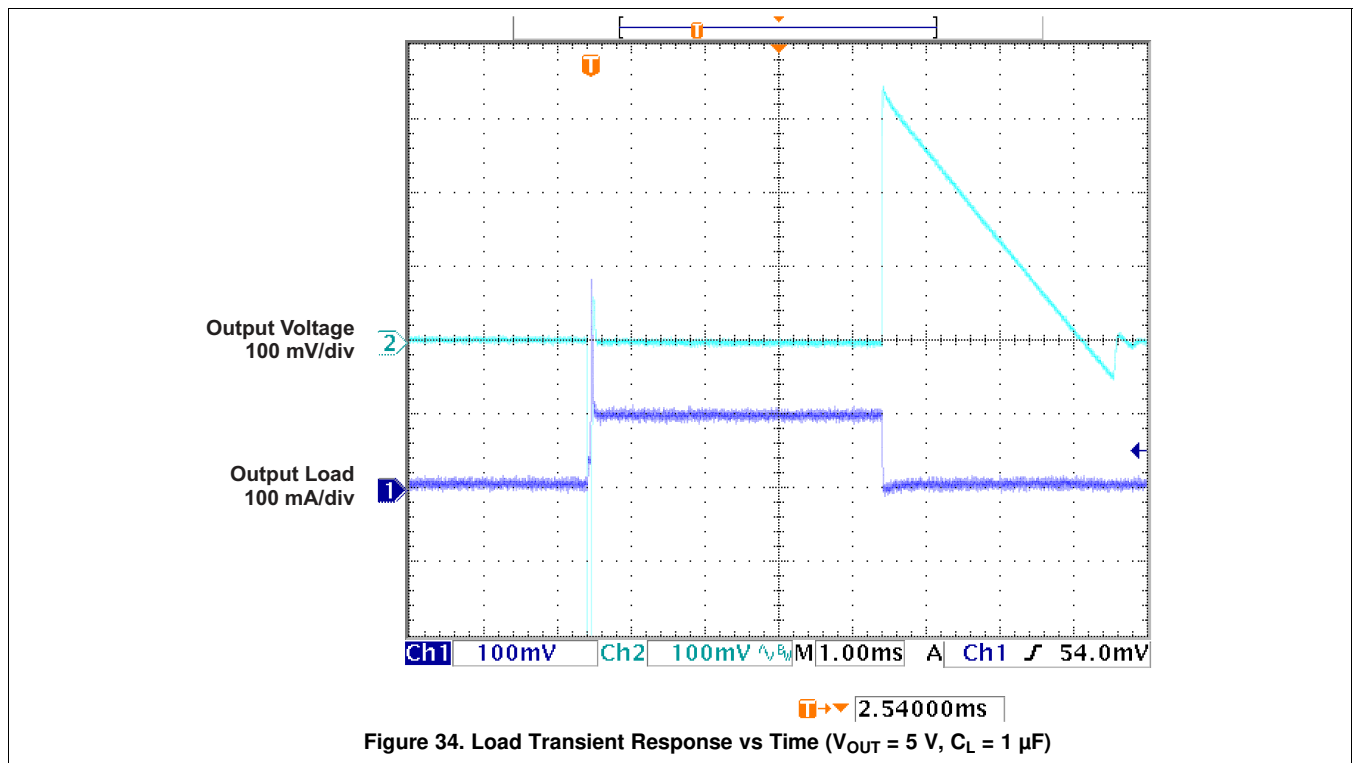
# 9 Power Supply Recommendations

Maximum input voltage should be limited to 30 V for proper operation. Place input and output capacitors as close to the device as possible to take advantage of their high frequency noise filtering properties.

# 10 Layout

## 10.1 Layout Guidelines

- Make sure that traces on the input and outputs of the device are wide enough to handle the desired currents. For this device, the output trace will need to be larger in order to accommodate the larger available current.
- Place input and output capacitors as close to the device as possible to take advantage of their high frequency noise filtering properties.

## 10.2 Layout Example
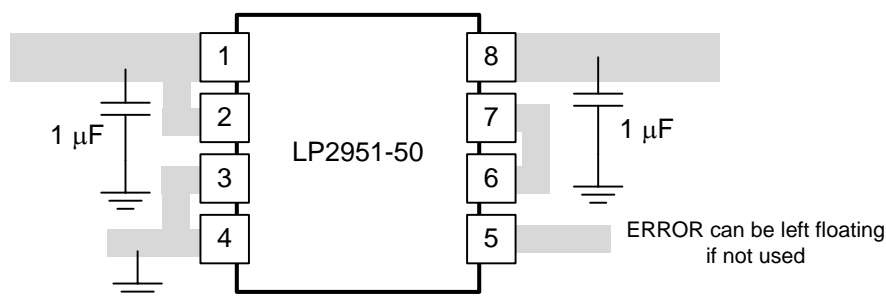


**Figure 35. LP2951 Layout Example (D or P Package)**

# 11 Device and Documentation Support

## 11.1 Trademarks

All trademarks are the property of their respective owners.

## 11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *LP2950  LP2951*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2950-30LP | LIFEBUY | TO-92 | LP | 3 | 1000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 125 | KY5030 | |
| LP2950-30LPR | LIFEBUY | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 125 | KY5030 | |
| LP2950-30LPRE3 | LIFEBUY | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 125 | KY5030 | |
| LP2950-33LPE3 | LIFEBUY | TO-92 | LP | 3 | 1000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 125 | KY5033 | |
| LP2950-33LPRE3 | ACTIVE | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 125 | KY5033 | Samples |
| LP2950-50LPRE3 | ACTIVE | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 125 | KY5050 | Samples |
| LP2951-30D | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5130 | |
| LP2951-30DR | LIFEBUY | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5130 | |
| LP2951-30DRGR | LIFEBUY | SON | DRG | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ZUD | |
| LP2951-33D | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5133 | |
| LP2951-33DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5133 | Samples |
| LP2951-33DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5133 | Samples |
| LP2951-33DRGR | ACTIVE | SON | DRG | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ZUE | Samples |
| LP2951-50D | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5150 | |
| LP2951-50DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5150 | Samples |
| LP2951-50DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | KY5150 | Samples |
| LP2951-50DRGR | ACTIVE | SON | DRG | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ZUF | Samples |
| LP2951D | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LP2951 | |
| LP2951DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LP2951 | Samples |
| LP2951DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LP2951 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

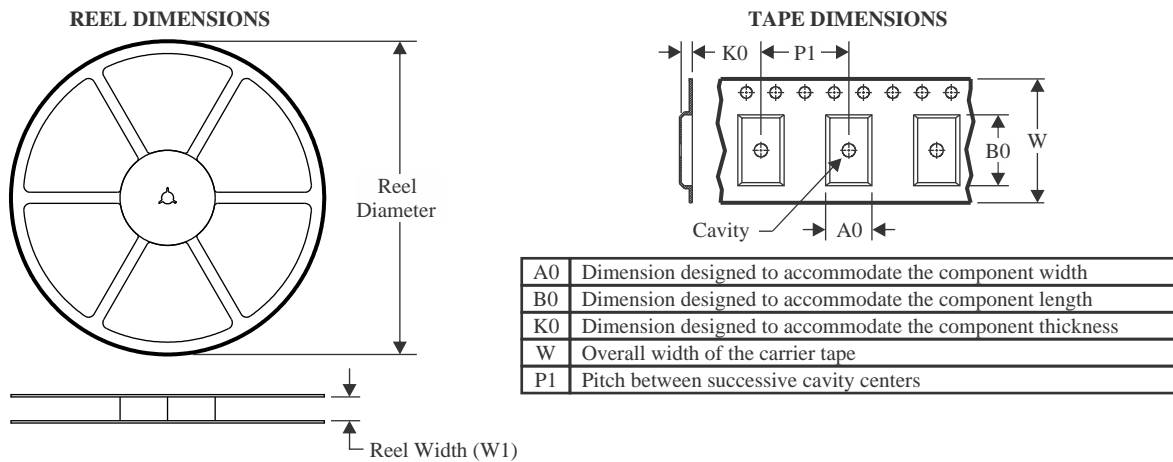In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LP2951 :**

• Automotive : LP2951-Q1

NOTE: Qualified Version Definitions:

•  Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP2951-30DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LP2951-30DRGR | SON | DRG | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LP2951-33DRGR | SON | DRG | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LP2951-50DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LP2951-50DRGR | SON | DRG | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LP2951DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP2951-30DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LP2951-30DRGR | SON | DRG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| LP2951-33DRGR | SON | DRG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| LP2951-50DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LP2951-50DRGR | SON | DRG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| LP2951DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

# PACKAGE MATERIALS INFORMATION

## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LP2951-30D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LP2951-33D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LP2951-50D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LP2951D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
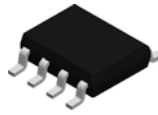
.228-.244  TYP
[5.80-6.19]

PIN 1 ID AREA

.189-.197
[4.81-5.00]
NOTE 3

.150-.157
[3.81-3.98]
NOTE 4

6X .050
[1.27]

2X
.150
[3.81]

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25]Ⓜ C A B

SEATING PLANE

◯ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010  TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C  02/2019
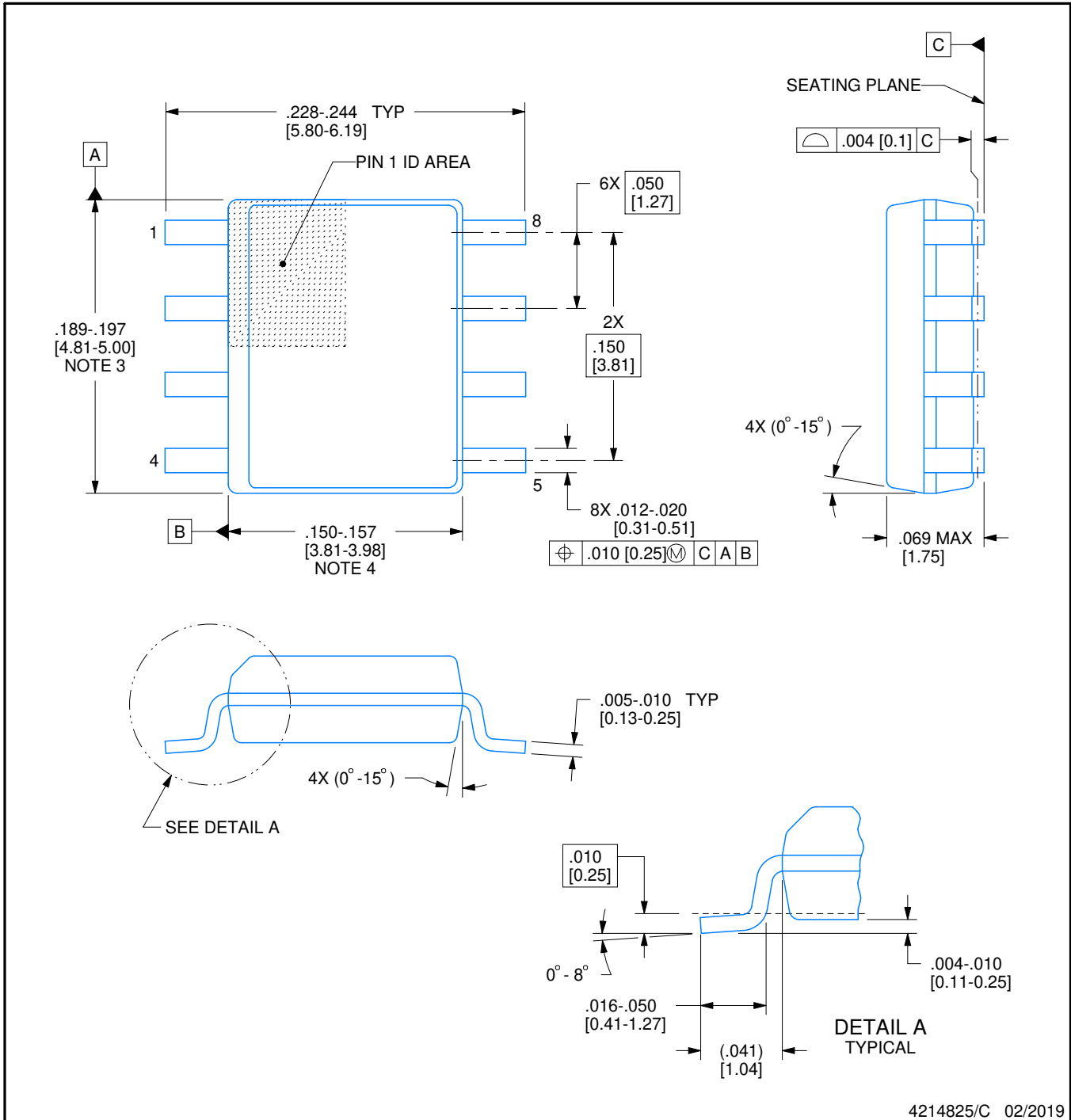
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
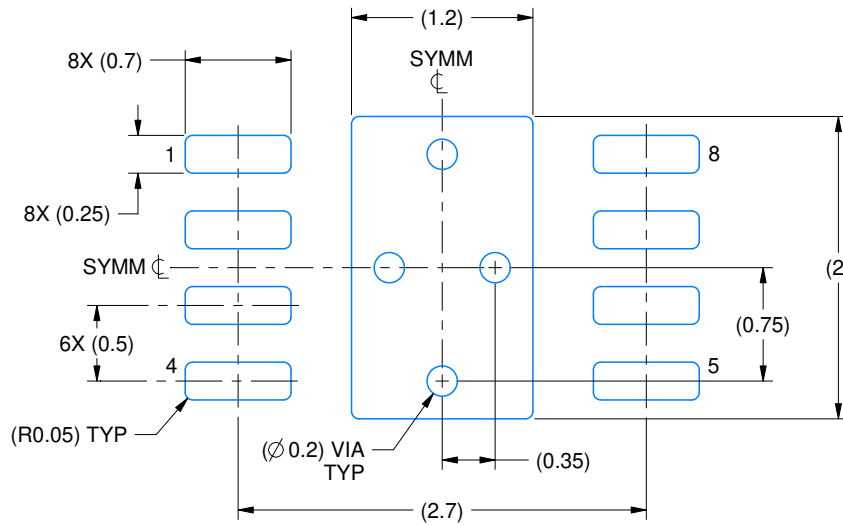5. Reference JEDEC registration MS-012, variation AA.

8X (.061 )
[1.55]

SYMM

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM

(R.002 ) TYP
[0.05]

4

5

6X (.050 )
[1.27]

(.213)
[5.4]

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND
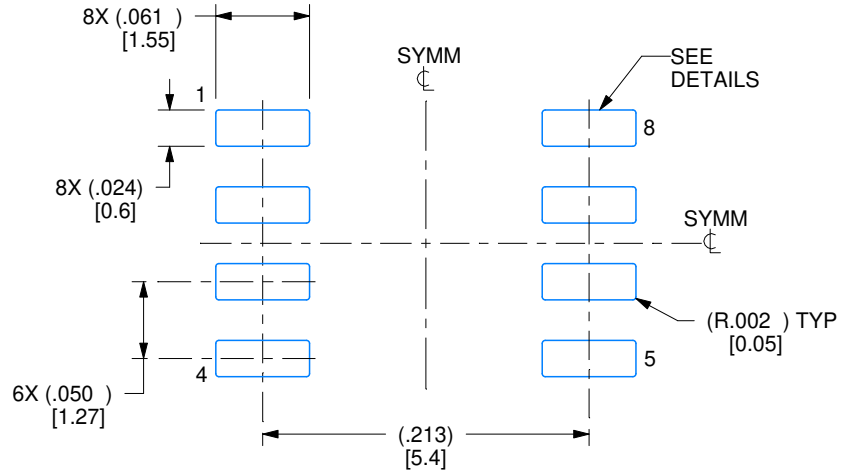
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061  )
[1.55]

SYMM

1

8X (.024)
[0.6]

SYMM

8

(R.002  ) TYP
[0.05]

6X (.050  )
[1.27]

4

5

(.213)
[5.4]

**SOLDER PASTE EXAMPLE**
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S−PWSON−N8)                    PLASTIC SMALL OUTLINE NO−LEAD

3,10
2,90 ← A

B

8        5

3,10
2,90

Pin 1 Index Area
Top and Bottom

1        4

0,20 Nominal
Lead Frame

0,80
0,70

0,08 C

Seating Plane

0,05
0,00
Seating Height

C

0,50

8X 0,60
0,40

1        4

Exposed Thermal Die Pad
D

8        5

8X 0,25 ±0,05

0,10 M C A B
0,05 M C

Bottom View                    4205379/C 12/10

NOTES:   A.  All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         C.  SON (Small Outline No−Lead) package configuration.
         D.  The package thermal pad must be soldered to the board for thermal and mechanical performance.
             See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.  JEDEC MO−229 package registration pending.

**TEXAS INSTRUMENTS**
www.ti.com

A | 3.1 / 2.9 | B

PIN 1 INDEX AREA

3.1 / 2.9

0.8 / 0.7

C

SEATING PLANE

$\boxed{\frown | 0.08 | C}$

0.05 / 0.00

EXPOSED THERMAL PAD

1.2 ± 0.1

(0.2) TYP

4

5

2X [1.5]

2 ± 0.1

1

8

6X [0.5]

PIN 1 ID

8X 0.6 / 0.4

8X 0.3 / 0.2

$\boxed{\oplus | 0.1 ⓂC A B}$
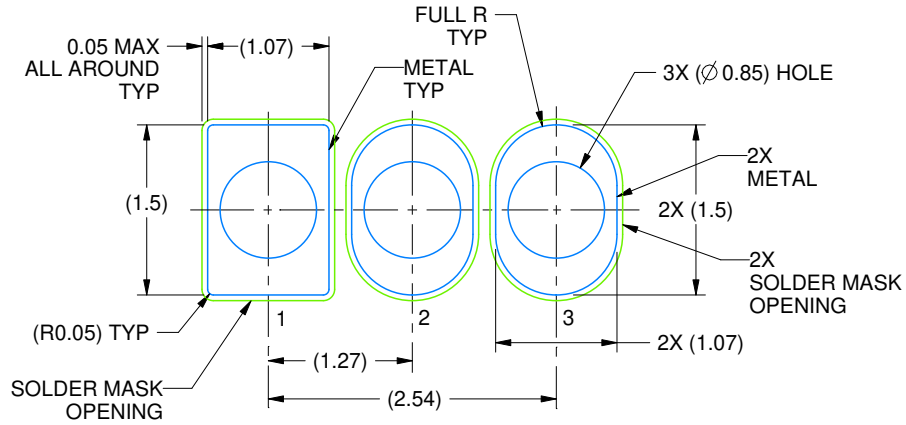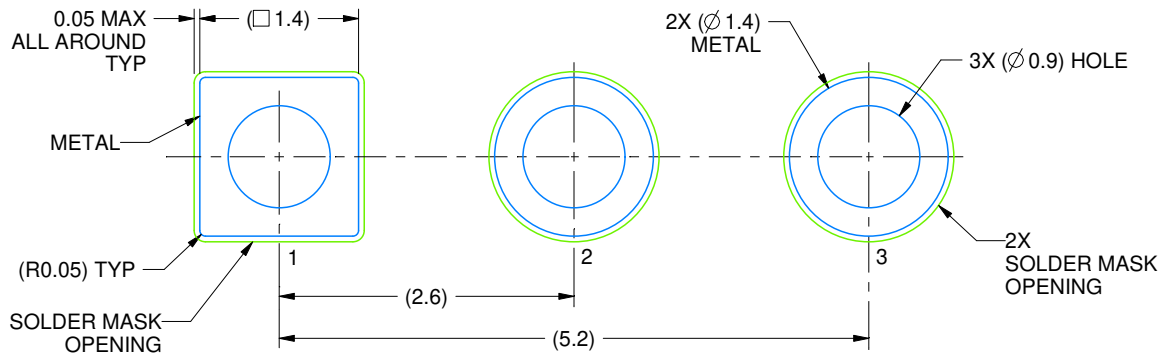$\boxed{0.08 Ⓜ C}$

4218885/A   03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

8X (0.7)

(1.2)

SYMM
℄

1

8

8X (0.25)

SYMM ℄

(2)

6X (0.5)

(0.75)

4

5

(R0.05) TYP

(⌀ 0.2) VIA
TYP

(0.35)

(2.7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218885/A   03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

8X (0.7)

8X (0.25)

1

SYMM

6X (0.5)

4

(R0.05) TYP

SYMM

METAL
TYP

8

(1.79)

5

(1.13)

(2.7)
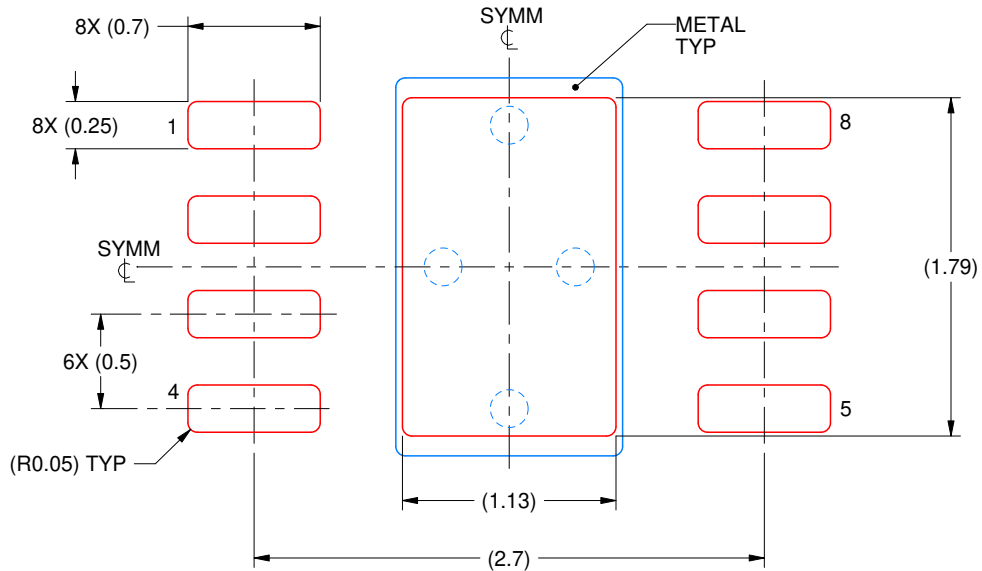
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A   03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040001-2/F

TEXAS
INSTRUMENTS

FORMED LEAD OPTION
OTHER DIMENSIONS IDENTICAL
TO STRAIGHT LEAD OPTION

STRAIGHT LEAD OPTION
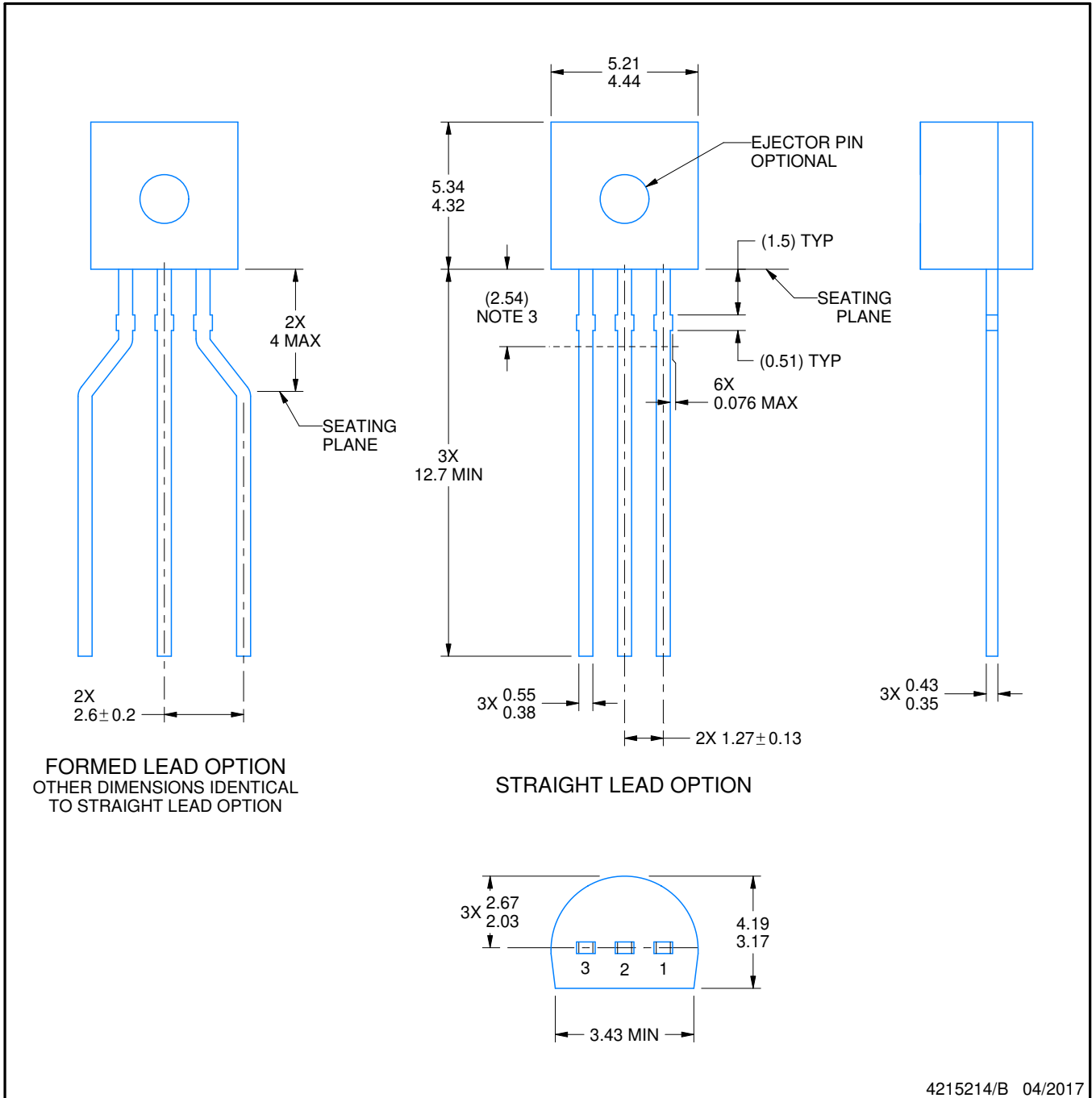
4215214/B   04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

TEXAS
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0.05 MAX
ALL AROUND
TYP

(1.07)

FULL R
TYP

METAL
TYP

3X (⌀ 0.85) HOLE

(1.5)

2X
METAL

2X (1.5)

2X
SOLDER MASK
OPENING

(R0.05) TYP

1

2

3

2X (1.07)

SOLDER MASK
OPENING

(1.27)

(2.54)

### LAND PATTERN EXAMPLE
### STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

0.05 MAX
ALL AROUND
TYP

(□ 1.4)

2X (⌀ 1.4)
METAL

3X (⌀ 0.9) HOLE

METAL

(R0.05) TYP

1

2

3

2X
SOLDER MASK
OPENING

SOLDER MASK
OPENING

(2.6)

(5.2)

### LAND PATTERN EXAMPLE
### FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B   04/2017

13.7
11.7

32
23

(2.5) TYP

0.5 MIN

16.5
15.5

11.0
8.5

9.75
8.50

19.0
17.5

⌀ 3.7-4.3 TYP

2.9
2.4 TYP

6.75
5.95

13.0
12.4
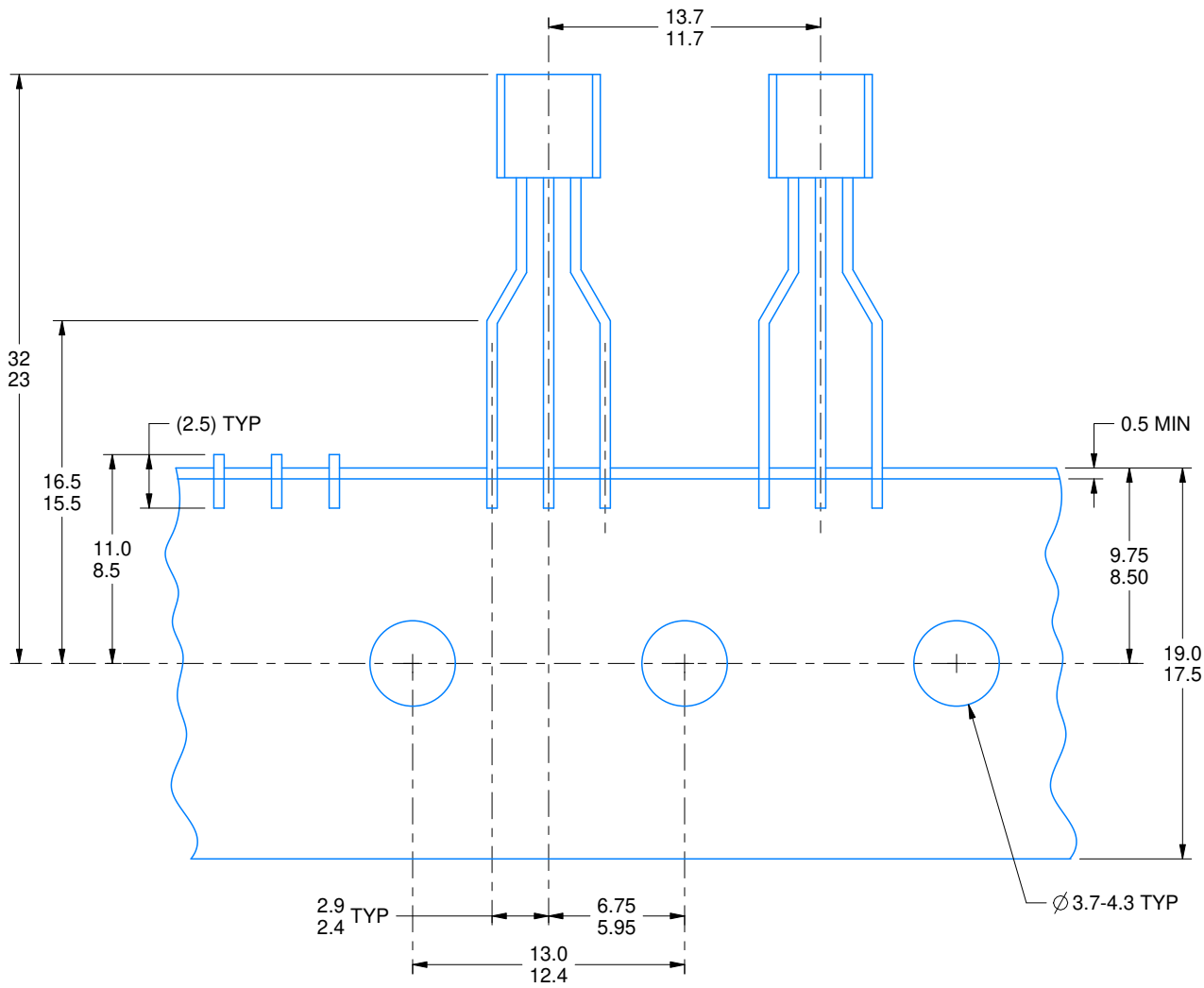
FOR FORMED LEAD OPTION PACKAGE

4215214/B   04/2017

# IMPORTANT NOTICE AND DISCLAIMER