

UC1825B-SP evaluation module (EVM)

The UC1825BEVM-CVAL is the evaluation module (EVM) for the UC1825B-SP and provides a platform to electrically evaluate its features. This user's guide provides details about the EVM, its configuration, schematics, and BOM.

Contents

1	Introduction	3
2	System Design Theory	4
3	Test Setup and Results	8
4	Board Layout.....	23
5	Schematics and Bill of Materials	30

List of Figures

1	Test Setup	8
2	Efficiency vs Output Current	10
3	Load Regulation vs Output Current	11
4	Frequency Response of 22 V _{IN}	12
5	Frequency Response of 48 V _{IN}	13
6	Thermal Characteristics With 22 V _{IN}	13
7	Thermal Characteristics With 48 V _{IN}	14
8	Output Voltage Ripple With 22 V _{IN}	15
9	Output Voltage Ripple With 48 V _{IN}	15
10	Partial Step Down Transient With 22 V _{IN}	16
11	Full Step Down Transient With 22 V _{IN}	16
12	Full Step Up Transient With 22 V _{IN}	17
13	Partial Step Down Transient With 48 V _{IN}	17
14	Full Step Down Transient With 48 V _{IN}	18
15	Full Step Up Transient With 48 V _{IN}	18
16	No Load Startup With 22 V _{IN}	19
17	Full Load Startup With 22 V _{IN}	19
18	No Load Startup With 48 V _{IN}	20
19	Full Load Startup With 48 V _{IN}	20
20	Full Load Shutdown With 22 V _{IN}	21
21	Full Load Shutdown With 48 V _{IN}	21
22	Voltage Stress Across Main Switching MOSFETS Q1 and Q2	22
23	Voltage Stress Across Output Diode	22
24	Top Overlay	23
25	Top Solder	24
26	Top Layer	24
27	Signal Layer 1	25
28	Signal Layer 2	25
29	Bottom Layer.....	26
30	Bottom Solder.....	26

31	Bottom Overlay	27
32	Drill Drawing	28
33	Board Dimensions.....	29
34	UC1825BEVM-CVAL Schematic 01	30
35	UC1825BEVM-CVAL Schematic 02	31

List of Tables

1	Test Parameters	8
2	48 V _{IN} Efficiency Raw Data.....	10
3	22 V _{IN} Efficiency Raw Data.....	10
4	48 V _{IN} Load Regulation Raw Data	11
5	22 V _{IN} Load Regulation Raw Data	11
6	Frequency Response Characteristics of 22 V _{IN}	12
7	Frequency Response Characteristics of 48 V _{IN}	13
8	Notable Thermal Values for 22 V _{IN}	14
9	Notable Thermal Values for 48 V _{IN}	14
10	Bill of Materials	33

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The UC1825BEVM-CVAL uses the UC1825B-SP to supply power using a push-pull topology. The UC1825B-SP supplies both outputs necessary for a push pull topology using its two outputs in a radiation improved package. Both low side MOSFETs are switched using the UC1825B-SP's integrated drivers. If isolation gate drive transformers are used, the UC1825B-SP could be used to supply output signals for both half bridge and full bridge applications. The UC1825B-SP has the soft start function integrated for decreased external components.

1.1 Features

- Pulse-by-pulse current limiting using UC1825B-SP
- Dual output PWM control using UC1825B-SP
- Low start-up current of 1.1 mA
- Dedicated soft-start pin

1.2 Applications

- Space satellite isolated power supplies
- Radiation hardened applications
- Space satellite payloads

1.3 Description

CAUTION



Do not touch! Surface of EVM gets hot. Contact may cause burns.

The UC1825BEVM-CVAL uses the UC1825B-SP as a dual output controller that has integrated drivers for a push-pull topology. The push-pull topology was selected to avoid having to use external high side drivers and take advantage of the low output noise the topology allows for. The UC1825B-SP originally supported voltage mode topologies, but with minimal external components can support current mode topologies as well. The RAMP pin is used for the input current sense and the ILIM pin is used as the current limit pin. External components are needed to ensure slope compensation is implemented. The soft start pin is critical for many designs and is shown in the EVM using the UC1825B-SP's integrated soft start pin.

2 System Design Theory

2.1 Switching Frequency

Choosing a switching frequency has a trade off between efficiency and bandwidth. Higher switching frequencies will have larger bandwidth, but a lower efficiency than lower switching frequencies. A switching frequency of 215 kHz was chosen as a trade off between bandwidth and efficiency. Using equations provided by the data sheet for the UC1825B-SP, R_T and C_T were chosen to be 10 k Ω and 680 pF, respectively. The equation from the data sheet to calculate the switching frequency using these values is shown in Equation 1.

$$f_{osc} \approx \frac{1.46}{R_T \times C_T} \quad (1)$$

$$f_{osc} \approx \frac{1.46}{7.15 \text{ k}\Omega \times 680 \text{ pF}} = 215 \text{ kHz} \quad (2)$$

2.2 Transformer

The transformer of the design consists of two major values, turns ratio and primary side inductance. There is no minimum limit to the turns ratio of the transformer, only a maximum limit. The following equation will give the turns ratio as a function of duty cycle which if the maximum duty cycle of the converter is used will give you a maximum turns ratio. The UC1825B-SP design targeted a duty cycle of 30%. Since this design is for a dual output device the duty cycle must stay below 50%. If both outputs were running above 50% duty cycle they would have to overlap which is not possible for the topology. The equation of the turns ratio of the transformer is Equation 3.

$$N_{psMAX} = \frac{2 \times V_{inMIN} \times D_{lim}}{(V_{out} + V_{ripple})} \quad (3)$$

$$N_{psMAX} = \frac{2 \times 22 \text{ V} \times 0.3}{(5 \text{ V} + 0.7 \text{ V})} = 2.31 \quad (4)$$

Often the turns ratio will slightly change in design due to how the transformer is manufactured. For the UC1825B-SP design a turns ratio of 2.2 was used. Another turns ratio that is important is the turns ratio of the auxiliary winding. The auxiliary winding is found by figuring out what positive voltage is needed from the auxiliary winding. Selecting this voltage lets one pick the turns ratio from the secondary to the auxiliary winding, which in turn allows for the turns ratio from primary to auxiliary to be found. The equation for the turns ratio is Equation 5.

$$N_{as} = \frac{N_{ps} \times V_{aux}}{V_{inMIN}} \quad (5)$$

$$N_{as} = \frac{2.2 \times 15 \text{ V}}{22 \text{ V}} = 1.5 \quad (6)$$

An auxiliary winding of 1.5 was used for the UC1825B-SP design. The primary inductance of the transformer is found from picking an appropriate magnetizing current. The magnetizing current of the transformer is the amount of current drawn through the windings of the transformer when the output is open circuited. Decreasing the magnetizing current will increase the inductance of the transformer, perhaps to unreasonable values. Increasing the magnetizing current will cause efficiency to decrease. It is desirable to keep the magnetizing current low, thus 6% was picked for the design value. The equation for the auxiliary winding turns ratio is Equation 7.

$$L_p = \frac{N_{ps}^2 \times V_{inMIN} \times D_{lim}}{f_{osc} \times \%I_{mag} \times I_{out}} \quad (7)$$

$$L_p = \frac{2.2 \times 48 \times 0.13}{215 \text{ kHz} \times 0.06 \times 10} = 106 \text{ }\mu\text{H} \quad (8)$$

There are quite a few physical limitations when making transformers that will affect the inductance value. For the UC1825B-SP design a primary inductance of 120 μH was used. The output inductor was then picked based on the output inductor ripple current with Equation 9.

$$L_{inductor} = \frac{\left(\frac{V_{inMAX}}{N_{ps}} - V_f - V_{out}\right) \times D_{MIN}}{f_{osc} \times I_{out} \times \%I_{ripple}} \quad (9)$$

$$L_{inductor} = \frac{\left(\frac{48 \text{ V}}{2.2} - 0.7 \text{ V} - 5 \text{ V}\right) \times 0.13}{215 \text{ kHz} \times 10 \text{ A} \times 0.45} = 2.14 \text{ }\mu\text{H} \quad (10)$$

In the final design, a 2.2 μH inductor was used. The peak and primary currents of the transformer are also generally useful for figuring out the physical structure of the transformer, so equations are listed below. Note these equations are only true for continuous conduction mode. Peak currents are higher at the maximum input voltage while the RMS current is highest at the minimum input voltage. These are also idea values and do not take into account efficiency. Final designs needs to be optimized depending on the specific application requirements. See the following equations for this design:

$$I_{\text{secMAX}} = I_{\text{out}} + 0.5 \times \%_{\text{ripple}} \times I_{\text{out}} \quad (11)$$

$$I_{\text{secMAX}} = 10 \text{ A} + 0.5 \times 0.445 \times 10 \text{ A} = 12.23 \text{ A} \quad (12)$$

$$I_{\text{priMAX}} = \frac{I_{\text{secMAX}} + 0.5 \times \%_{\text{mag}} \times I_{\text{out}}}{N_{\text{ps}}} \quad (13)$$

$$I_{\text{priMAX}} = \frac{12.23 \text{ A} - 0.5 \times 0.06 \times 10 \text{ A}}{2.2} = 5.7 \text{ A} \quad (14)$$

$$I_{\text{secMAX}}(V_{\text{inMIN}}) = I_{\text{out}} + \frac{D_{\text{MAX}} \times \left(\frac{V_{\text{inMIN}}}{N_{\text{ps}}} - (V_{\text{out}} + V_f) \right)}{2 \times f_{\text{osc}} \times L_{\text{inductor}}} \quad (15)$$

$$I_{\text{secMAX}}(V_{\text{inMIN}}) = 10 \text{ A} + \frac{0.285 \times \left(\frac{22 \text{ V}}{2.2} - (5 \text{ V} + 0.7 \text{ V}) \right)}{2 \times 215 \text{ kHz} \times 2.2 \mu\text{H}} = 11.3 \text{ A} \quad (16)$$

$$I_{\text{priMAX}}(V_{\text{inMIN}}) = \frac{I_{\text{secMAX}}(V_{\text{inMIN}}) + 0.5 \times \%_{\text{mag}} \times I_{\text{out}}}{N_{\text{ps}}} \quad (17)$$

$$I_{\text{priMAX}}(V_{\text{inMIN}}) = \frac{11.3 \text{ A} - 0.5 \times 0.06 \times 10}{2.2} = 5.27 \text{ A} \quad (18)$$

$$I_{\text{secMIN}}(V_{\text{inMIN}}) = I_{\text{out}} - \frac{D_{\text{MAX}} \times \left(\frac{V_{\text{inMIN}}}{N_{\text{ps}}} - (V_{\text{out}} + V_f) \right)}{2 \times f_{\text{osc}} \times L_{\text{inductor}}} \quad (19)$$

$$I_{\text{secMIN}}(V_{\text{inMIN}}) = 10 \text{ A} - \frac{0.285 \times \left(\frac{22 \text{ V}}{2.2} - (5 \text{ V} + 0.7 \text{ V}) \right)}{2 \times 215 \text{ kHz} \times 2.2 \mu\text{H}} = 8.7 \text{ A} \quad (20)$$

$$I_{\text{priMIN}}(V_{\text{inMIN}}) = \frac{I_{\text{secMIN}}(V_{\text{inMIN}}) - 0.5 \times \%_{\text{mag}} \times I_{\text{out}}}{N_{\text{ps}}} \quad (21)$$

$$I_{\text{priMIN}}(V_{\text{inMIN}}) = \frac{8.7 \text{ A} - 0.5 \times 0.06 \times 10}{2.2} = 3.82 \text{ A} \quad (22)$$

$$t_{\text{onMAX}} = \frac{(V_{\text{out}} + V_f) \times N_{\text{ps}}}{2 \times f_{\text{osc}} \times V_{\text{inMIN}}} \quad (23)$$

$$t_{\text{onMAX}} = \frac{(5 \text{ V} + 0.7 \text{ V}) \times 2.2}{2 \times 215 \text{ kHz} \times 22 \text{ V}} = 1.33 \mu\text{s} \quad (24)$$

$$m_{\text{pri}} = \frac{I_{\text{priMAX}}(V_{\text{inMIN}}) - I_{\text{priMIN}}(V_{\text{inMIN}})}{t_{\text{onMAX}}} \quad (25)$$

$$m_{\text{pri}} = \frac{5.27 - 3.82}{1.33 \mu\text{s}} = 1090226 \text{ A/s} \quad (26)$$

$$I_{\text{priRMS}} = \sqrt{D_{\text{MIN}} \times \left(\frac{(m_{\text{pri}} \times t_{\text{onMAX}})^2}{3} + \frac{m_{\text{pri}}}{2} \times I_{\text{priMIN}}(V_{\text{inMIN}}) \times t_{\text{onMAX}} + I_{\text{priMIN}}(V_{\text{inMIN}})^2 \right)} \quad (27)$$

$$I_{\text{priRMS}} = \sqrt{0.285 \times \left(\frac{(1090226 \text{ A/s} \times 1.33 \mu\text{s})^2}{3} + \frac{1090226 \text{ A/s}}{2} \times 3.82 \text{ A} \times 1.33 \mu\text{s} + (3.82 \text{ A})^2 \right)} = 2.27 \text{ A} \quad (28)$$

2.3 RCD and Diode Clamp

For the UC1825BEVM-CVAL a resistor and capacitor in combination with a diode was used to clamp the voltage of the switch node. The resistor and capacitor is generally a value that is found through testing, but starting values can be obtained. To figure out the resistor and capacitor needed for the RCD clamp, one must first decide how much the node is allowed to overshoot. The equation for finding the voltage of the clamp is Equation 29.

$$V_{\text{clamp}} = K_{\text{clamp}} \times N_{\text{ps}} \times (V_{\text{out}} + V_{\text{Diode}}) \quad (29)$$

Note that K_{clamp} is recommended to be 1.5 as this will allow for only around 50% overshoot. Knowing the parasitic inductance of the transformer and how much the RCD clamp voltage is allowed to change over the switching cycle, can allow one to figuring out starting values for the resistor and capacitor using Equation 30 and Equation 31.

$$R_{\text{clamp}} = \frac{V_{\text{clamp}}^2}{\frac{1}{2} \times L_{\text{leakage}} \times I_{\text{priRMS}}^2 \times \left(\frac{V_{\text{clamp}}}{V_{\text{clamp}} - N_{\text{ps}} \times (V_{\text{out}} + V_{\text{Diode}})} \right) \times f_{\text{osc}}} \quad (30)$$

$$C_{\text{clamp}} = \frac{V_{\text{clamp}}}{\Delta V_{\text{clamp}} \times V_{\text{clamp}} \times R_{\text{clamp}} \times f_{\text{osc}}} \quad (31)$$

A starting value of 10% is generally used for ΔV_{clamp} .

2.4 Output Diode

The voltage stress by the converter on the diode can be found with [Equation 32](#).

$$V_{\text{DiodeStress}} = V_{\text{out}} + \frac{V_{\text{inMAX}}}{N_{\text{ps}}} \quad (32)$$

$$V_{\text{DiodeStress}} = 5 \text{ V} + \frac{48 \text{ V}}{2.2} = 26.8 \text{ V} \quad (33)$$

Note that any diode picked should have a voltage rating of well above this value as it does not include parasitic spikes in the equation. The UC1825-SP diode was picked to have a voltage rating of 60 V.

2.5 Main Switching MOSFETs

Each switch applies the input voltage across the transformer and the voltage is then divided down by the turns ratio and applied to the secondary side. Since the magnitude of the voltage across the windings is the input voltage, when the switch is off the primary switching MOSFETs will see twice the input voltage as the voltage stress plus some amount of ringing. This means the MOSFETs chosen for a push-pull topology should have a voltage rating of about 2.5 to 3 times higher than the input voltage.

2.6 Output Filter and Capacitance

For most designs, a ripple voltage is picked and the output capacitance is figured out from that value. The output capacitance value needs to be able to withstand a full output current step as well as keep the voltage ripple of the output low. The UC1825B-SP design started similar to that using the equations for voltage ripple and load step with [Equation 34](#) and [Equation 36](#).

$$C_{\text{out}} > \frac{I_{\text{out}} \times 2 \times D_{\text{MAX}}}{V_{\text{ripple}} \times f_{\text{sw}}} \quad (34)$$

$$C_{\text{out}} > \frac{10 \text{ A} \times 2 \times 0.3}{50 \text{ mV} \times 200 \text{ kHz}} = 600 \text{ } \mu\text{F} \quad (35)$$

$$C_{\text{out}} > \frac{1}{2\pi \times \Delta V_{\text{out}} \times f_{\text{sw}}} \quad (36)$$

$$C_{\text{out}} > \frac{10 \text{ A}}{2\pi \times 0.3 \text{ V} \times 5 \text{ kHz}} = 1060 \text{ } \mu\text{F} \quad (37)$$

A value of around 1145 μF was chosen to keep output voltage ripple low. Note that the output voltage ripple in the design was further decreased by adding an output filter and by adding an inductor after a small portion of the output capacitance. This was done in order to keep output voltage ripple as low as possible. Six ceramic capacitors were picked to be placed before the output filter and then the large tantalum capacitors with some small ceramics were added to be part of the output filter. The initial ceramics will help with the initial current ripple, but have a very large output voltage ripple. This voltage ripple will be attenuated by the inductor and capacitor combination placed between the ceramic capacitors and the output. The equations below allow for finding the amount of attenuation that will come from a specific output filter inductance. An inductance of 500 nH was chosen to attenuate the output voltage ripple. The value was chosen to put the resonant frequency pole well before the switching frequency of the design as well as the zero from the ESR of the bulk capacitors to provide more attenuation.

$$F_{\text{resonant}} = \frac{1}{2\pi \times \sqrt{L_{\text{filter}} \times C_{\text{outBulk}}}} \quad (38)$$

$$F_{\text{resonant}} = \frac{1}{2\pi \times \sqrt{0.5 \text{ nH} \times 1127 \text{ } \mu\text{F}}} = 6.7 \text{ kHz} \quad (39)$$

$$F_{\text{Zero}} = \frac{1}{2\pi \times C_{\text{outBulk}} \times \text{ESR}_{\text{outBulk}}} \quad (40)$$

$$F_{\text{Zero}} = \frac{1}{2\pi \times 1127 \text{ } \mu\text{F} \times 0.009 \text{ } \Omega} = 15.69 \text{ kHz} \quad (41)$$

$$\text{Attenuation}_{f_{\text{sw}}} = 40 \times \log_{10}\left(\frac{f_{\text{sw}}}{f_{\text{resonant}}}\right) - 20 \times \log_{10}\left(\frac{f_{\text{sw}}}{f_{\text{zero}}}\right) \quad (42)$$

$$\text{Attenuation}_{f_{\text{sw}}} = 40 \times \log_{10}\left(\frac{200 \text{ kHz}}{6.7 \text{ kHz}}\right) - 20 \times \log_{10}\left(\frac{200 \text{ kHz}}{15.69 \text{ kHz}}\right) = 36.88 \text{ dB} \quad (43)$$

Sometimes the output filter can cause peaking at high frequencies, this can be damped by adding a resistor in parallel with the inductor which will decrease efficiency. For the UC1825B-SP design 0.5 Ω was used as a very conservative value. The resistance needed to damp the peaking can be calculated using the following equations:

$$\omega_o = \sqrt{\frac{2(C_{oCerm} \parallel C_{oEutk})}{L_{Filter} \times C_{oCerm} \times C_{oEutk}}} \quad (44)$$

$$\omega_o = \sqrt{\frac{2(19 \mu F \parallel 1127 \mu F)}{500 \text{ nH} \times 19 \mu F \times 1127 \mu F}} = 463 \text{ kHz} \quad (45)$$

$$R_{Filter} = \frac{R_o \times L_{Filter} \times (C_{oCerm} \parallel C_{oEutk}) - \frac{L_{Filter}}{\omega_o}}{R_o \times (C_{oCerm} \parallel C_{oEutk}) - L_{Filter} \times C_{oCerm}} \quad (46)$$

$$R_{Filter} = \frac{0.5 \times 500 \text{ nH} \times (19 \mu F \parallel 1127 \mu F) - \frac{500 \text{ nH}}{463 \text{ kHz}}}{\frac{0.5 \times (19 \mu F \parallel 1127 \mu F)}{463 \text{ kHz}} - 500 \text{ nH} \times 19 \mu F} = 0.232 \Omega \quad (47)$$

2.7 Compensation

Type IIB compensation was picked for the topology, adding a pole and a zero to the frequency response. The location of where the pole and zero should be placed will depend on the desired crossover frequency and the ESR zero of the output capacitors. The zero in compensation should be placed at least a decade before the crossover frequency for the maximum phase boost. Note that compensation values were picked with a crossover frequency of 5 kHz in mind for this design. The pole from the compensation should be placed at the zero created by the ESR of the output capacitor.

$$f_{zESR} = \frac{1}{2\pi \times C_{out} \times ESR} = \frac{1}{2\pi \times 1146 \mu F \times 0.009 \Omega} = 15.43 \text{ kHz} \quad (48)$$

$$f_{pCOMP} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} = \frac{1}{2\pi \times 4.75 \text{ k}\Omega \times 2200 \text{ pF}} = 15.23 \text{ kHz} \quad (49)$$

$$f_{zCOMP} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = \frac{1}{2\pi \times 4.75 \text{ k}\Omega \times 0.12 \mu F} = 279 \text{ Hz} \quad (50)$$

The zero from compensation was placed well before the 500-Hz mark which is appropriate. The pole from compensation was optimized while the circuit was tested and thus it was found that placing the pole a little bit earlier smoothed out the frequency response.

2.8 Sense Resistor

The sense resistor is used to sense the ripple current from the transformer as well as shutdown the switching cycle if the peak current of the converter is over the current limit set. The voltage threshold of the CS pin is around 1 V and the shutdown current should be above the max current you expect. What the max current limit will be will depend on the specific design. The equation used to find the max current limit is [Equation 51](#).

$$R_{CS} = \frac{V_{CS_Threshold}}{I_{limit}} \quad (51)$$

$$R_{CS} = \frac{1 \text{ V}}{6.66 \text{ A}} = 0.15 \Omega \quad (52)$$

3 Test Setup and Results

3.1 Test Setup

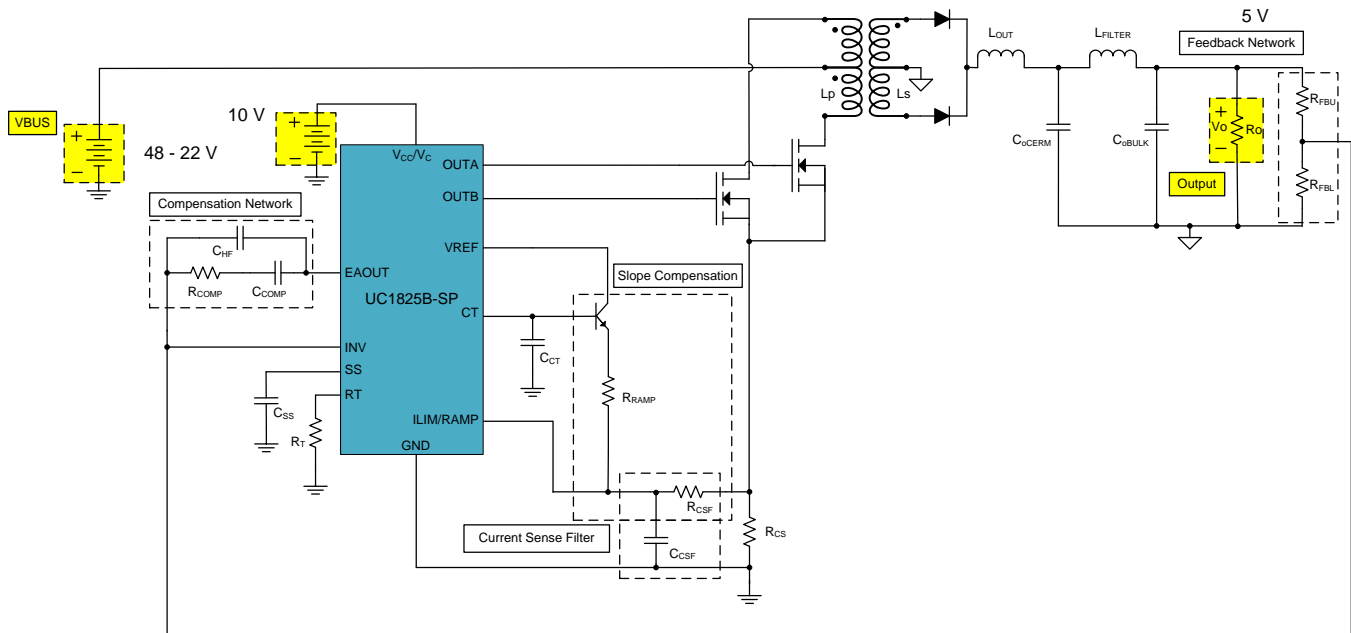


Figure 1. Test Setup

WARNING

The UC1825BEVM-CVAL (EVM) is intended only for the developer's evaluation of the UC1825B-SP Current Mode PWM Controller device.

This EVM is not designed nor intended to simulate actual end product or subassembly applications involving high voltages often found in isolated topologies exceeding the specified electrical circuit ratings for UC1825BEVM-CVAL.

To minimize potential risk of personal injury, death, or damage to the EVM itself, application of any differential voltages applied between the electrical grounds of each input and output side of the evaluation module is strictly prohibited.

All tests were done with 10 V_{IN} on the UC1825B-SP unless otherwise specified.

Table 1. Test Parameters

PARAMETER	SPECIFICATIONS
Input Power Supply	22 to 48 VDC
Output Voltage	5 VDC
Output Current	0 to 10 A
Output Current Pre-load	0.5 mA
Operating Temperature	25°C
Switching Frequency of UC1825B-SP	215 kHz
Peak Input Current Limit	7 A

Table 1. Test Parameters (continued)

PARAMETER	SPECIFICATIONS
Bandwidth	~5 kHz
Phase Margin	~80°

3.2 Test Results

3.2.1 Efficiency

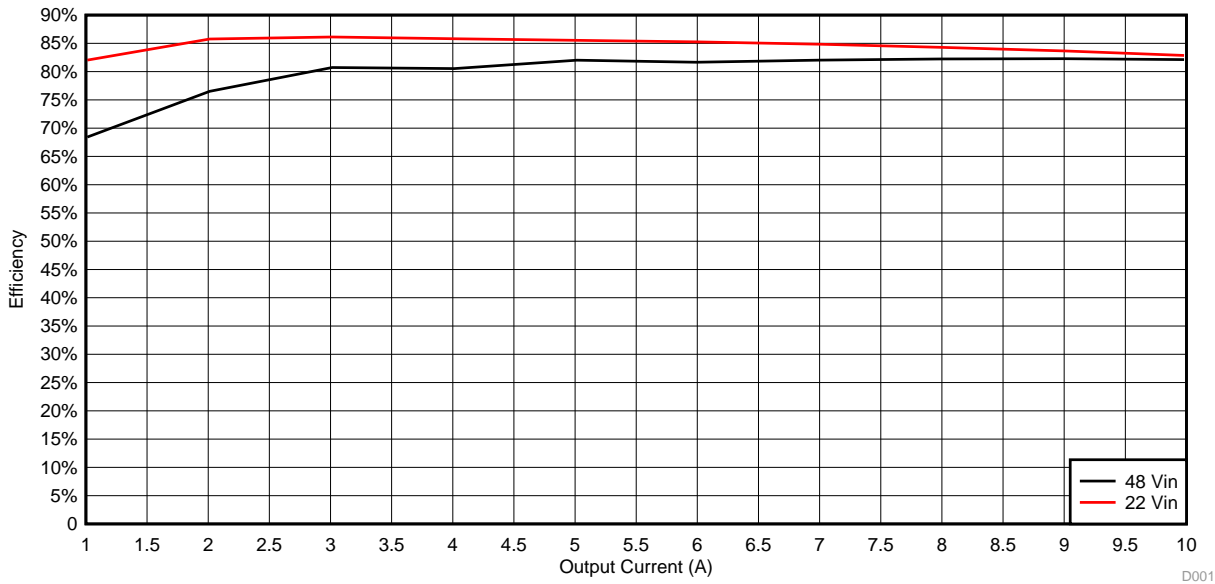


Figure 2. Efficiency vs Output Current

Please note that the test for Figure 2 was done such that the effect of the UC1825B-SP is not included in the efficiency measurement. The efficiency numbers are for the push-pull converter without the UC1825B-SP included.

Table 2. 48 V_{IN} Efficiency Raw Data

V _{IN}	I _{IN}	V _{OUT}	I _{OUT}	P _{IN}	P _{OUT}	Efficiency
48.5	1.24	4.93	9.98	59.9	49.2	0.821
48.6	1.11	4.93	8.99	53.9	44.3	0.823
48.6	0.99	4.93	7.99	47.9	39.4	0.822
48.6	0.87	4.93	7.01	42.2	34.6	0.820
48.6	0.75	4.93	5.99	36.2	29.6	0.817
48.6	0.62	4.93	5.02	30.2	24.7	0.820
48.6	0.51	4.93	4.01	24.6	19.8	0.805
48.6	0.38	4.93	3.01	18.4	14.9	0.807
48.6	0.27	4.93	2.01	13.0	9.9	0.765
48.6	0.15	4.94	1.01	7.3	5.0	0.684
48.6	0.00	4.94	0.00	0.0	0.0	0.000

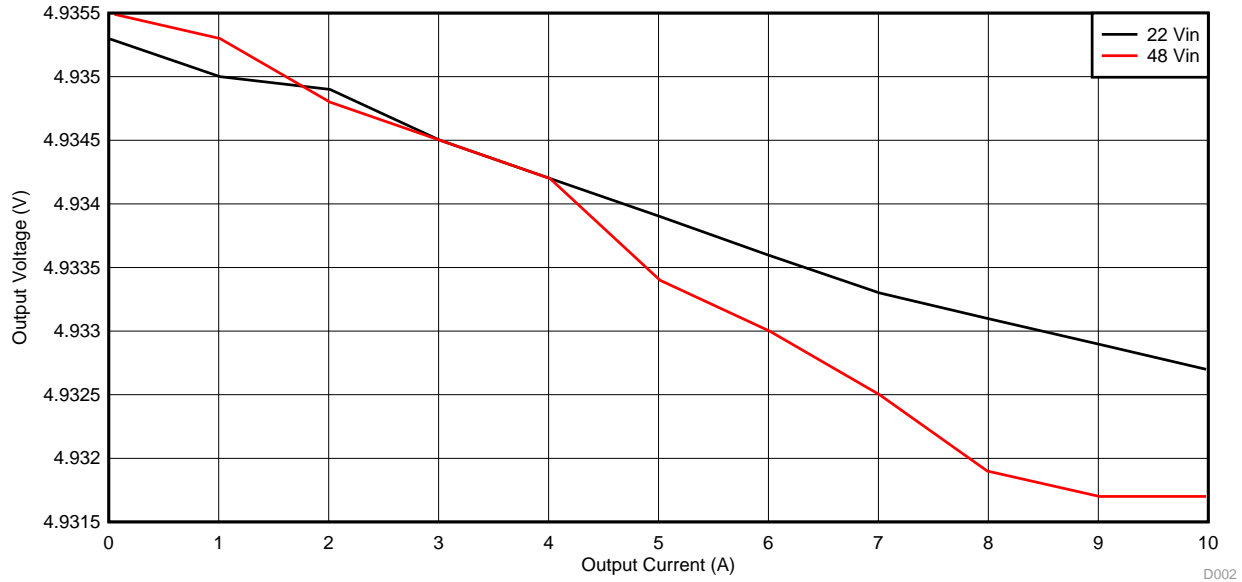
Table 3. 22 V_{IN} Efficiency Raw Data

V _{IN}	I _{IN}	V _{OUT}	I _{OUT}	P _{IN}	P _{OUT}	Efficiency
22.12	2.69	4.93	9.98	59.4	49.2	0.83
22.14	2.40	4.93	9.01	53.1	44.4	0.84
22.16	2.11	4.93	7.99	46.7	39.4	0.84
22.17	1.84	4.93	7.01	40.8	34.6	0.85
22.19	1.57	4.93	6.01	34.8	29.6	0.85
22.21	1.30	4.93	5.01	28.9	24.7	0.86
22.23	1.04	4.93	4.01	23.1	19.8	0.86

Table 3. 22 V_{IN} Efficiency Raw Data (continued)

V _{IN}	I _{IN}	V _{OUT}	I _{OUT}	P _{IN}	P _{OUT}	Efficiency
22.25	0.78	4.93	3.01	17.3	14.9	0.86
22.26	0.52	4.93	2.01	11.6	9.9	0.86
22.28	0.27	4.94	1.01	6.1	5.0	0.82
22.30	0.00	4.94	0.00	0.0	0.0	0.00

3.2.2 Load Regulation


Figure 3. Load Regulation vs Output Current

The test for [Figure 3](#) was done at different input voltages shown by the separate curves and taken over output current.

Table 4. 48 V_{IN} Load Regulation Raw Data

V _{OUT}	I _{OUT}
4.9327	9.98
4.9329	8.99
4.9331	7.99
4.9333	7.01
4.9336	5.99
4.9339	5.02
4.9342	4.01
4.9345	3.01
4.9349	2.01
4.935	1.01
4.9353	0.00

Table 5. 22 V_{IN} Load Regulation Raw Data

V _{OUT}	I _{OUT}
4.9317	9.98
4.9317	9.01

Table 5. 22 V_{IN} Load Regulation Raw Data (continued)

V _{OUT}	I _{OUT}
4.9319	7.99
4.9325	7.01
4.933	6.01
4.9334	5.014
4.9342	4.013
4.9345	3.013
4.9348	2.012
4.9353	1.011
4.9355	0

3.2.3 Frequency Response

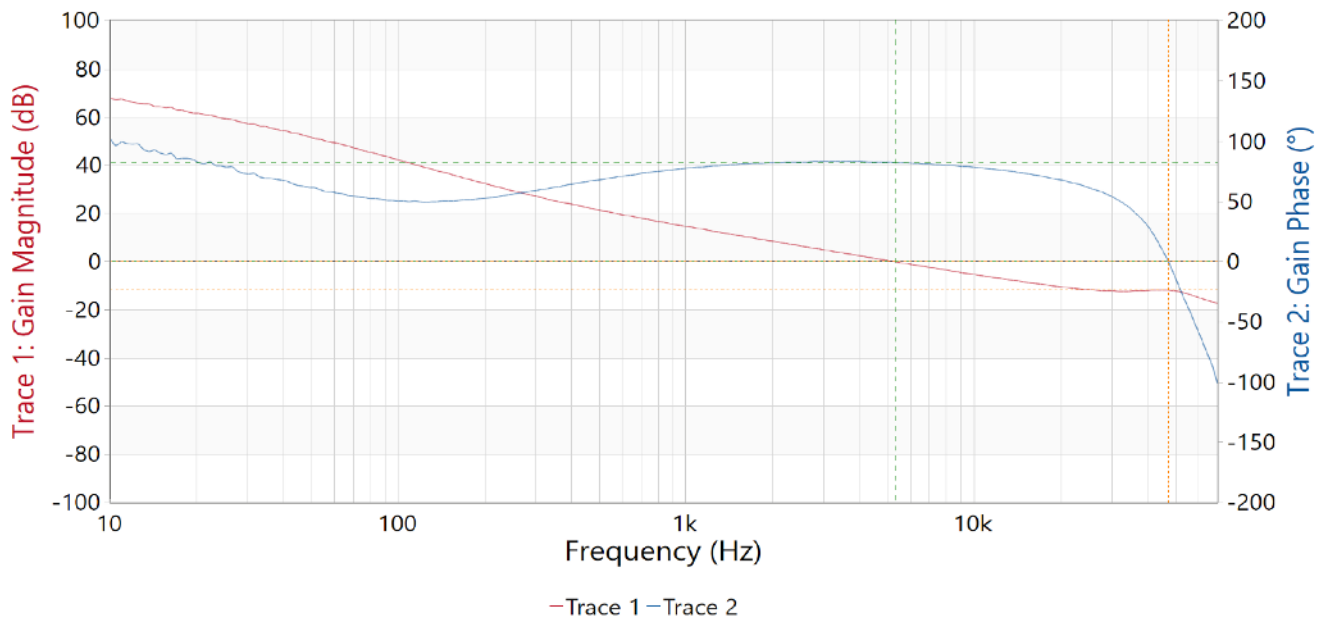


Figure 4. Frequency Response of 22 V_{IN}

Frequency response in [Figure 4](#) was measured with 22 V on the input and with an output current of 10 A.

Table 6. Frequency Response Characteristics of 22 V_{IN}

PARAMETER	VALUE
Crossover Frequency	5.35 kHz
Phase Margin	82.44°
Phase Crossover	47.23 kHz
Gain Margin	-11.82 dB

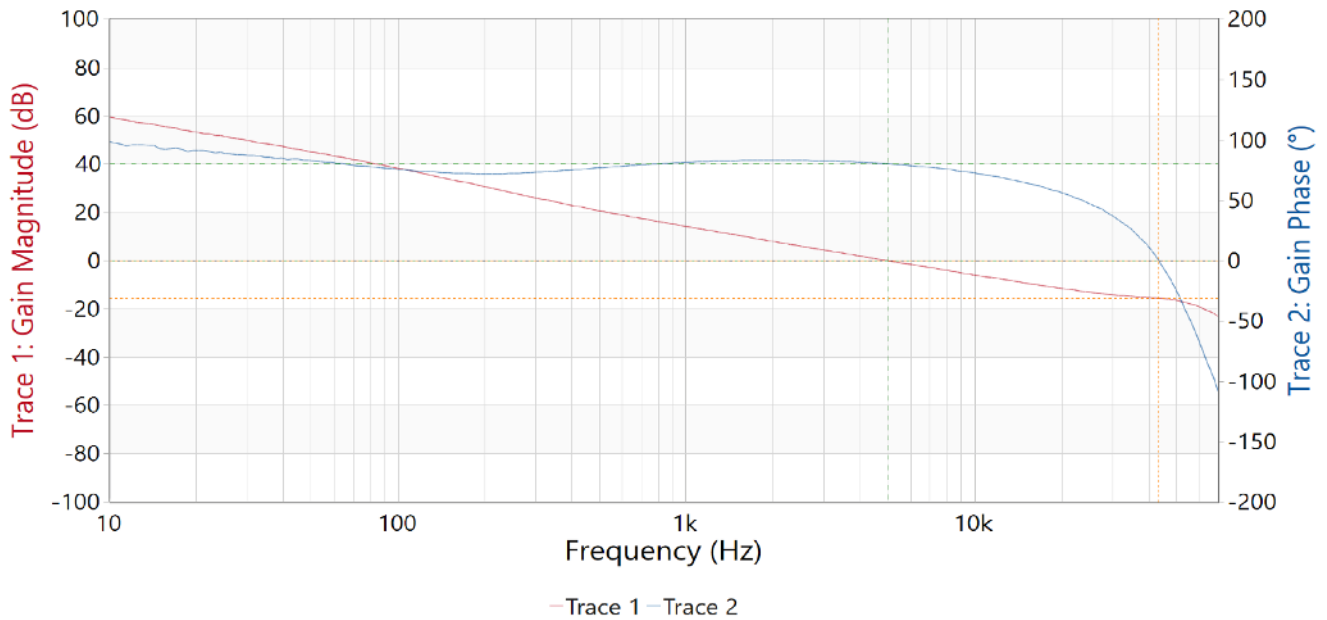


Figure 5. Frequency Response of 48 V_{IN}

Frequency response in Figure 5 was measured with 48 V on the input and with an output current of 10 A.

Table 7. Frequency Response Characteristics of 48 V_{IN}

PARAMETER	VALUE
Crossover Frequency	5.06 kHz
Phase Margin	80.33°
Phase Crossover	43.53 kHz
Gain Margin	-15.60 dB

3.2.4 Thermal Characteristics

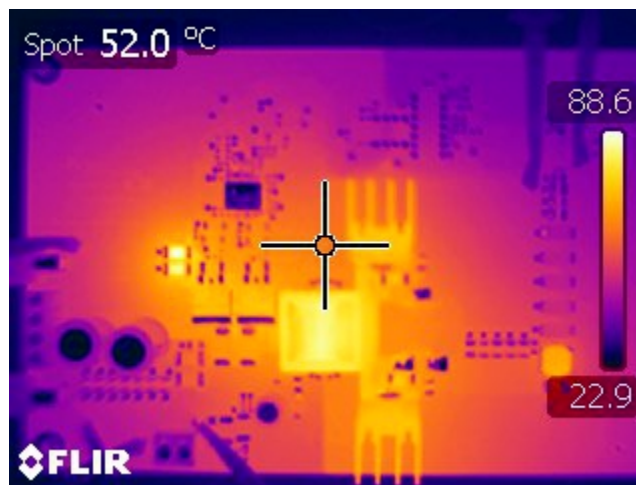


Figure 6. Thermal Characteristics With 22 V_{IN}

Table 8. Notable Thermal Values for 22 V_{IN}

AREA	TEMPERATURE
Output Diode (D10 and D11)	62.0°C
Resistor Snubber (R23 and R26)	59.7°C
Output Filter Inductor (L1)	57.8°C
Main Switching MOSFET (Q1 and Q2)	61.7°C
Sense Resistors (R16 and R17)	82.0°C
Transformer (T1)	80.0°C

Thermal picture in [Figure 6](#) was done with 22 V on the input and 10-A output for 20 minutes.

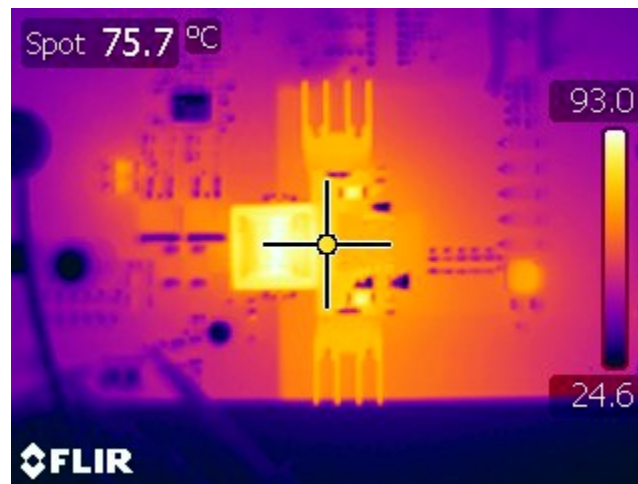


Figure 7. Thermal Characteristics With 48 V_{IN}

Thermal picture in [Figure 7](#) was done with 48 V on the input and 10-A output for 20 minutes.

Table 9. Notable Thermal Values for 48 V_{IN}

AREA	TEMPERATURE
Output Diode (D10 and D11)	87.9°C
Resistor Snubber (R23 and R26)	83.1°C
Output Filter Inductor (L1)	61.4°C
Main Switching MOSFET (Q1 and Q2)	56.5°C
Sense Resistors (R16 and R17)	56.7°C
Transformer (T1)	91.9°C

3.2.5 Output Voltage Ripple

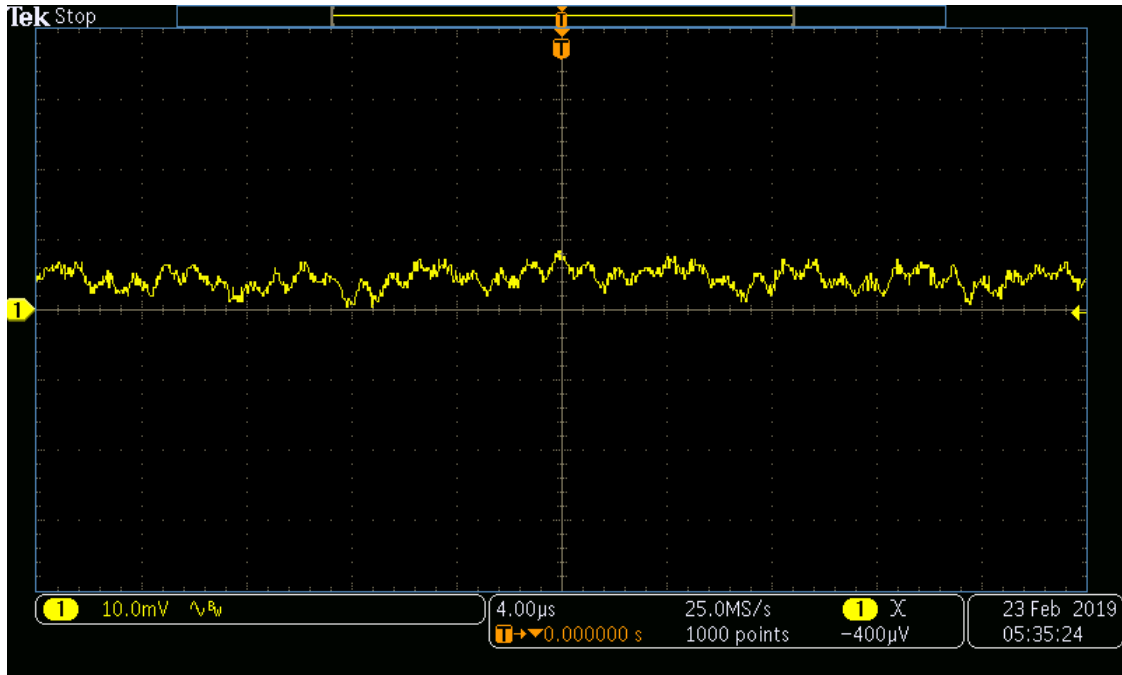


Figure 8. Output Voltage Ripple With 22 V_{IN}

Output voltage ripple test in Figure 8 was done with 22-V input and 10 A of output current.

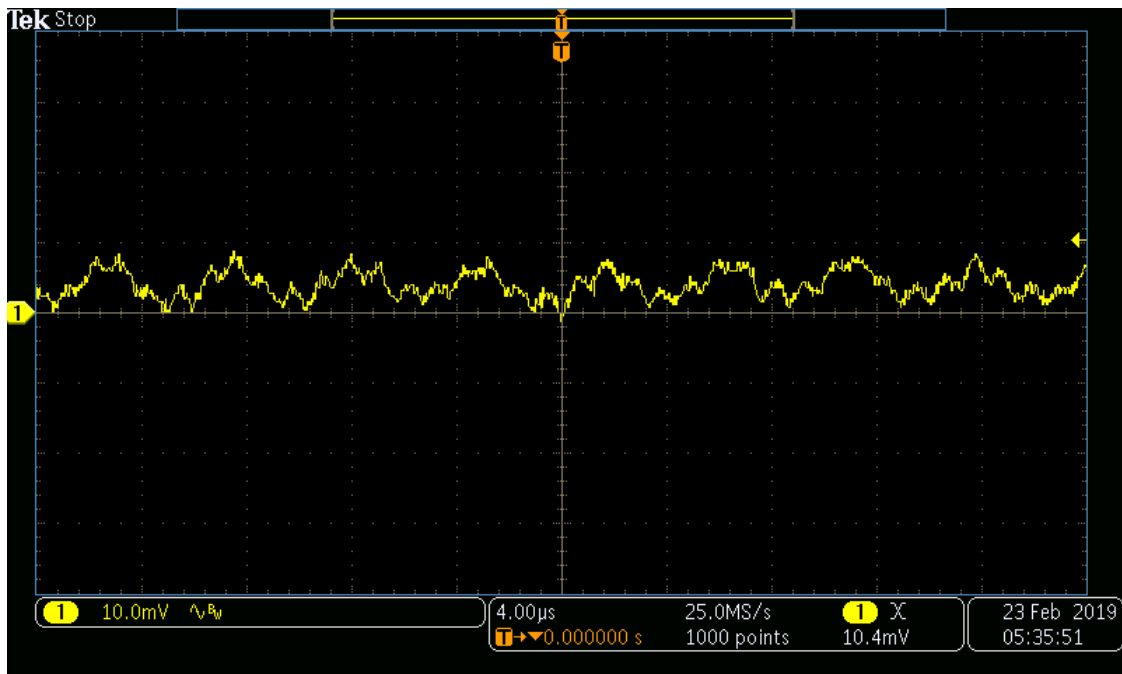


Figure 9. Output Voltage Ripple With 48 V_{IN}

Output voltage ripple test in Figure 9 was done with 48-V input and 10 A of output current.

3.2.6 Transients

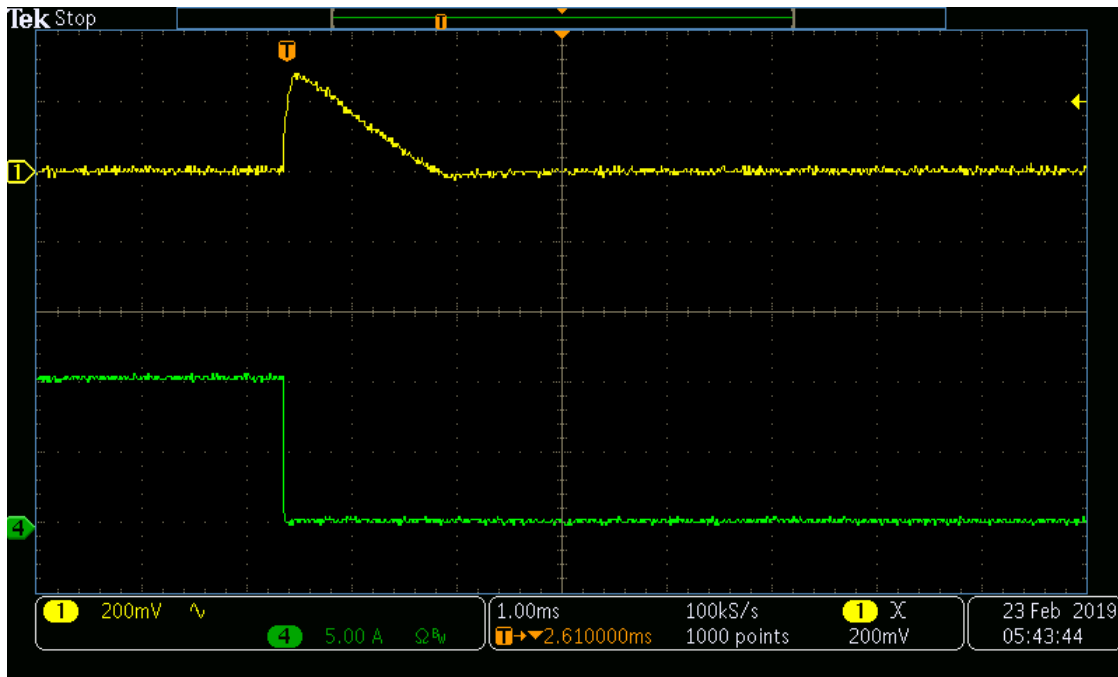


Figure 10. Partial Step Down Transient With 22 V_{IN}

Partial step down transient in Figure 10 was done with 22-V input and current was stepped from 10 A to 0.16 A.

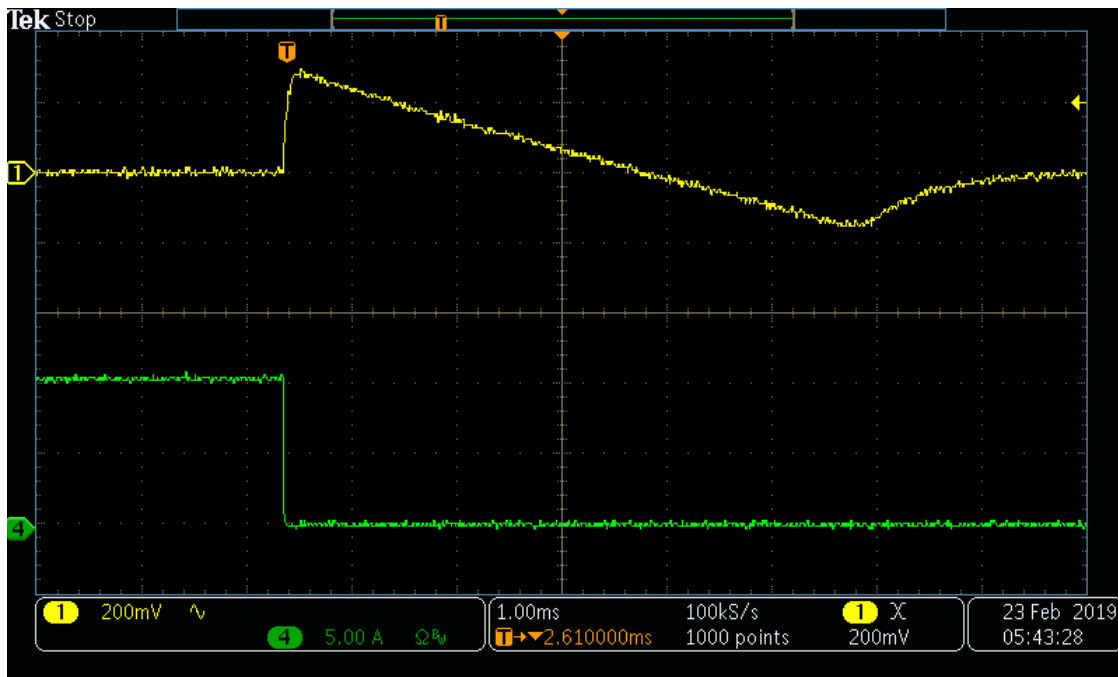


Figure 11. Full Step Down Transient With 22 V_{IN}

Full step down transient in Figure 11 was done with 22-V input and current was stepped from 10 A to 0 A.

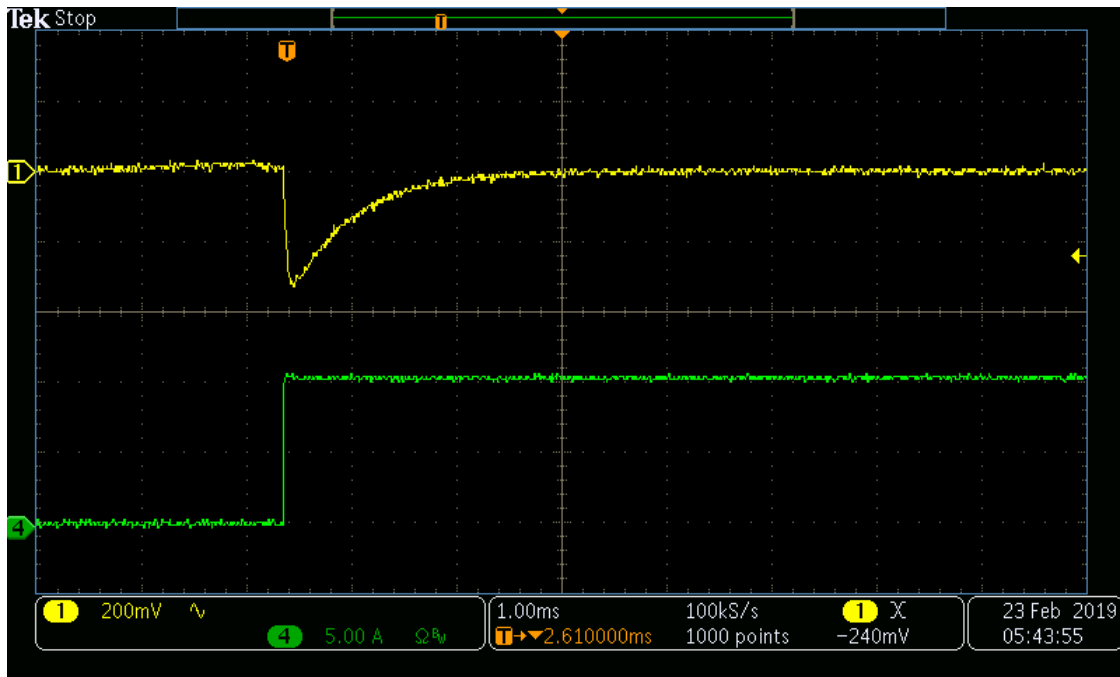


Figure 12. Full Step Up Transient With 22 V_{IN}

Step up transient in Figure 12 was done with 22-V input and current was stepped from 0 A to 10 A.

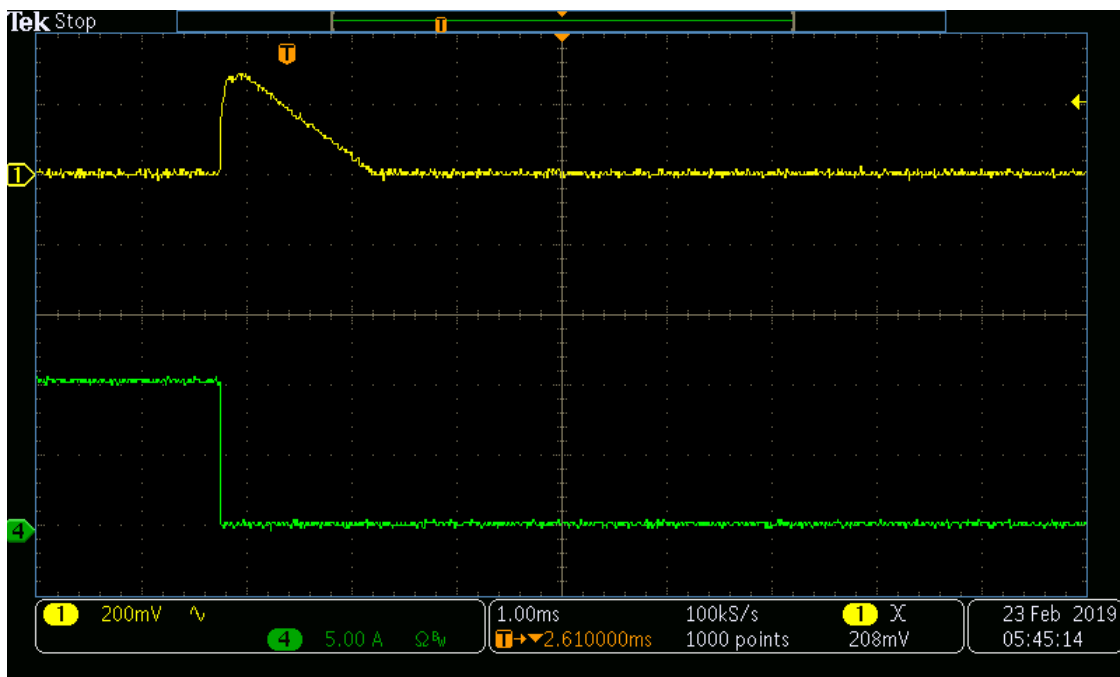


Figure 13. Partial Step Down Transient With 48 V_{IN}

Partial step down transient in Figure 13 was done with 48-V input and current was stepped from 10 A to 0.16 A.

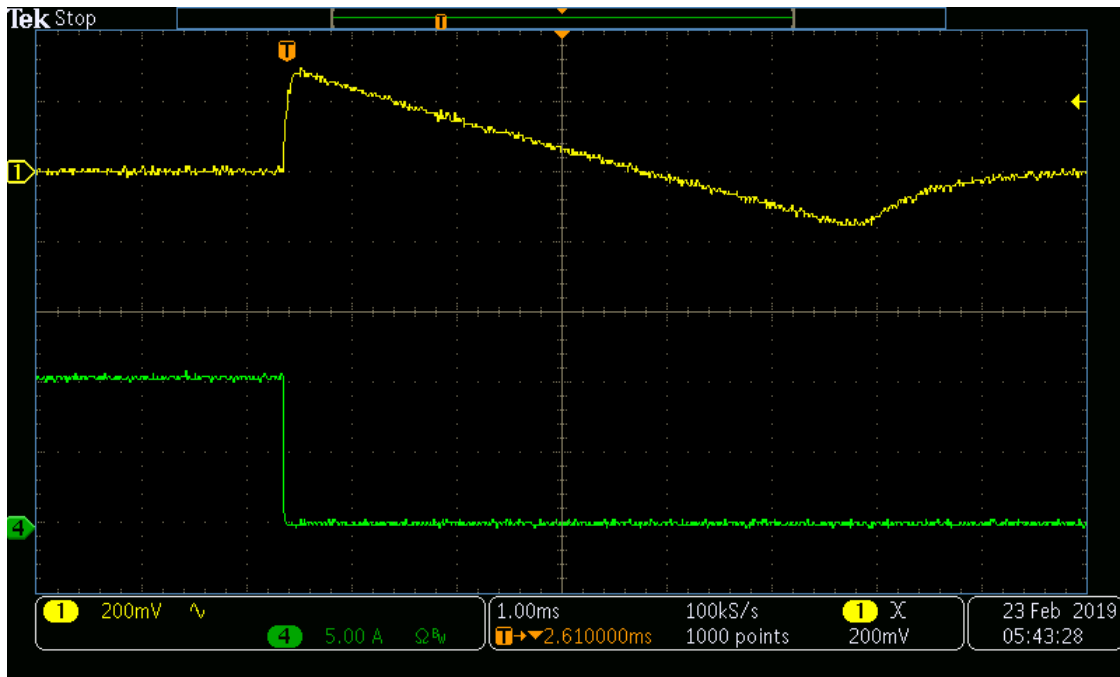


Figure 14. Full Step Down Transient With 48 V_{IN}

Full step down transient in Figure 14 was done with 48-V input and current was stepped from 10 A to 0 A.

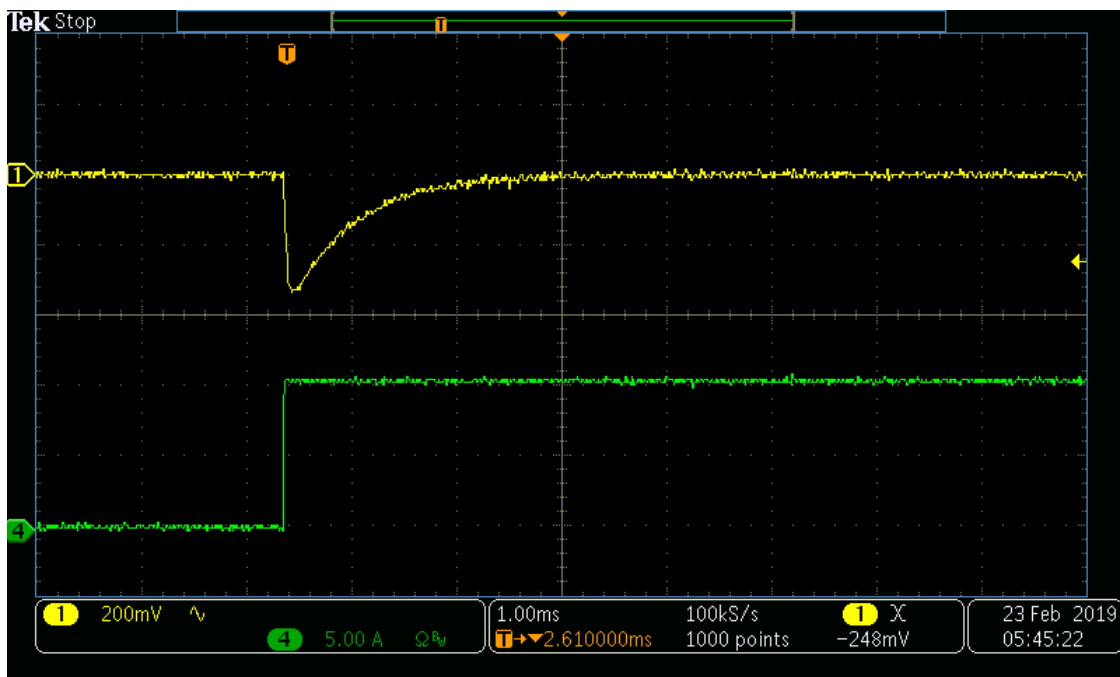


Figure 15. Full Step Up Transient With 48 V_{IN}

Full step up transient in Figure 15 was done with 48-V input and current was stepped from 0 A to 10 A.

3.2.7 Startup

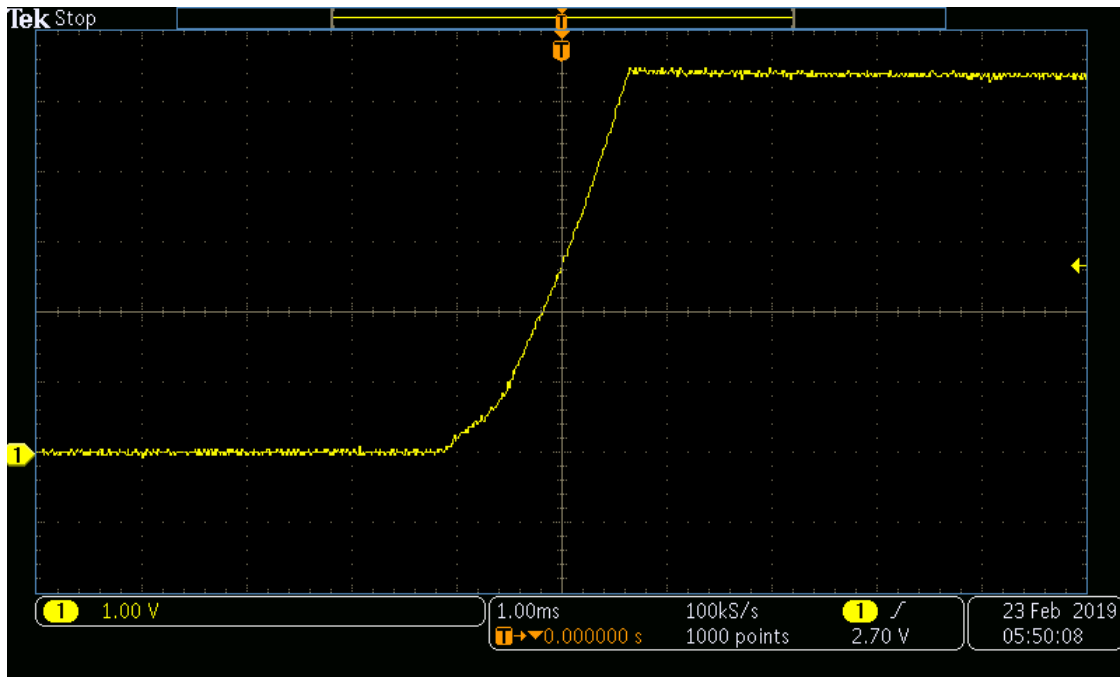


Figure 16. No Load Startup With 22 V_{IN}

No load startup in Figure 16 was done with 22 V on the input and a 0-A output. Note that the output overshoot does eventually drop down to the regulated 5 V.

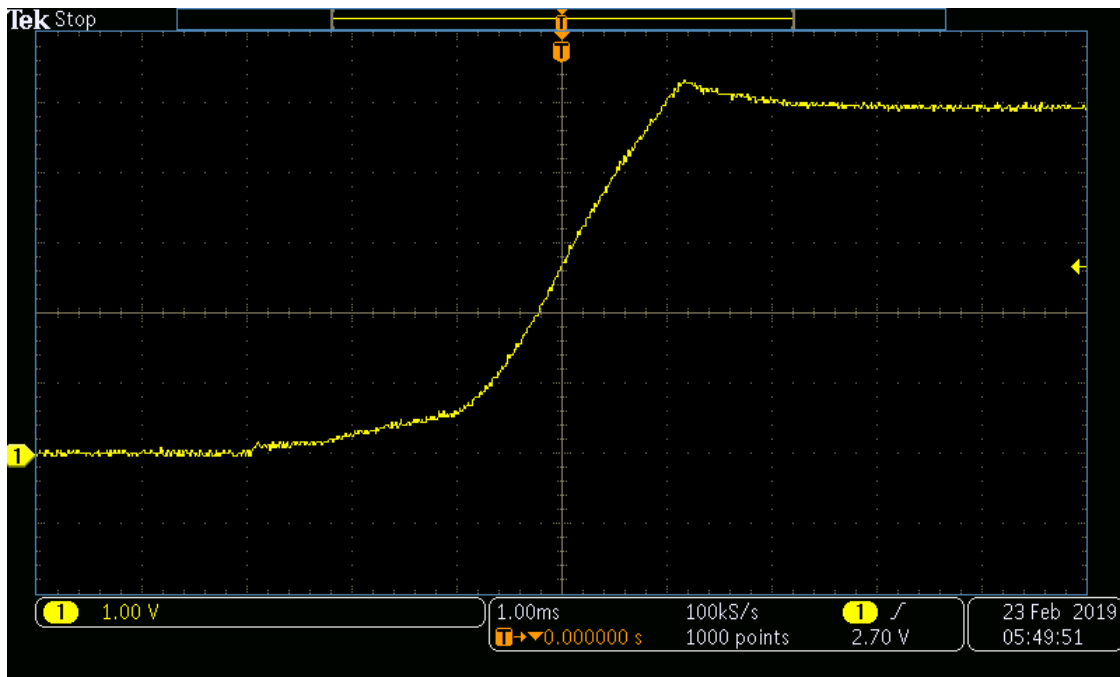


Figure 17. Full Load Startup With 22 V_{IN}

Full load startup in Figure 17 was done with 22 V on the input and a 10-A output.

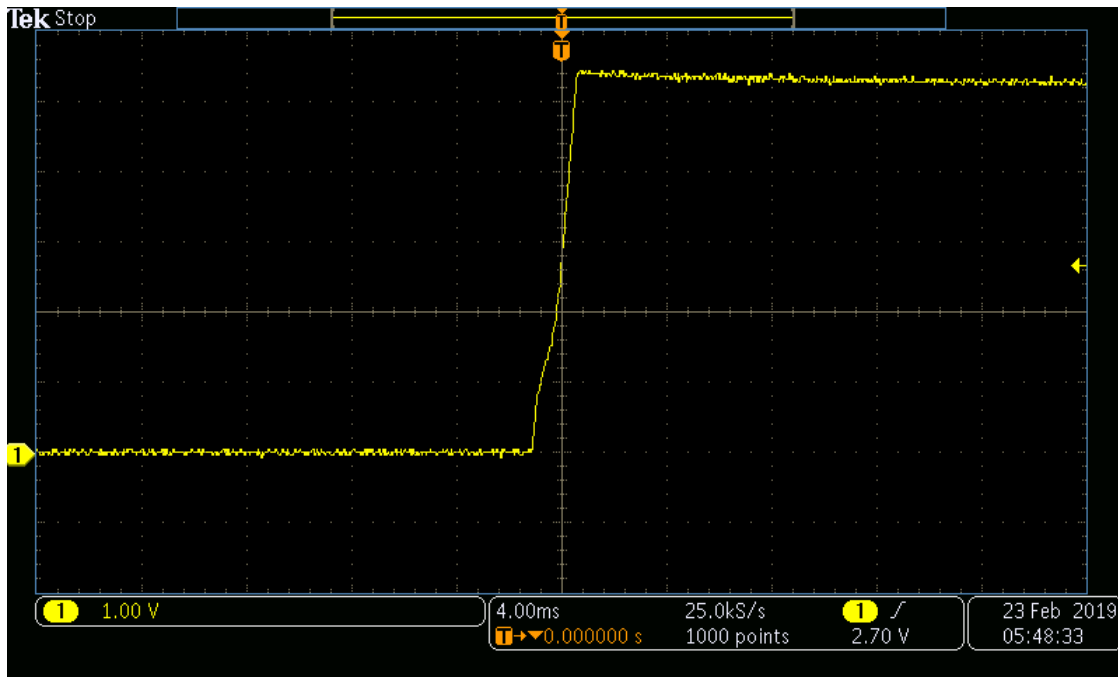


Figure 18. No Load Startup With 48 V_{IN}

No load startup in Figure 18 was done with 48 V on the input and a 0-A output. Note that the output overshoot does eventually drop down to the regulated 5 V.

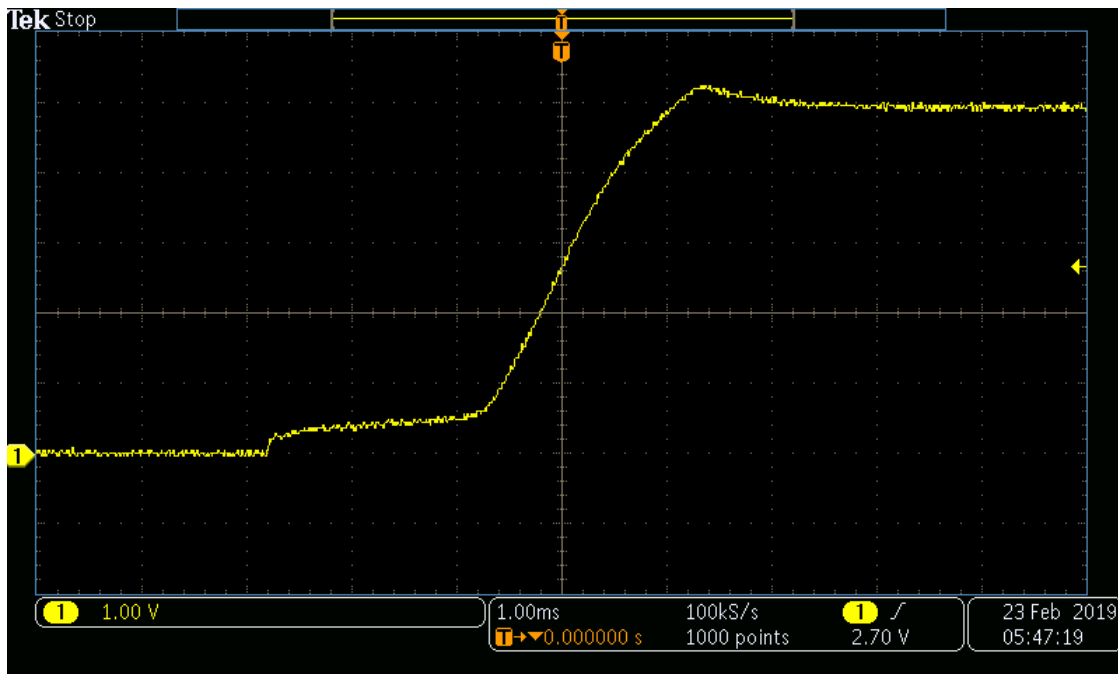


Figure 19. Full Load Startup With 48 V_{IN}

Full load startup in Figure 19 was done with 48 V on the input and a 10-A output.

3.2.8 Shutdown

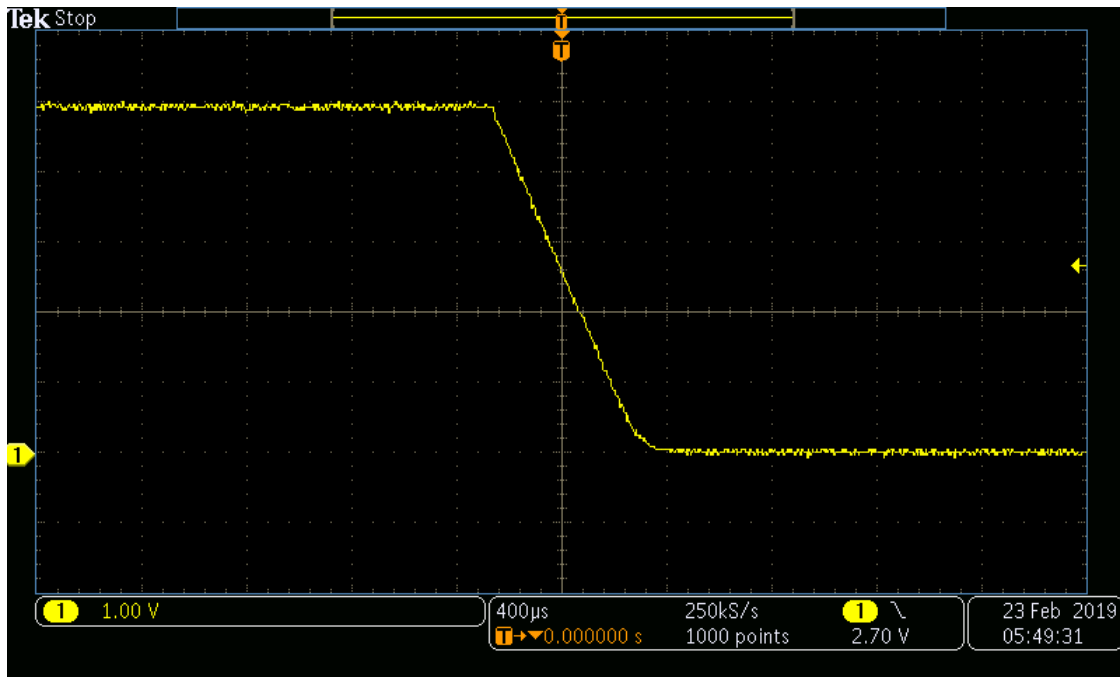


Figure 20. Full Load Shutdown With 22 V_{IN}

Full load shutdown in Figure 20 was done with 22 V on the input and a 10-A load on the output.

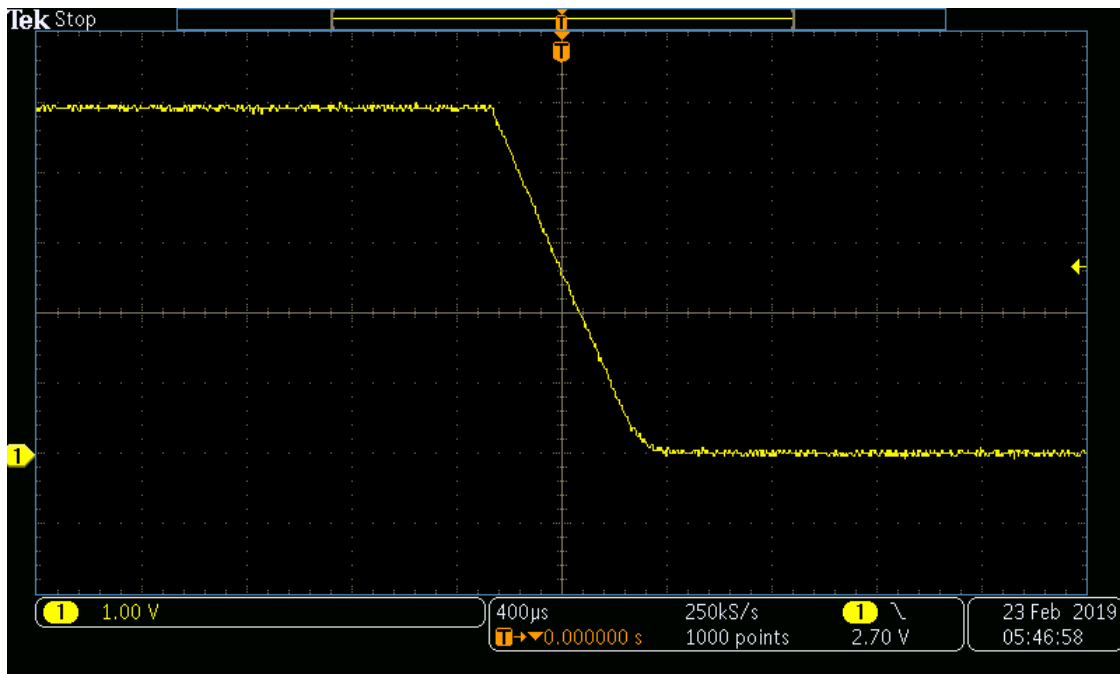


Figure 21. Full Load Shutdown With 48 V_{IN}

Full load shutdown in Figure 21 was done with 48 V on the input and a 10-A load on the output.

3.2.9 Component Stress

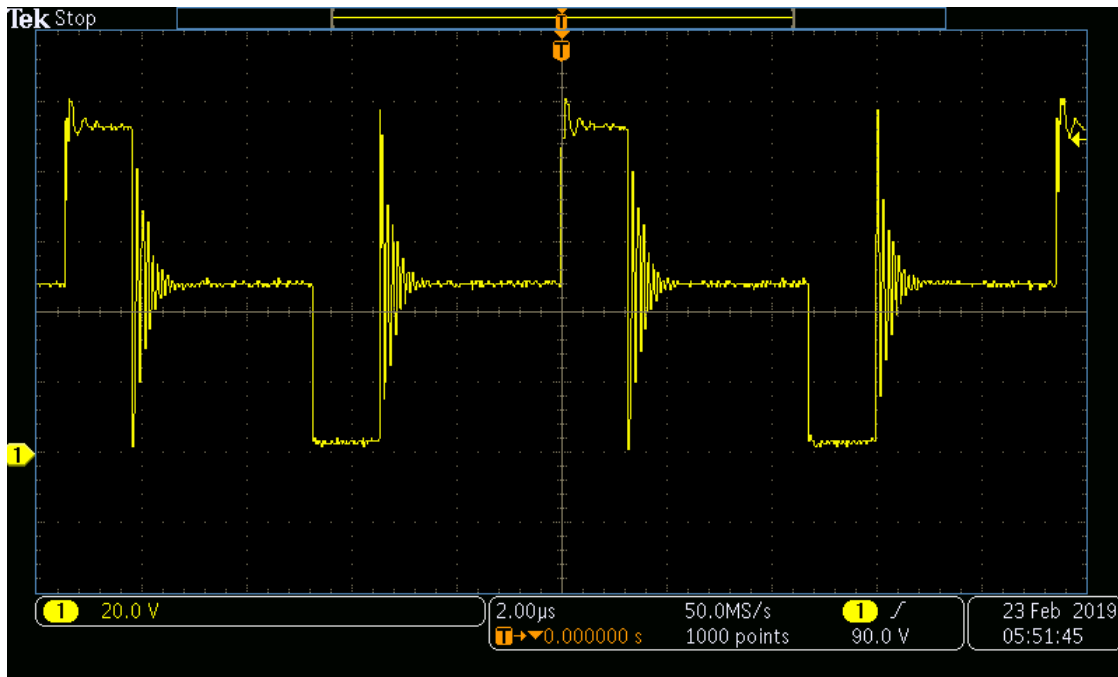


Figure 22. Voltage Stress Across Main Switching MOSFETS Q1 and Q2

The test in Figure 22 was done with 48 V on the input and a 10-A output load.

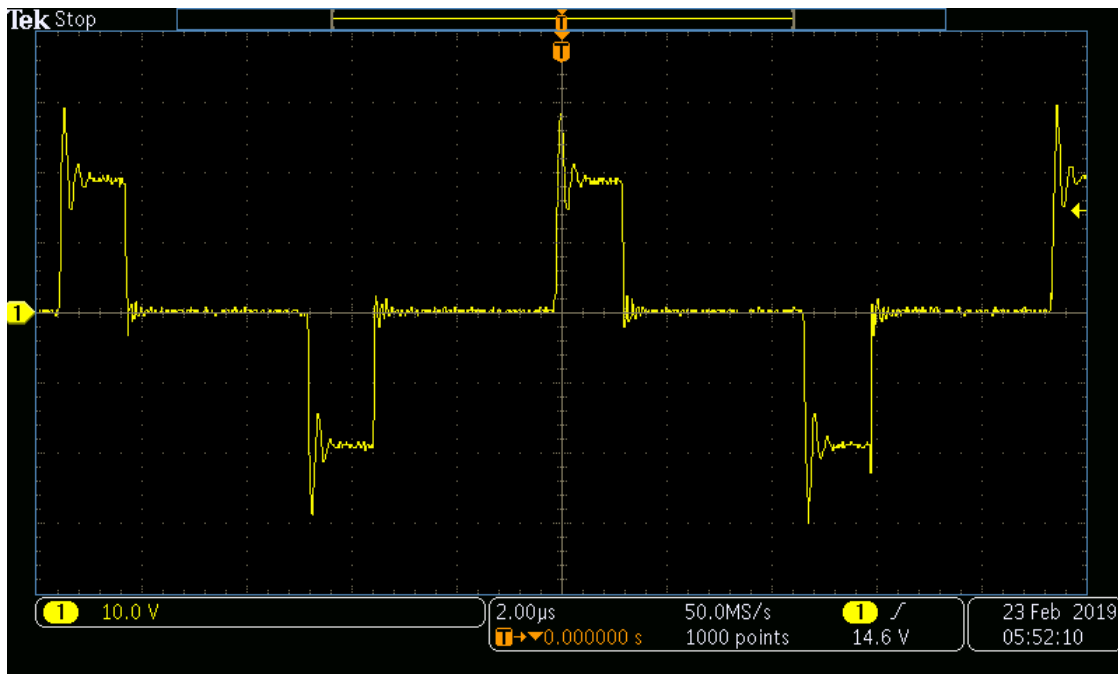


Figure 23. Voltage Stress Across Output Diode

The test in Figure 23 was done with 48 V on the input and a 10-A output load.

4 Board Layout

Care was taken in the layout to ensure that high current path lengths were minimized as well as providing multiple layers for high current input/outputs. Signals were kept to the top layer, except when it was necessary to use the bottom layer. Internal layers were used for creating large planes for input/output current as well as the switch nodes of the topology. Areas that dissipate large amounts of power such as the RCD clamp and the sense resistors were placed on large copper planes in order to allow the thermal properties of the parts to keep the temperature down as much as possible. Care was also taken to have the high switching current path short. The switching current path starts at the input capacitors, through the transformer into the MOSFETs, and then finally through the sense resistors and back into the input capacitors. On the secondary side the high switching current path is from the ground of the output capacitors, through the transformer, and then to the output.

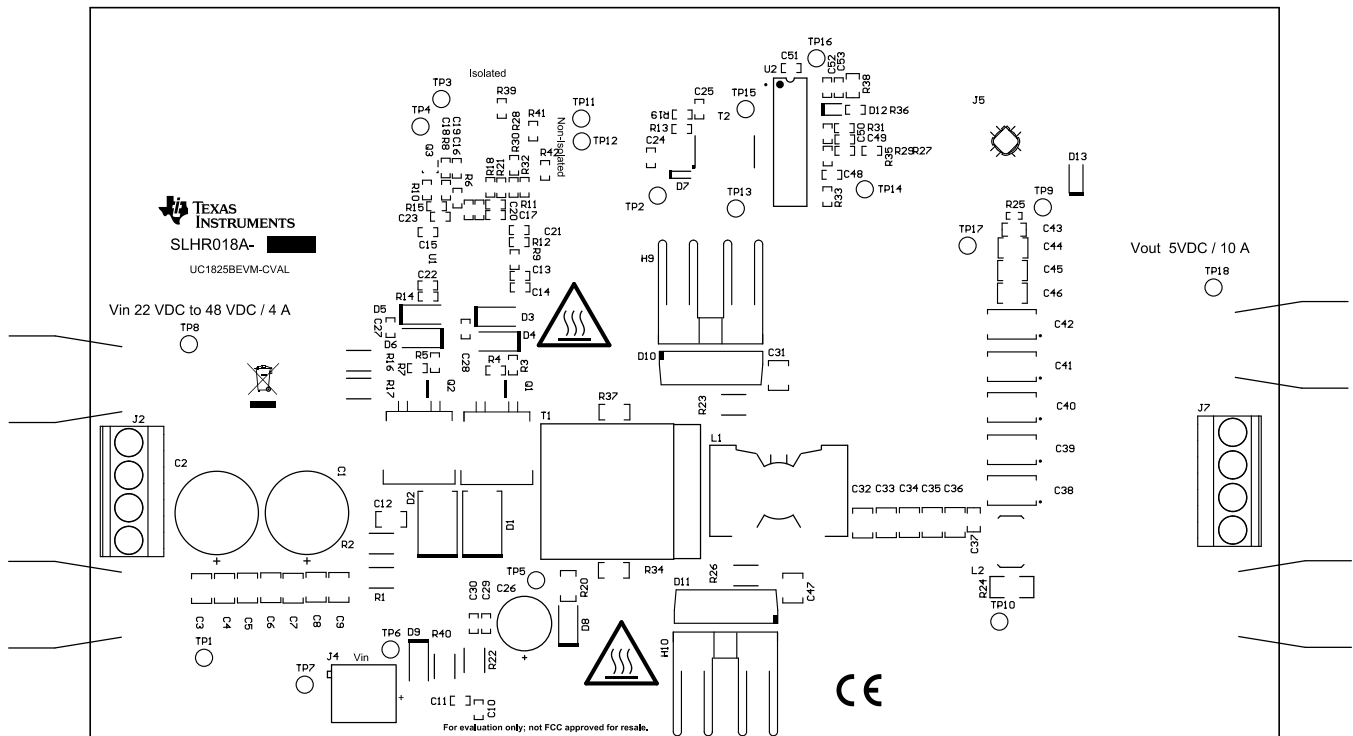


Figure 24. Top Overlay

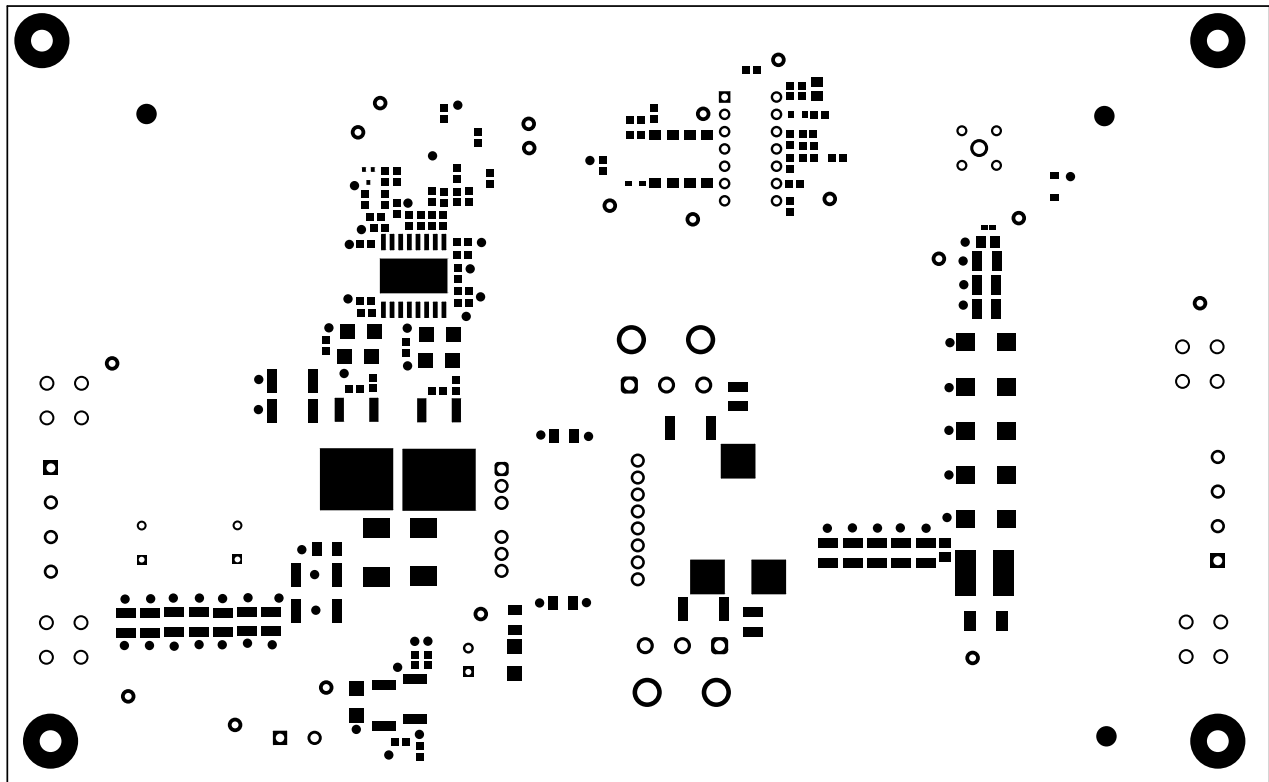


Figure 25. Top Solder

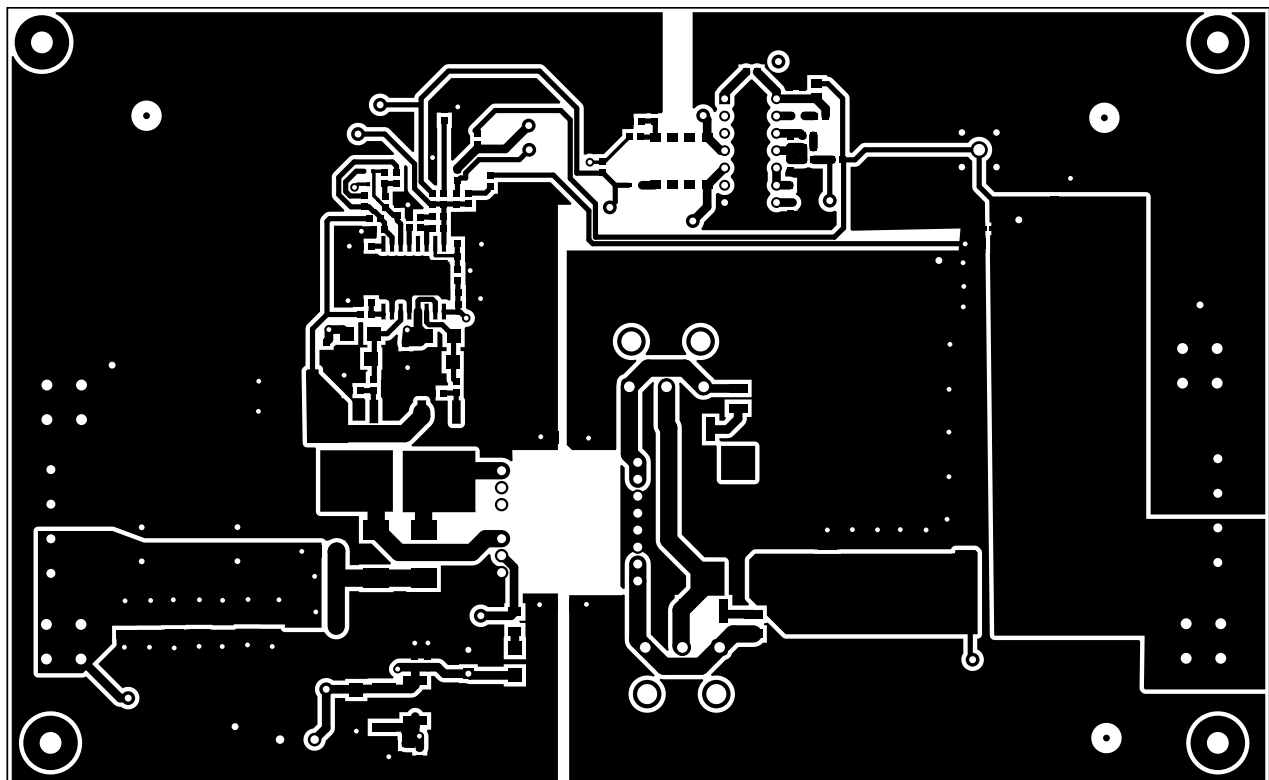


Figure 26. Top Layer

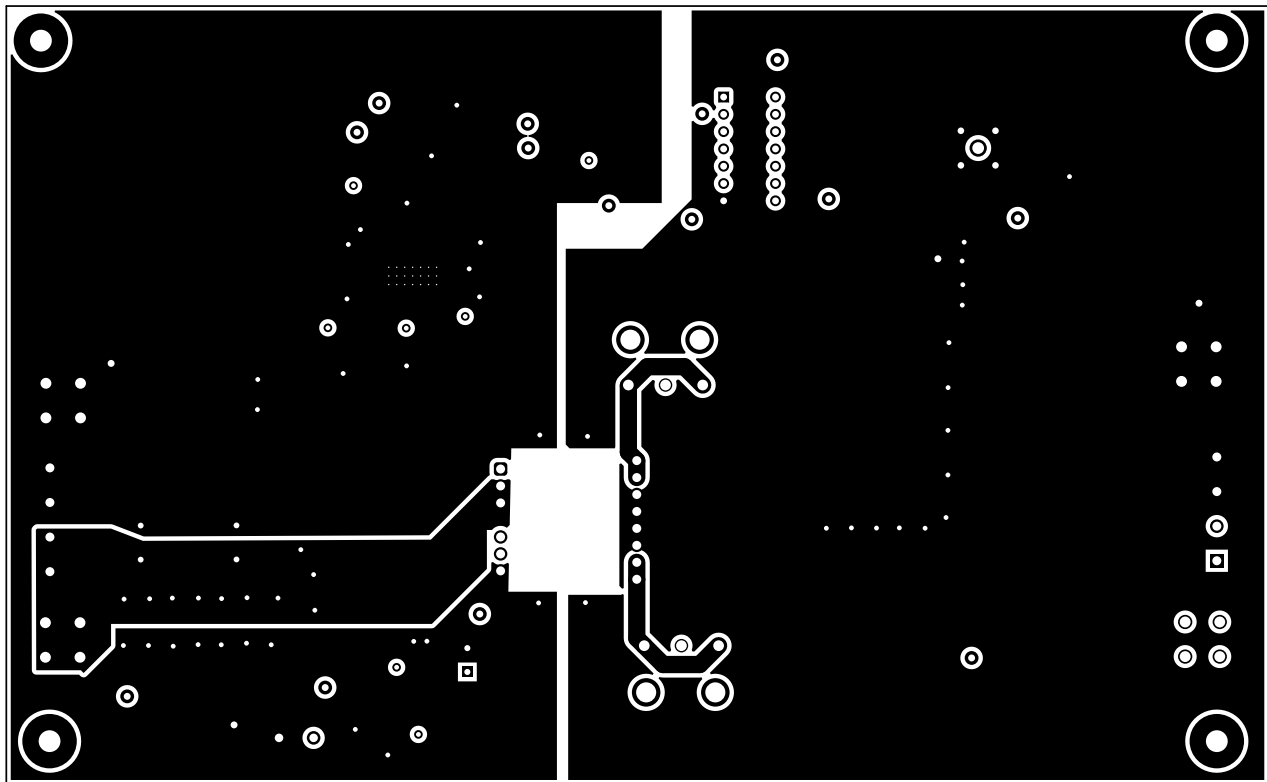


Figure 27. Signal Layer 1

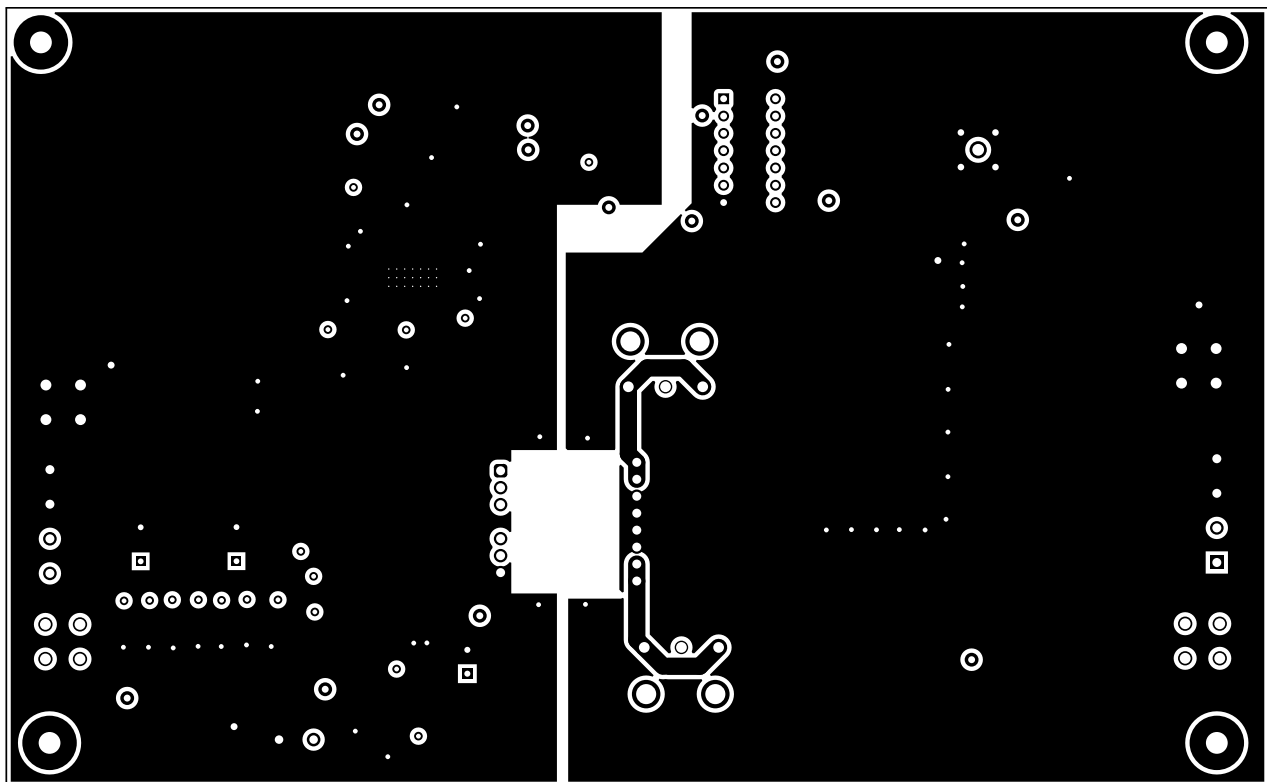


Figure 28. Signal Layer 2

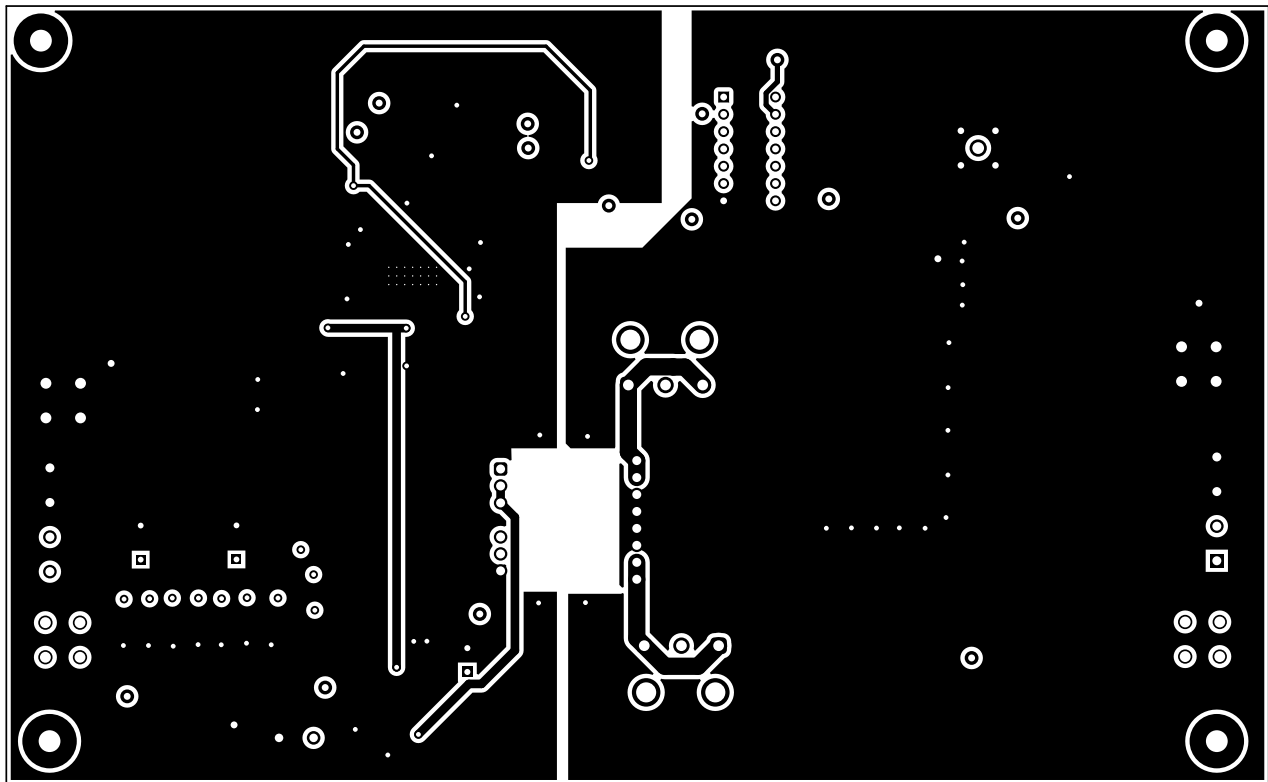


Figure 29. Bottom Layer

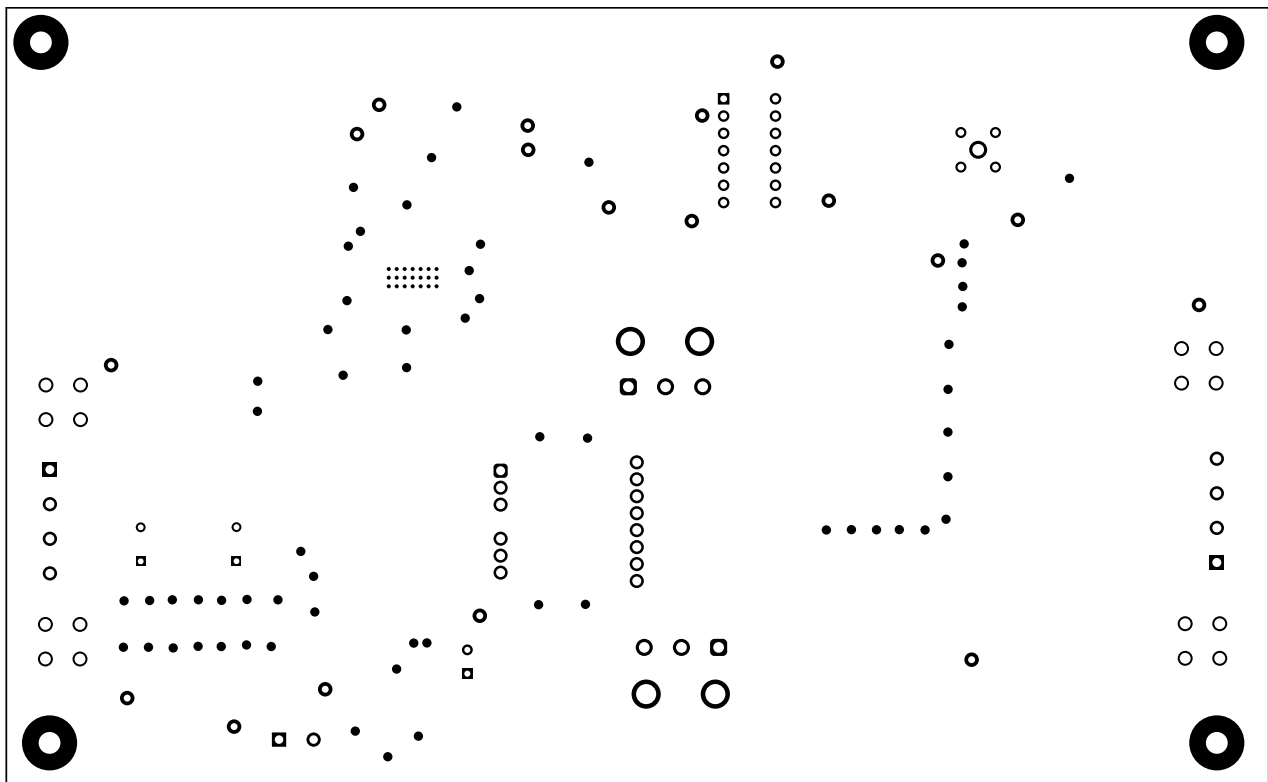


Figure 30. Bottom Solder

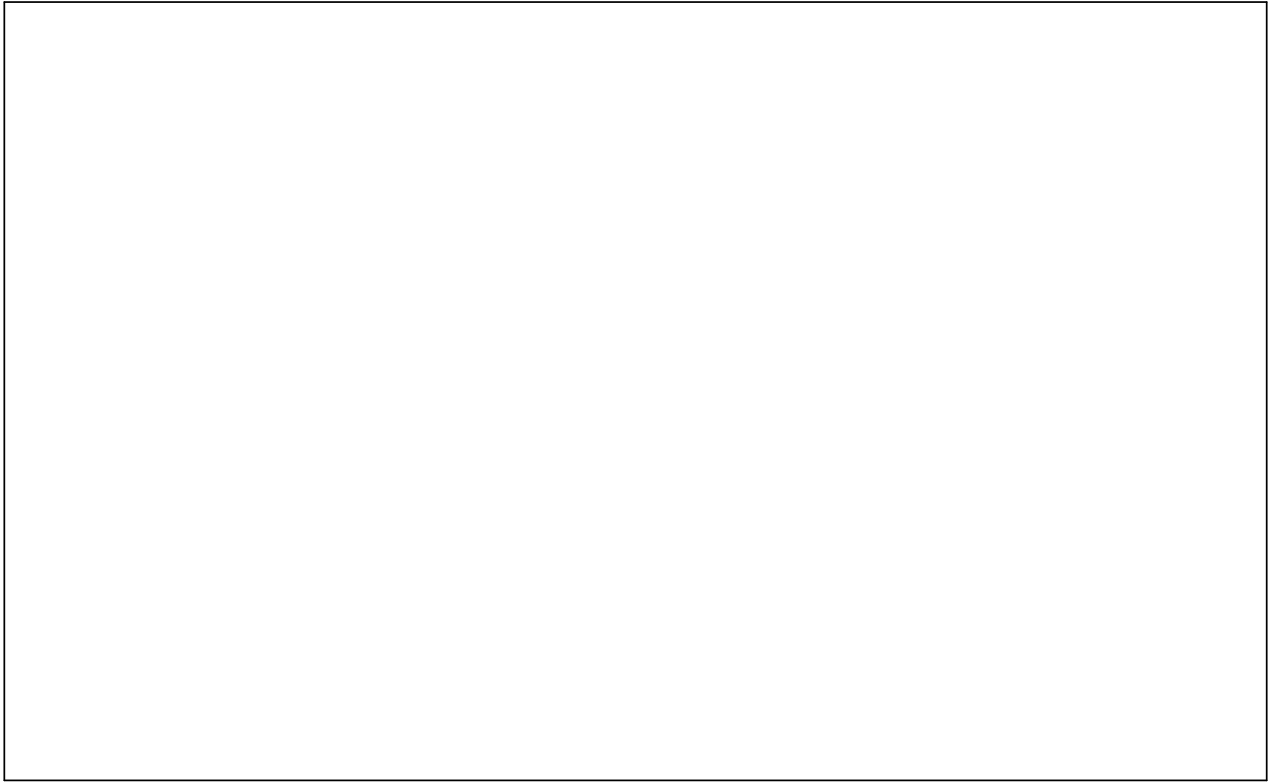
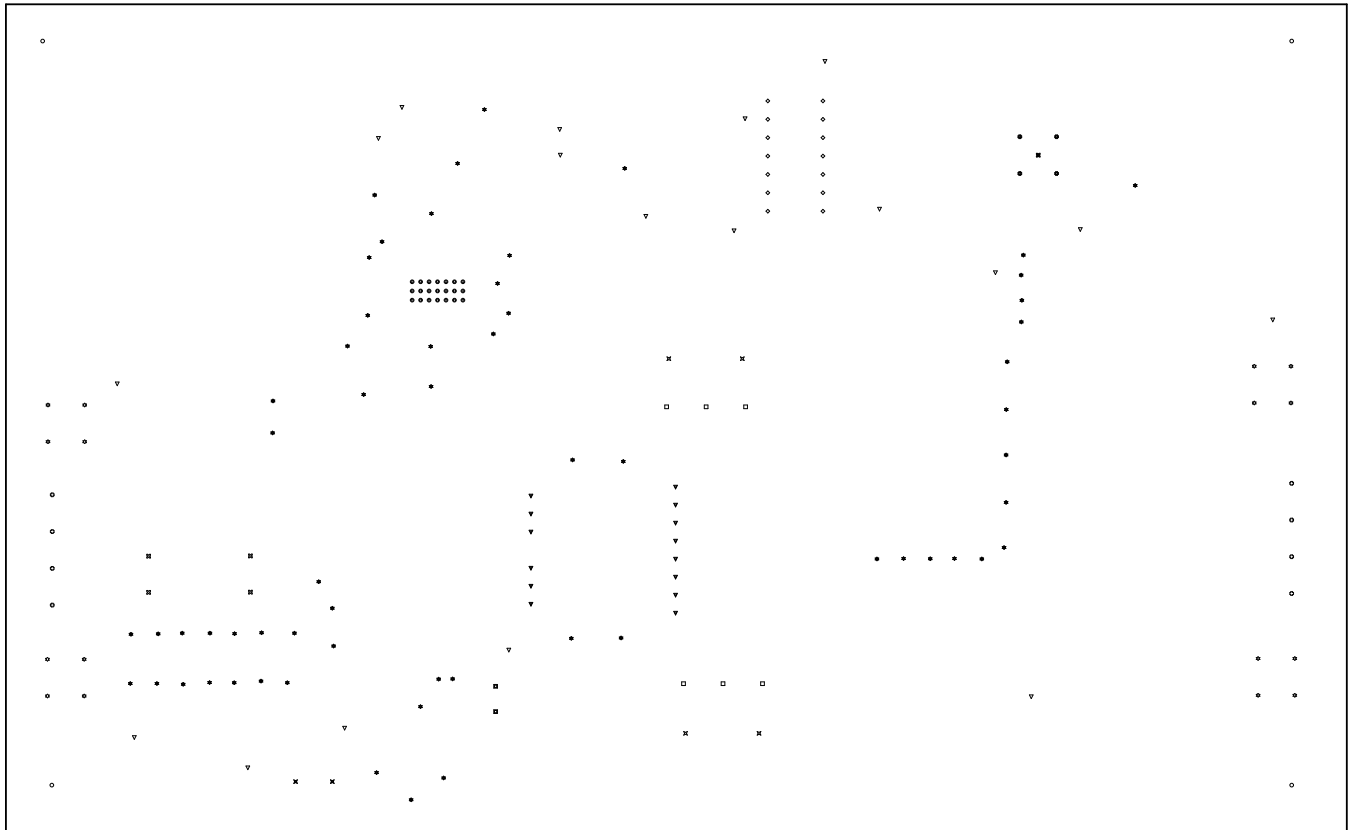


Figure 31. Bottom Overlay



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
⊙	21	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
⊛	60	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	
⊞	4	33.47mil (0.850mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	2	35.00mil (0.889mm)	PTH	Round	Top Layer - Bottom Layer	
⊚	4	38.00mil (0.965mm)	PTH	Round	Top Layer - Bottom Layer	
◇	14	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer	
▽	18	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	2	49.21mil (1.250mm)	PTH	Round	Top Layer - Bottom Layer	
▽	14	51.97mil (1.320mm)	PTH	Round	Top Layer - Bottom Layer	+/-1.18mil
⊞	8	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	6	62.00mil (1.575mm)	PTH	Round	Top Layer - Bottom Layer	
⊚	16	62.99mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	+3.94mil/-0.00mil
⊞	1	68.00mil (1.727mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	4	116.00mil (2.946mm)	PTH	Round	Top Layer - Bottom Layer	
○	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	
	178 Total					

Figure 32. Drill Drawing



Figure 33. Board Dimensions

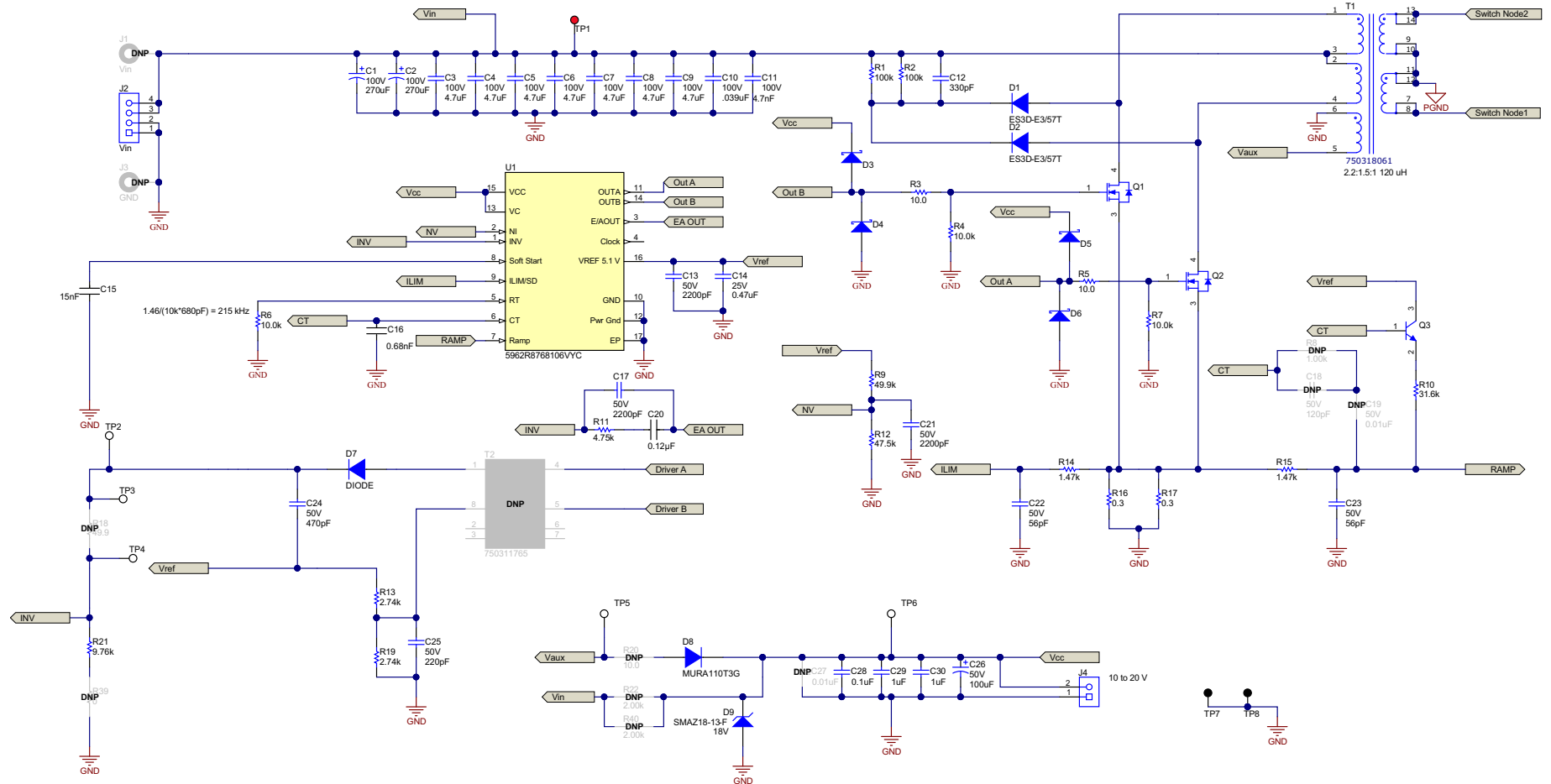


Figure 35. UC1825BEVM-CVAL Schematic 02

5.2 Bill of Materials

Table 10. Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		SLHR018	Any		
C1, C2	2	270uF	CAP, AL, 270 uF, 100 V, +/- 20%, 0.033 ohm, TH	D12.5xL30mm	EKYB101ELL271MK30S	Chemi-Con		
C3, C4, C5, C6, C7, C8, C9, C33, C34, C35, C36, C45	12	4.7uF	CAP, CERM, 4.7 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 1210	1210	CGA6M3X7S2A475K200AB	TDK		
C10	1	0.039uF	CAP, CERM, 0.039 uF, 100 V, +/- 10%, X7R, 0603	0603	C0603C393K1RACTU	Kemet		
C11	1	4700pF	CAP, CERM, 4700 pF, 100 V, +/- 10%, X7R, 0603	0603	06031C472KAT2A	AVX		
C12	1	330pF	CAP, CERM, 330 pF, 630 V, +/- 5%, C0G/NP0, 1206	1206	GRM31A5C2J331JW01D	MuRata		
C13, C17, C21	3	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C222K5RACTU	Kemet		
C14	1	0.47uF	CAP, CERM, 0.47 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7R1E474K080AB	TDK		
C15	1		Cap Ceramic 0.015uF 50V X7R 10% Pad SMD 0603 125°C T/R	0603	C0603C153K5RACTU	Kemet		
C16	1		YAGEO (PHYCOMP) CC0603KRX7R9BB681 SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 680 pF, 50 V, 10%, X7R, CC Series	0603 (1608 Metric)	CC0603KRX7R9BB681	YAGEO		
C20	1		CAP Ceramic 0.12uF 10% X7R 0603 SMD	0603 (1608 metric)	C0603C124K3RAC7867	KEMET		
C22, C23	2	56pF	CAP, CERM, 56 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A560JAT2A	AVX		
C24	1	470pF	CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, 0603	0603	885012206081	Würth Elektronik		
C25	1	220pF	CAP, CERM, 220 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C221K5RACTU	Kemet		
C26	1	100uF	CAP, AL, 100 uF, 50 V, +/- 20%, 0.12 ohm, TH	CAP, 8x11.5mm	50ZLJ100MT78X11.5	Rubycon		
C28, C49, C52	3	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R1H104K080AA	TDK		
C29, C30	2	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden		
C31, C47	2	4700pF	CAP, CERM, 4700 pF, 500 V, +/- 10%, X7R, 1210	1210	VJ1210Y472KXEAT5Z	Vishay-Vitramon		
C32, C44	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 1210	1210	C1210C104K5RACTU	Kemet		
C37, C43	2	2200pF	CAP, CERM, 2200 pF, 100 V, +/- 10%, X7R, 0805	0805	08051C222KAT2A	AVX		
C38, C39, C40, C41, C42	5	220uF	CAP, TA, 220 uF, 10 V, +/- 10%, 0.045 ohm, SMD	7343-43	T495X227K010ATE045	Kemet		
C46	1	22uF	CAP, CERM, 22 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P1X7R1C226M250AC	TDK		

Table 10. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C48	1	0.22uF	CAP, CERM, 0.22 uF, 16 V, +/- 10%, X7R, 0603	0603	885012206048	Würth Elektronik		
C51	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	885012006057	Würth Elektronik		
C53	1	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0603	0603	EMK107BB7225MA-T	Taiyo Yuden		
D1, D2	2	200V	Diode, Ultrafast, 200 V, 3 A, SMC	SMC	ES3D-E3/57T	Vishay-Semiconductor		
D3, D4, D5, D6	4	30V	Diode, Schottky, 30 V, 1 A, SMA	SMA	B130-13-F	Diodes Inc.		
D7	1	75V	Diode, Switching, 75 V, 0.3 A, SOD-523F	SOD-523F	1N4148WT	Fairchild Semiconductor		
D8	1	100V	Diode, Ultrafast, 100 V, 2 A, SMA	SMA	MURA110T3G	ON Semiconductor		
D9	1	18V	Diode, Zener, 18 V, 1 W, AEC-Q101, SMA	SMA	SMAZ18-13-F	Diodes Inc.		
D10, D11	2	60V	Diode, Schottky, 60 V, 40 A, TH	TO-247	VS-40CPQ060PBF	Vishay-Semiconductor		
D12	1	Green	LED, Green, SMD	2x1.4mm	LG M67K-G1J2-24-Z	OSRAM		
D13	1	6V	Diode, Zener, 6 V, 500 mW, SOD-123	SOD-123	MMSZ5233B-7-F	Diodes Inc.		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
H9, H10	2			16.26x25.4x16.26 mm	634-10ABPE	Wakefield-Vette		
J2, J7	2		Terminal Block, 4x1, 5.08mm, TH	4x1 Terminal Block	39544-3004	Molex		
J4	1		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology		
J5	1		Compact Probe Tip Circuit Board Test Points, TH, 25 per	TH Scope Probe	131-5031-00	Tektronix		
L1	1	2.2uH	Inductor, Shielded Drum Core, Mn-Zn, 2.2 uH, 28 A, 0.0015 ohm, SMD	21.8x14.5x21.5mm	7443630220	Würth Elektronik		
L2	1	500nH	Inductor, Shielded, Ferrite, 500 nH, 12 A, 0.0066 ohm, AEC-Q200 Grade 1, SMD	8x8x4.5 mm	SRN8040TA-R50Y	Bourns		
Q1, Q2	2	250V	MOSFET, N-CH, 250 V, 25 A, DDPK	DDPK	IPB600N25N3 G	Infineon Technologies		None
Q3	1	40 V	Transistor, NPN, 40 V, 0.2 A, SOT-323	SOT-323	MMBT3904WT1G	ON Semiconductor		
R1, R2	2	100k	RES, 100 k, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW2512100KFKEG	Vishay-Dale		
R3, R5	2	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo America		
R4, R6, R7, R33	4	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic		
R9	1	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo		
R10	1	31.6k	RES, 31.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060331K6FKEA	Vishay-Dale		
R11	1	4.75k	RES, 4.75 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K75FKEA	Vishay-Dale		

Table 10. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R12	1	47.5k	RES, 47.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF4752V	Panasonic		
R13, R19	2	2.74k	RES, 2.74 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06032K74FKEA	Vishay-Dale		
R14, R15	2	1.47k	RES, 1.47 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K47FKEA	Vishay-Dale		
R16, R17	2	0.3	RES, 0.3, 1%, 2 W, 2512	2512	CSRN2512FKR300	Stackpole Electronics Inc		
R21	1	9.76k	RES, 9.76 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06039K76FKEA	Vishay-Dale		
R23, R26	2	3.00	RES, 3.00, 1%, 1 W, 2512	2512	ERJ-1TRQF3R0U	Panasonic		
R24	1	0.5	RES, 0.5, 1%, 1 W, 2010	2010	CSRN2010FKR500	Stackpole Electronics Inc		
R25	1	10.0k	RES, 10.0 k, 0.1%, 0.063 W, 0402	0402	MCR01MRTF1002	Rohm		
R28	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo America		
R29	1	40.2k	RES, 40.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060340K2FKEA	Vishay-Dale		
R30	1	2.00k	RES, 2.00 k, 1%, 0.1 W, 0603	0603	RC0603FR-072KL	Yageo America		
R31	1	30.0k	RES, 30.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730KL	Yageo		
R32	1	2.05k	RES, 2.05 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K05L	Yageo		
R34, R37	2	0	RES, 0, 5%, 0.25 W, 1206	1206	RC1206JR-070RL	Yageo America		
R35	1	17.2k	RES, 17.2 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD0717K2L	Yageo America		
R36	1	360	RES, 360, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603360RJNEA	Vishay-Dale		
R41, R42	2	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc		
T1	1		TRANSFORMER	PTH_25MM0_22MM2	750318061	Würth Electronics		
TP1, TP9, TP10	3		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP2, TP3, TP4, TP5, TP6, TP11, TP12, TP13, TP14, TP15, TP16	11		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		
TP7, TP8, TP17, TP18	4		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1	1		RAD-TOLERANT CLASS V, HIGH-SPEED PWM CONTROLLER, HKT0016A (CFP-16)	HKT0016A	5962R8768106VYC	Texas Instruments		Texas Instruments
U2	1		Isolated Feedback Generator, -55 to 125 degC, 14-pin CDIP (J)	J0014A	5962-8944101VCA	Texas Instruments		
C18	0	120pF	CAP, CERM, 120 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H121JA01D	MuRata		
C19	0	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0603	0603	CL10B103KB8NCNC	Samsung Electro-Mechanics		

Table 10. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C27	0	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H103KA01D	MuRata		
C50	0	2700pF	CAP, CERM, 2700 pF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E272KA01D	MuRata		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J6	0		Banana Jack Insul Nylon Red, R/A, TH	CTE_CT3151SP-2	CT3151SP-2	Cal Test Electronics		
J3, J8	0		Banana Jack Insul Nylon Black, R/A, TH	CTE_CT3151SP-0	CT3151SP-0	Cal Test Electronics		
R8	0	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale		
R18, R27	0	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo America		
R20	0	10.0	RES, 10.0, 1%, 0.25 W, 1206	1206	RC1206FR-0710RL	Yageo America		
R22, R40	0	2.00k	RES, 2.00 k, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW25122K00FKEG	Vishay-Dale		
R38	0	0	RES, 0, 0%, W, AEC-Q200 Grade 0, 0805	0805	PMR10EZPJ000	Rohm		
R39	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc		
T2	0	1.2mH	Transformer, 1200 uH, SMD	8.64x9.02mm	750311765	Würth Elektronik		

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated