

# NP100N04PUK

R07DS0545EJ0200

Rev. 2.00

May 24, 2018

## MOS FIELD EFFECT TRANSISTOR

### Description

NP100N04PUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

### Features

- Super low on-state resistance  
 $R_{DS(on)} = 2.3 \text{ m}\Omega \text{ MAX. ( } V_{GS} = 10 \text{ V, } I_D = 50 \text{ A )}$
- Low Ciss  $C_{iss} = 4700 \text{ pF TYP. ( } V_{DS} = 25 \text{ V )}$
- Designed for automotive application and AEC-Q101 qualified

### Ordering Information

Part No.	Lead Plating	Packing		Package
NP100N04PUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263(MP-25ZP)
NP100N04PUK-E2-AY *1			Taping (E2 type)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode.)

### Absolute Maximum Ratings (T<sub>A</sub>=25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25 °C)	I <sub>D(DC)</sub>	±100	A
Drain Current (pulse) *1, 3	I <sub>D(pulse)</sub>	±400	A
Total Power Dissipation (T <sub>C</sub> = 25 °C)	P <sub>T1</sub>	176	W
Total Power Dissipation (T <sub>A</sub> = 25 °C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to 175	°C
Repetitive Avalanche Current *2, 3	I <sub>AR</sub>	43	A
Repetitive Avalanche Energy *2, 3	E <sub>AR</sub>	185	mJ

### Thermal Resistance

Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub> *3	0.85	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub> *3	83.3	°C/W

Notes \*1. T<sub>C</sub> = 25°C, P<sub>W</sub> ≤ 10 μs, Duty Cycle ≤ 1%

\*2. R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V

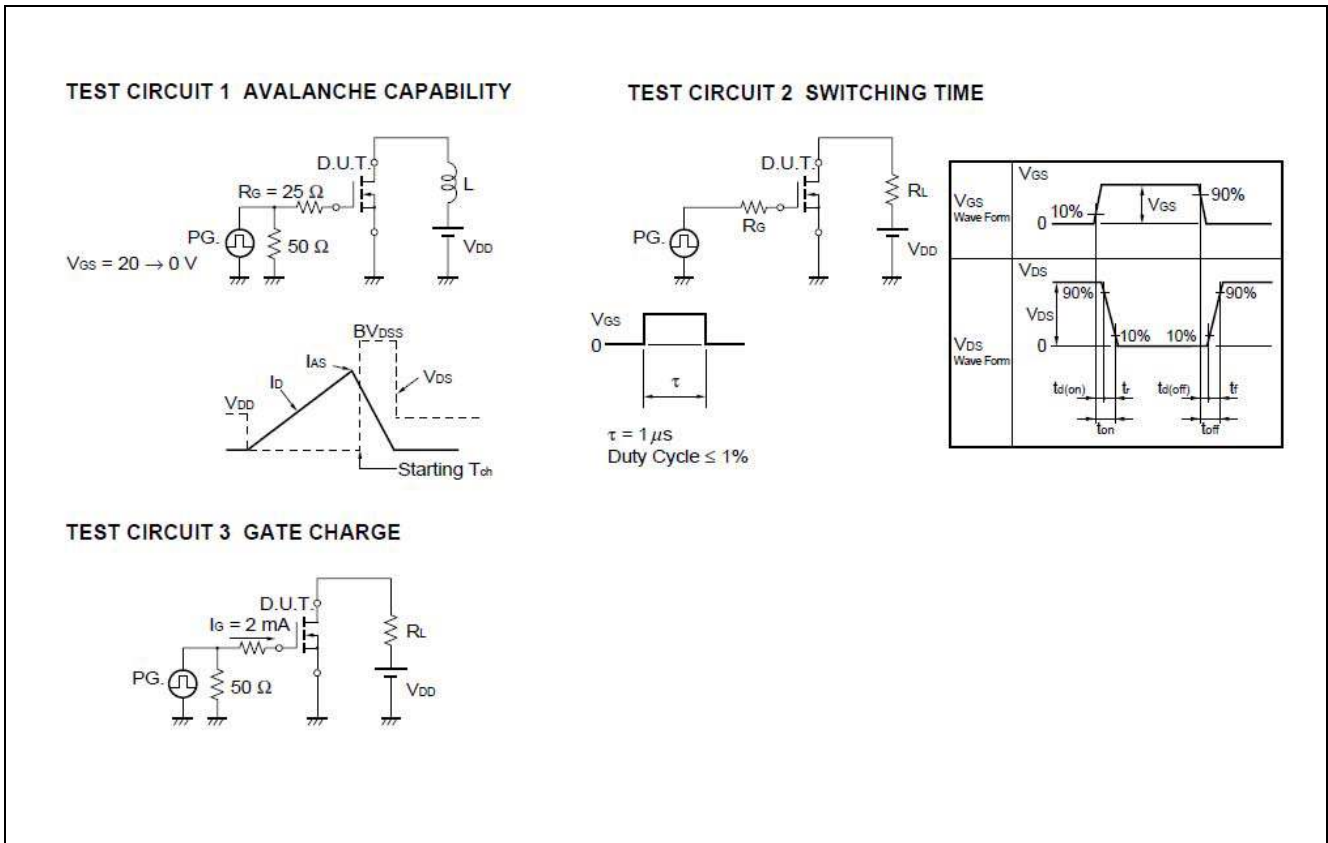
\*3. Not subject of production test. Verified by design/characterization.

Electrical Characteristics (T<sub>A</sub>=25°C)

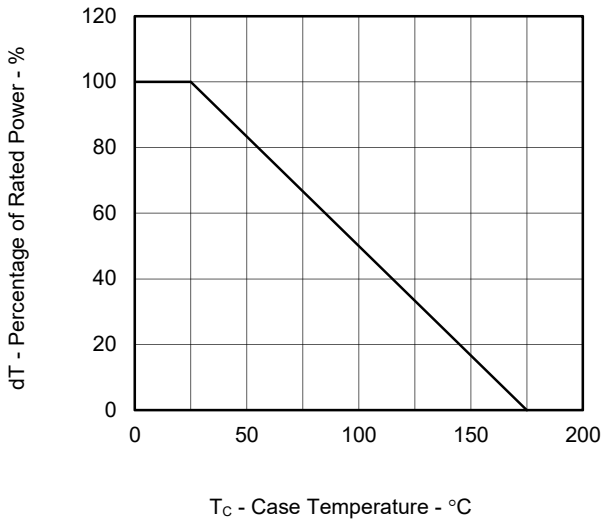
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	40	80		S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 50 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>		1.9	2.3	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A
Input Capacitance *2	C <sub>iss</sub>		4700	7050	pF	V <sub>DS</sub> = 25 V
Output Capacitance *2	C <sub>oss</sub>		660	990	pF	V <sub>GS</sub> = 0 V
Reverse Transfer Capacitance *2	C <sub>rss</sub>		270	490	pF	f = 1 MHz
Turn-on Delay Time *2	t <sub>d(on)</sub>		28	70	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 50 A
Rise Time *2	t <sub>r</sub>		14	40	ns	V <sub>GS</sub> = 10 V
Turn-off Delay Time *2	t <sub>d(off)</sub>		70	140	ns	R <sub>G</sub> = 0 Ω
Fall Time *2	t <sub>f</sub>		10	30	ns	
Total Gate Charge *2	Q <sub>G</sub>		80	120	nC	V <sub>DD</sub> = 32 V
Gate to Source Charge	Q <sub>GS</sub>		21		nC	V <sub>GS</sub> = 10 V
Gate to Drain Charge	Q <sub>GD</sub>		20		nC	I <sub>D</sub> = 100 A
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>	0.9	1.5		V	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		52		ns	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>		78		nC	di/dt = 100 A/μs

Note. \*1 Pulse test

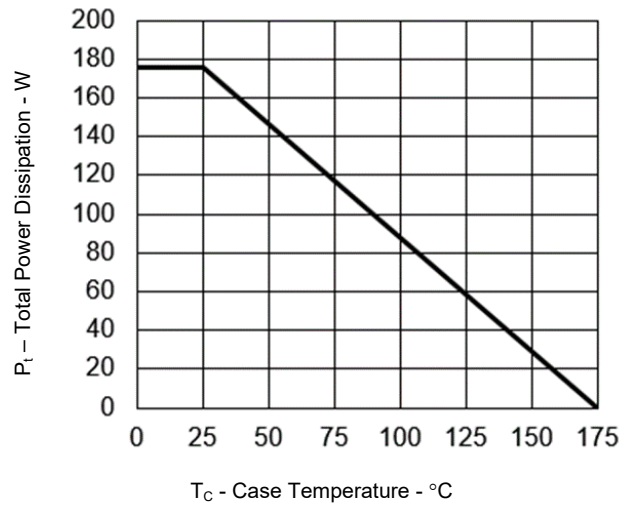
Note. \*2 Not subject of production test. Verified by design/characterization.



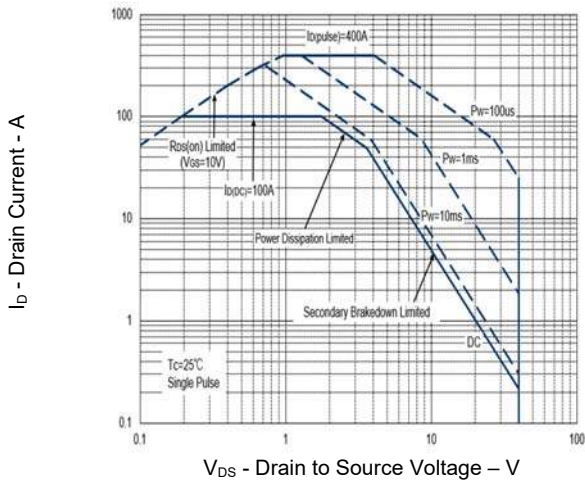
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



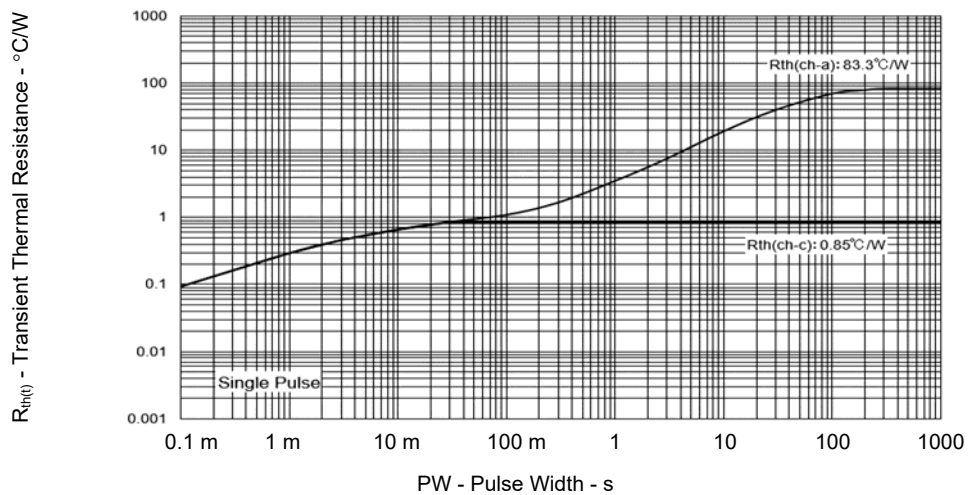
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



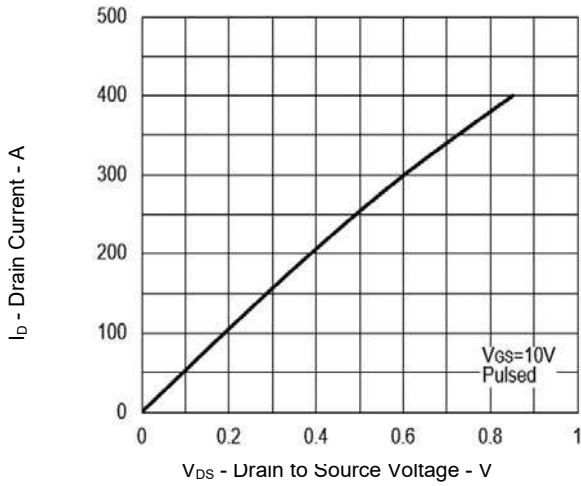
FORWARD BIAS SAFE OPERATING AREA



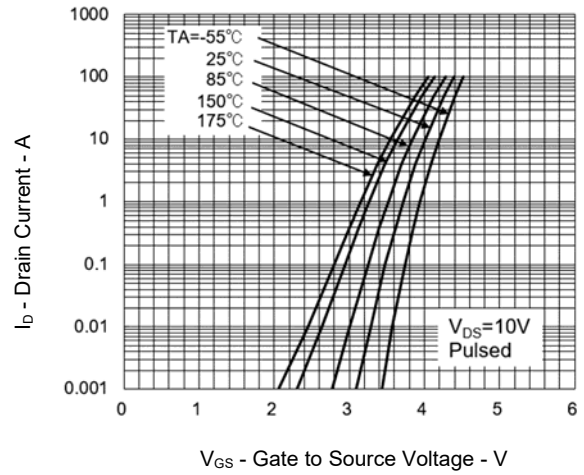
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



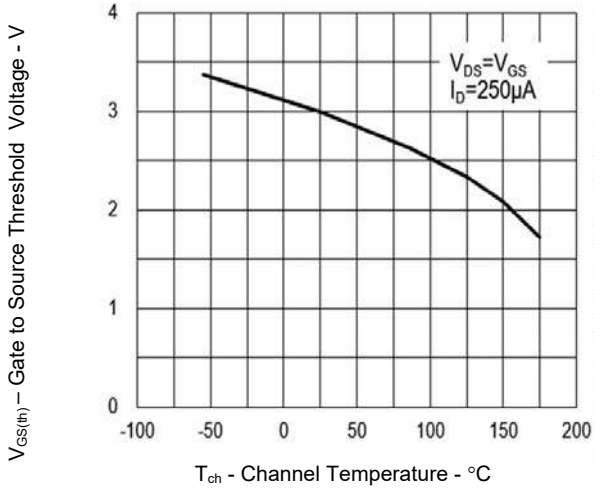
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



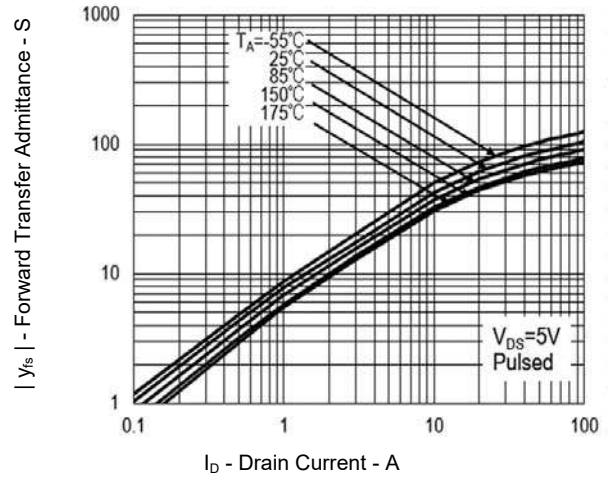
FORWARD TRANSFER CHARACTERISTICS



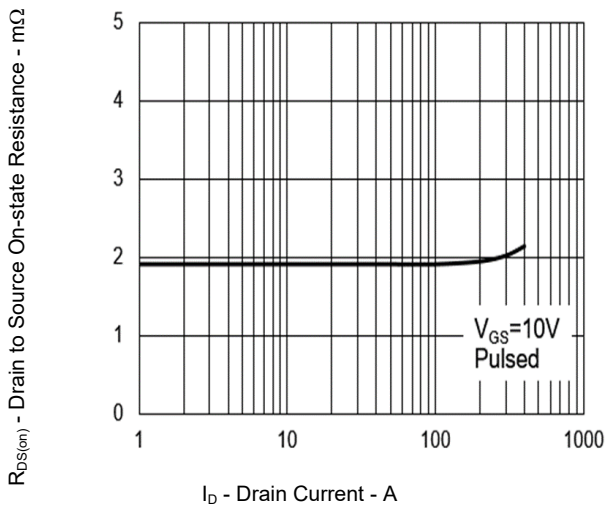
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



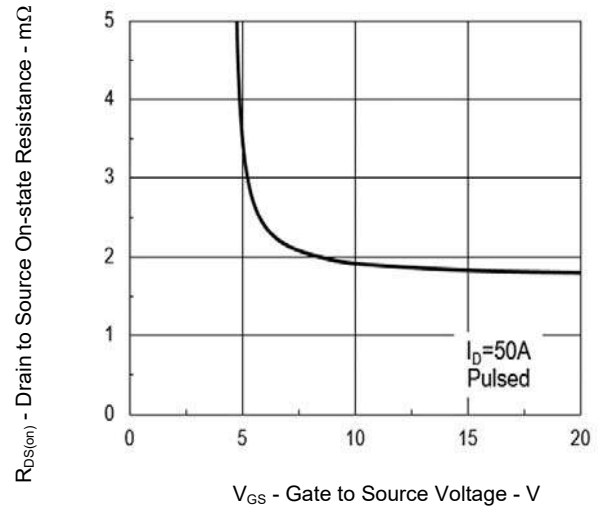
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



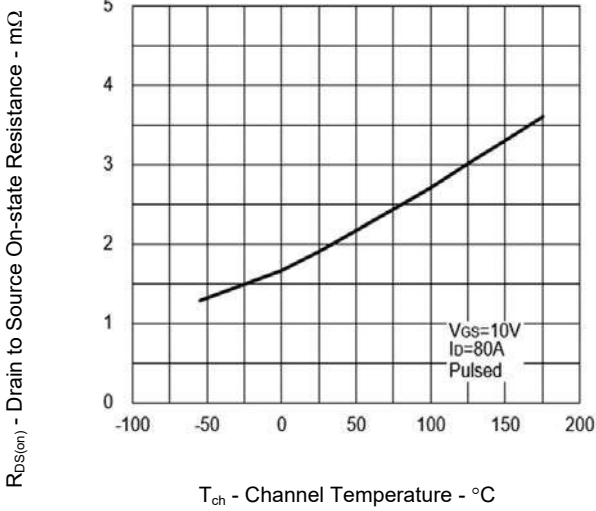
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



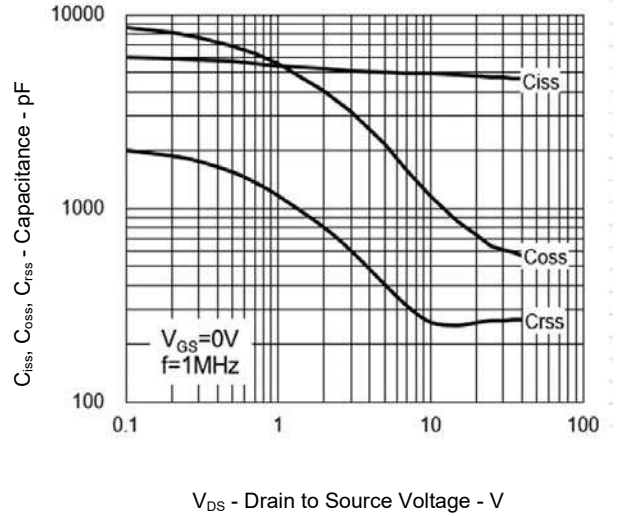
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



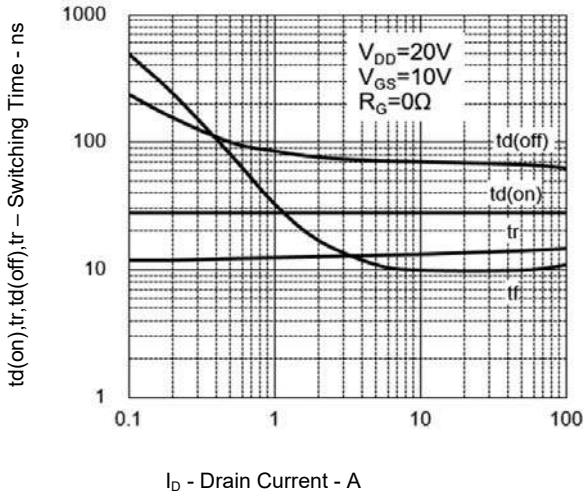
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



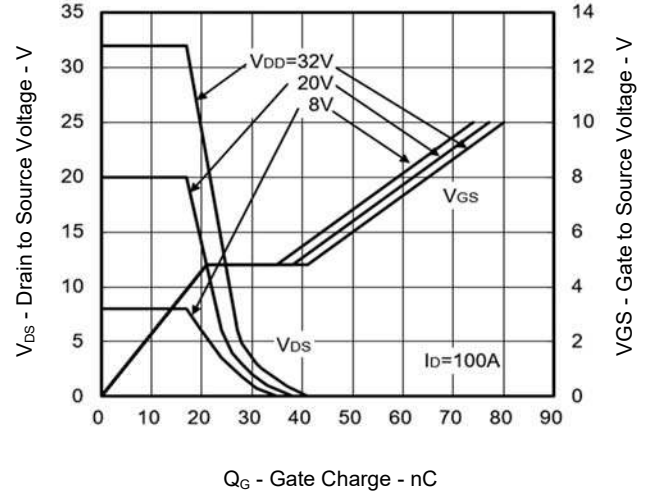
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



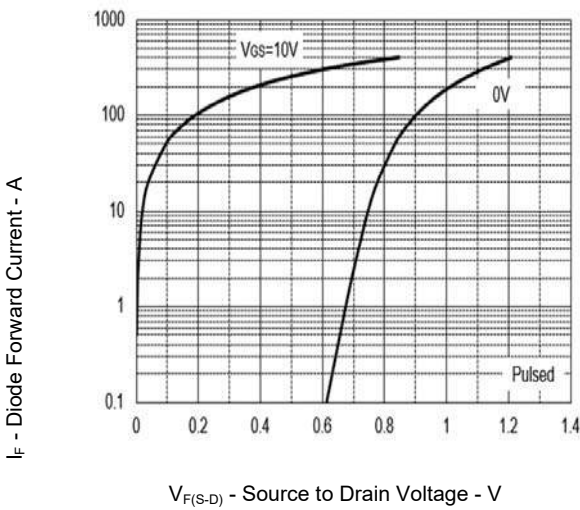
SWITCHING CHARACTERISTICS



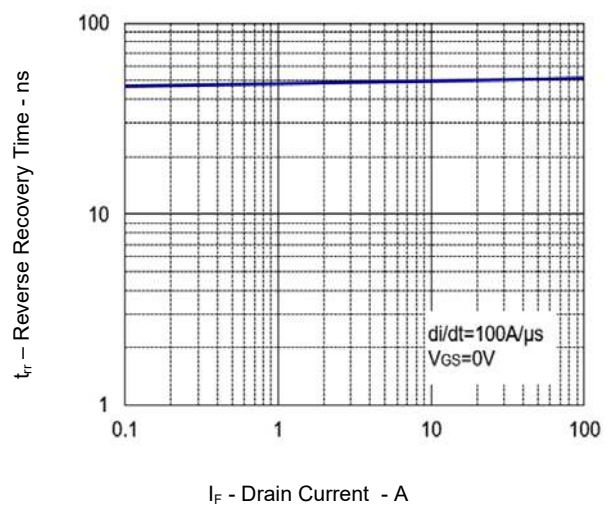
DYNAMIC INPUT CHARACTERISTICS



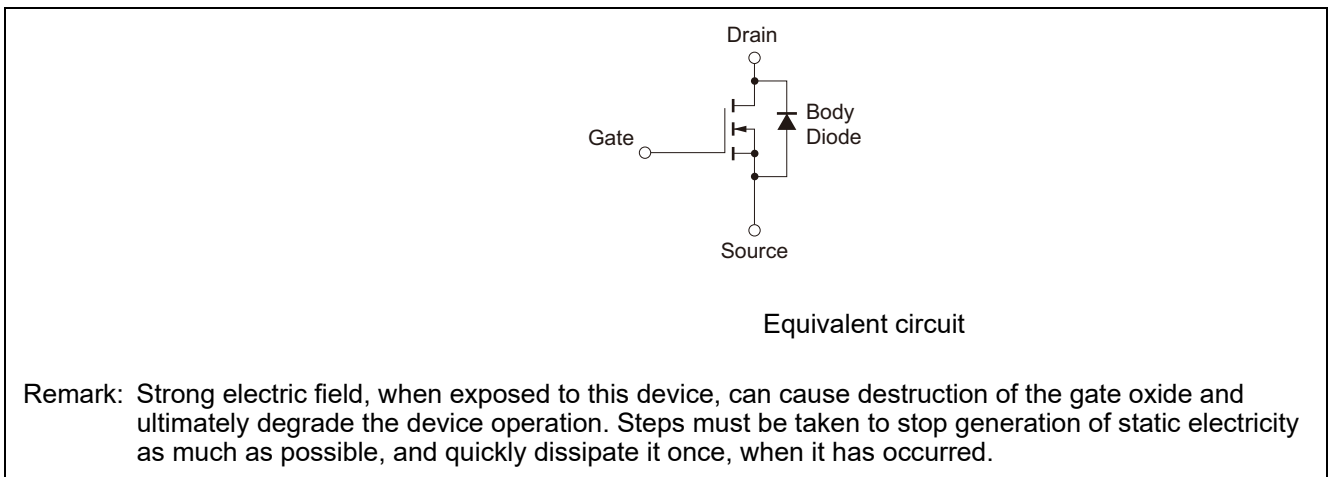
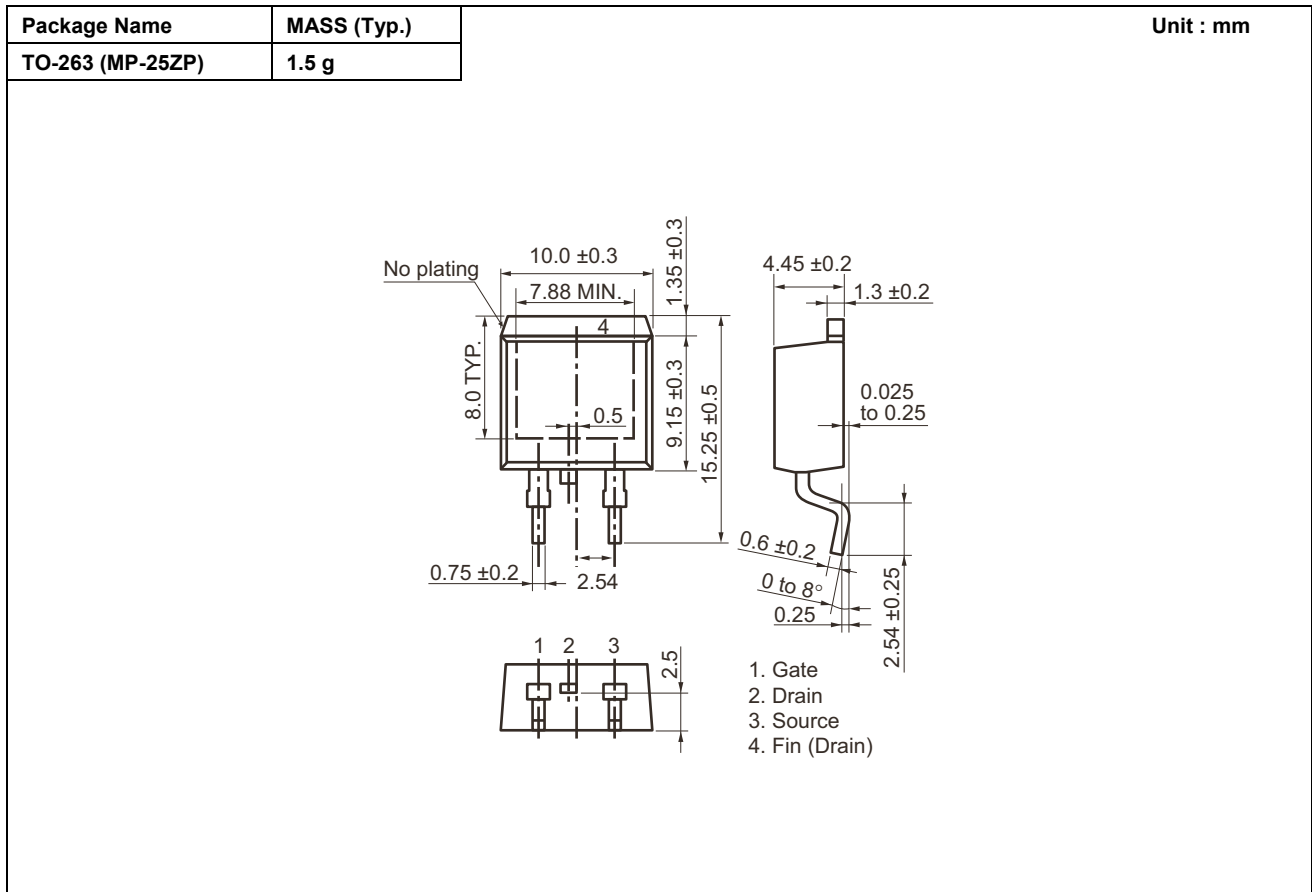
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT



Package Dimensions



<b>Revision History</b>	<b>NP100N04PUK Preliminary Datasheet</b>
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Rev.	Date	Description	
		Page	Summary
0.01	Apr 26, 2010	-	1st edition
2.00	May 24 ,2018	1	Note 3 was added
		2	Note 2 was added

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