AN3028
Application note

EVLVIP16L-4WFN: 16 V / 4.5 W, 60 kHz non-isolated flyback demonstration board using the VIPer16LN

Introduction

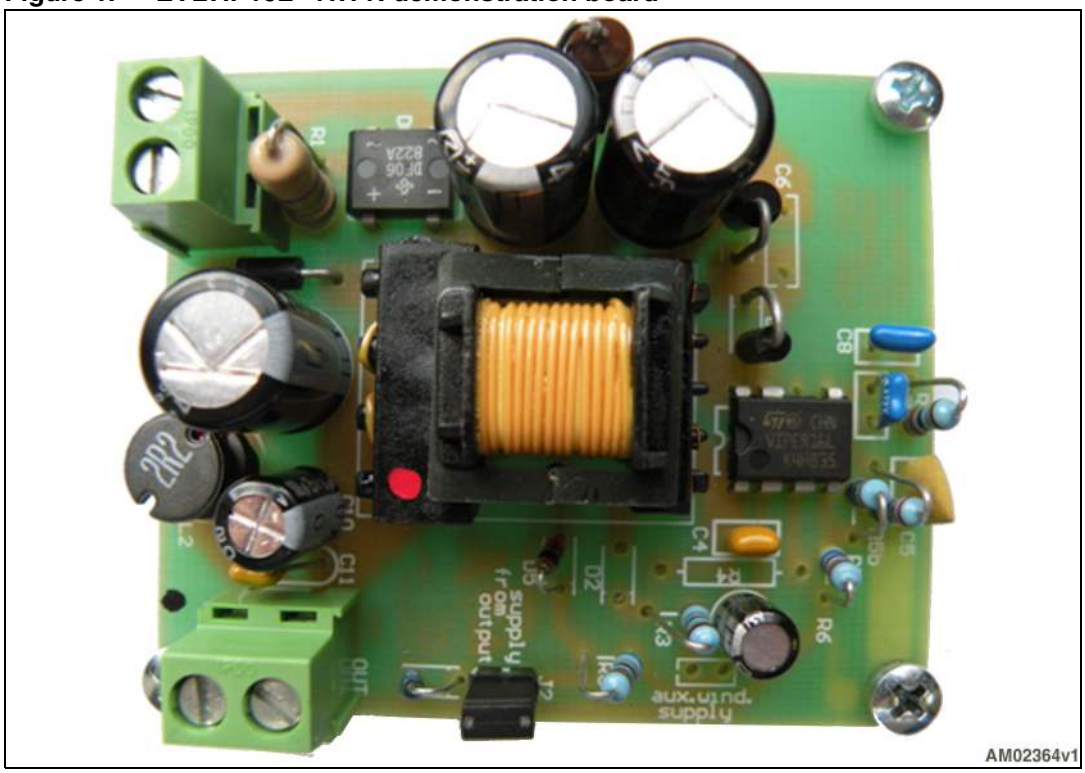
This document describes a 16 V - 280 mA power supply set in non-isolated flyback topology with the VIPer16LN, a new offline high-voltage converter by STMicroelectronics.

The features of the device include an 800 V avalanche rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, current limiting with adjustable setpoint, on-board soft-start, and safe auto-restart after a fault condition.

Moreover, the VIPer16LN can work with or without the auxiliary winding. Operating with the auxiliary winding, it can attain very low standby consumption. Operating without the auxiliary winding, the IC is supplied by an internal current generator, thus saving the cost of the transformer's auxiliary winding. Both possibilities are discussed in this application note.

The protections available include a thermal shutdown with hysteresis, delayed overload protection, and open-loop failure protection (available only if the auxiliary winding is used).

Figure 1. EVLVIP16L- 4WFN demonstration board



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1 Adapter features

The electrical specifications of the demonstration board are listed in *Table 1*.

Table 1. Electrical specifications

Symbol	Parameter	Value
V_{IN}	Input voltage range	[$90V_{RMS}$; $265V_{RMS}$]
V_{OUT}	Output voltage	16 V
I_{OUT}	Max output current	0.28 A
Δ_{VOUT_LF}	Precision of output regulation	±5%
Δ_{VOUT_HF}	High-frequency output voltage ripple	50 mV
T_A	Max ambient operating temperature	60 ºC

2 Circuit description

The power supply is set in flyback topology. The schematic is given in *Figure 2*, the bill of materials in *Table 2*. The input section includes a resistor R1 for inrush current limiting, a diode bridge (D0) and a Pi filter for EMC suppression (C1, L1, C2). The transformer core is a standard E16. A transil clamp network (D1, D4) is used for leakage inductance demagnetization.

The output voltage value is set simply through the R5-R6 voltage divider between the output terminal and the FB pin, according to the following formula:

Equation 1

$$V_{OUT} = 3.3V \cdot \left(1 + \frac{R6}{R5}\right)$$

The FB pin is the inverting input of an error amplifier whose non-inverting input is an accurate 3.3 V voltage reference. In the schematic the resistor R5 has been split into R5a and R5b in order to allow better tuning of the output voltage value. The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin and is made up of C7, C8 and R7.

The output rectifier D3 has been selected according to the calculated maximum reverse voltage, forward voltage drop and power dissipation and is a power Schottky.

The LIM pin has been left open, thus the current limitation is set to the default value, I_{DLIM}. If a lower current limitation is required, a resistor of an appropriate value should be connected between the LIM and GND pins, according to the I_{DLIM} vs. R_{LIM} graphic shown in the VIPer16LN datasheet.

A small LC filter has been added at the output in order to filter the high-frequency ripple without increasing the size of the output capacitors and a 100 nF capacitor has been placed very close to the output connector solder points in order to limit the spike amplitude.

At power-up the DRAIN pin supplies the internal HV startup current generator which charges the C3 capacitor up to V_{DDon}. At this point the power MOSFET starts switching, the generator is turned off, and the IC is powered by the energy stored in C3.

If both the jumpers J and J1 are left open, the VIPer16LN is self-supplied through the internal high-voltage startup current generator, which is turned on as the V_{DD} voltage falls down to V_{DDcs_on} and is switched off as it reaches V_{DDon}.

If the jumper J is selected, the IC is supplied by the auxiliary winding, through D2 and R3. In this case the V_{DD} voltage increases with the load on the regulated output. In order to avoid exceeding the V_{DD} operating range, an external clamp (Dz, Rz) has been added.

If the jumper J2 is selected, the VIPer16LN is supplied from the output through D6. In *Figure 3* the V_{DD} waveforms for both cases (self-supply and supply from the output) are shown. It is worth noting that in the latter case the self-supply is excluded by keeping the V_{DD} voltage always above the V_{DDcs_on} value. This is achievable only if the output voltage is high enough, thus the minimum value which allows this setting to be used is $V_{OUT} \geq V_{DDcs\_on} + Vy6 \approx 12$ V. If the value of V_{OUT} is lower, the self-supply can be excluded only through the auxiliary winding.

Figure 2. Application schematic

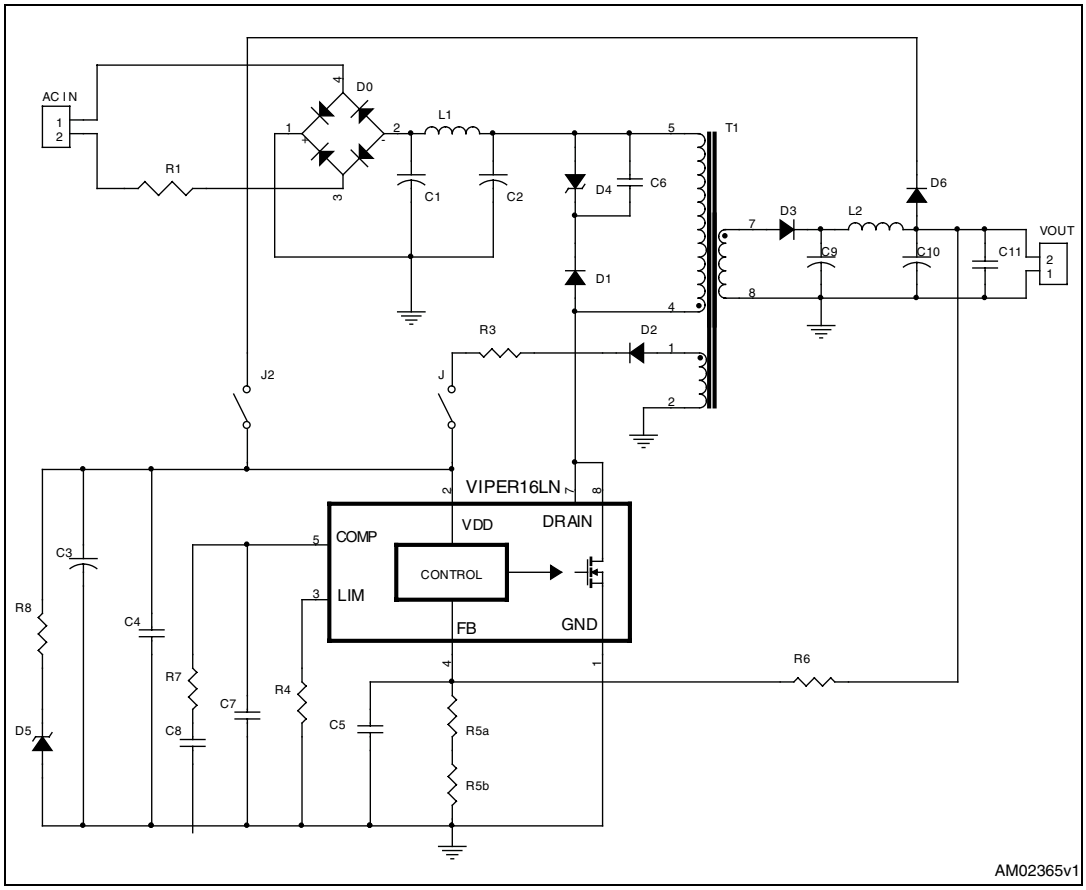


Table 2. Bill of material

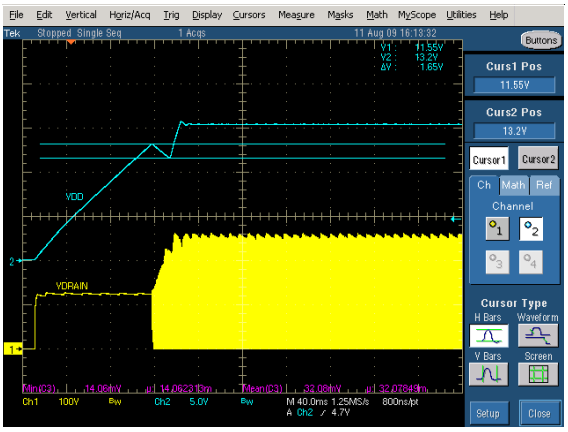
Reference	Part	Description	Manufacturer
C1, C2		4.7 µF, 400 V NHG serie electrolytic capacitor	Panasonic
C3		10 µF, 35 V GA serie electrolytic capacitor	Panasonic
C4, C11		100 nF, 50 V RPER7 serie ceramic capacitor	Murata
C5		150 pF, 100 V 682 serie ceramic capacitor	AVX
C6	Not mounted		
C7		4.7 nF, 50 V B3798x serie ceramic capacitor	EPCOS
C8		150 nF, 50 V B3798x serie ceramic capacitor	EPCOS
C9		470 µF, 25 V ZL serie ultra-low ESR electrolytic capacitor	Rubycon
C10		100 µF, 25 V VR serie electrolytic capacitor	Nichicon
D0	DF06M	600 V 1 A diode bridge	Vishay
D1	STTH1L06	Clamp diode	STMicroelectronics
D2	BAT46	Small signal diode	STMicroelectronics

Table 2. Bill of material (continued)

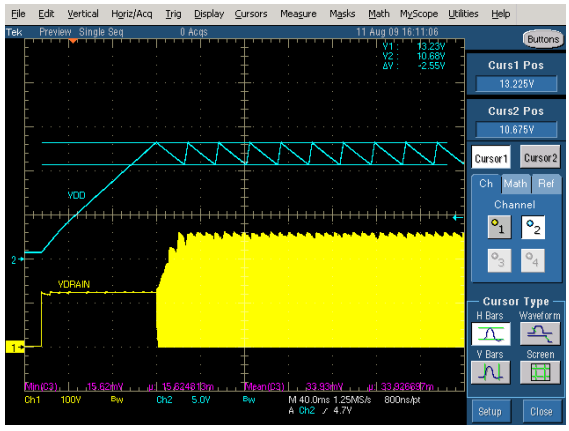
Reference	Part	Description	Manufacturer
D3	STPS2H100	Output diode 2 A, 100 V	STMicroelectronics
D4	P6KE300A	Transil	STMicroelectronics
D5	BZX79-C18	18 V Zener diode	NXP
D6	Not mounted	Small signal diode (1N4148)	
R1		4.7 Ω 3/4 W resistor	
R3		15 Ω 1/4W resistor	
R4	Not mounted		
R5a		10 kΩ 1% 1/4W resistor	
R5b		2.2 kΩ 1% 1/4W resistor	
R6		47 kΩ 1% 1/4W resistor	
R7		33 kΩ 1/4W resistor	
R8		68 kΩ1/4W resistor	
L2	RFB0807-2R2L	2.2 µH power inductor	Coilcraft
J,J2		jumpers	
T1	1335.0062	Transformer	MAGNETICA
IC	VIPer16LN		STMicroelectronics

Figure 3. V_{DD} waveforms

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)



3 Transformer

The characteristics of the transformer are listed in the table below

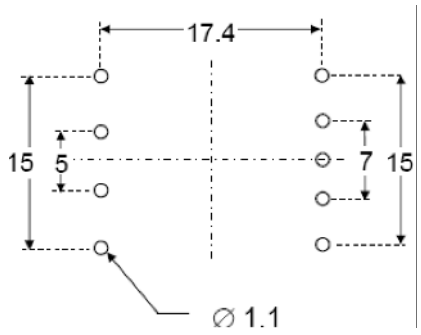
Table 3. Transformer characteristics

Parameter	Test conditions	Value
Manufacturer		MAGNETICA
Part number		1335.0062
Primary inductance	Measured at 1 kHz 0.1 V	1.2 mH ±15%
Leakage inductance	Measured at 10 kHz 0.1 V	2.9%
Primary to secondary turn ratio (4 - 5)/(7, 8)	Measured at 10 kHz 0.1 V	7.85 ±5%
Primary to auxiliary turn ratio (4 - 5)/(1 - 2)	Measured at 10 kHz 0.1 V	7.33 ±5%

The figures below show the size and pin distances (mm) of the transformer.

Figure 4. Transformer size and pin diagram

(a) Pin distances



(b) Electrical diagram

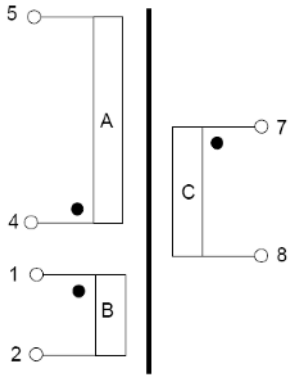
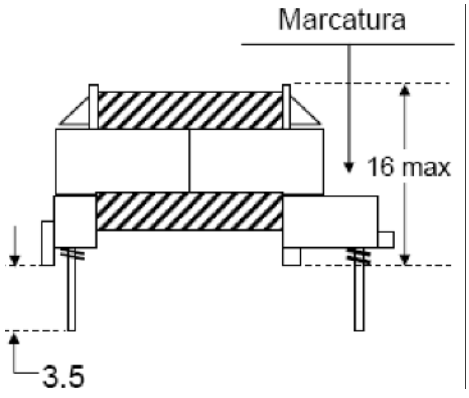
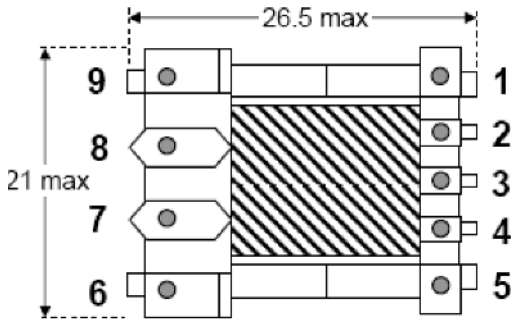


Figure 5. Transformer size

(a) Side view



(b) Terminal view



4 Testing the board

4.1 Typical waveforms

Drain voltage and current waveforms in full-load condition are shown for the two nominal input voltages in *Figure 6* and *7*, and for minimum and maximum input voltage in *Figure 8* and *9* respectively.

Figure 6. Drain current and voltage at max load 115 Vac

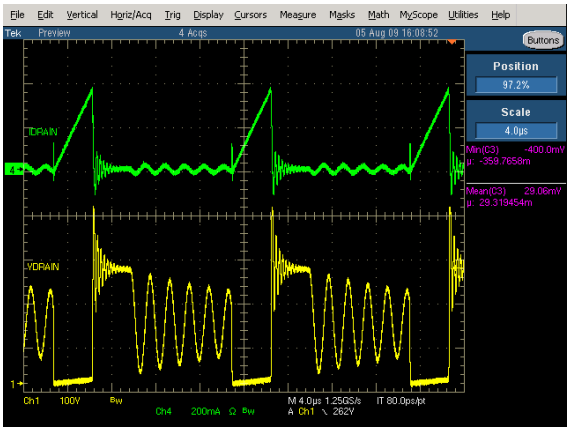


Figure 7. Drain current and voltage at max load 230 Vac

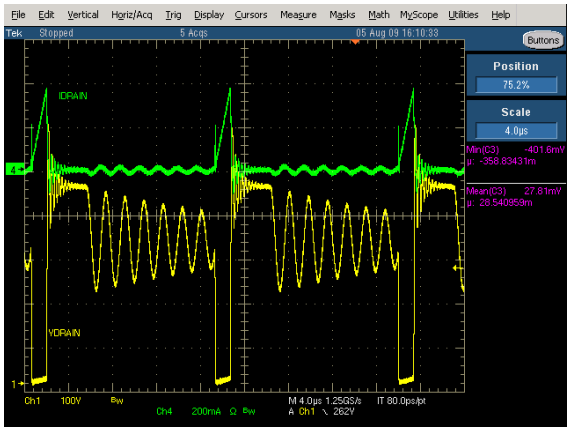


Figure 8. Drain current and voltage at max load 90 Vac

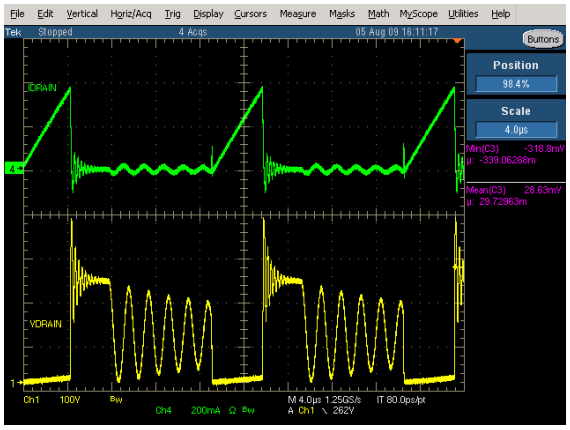
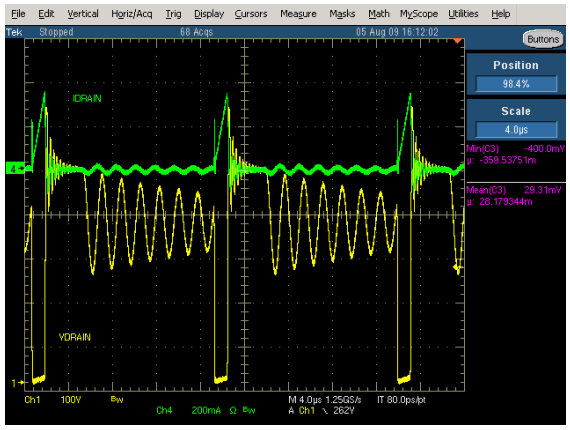


Figure 9. Drain current and voltage at max load 265 Vac



5 Line-load regulation and output voltage ripple

The output voltage of the board has been measured in different line and load conditions. The results are shown in *Table 4*. The output voltage is practically not affected by the line condition and by the IC biasing (self-supply or not).

Table 4. Output voltage line-load regulation

V_{INAC} (V)	Vout							
	No load		50% load		75% load		100% load	
	Without self-supply	With self-supply	Without self-supply	With self-supply	Without self-supply	With self-supply	Without self-supply	With self-supply
90	15.91	15.91	15.72	15.73	15.74	15.75	15.76	15.76
115	15.91	15.92	15.71	15.71	15.72	15.73	15.74	15.73
150	15.91	15.92	15.70	15.70	15.72	15.71	15.72	15.71
180	15.91	15.92	15.69	15.69	15.71	15.70	15.69	15.67
230	15.91	15.92	15.69	15.69	15.67	15.67	15.66	15.65
265	15.91	15.92	15.69	15.69	15.69	15.66	15.65	15.65

Figure 10. Line regulation

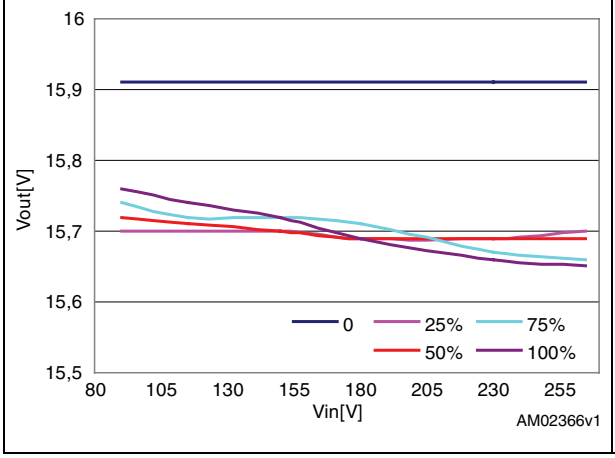
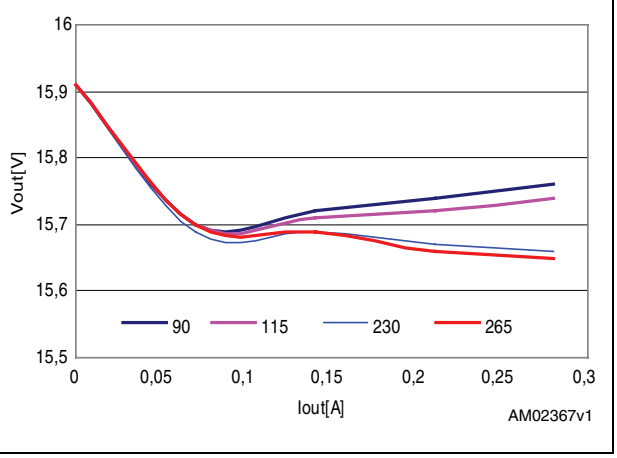


Figure 11. Load regulation



The ripple at the switching frequency superimposed at the output voltage has also been measured and the results are shown in *Table 5*. The board is provided with an LC filter to better filter the voltage ripple.

Table 5. Output voltage ripple at half and full load

V_{INAC} (V)	V_{OUT} (mV)	
	Half load	Full load
90	40	70
115	32	65
230	32	45
265	32	40

Figure 12. Output voltage ripple 115V_{INAC} full load

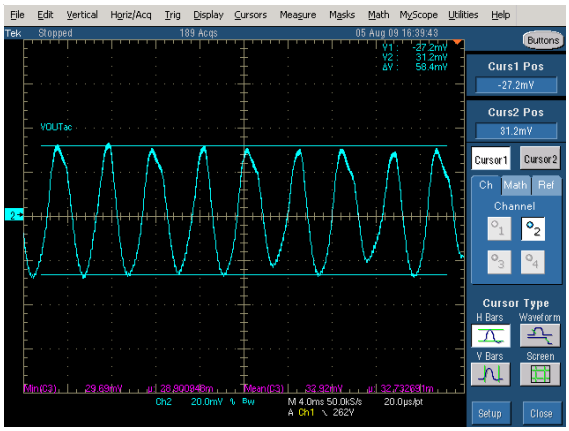
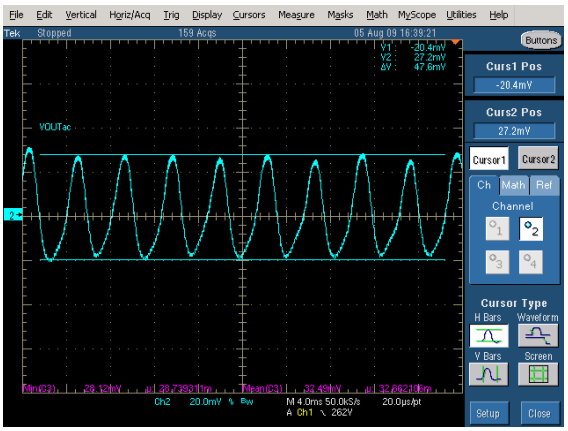


Figure 13. Output voltage ripple 230V_{INAC} full load



6 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold, V_{COMPL} (1.1 V, typical), the switching is disabled and no more energy is transferred to the secondary side. So, the output voltage decreases and the regulation loop makes the COMP pin voltage increase again. As it rises 40mV above the V_{COMPL} threshold, the normal switching operation is resumed. This results in a controlled on/off operation (referred to as “burst mode) as long as the output power is low enough to require a turn-on time lower than the minimum turn-on time of the VIPer16LN. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy-saving regulations.

The figures below show the output voltage ripple when the converter is not loaded or lightly loaded and supplied with 115 V_{AC} and with 230 V_{AC} respectively.

Figure 14. Output voltage ripple at 115 V_{INAC} no load

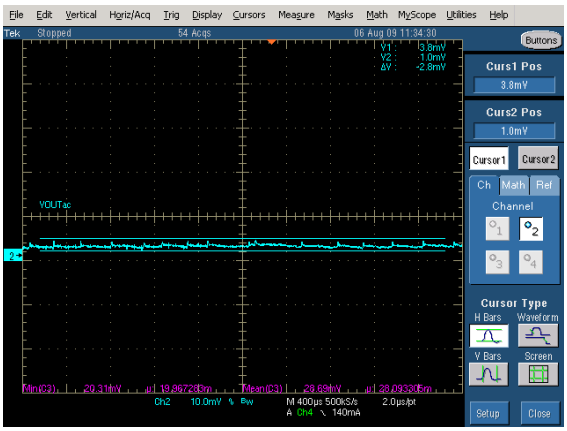


Figure 15. Output voltage ripple at 230 V_{INAC} no load

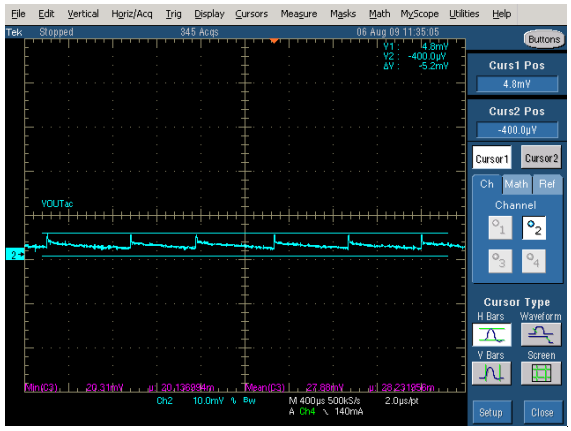


Figure 16. Output voltage ripple at 115V_{INAC} 25 mA

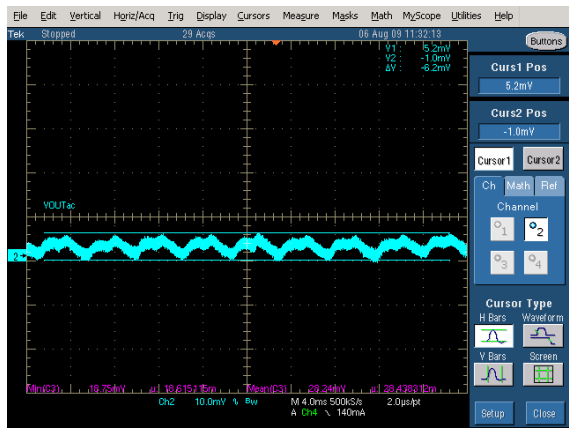


Figure 17. Output voltage ripple at 230V_{INAC} 25 mA

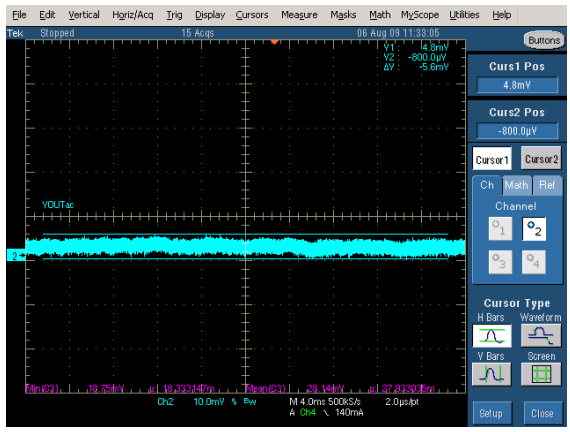


Table 6 shows the measured value of the burst mode frequency ripple measured in different operating conditions. The output voltage ripple in burst mode operation is very low.

Table 6. Output voltage ripple at no load and light load

V_{INAC} (V)	V_{OUT} (mV)	
	No load	25 mA load
90	2	7
115	2	7
230	4	8
265	4	9

6.1 Efficiency

The efficiency of the converter has been measured in different load and line voltage conditions, both with and without the self-supply function.

According to the ENERGY STAR® average active mode testing efficiency method, the efficiency measurements have been done at full load and at 75%, 50% and 25% of full load for different input voltages. The results are given in *Table 7*.

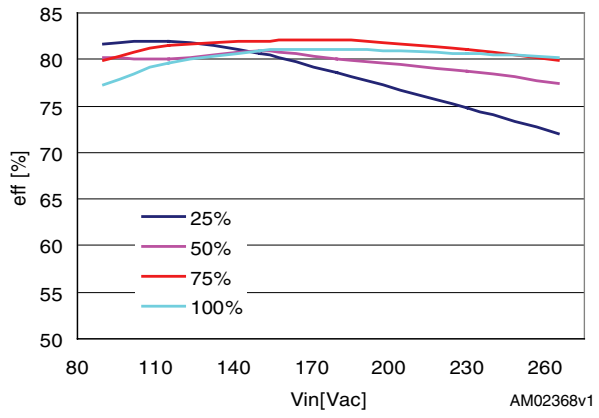
Table 7. Efficiency

V_{INAC} (V)	Efficiency (%)							
	Full load		75% load		50% load		25% load	
	Without self-supply	With self-supply	Without self-supply	With self-supply	Without self-supply	With self-supply	Without self-supply	With self-supply
90	77.94	75.38	79.83	76.85	81.20	76.22	81.59	72.25
115	80.20	77.31	81.43	77.81	81.15	76.16	81.89	70.63
150	81.59	77.98	81.94	77.31	81.94	74.84	80.63	67.63
180	81.70	77.51	82.11	76.61	81.10	73.22	78.62	64.68
230	81.32	76.14	81.06	74.58	79.80	70.18	74.82	59.82
265	80.81	74.94	79.95	72.89	78.50	67.96	72.07	56.32

For better visibility of the results they have also been plotted in the following figures. In *Figure 18* the efficiency versus V_{IN} for the four different load values is plotted. In *Figure 19* the efficiency as a function of the load is shown for different values of the input voltage.

Figure 18. Efficiency vs. V_{IN}

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)

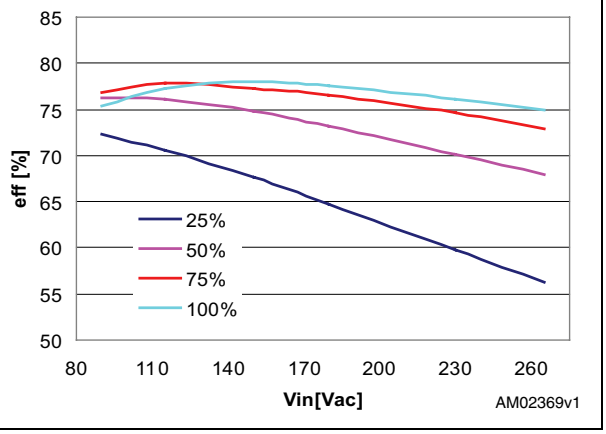
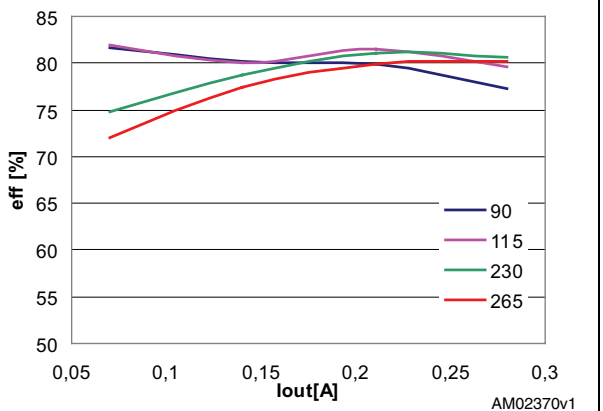
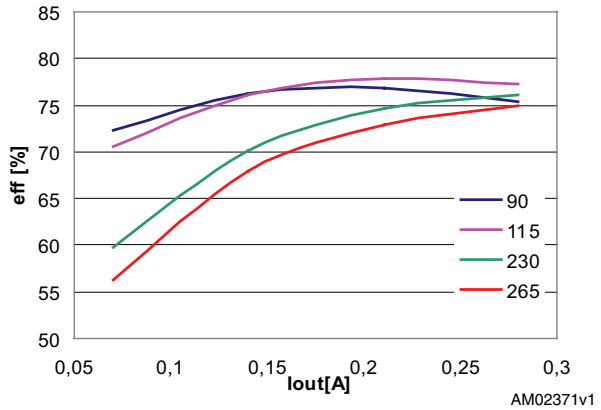


Figure 19. Efficiency vs. load

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)



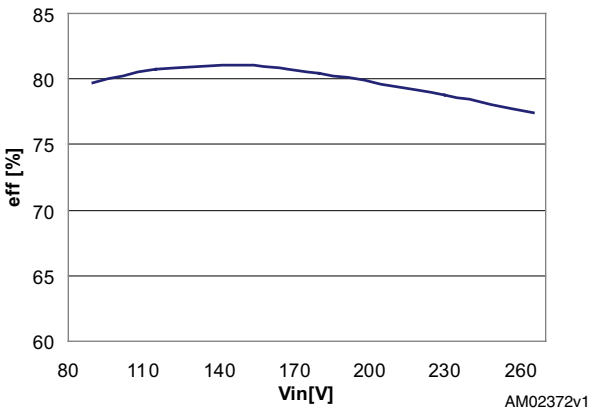
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load. *Table 8* gives the active mode efficiency calculated from the values in *Table 7*. For clarity the values from *Table 8* are plotted in *Figure 20*.

Table 8. Active mode efficiencies

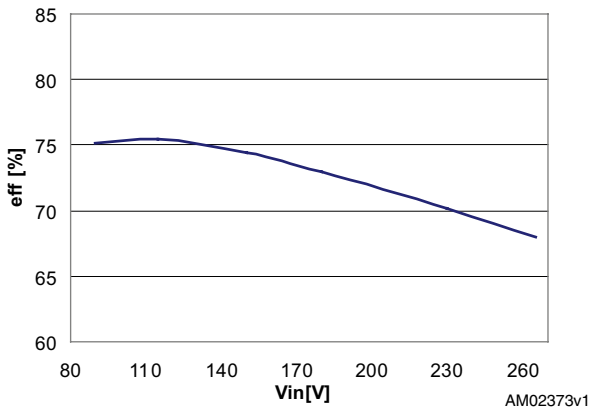
V_{INAC} (V_{RMS})	Active mode efficiency (%)	
	Without self-supply	With self-supply
90	79.72	75.18
115	80.75	75.48
150	81.09	74.44
180	80.46	73.00
230	78.83	70.18
265	77.42	68.03

Figure 20. Active mode efficiency vs. V_{IN}

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)



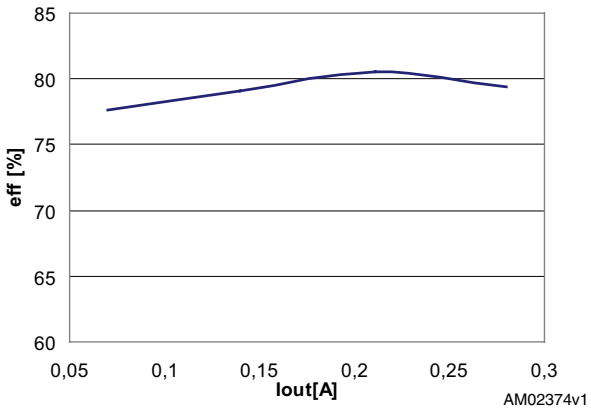
In *Table 9* and *Figure 21* the averaged value of the efficiency versus load is given (the average has been done considering the efficiency at different values of the input voltage).

Table 9. Line voltage averaged efficiency vs. load

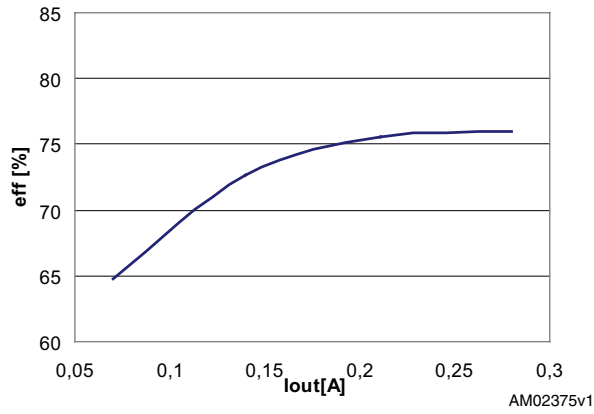
Load (% of full load)	Efficiency (%)	
	Without self-supply	With self-supply
100	79.43	75.94
75	80.57	75.53
50	79.12	72.63
25	77.59	64.76

Figure 21. Input voltage averaged efficiency vs. load

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)



In the version 2.0 of the ENERGY STAR® program requirement for single voltage external AC-DC power supplies (see *References*), the power supplies are divided in two categories: low-voltage power supplies and standard power supplies with respect to the nameplate output voltage and current. An external power supply, in order to be considered a low-voltage power supply, needs to have a nameplate output voltage lower than 6 V and a nameplate output current greater than or equal to 550 mA.

The tables below show the EPA energy efficiency criteria for AC-DC power supplies in active mode for standard models and for low voltage models respectively.

Table 10. Energy efficiency criteria for standard models

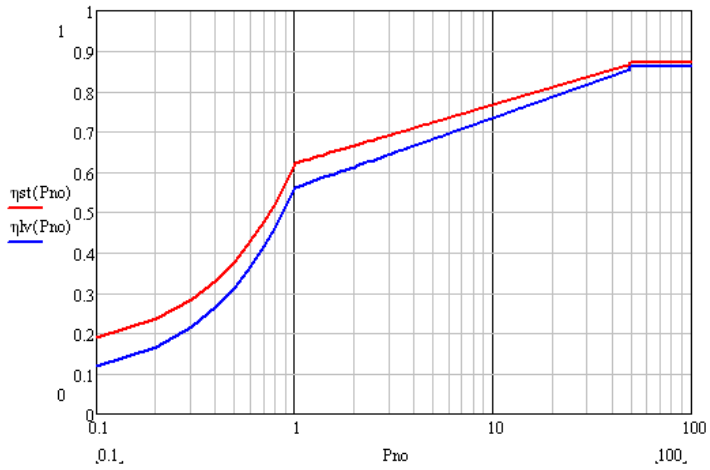
Nameplate output power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)
0 to = 1 watt	= 0.48*Pno+0.140
> 1 to = 49 watts	= [0.0626 * ln (P_{no})] + 0.622
> 49 watts	= 0.870

Table 11. Energy efficiency criteria for low-voltage models

Nameplate output power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)
0 to = 1 watt	= 0.497 *Pno+0.067
> 1 to = 49 watts	= [0.075 * ln (Pno)] + 0.561
> 49 watts	= 0.860

The criteria are plotted in *Figure 22*, where the red line is the criteria for the standard model and the blue line is the criteria for the low-voltage model. The P_{NO} axe is in logarithmic scale.

Figure 22. ENERGY STAR® efficiency criteria



The power supply presented is from a standard model and, in order to be compliant with the ENERGY STAR® requirements, needs to have efficiency higher than 71.6%. If the self-supply is excluded, the efficiency results (see *Table 9*) are higher than the recommended value within the whole input voltage range.

6.2 Light-load performance

The input power of the converter has been measured in no-load condition for different input voltages and the results are given in *Table 12*.

Table 12. No-load input power

V_{IN_AC} (VRMS)	P_{IN} (mW)	
	Without self-supply	With self-supply
90	21	88
115	22	110
150	25	146
180	26	175
230	29	224
265	32	258

In version 2.0 of the ENERGY STAR® program the power consumption of the power supply when it is not loaded is also considered. The criteria for compliance are given in the table below:

Table 13. Energy consumption criteria for no load

Nameplate output power (P_{no})	Maximum power in no load for AC-DC EPS
0 to = 50 watt	< 0.3 watts
> 50 watts < 250 watts	< 0.5 watts

The performance of the presented board (when the self-supply function is not used) is much better than required, the power consumption is about ten times lower than the ENERGY STAR® limit. Even if the performance seems to be disproportionally better than the requirements, it is worth noting that often the AC-DC adapter or battery charger manufacturers have very strict requirements about no-load consumption and when the converter is used as an auxiliary power supply, the line filter is often the main line filter of the entire power supply that considerably increases standby consumption.

Even if the ENERGY STAR® program does not have other requirements regarding light-load performance, in order to give complete information we also show the input power and efficiency of the demonstration board in two other low-load cases. *Table 14* and *15* show the performance when the output load is 25 mW and 50 mW respectively.

Table 14. Low-load performance, P_{OUT} = 25 mW

V_{IN_AC}	P_{OUT} (mW)	P_{IN} (mW)		efficiency (%)	
		Without self-supply	With self-supply	Without self-supply	With self-supply
90	25	56.00	124	44.64	20.16
115	25	58.46	149	42.76	16.78
150	25	62.23	185	40.17	13.51
180	25	62.77	213	39.83	11.72
230	25	65.63	262	38.09	9.56
265	25	67.51	296	37.03	8.44

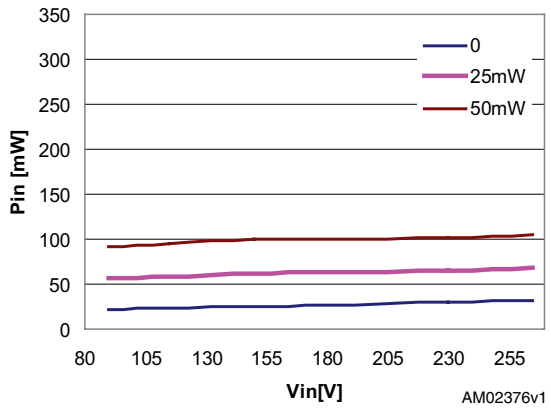
Table 15. Low-load performance, P_{OUT} = 50 mW

V_{IN_AC}	P_{OUT} (mW)	P_{IN} (mW)		efficiency (%)	
		Without self-supply	With self-supply	Without self-supply	With self-supply
90	50	91	161	54.55	31.09
115	50	94	187	52.98	26.74
150	50	100	224	50.00	22.30
180	50	100	252	50.00	19.84
230	50	102	300	48.88	16.67
265	50	105	335	47.62	14.95

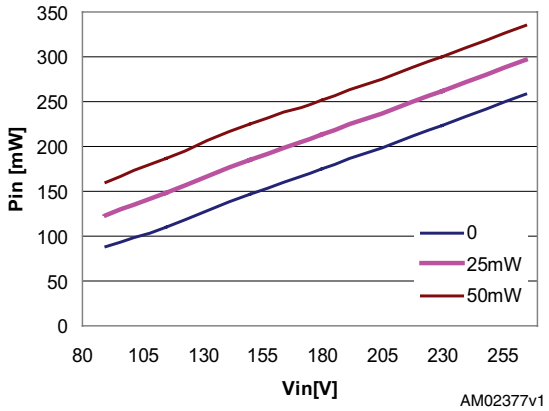
The input power vs. input voltage for no-load and low-load condition (*Table 12*, *14* and *15*) are shown in the figures below.

Figure 23. P_{IN} vs. V_{IN} at P_{OUT} = 0; 25 mW; 50 mW

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)



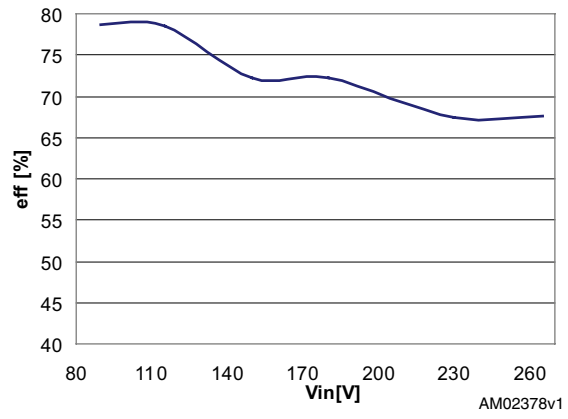
Depending on the equipment supplied, we can have several criteria to measure the standby or light-load performance of a converter. One criterion is the measure of the output power when the input power is equal to one watt. In *Table 16* the output power needed to have 1 W of input power in different line conditions is given. *Figure 24* shows the output power corresponding to P_{IN} = 1 W for different values of the input voltage.

Table 16. P_{OUT} at P_{IN} = 1 W

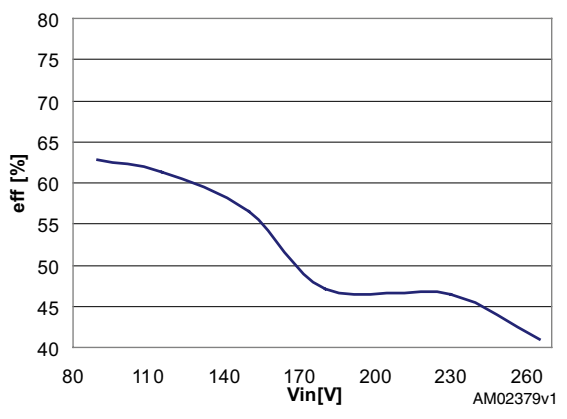
V_{IN_AC}	P_{IN} (W)	P_{OUT} (W)		efficiency (%)	
		Without self-supply	With self-supply	Without self-supply	With self-supply
90	1	0.786	0,629	78.66	62,88
115	1	0.786	0,613	78.56	61,27
150	1	0.722	0,566	72,27	56,52
180	1	0.722	0,471	72,27	47,10
230	1	0.675	0,464	67,51	46,40
265	1	0.677	0,410	67,68	41,03

Figure 24. P_{OUT} at P_{IN} = 1 W

a) without self-supply (J2 selected)



b) with self-supply (J and J2 not selected)



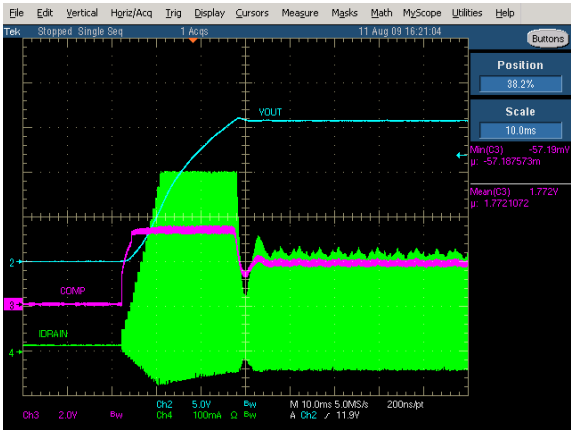
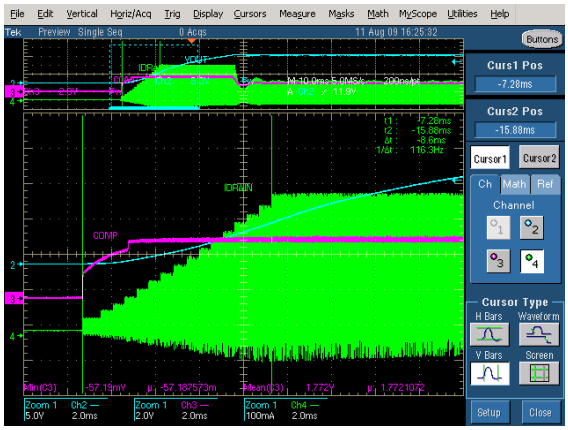
7 IC features

7.1 Soft-start

At startup the current limitation value reaches I_{DLIM} after an internally set time, t_{SS}, whose typical value is 8.5 msec. This time is divided into 16 time intervals, each corresponding to a current limitation step progressively increasing. In this way the drain current is limited during the output voltage increase, thus reducing the stress on the secondary diode.

The soft-start phase is shown in *Figure 25*.

Figure 25. Soft-start

a) soft-start at startup	b) soft-start at startup (zoom)
	

7.2 Overload protection

In case of overload or short-circuit (see *Figure 26* a), the drain current reaches the I_{DLIM} value (or the one set by the user through the R_{LIM} resistor). Every cycle that this condition is met, a counter is incremented. If it is maintained continuously for the time t_{OVL} (50 msec typical, set internally), the overload protection is tripped, the power section is turned off, and the converter is disabled for a $t_{RESTART}$ time (1 sec typical). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (*Figure 26* b). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low-power throughput and avoids overheating the IC in case of repeated overload events.

Moreover, every time the protection is tripped, the internal soft-start function is invoked (*Figure 27*a), in order to reduce the stress on the secondary diode.

After the short removal, the IC resumes working normally. If the short is removed during t_{SS} or t_{OVL}, i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (*Figure 27*b).

Figure 26. Output short applied and OLP in steady-state

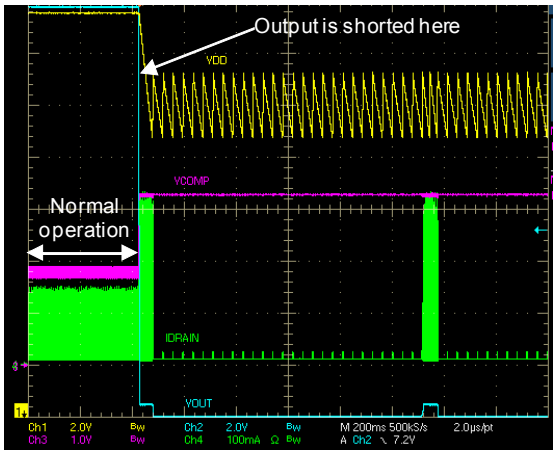
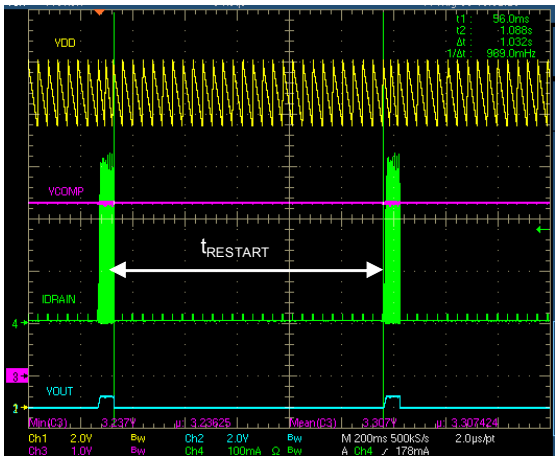
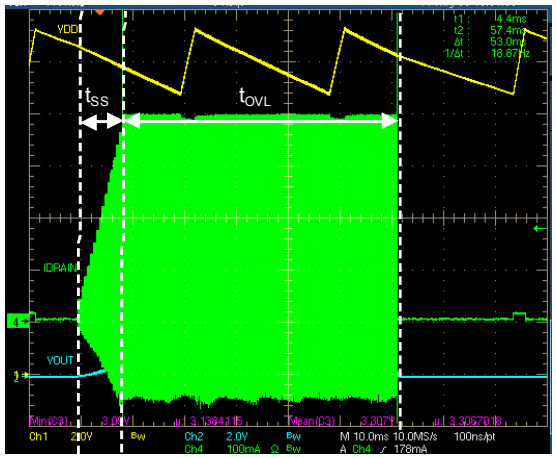
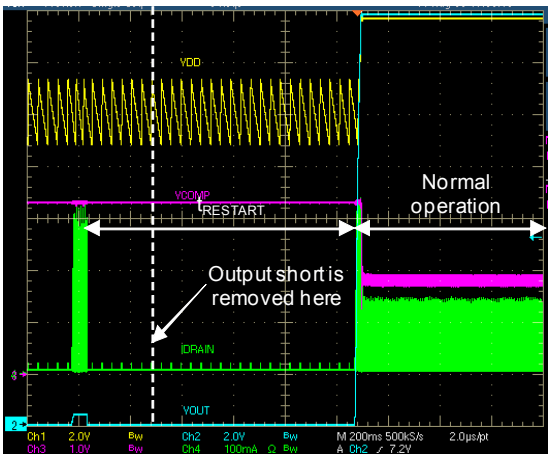
a) short-circuit applied: OLP tripping	b) short-circuit maintained: OLP auto-restart and $t_{RESTART}$
	

Figure 27. OLP in steady-state and output short removed

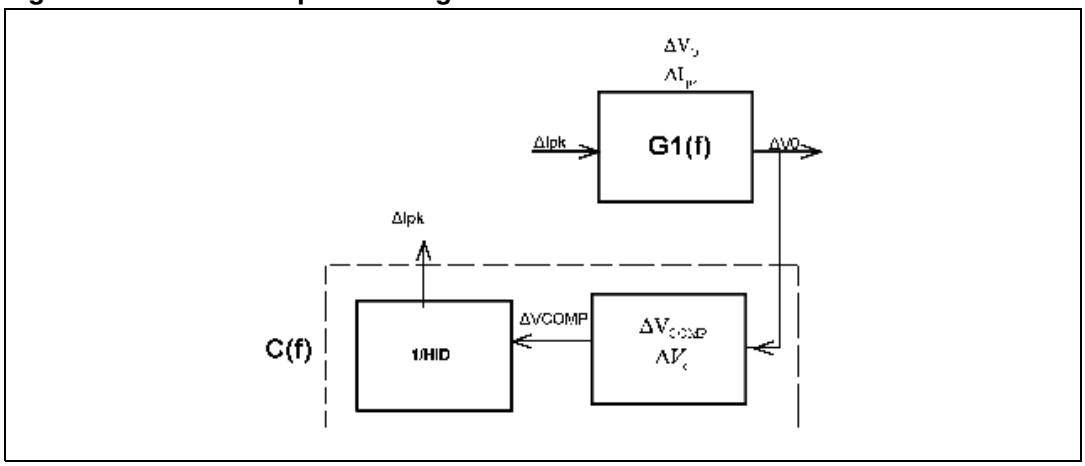
a) short-circuit maintained: soft-start and t_{OVL}	b) short-circuit removed: OLP auto-restart
	

8 Guidelines for feedback loop calculation

8.1 Transfer function

The set PWM modulator + power stage is referred to as the “power plant” and is indicated by G1(f), while C(f) is the “controller”, i.e. the network which is in charge of ensuring the stability of the system.

Figure 28. Control loop block diagram



The mathematical expression of the power plant G1(f) is the following:

Equation 2

$$G_1(f) = \frac{\Delta V_O}{\Delta I_{pk}} = \frac{Vo \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p})} = \frac{Vo \cdot (1 + \frac{j \cdot f}{fz})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot f}{fp})}$$

where fp is the pole due to the output load and fz the zero due to the ESR of the output capacitor:

Equation 3

$$fp = \frac{1}{\pi \cdot C_{OUT} \cdot (R_{OUT} + 2ESR)}$$

Equation 4

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR}$$

The mathematical expression of the compensator C(f) is:

Equation 5

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_o} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{2 \cdot \pi \cdot f \cdot j \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where:

Equation 6

$$Co = -\frac{Gm}{C7 + C8} \cdot \frac{R5}{R5 + R6}$$

Equation 7

$$fZc = \frac{1}{2 \cdot \pi \cdot R7 \cdot C8}$$

Equation 8

$$fPc = \frac{C7 + C8}{2 \cdot \pi \cdot R7 \cdot C7 \cdot C8}$$

are chosen in order to ensure the stability of the overall system.

Gm = 2 mA/V (typical) is the VIPer16LN transconductance.

8.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency, for instance:

fZc = fp/2

fPc = fz

fcross = 4kHz = fsw/10

G1(cross) can be calculated from *Equation 2* and since by definition it is |C(*fcross*)*G1(*fcross*)|= 1, C_0 can be calculated as follows:

Equation 9

$$C_0 = \frac{\left|2 \cdot \pi \cdot fcross \cdot j\right| \cdot \left|1 + \frac{fcross \cdot j}{fPc}\right|}{\left|1 + \frac{fcross \cdot j}{fZc}\right|} \cdot \frac{H_{ID}}{\left|G1(fcross)\right|}$$

At this point the Bode diagram of G1(f)*C(f) can be plotted in order to check the phase margin for the stability.

If the margin is not high enough, another choice should be done for fZc, fPc and fcross, and the procedure repeated.

When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated using the formulas below, as follows:

Equation 10

$$R5 = \frac{R6}{\frac{Vout}{3.3} - 1}$$

Equation 11

$$C7 = \frac{fZc}{fPc} \cdot \frac{Gm}{|C0|} \cdot \frac{R5}{R5 + R6}$$

Equation 12

$$C8 = C7 \cdot \left(\frac{fPc}{fZc} - 1 \right)$$

Equation 13

$$R7 = \frac{C7 + C8}{2 \cdot \pi \cdot fPc \cdot C7 \cdot C8}$$

9 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for the 115 VAC mains input, full-load condition, both with and without the self-supply function. The results are shown in *Figure 29* and *30* and summarized in *Table 17*.

It is worth noting that when the self-supply function is used, the VIPer16LN temperature is higher, due to the power dissipated by the HV startup generator.

Figure 29. Thermal measurements at 115Vac, no self-supply

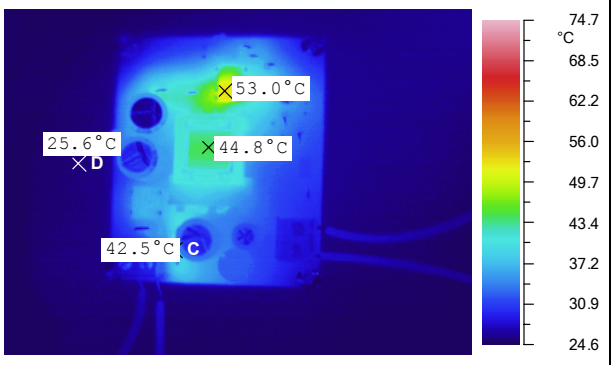


Figure 30. Thermal measurements at 115Vac, self-supply

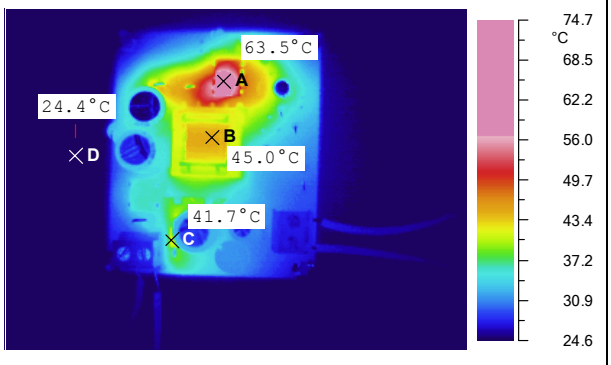


Table 17. Temperature of key components at 115 Vac full load

Point	Temperature [°C]		Reference
	Without self-supply	With self-supply	
A	44.8	45.8	Transformer
B	42.5	41.7	Output diode
C	53.0	63.5	VIPer16LN
D	25.6	24.4	Ambient temperature

10 EMI measurements

Pre-compliance tests to EN55022 (Class B) European normative have been performed using an EMC analyzer and an LISN.

The quasi-peak and average EMC measurements at 230 Vac full load have been performed and the results are shown in *Figure 31* and *Figure 32* respectively.

Figure 31. Quasi-peak measurement at 230Vac, full load

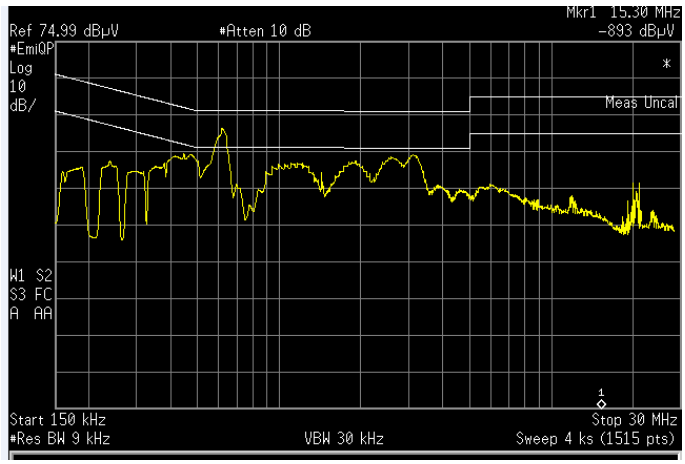
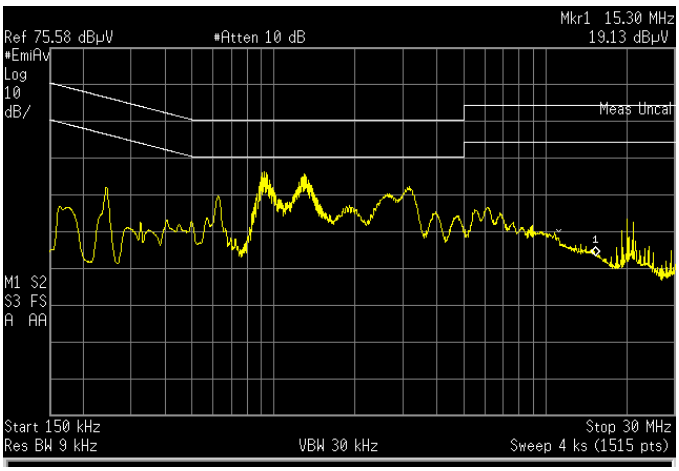
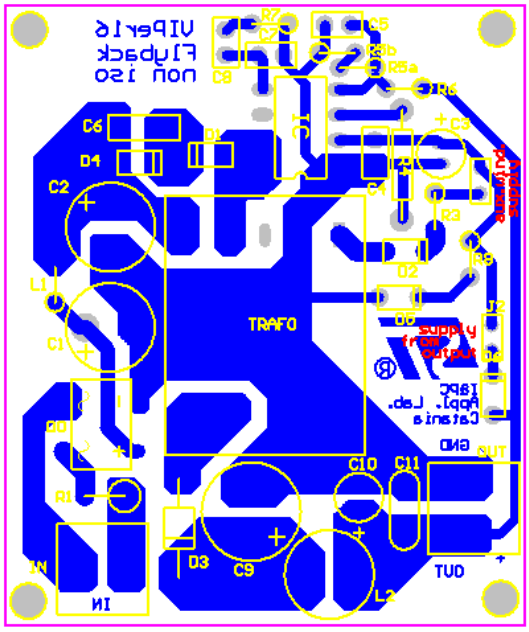


Figure 32. Average measurement at 230Vac, full load



11 Board layout

Figure 33. Bottom layer



12 Conclusions

The VIPer16LN allows a simple design of a non-isolated converter with few external components. In this document a non-isolated flyback has been described and characterized. Special attention has been given to low-load performance and the bench results were good with very low input power in light-load condition. The efficiency has been compared to the requirements of the ENERGY STAR® program (version 2.0) for an external AC/DC adapter with very good results in that the measured active mode efficiency is always higher with respect to the minimum required.

Appendix A Test equipment and measurement of efficiency and low-load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

Figure 34 shows how the wattmeter is connected to the UUT (Unit Under Test) and to the AC source and the wattmeter internal block diagram.

An electronic load has been connected to the output of the power converter (UUT), allowing to set and measure the converter's load current, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage.

The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter's efficiency which has been measured in different input/output conditions.

A.1 Measuring input power

With reference to *Figure 34*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch in *Figure 34* is in position 1 (see also the simplified scheme of *Figure 35*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in low-load condition). In case of high UUT input current, the voltage drop can be relevant (compared to the UUT real input voltage). If this is the case, the switch in *Figure 34* can be changed to position 2 (see simplified scheme of *Figure 36*) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

The voltage across the voltmeter causes a leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance). If the switch of *Figure 34* is in position 2 (see simplified scheme of *Figure 36*), the voltmeter leakage current is measured by the ammeter together with the UUT input current, causing a measurement error. The error is negligible if the UUT input current is much higher than the voltmeter leakage. If the UUT input current is low and not much higher than the voltmeter leakage current, it is probably better to set the switch of *Figure 34* to position 1.

If we are not sure which measurement scheme has the lesser effect on the result, we can try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at

least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period.

If AC input power is not stable over a 5-minute period, the average power or accumulated energy shall be measured over time for both AC input and DC output.

Some wattmeter models allow integrating the measured input power in a time range and then measuring the energy absorbed by the UUT during the integration time. The average input power is calculated by dividing by the integration time itself.

Figure 34. Connections of the UUT to the wattmeter for power measurements

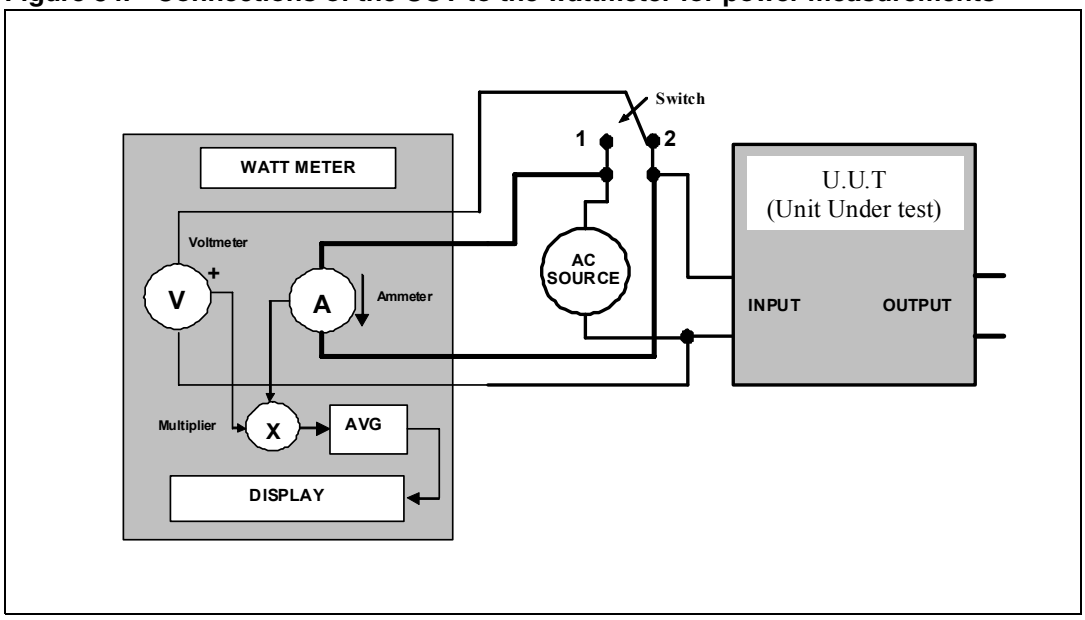


Figure 35. Switch in position 1 - setting for standby measurements

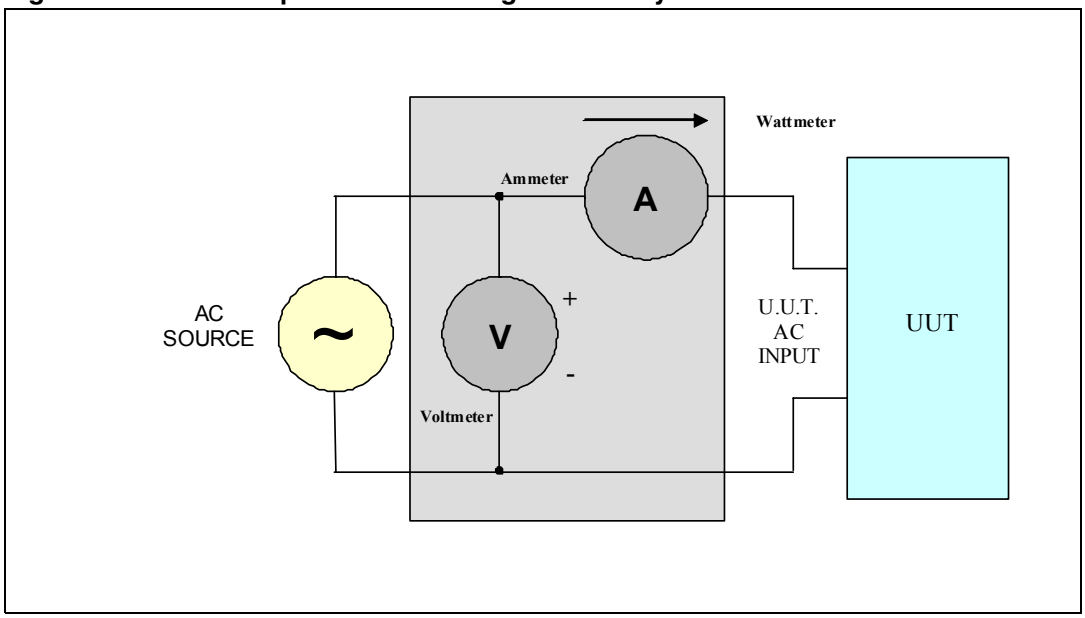
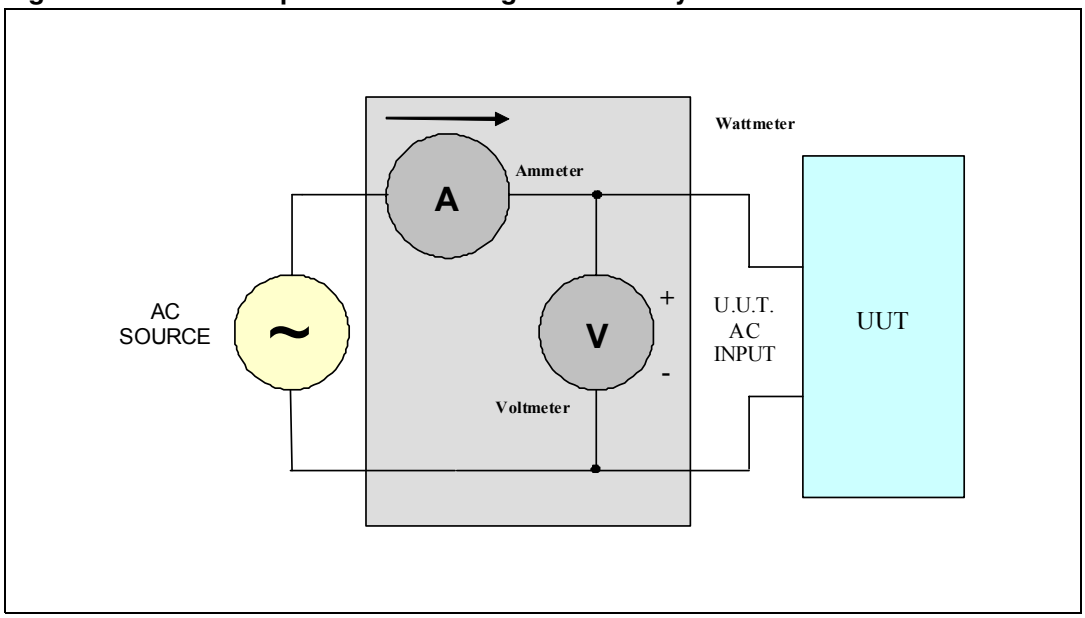


Figure 36. Switch in position 2 - setting for efficiency measurements



References

1. ENERGY STAR® program requirements for single voltage external AC/DC adapter (Version 2.0)
2. VIPer16 datasheet

Revision history

Table 18. Document revision history

Date	Revision	Changes
01-Aug-2011	1	Initial release