Power Charge Pump and Low Drop Voltage Regulator TLE 4307

Power Charge Pump Circuit Features

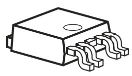
- High Current Capability
- Short Circuit Protection
- Overtemperature Protection
- Active Zener Circuit

Very Low Drop Voltage Regulator Features

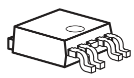
- 3.3 V or 3.8 V output voltage
- Low Output Voltage Tolerance
- High Current Capability 800 mA
- Short Circuit Protection
- Overtemperature Protection

General Features

- Optimized SMD Package
- Industrial type



P-TO252-5-1



P-TO252-5-11

Functional Description

The TLE 4307 is a monolithic integrated power charge pump with a Low Drop Voltage Regulator. The power charge pump loads an energy storage capacitor at pin C. The voltage regulator supplies 3.3 V or 3.8 V out of this storage capacitor with up to 800 mA output current. The TLE 4307 is intended for use with DC supplies for consumer or industrial applications.

Type	Ordering Code	Package
TLE 4307 DV33	Q67006-A9444	P-TO252-5-1, P-TO252-5-11
TLE 4307 DV38	Q67006-A9415	P-TO252-5-1, P-TO252-5-11

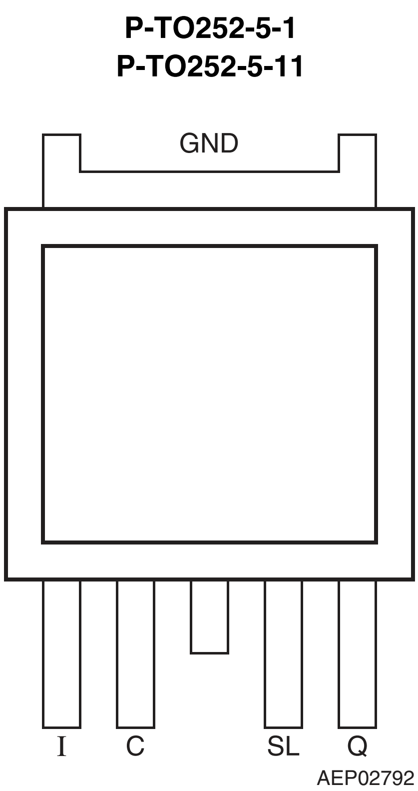


Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	I	**Input;** Connect to the input voltage source
2	C	**Charge-Pump Output;** Connect to the energy reservoir capacitor to GND
3	GND	**Ground**
4	SL	**Slewrate Control Input;** a capacitor from this pin to the Input pin I controls the slewrate during recirculation
5	Q	**Regulator Output;** connect to GND with a capacitor as specified for C_Q

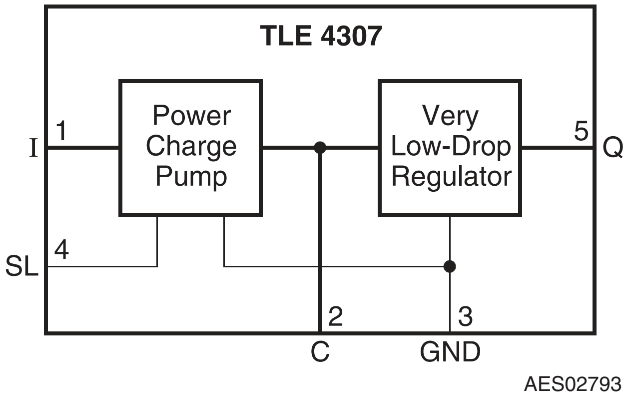


Figure 2 Block Diagram

Circuit Description

The TLE 4307 consists of 2 stages, the charge pump and the very low drop voltage regulator.

Charge Pump

The power stage is used as a switching element, that is driven by a buffer. A current source keeps the power stage on. When the output C of the charge pump reaches $V_{C,off}$, the power stage is switched off. It is active clamped, when the input I reaches $V_{I,cl}$. Optional, an external capacity can be connected between pin SL and I to limit the slew rate at the input, when an inductive load drives the IC. Saturation control as a function of the load current prevents any oversaturation of the power element. The regulator is additionally protected against overload and overtemperature.

Very Low Drop Regulator

The control amplifier compares a reference voltage, made highly accurate by resistance balancing, with a voltage proportional to the output voltage and drives the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The regulator is additionally protected against overload and overtemperature.

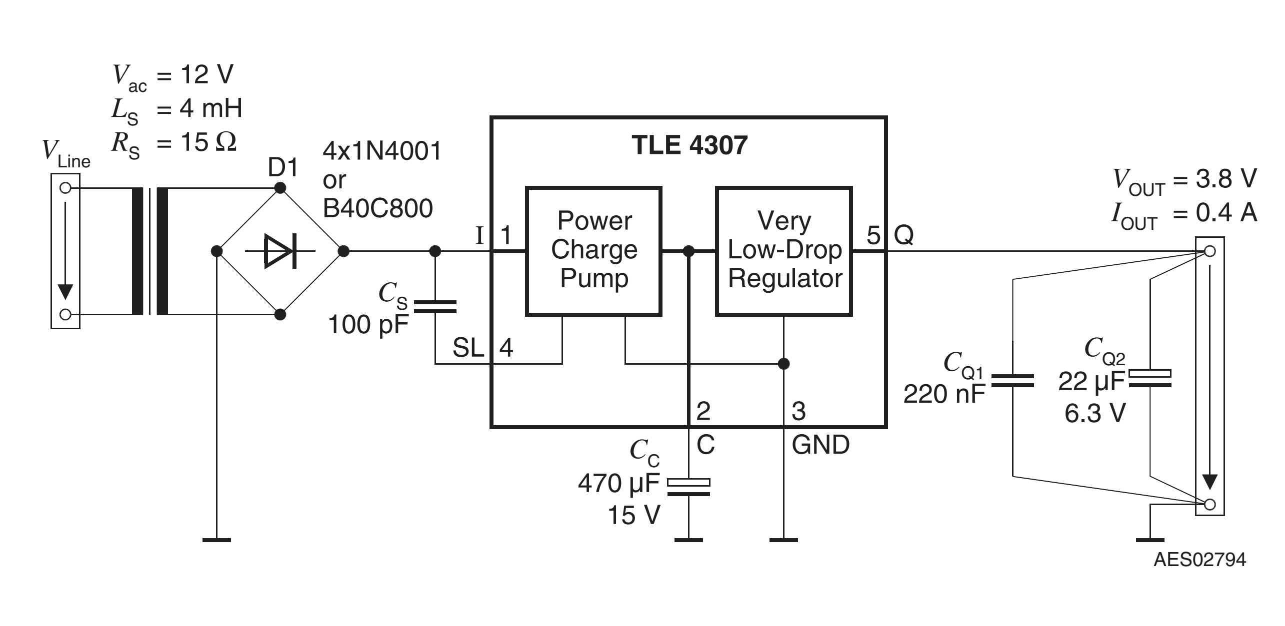


Figure 3 Application Example

Application Description

The IC is meant to be used with a DC power supply. The power charge pump limits the energy that is needed to drive the load at the output Q of the IC. The energy is stored to a capacity C_C, connected to pin C. When pin C reaches $V_{C,off}$, the power charge pump is switched off. Since the power supply consists of the inductance and a parasitic series resistance, the remaining available energy is dissipated in the external power supply and therefore does not stress the IC with this dispensable energy. The very low drop regulator is provided with the energy, stored in C_C. The regulator requires an output capacitor C_Q for the stability of the regulating circuit. Stability is guaranteed at values above 22 µF and an ESR ≤ 1 Ω within the operating temperature range.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input					
Input voltage	V_I	-0.3	V_{ICL}	V	V_{ICL} = Zener clamp voltage
Input current (during pump cycle)	I_I	-5	–	mA	internally limited
Input current (during active Zener operation)	I_I	-5	1000	mA	t_p < 1 ms; duty cycle 10%
Charge-Pump Output					
Voltage	V_C	-0.3	20	V	–
Current	I_C	–	–	mA	internally limited
Slewrate Input					
Voltage	V_{SL}	-0.3	4.0	V	–
Current	I_{SL}	-0.5	0.5	mA	–
Regulator Output					
Voltage	V_Q	-0.3	25	V	–
Current	I_Q	–	–	mA	internally limited
Temperature					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{Stg}	-50	150	°C	–
Thermal Data					
Junction-ambient	R_{thj-a}	–	70	K/W	–
	R_{thj-c}	–	4	K/W	–
ESD					
All pins to GND	V_{ESD}	-2	2	kV	HBM Model

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input voltage	V_I	0	V_{ICL}	V	–
Output current	I_I	0	600	mA	–
Junction temperature	T_j	-40	150	°C	–

Table 4 Electrical Characteristics

V_I = 12 V; 40 °C < T_j < 150 °C, all voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Current consumption; $I_q = I_I - I_Q$	I_q	–	1.2	2.5	mA	I_Q = 0 mA; V_I = 6 V
Current consumption; $I_q = I_I - I_Q$	$I_{q,10}$	–	1.4	3.0	mA	I_Q = 10 mA; V_I = 6 V
Current consumption; $I_q = I_I - I_Q$	$I_{q,250}$	–	4	10	mA	I_Q = 250 mA; V_I = 6 V
Charge Pump						
Switch off threshold	$V_{C,off}$	7.7	8.2	8.7	V	–
Input Clamp Voltage	$V_{I,cl}$	21	23	25	V	I_I = 250 mA
Current limit	$I_{C,max}$	0.7	1.2	1.6	A	V_C = 5 V
Drop voltage; $V_I - V_C$	V_{DR025}	–	0.8	1.1	V	I_C = 0.25 A
Drop voltage; $V_I - V_C$	V_{DR06}	–	1.2	1.5	V	I_C = 0.6 A
Drop voltage; $V_I - V_C$	V_{DR07}	–	1.4	2.0	V	I_C = 0.7 A
Main-Regulator						
Output voltage	V_Q	3.7	3.8	3.9	V	0 < I_Q < 250 mA; TLE 4307 DV38
Output voltage	V_Q	3.2	3.3	3.4	V	0 < I_Q < 250 mA; TLE 4307 DV33
Current limit	$I_{Q,max}$	0.8	1.2	1.6	A	–
Drop voltage; $V_C - V_Q$	V_{DR025}	–	0.2	0.4	V	I_Q = 0,25 A[1)]
Drop voltage; $V_C - V_Q$	V_{DR06}	–	0.4	0.7	V	I_Q = 0.6 A[1)]
Drop voltage; $V_C - V_Q$	V_{DR08}	–	1.0	2.0	V	I_Q = 0.8 A[1)]
Over all Drop voltage; $V_I - V_Q$	V_{DR}	–	1.1	1.3	V	I_Q = 0.25 A[1)]
Load regulation	ΔV_{QLO}	–	20	40	mV	200 mA < I_Q < 600 mA
Line regulation	ΔV_{QLI}	–	–	20	mV	5 V < V_C < 8.7 V; I_Q = 10 mA

Table 4 Electrical Characteristics (cont'd)

V_I = 12 V; 40 °C < T_j < 150 °C, all voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	**Typ.**	**Max.**		
Power Supply Ripple rejection	$PSRR$	-40	–	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Output Capacitor	C_Q	22	–	–	µF	ESR < 1 Ω
Slewrate Input						
Input Resistance	R_{SL}	60	120	200	kΩ	V_{SL} = 0.2 V

1) Drop Voltage measured when the output voltage has dropped 100 mV from the nominal value.

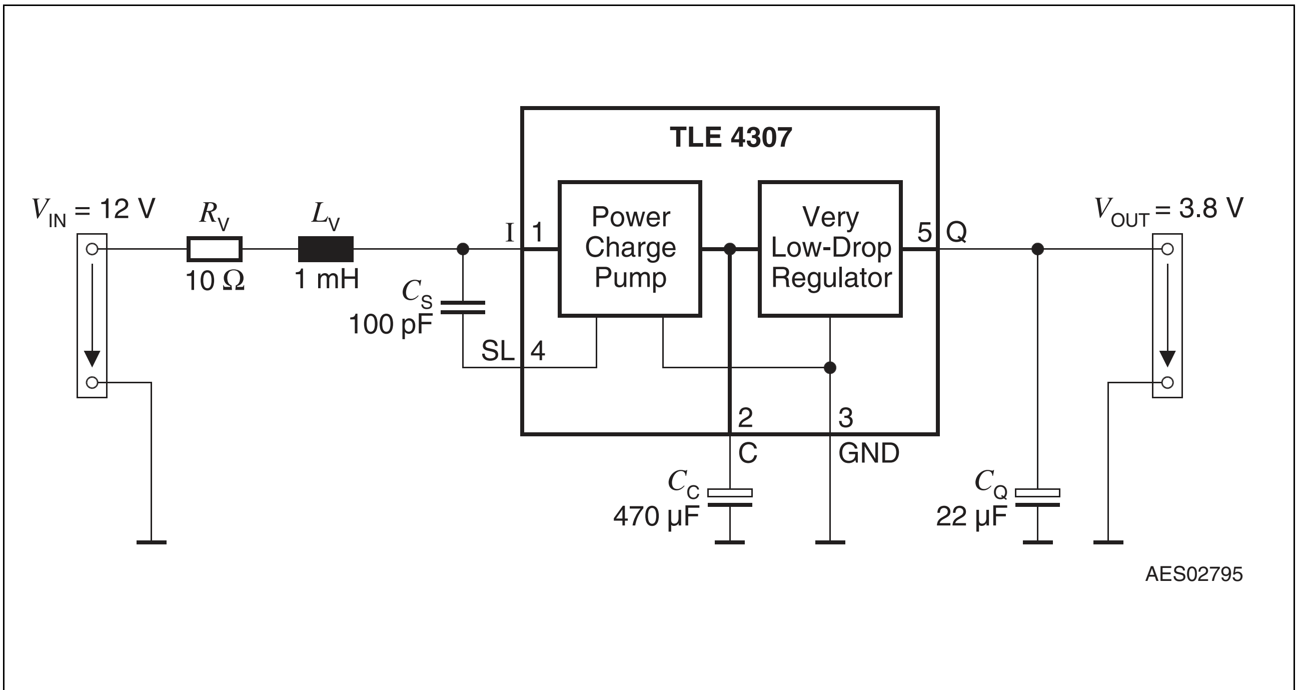


Figure 4 Measurement Circuit

Package Outlines

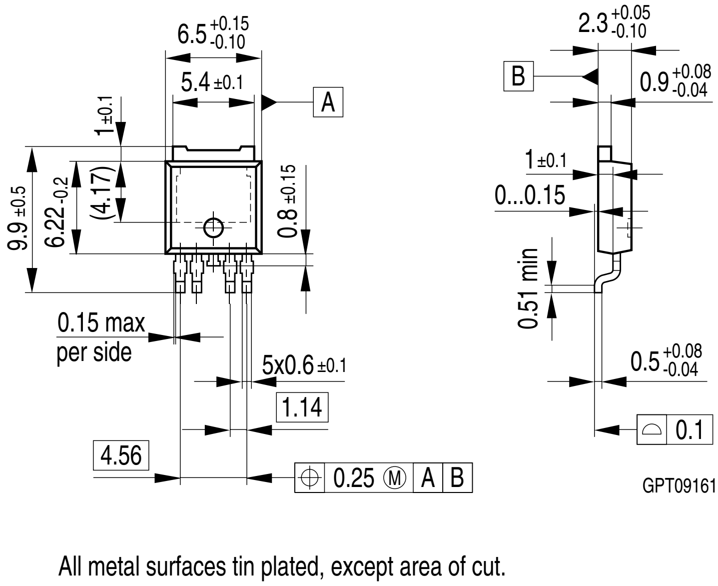


Figure 5 **P-TO252-5-1** (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

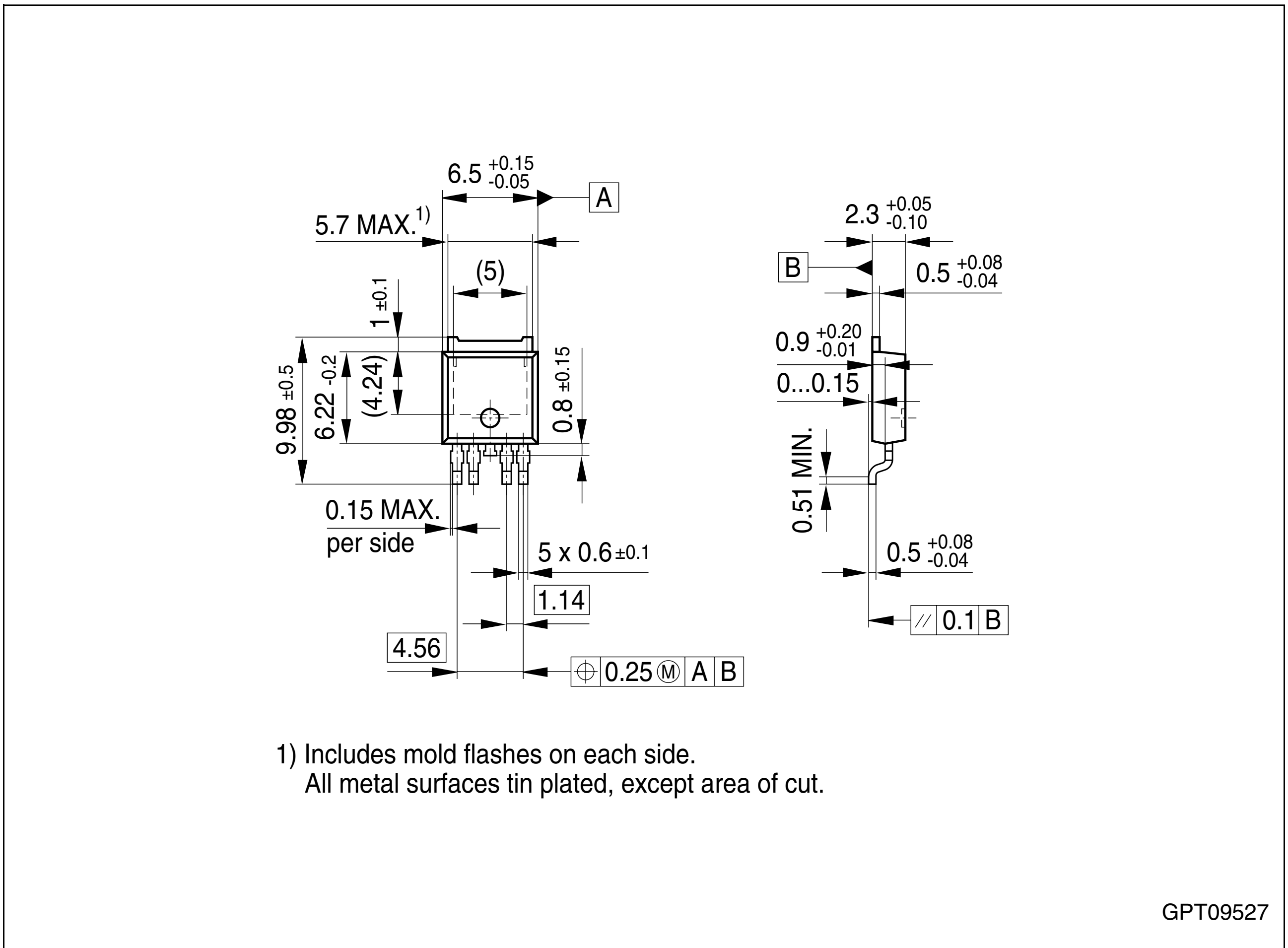

Figure 6 **P-TO252-5-11** (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

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