IXYS
INTEGRATED CIRCUITS DIVISION

CPC5712
Voltage Monitor with Detectors

Features

- CPC5712 Outputs:
  - Two Independent Programmable Level Detectors with Programmable Hysteresis
  - Fixed-Level Polarity Detector with Hysteresis
  - Differential Linear Output
- Minimum External Components
- Excellent Common-Mode Rejection Ratio (CMRR) ≥ 55dB
- Application circuits meet isolation requirements of worldwide telephony standards
- Worldwide telephone network compatibility
- Single Supply Operation, 3.0V to 5.5V
- High differential input impedance
- Very low common-mode input impedance
- Fixed Gain
- TTL Compatible CMOS Logic Level outputs
- Small SOP 16-Pin package

Applications

- VoIP Gateways, IP-PBX, xDSL
- TIP/RING Monitoring
  - Line-In-Use Detection
  - Polarity Detection for Caller ID, Enhanced 911
  - Battery Detection, PSTN Check
- Non-telephony voltage level detection applications
  - Instrumentation
  - Industrial Controls

Description

The CPC5712 is a special purpose Voltage Monitor with Detectors integrated circuit that is used in various high-voltage telephony applications such as VoIP gateways and IP-PBXs. The device monitors the TIP/RING potential through a high-impedance divider (resistor isolation) to derive two programmable signal level detects, polarity information, and a scaled representation of the phone line voltages. In use, the resistor divider and the high input impedance of the CPC5712 make the circuit practically undetectable on the line.

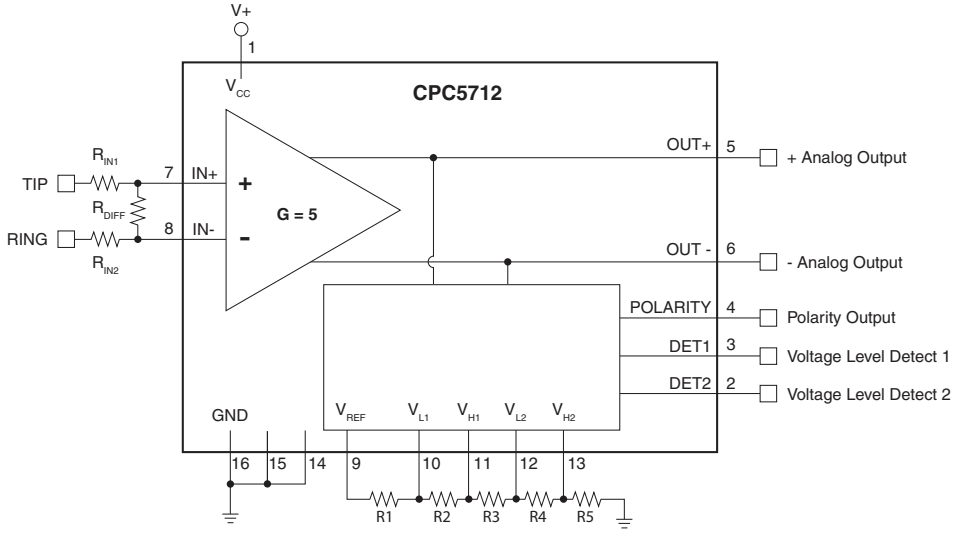
The two voltage-level detects are programmed with external resistors, which gives the designer complete freedom with respect to line voltage detection levels. The level settings also have programmable hysteresis to prevent false triggering conditions. Detection of these levels allows the user to determine the condition of the line.

This device can also be used in non-telephony applications such as instrumentation and industrial controls, especially when a low-level differential level needs to be detected in the presence of a large common-mode voltage.

Ordering Information

Part	Description
CPC5712U	16-Pin SOP (100/Tube)
CPC5712UTR	16-Pin SOP (2000/Reel)

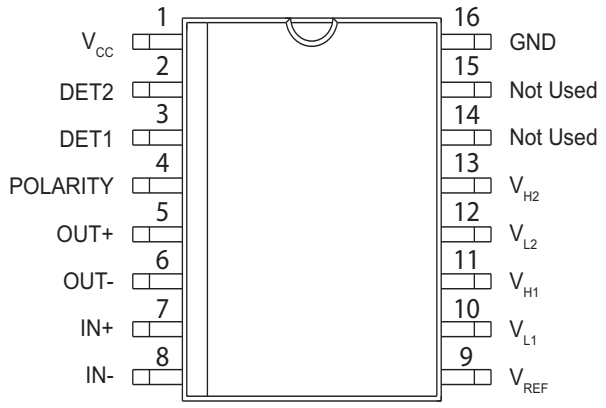
CPC5712 With Support Components



1. Specifications

1.1 Package Pinout

CPC5712 Pinout



1.2 Pin Description

Pin	Name	Description
1	V_{CC}	Supply Voltage
2	DET2	Output, Detector 2
3	DET1	Output, Detector 1
4	POLARITY	Output, represents polarity of input signal
5	OUT+	Output, amplifier non-inverting
6	OUT-	Output, amplifier inverting
7	IN+	Input, amplifier non-inverting
8	IN-	Input, amplifier inverting
9	V_{REF}	Output, Reference used to set threshold levels
10	V_{L1}	Input, sets DET1 low voltage detection threshold
11	V_{H1}	Input, sets DET1 high voltage detection threshold
12	V_{L2}	Input, sets DET2 low voltage detection threshold
13	V_{H2}	Input, sets DET2 high voltage detection threshold
14	Not Used	Do not use, connect to ground
15	Not Used	Do not use, connect to ground
16	GND	Ground

1.3 Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_{CC}	-0.3	6.0	V
Storage temperature	-40	+125	°C
Power dissipation	-	50	mW

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Rating

ESD Rating (Human Body Model)
4000 V

1.5 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
V_{CC}	V_{CC}	3.0	5.5	V
Input Common Mode Current [1]	$\lvert I_{CM} \rvert$	-	12	µA
V_{REF} Loading [2]				
Resistive	R_{REF}	20	1000	kΩ
Capacitive	C_{REF}	-	220	pF
OUT+ and OUT- Loading				
Capacitive	C_{OUT}	C_{OUT}	300	pF
Current	I_{OUT}	-500	+500	µA
Operating Temperature	T_A	-40	+85	°C

[1] Input common-mode current per pin must not exceed limit.
[2] Resistive and Capacitive loads on the V_{REF} output must remain within these limits.

1.6 Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by production testing.

Typical values are characteristic of the device at 25°C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements. Unless otherwise noted, all electrical specifications are listed for T_A=25°C and V_{CC} = 3V to 5.5V.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
DC Characteristics						
Supply Voltage		V_{CC}	3	-	5.5	V
Supply Current	V_{REF} and all outputs open, Pins 14 and 15 = Gnd.	I_{CC}				mA
	V_{CC}=3V		1.1	1.42	1.9	
	V_{CC}=5.5V		1.5	1.72	2.4	
AC Characteristics						
Differential Input Resistance		R_{IN}	10	-	-	MΩ
Output Offset Voltage	R_{DIFF} = 806kΩ, V_{IN}=0V	V_{OUT+}	-5	-	5	mV
		V_{OUT-}	-5	-	5	mV
Comparator Input Offset Voltage	R_{DIFF} = 806kΩ, From V_{IN} through to the comparators, Measured at V_{OUT+} and V_{OUT-}	-	-20	-	20	mV
Input Offset Current	I_{CM}=0µA	I_{IO}	-45	-	45	nA
Reference Voltage	V_{CC}=3V, V_{CC}=5.5V I_{REF}=0µA, I_{REF}=-80µA	V_{REF}	1.4	1.5	1.6	V
Common-Mode Rejection Ratio	$I_{CM} \leq$ 12µA, 0-120 Hz	CMRR	55	-	-	dB
Differential Gain	0 < f ≤ 20kHz	-	4.85	5.00	5.15	-
Polarity Detection Characteristics						
Polarity Detection Threshold Voltage	Differential signal applied to IN+ and IN-	V_{IN}	±22	±37	±54	mV
Digital Output Characteristics						
Output Voltage, High	I_{OH}=-5mA	V_{OH}	V_{CC}-0.6	-	-	V
Output Voltage, Low	I_{OL}=5mA	V_{OL}	-	-	0.4	V

2. Functional Description

2.1 Overview

Clare's CPC5712 is a generalized building block IC for telephone systems that is connected, through a resistor network, to the TIP and RING leads. From the TIP and RING line voltage, the CPC5712 provides a buffered and amplified differential linear representation output voltage, a polarity detect signal, and two programmable level detect signals. From these detected levels, certain line conditions can be inferred such as Line-In-Use and battery presence. The CPC5712 provides TTL/CMOS compatible outputs for the polarity and programmable level detectors.

The polarity detect and the two programmable level detects all incorporate hysteresis to provide noise immunity and eliminate rapid output state changes in the presence of large voice signals. Hysteresis settings for the two programmable level detects are independently programmable; however, the polarity hysteresis is internally fixed.

The high and low thresholds of the two programmable level detectors are set with external resistors, the selection of which is described below.

Positive polarity, POLARITY = HIGH, is indicated for an OUT+ level greater than the OUT- level while negative polarity is indicated for an OUT+ level less than OUT-. For a logic-high polarity detect output with a normal battery feed of TIP more positive than RING, the amplifier IN+ will need to be connected to the TIP lead via the high impedance input resistors. Detection and hysteresis thresholds for polarity are internal to the device.

The CPC5712 is connected to the TIP/RING interface through a high-impedance resistor divider to attenuate the signal. The resistors in the divider network become a distributed resistive isolation barrier between the high-voltage line side and the low voltage side. The attenuator and the CPC5712 present a high impedance to TIP and RING, making the circuit almost undetectable when used as a monitoring device.

2.2 Line Side Interface

IN+, IN-: Analog inputs. The differential signal across these inputs is amplified and brought out to the pins OUT+ and OUT-. A nominal reference voltage bias of 1.5V is applied to IN+ and IN- by circuitry internal to the chip. Because the voltage across TIP and RING can be very large, TIP and RING cannot be directly connected to IN+ and IN-. A resistor divider network defined by R_{IN1}, R_{IN2} and R_{DIFF} attenuates the high voltage signal across TIP and RING (see). The resulting low voltage differential signal across R_{DIFF} is applied to the inputs IN+ and IN-. Resistors R_{IN1}, R_{IN2} and R_{DIFF} are external resistors that must be supplied by the user.

Any component sizing and value recommendations given in the circuits described in this document will need to be reviewed with regard to the regulatory and safety requirements for each particular application. For example, the resistors selected for R_{IN1} and R_{IN2}, shown in , are recommended to be a pair of 1206 surface mount size resistors in series to provide for high-voltage isolation.

2.3 Monitor Output

OUT+, OUT-: Analog outputs. The differential signal across these outputs is the same as the differential input signal, except there has been a differential gain of 5 applied to it. A nominal reference voltage bias of 1.5V is applied to OUT+ and OUT- by circuitry internal to the chip.

2.4 Detector Outputs

DET2, DET1, POLARITY: Digital outputs. These signals show whether threshold 2 has been crossed, threshold 1 has been crossed, and the polarity of the TIP to RING potential.

When configured as shown in , POLARITY will be high after the TIP to RING potential (TIP more positive than RING) has increased to a nominal 2V. POLARITY will switch low after the TIP to RING voltage decreases to approximately -2V. For example, if the TIP to RING voltage starts at -48V, POLARITY will be low. As the TIP to RING voltage increases to +1V, POLARITY will remain low. As the TIP to RING voltage increases beyond it's internally set positive threshold, the POLARITY output will switch high. POLARITY will remain high until the TIP to RING voltage decreases below it's internally set negative threshold. Because these polarity thresholds are set internally they are not user adjustable.

In the case of the detector 2 switching points, DET2 will be low after the |TIP/RING| voltage has decreased below a threshold set at V_{L2}. DET2 will not transition high until after the |TIP/RING| voltage has increased above a threshold set at V_{H2}. This |TIP/RING| voltage will be larger than the threshold set at V_{L2}. As an example, the voltage at V_{L2} represents a |TIP/RING| threshold of 20V and V_{H2} represents a TIP/RING threshold of 22V. DET2 will be low if the |TIP/RING| voltage decreases below 20V, and it will remain low until the |TIP/RING| voltage increases above 22V. DET2 will change states for both positive and negative values of TIP/RING voltage as represented by |TIP/RING|. This means that DET2 will also be low if the TIP/RING voltage decreases below -20V and will remain low until the TIP/RING voltage increases beyond -22V. The user must rely on POLARITY to determine whether the TIP/RING threshold changed due to a positive or negative differential signal since DET2 does not contain any polarity information.

DET1 behaves similarly to DET2, except that it is triggered based on the voltage set at V_{L1} and V_{H1}. This means that DET1 will be low after the |TIP/RING| voltage has decreased below the value set by the voltage at V_{L1} and will not change high until after the |TIP/RING| voltage has increased above the value set by the voltage at V_{H1}. DET1 does not give any polarity information for the same reasons as defined for DET2. In the application circuit provided, the TIP/RING threshold levels of DET2 will always be higher than the threshold levels of DET1.

2.5 Detector Threshold Operation

V_{L1}, V_{H1}, V_{L2}, and V_{H2}: Inputs used to set the |TIP/RING| threshold levels that are to be detected. V_{H1} and V_{L1} are used to set the high and low threshold levels. The difference between V_{H1} and V_{L1} sets the hysteresis for the 1st threshold level. V_{H2} and V_{L2} are used to set the threshold and hysteresis for the 2nd threshold level. There is a digital output for both the 1st and 2nd threshold levels that shows when the |TIP/RING| voltage has crossed a threshold level and when it has exceeded the configured hysteresis level. This was explained in the DET1 and DET2 definitions. In general, the digital output will be low when the |TIP/RING| voltage has fallen below the $V_{L\#}$ level and will change high again once the |TIP/RING| voltage has risen above the $V_{H\#}$ level.

V_{REF}: An analog output that is similar to the DC bias level that is applied to OUT+ and OUT-. This voltage is brought off chip so that it can be used to define threshold detection levels. Load capacitance on this pin must be kept less than the value recommended in the table **Recommended Operating Conditions**. The total load resistance on this pin must be within the range specified in the table **Recommended Operating Conditions**.

Resistors R1, R2, R3, R4 and R5 are external resistors, which must be provided by the user. The selection of the resistors determines the voltages at V_{L2}, V_{H2}, V_{L1} and V_{H1} and therefore the threshold and hysteresis values for the 2 detectors.

The values for R1, R2, R3, R4, and R5 are easily determined. Select voltage levels for the 1st and 2nd threshold and hysteresis settings such that:

$$V_{H2} > V_{L2} > V_{H1} > V_{L1}$$

Then use the following algorithm to find the values of R2, R3, R4 and R5.

1. Select a value for R1.
2. $R2 = (R1(V_{H1}-V_{L1})) / V_{L1}$
3. $R3 = (R1(V_{L2}-V_{H1}))/ V_{L1}$
4. $R4 = (R1(V_{H2}-V_{L2})) / V_{L1}$
5. $R5 = (R1(V_{REF}/A-V_{H2})) / V_{L1}$

- $V_{REF} = 1.5V$
- $A = (2.5 (R_{DIFF})) / (R_{IN1} + R_{IN2} + R_{DIFF})$, which typically calculates to 0.05; in this case: 0.04938. See **Figure 1**.

Also, as shown in the table of **Recommended Operating Conditions**, the resistive load on the V_{REF} pin must fall within the range:

$$20k\Omega < (R1 + R2 + R3 + R4 + R5) < 1M\Omega$$

2.6 Power Connections

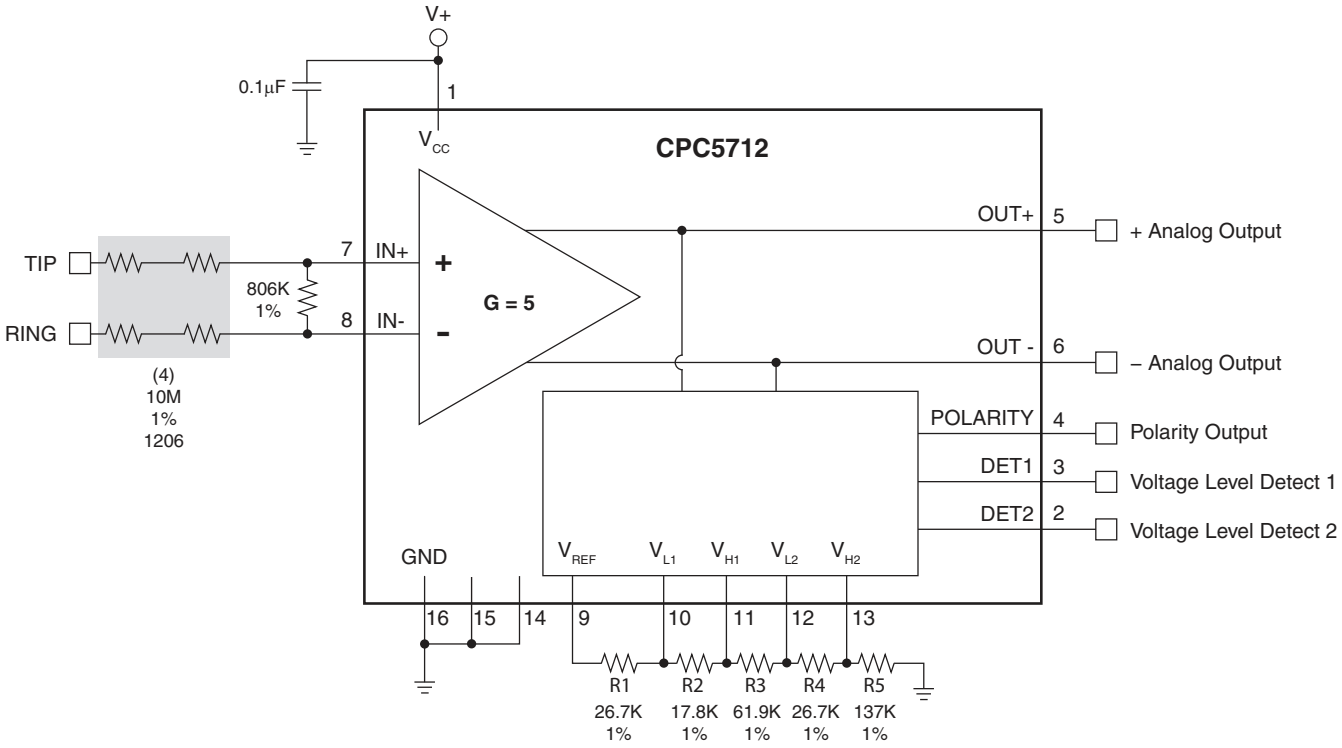
VCC, Ground: Power supply pins. These are used to supply voltage and ground to the chip.

3. Design Example

An application circuit that is based on information discussed in **Section 2.5 "Detector Threshold Operation" on page 6** is shown in **Figure 1**.

In the following telephony design example, it is desired to have a Line-In-Use ($\overline{\text{LIU}}$) detector set at 12V with a hysteresis of 3V, and a loop or battery-presence (LOOP) detector set at 5V with a hysteresis of 2V. The $\overline{\text{LIU}}$ detector will monitor the Public Switched Telephone Network (PSTN) twisted pair TIP and RING leads for a voltage level that indicates a device on the line is off-hook while the LOOP detector monitors for the presence of battery feed. In this example detector 2 (DET2) will be the $\overline{\text{LIU}}$ detector as it has the greater voltage detect thresholds.

Figure 1 CPC5712 Application Circuit



3.1 Line Interface

Between the CPC5712 and the TIP/RING line is a high impedance resistive divider network that provides sufficient impedance to meet the barrier insulation specifications in safety regulations and comply with the on-hook DC leakage to ground requirements from the various network compatibility specifications.

To ensure regulatory compliance, a 20MΩ or greater resistance is required from the individual TIP and RING leads to the IN+ and IN- inputs. For most applications where the tip and ring interface does not have a ground referenced surge protector, Clare recommends using two 1206-size 10MΩ resistors in series to provide the minimum impedance and to meet surge requirements. Resistors having a smaller physical footprint may be used when ground referenced surge protection is available.

In practice, each 1206-size resistor is capable of withstanding the 2000V peak waveforms typical of lightning surges on the phone line. Hence, two 1206 resistors can withstand 4000V lightning pulses.

3.2 Differential Input Resistor

The differential input resistor placed across the IN+ and IN- inputs provides two functions.

From the application perspective, this component provides a scaled down representation of the tip and ring line voltage to the CPC5712 inputs. The voltage applied to the inputs is easily calculated because it is derived from a simple resistive divider comprising the tip and ring input resistors and the differential input resistor.

For improved performance, the CPC5712 signal path is trimmed at the factory to reduce comparator detection errors caused by offset currents and voltages. The CPC5712's input offset effects are reduced by trimming the device with an 806kΩ input resistor. Using any other value resistor at the inputs negates the trim and introduces offset errors.

3.3 Voltage Detector Design

From the application requirements given above, the desired $\overline{LIU}$ detector threshold voltages are therefore:

- V_{H2} = 15V
- V_{L2} = 12V

and the detector thresholds for the LOOP detector are:

- V_{H1} = 5V
- V_{L1} = 3V

3.3.1 Calculate Resistor Values

From the design equations provided in **Section 2.5 "Detector Threshold Operation" on page 6** this gives:

- R1=R1
- R2=0.666667 R1
- R3=2.333333 R1
- R4=R1
- R5=5.125558 R1

Summing these equations provides the following result:

R1+R2+R3+R4+R5 = 10.12556 R1
and since this sum is bound by:
20kΩ < (R1 + R2 + R3 + R4 + R5) < 1MΩ

this reduces to: 20kΩ < (10.12556 R1) < 1MΩ.

Taking into account the additional constraint of resistor tolerance, 1% in this example, the range of allowable values for R1 is further reduced and becomes:
1.995kΩ < R1 < 97.782kΩ permitting a value for R1 to be chosen.

Selecting a standard value from the E96, 1% table for R1 of 26.7kΩ, the calculated values for the remaining resistors becomes:

- R2=17.8kΩ
- R3=62.3kΩ
- R4=26.7kΩ
- R5=136.85kΩ

Since the calculated values of R3 and R5 are not standard values, a reasonable compromise for these resistors is: R3=61.9kΩ, R5=137kΩ. See **Figure 1**.

3.3.2 Verify Resistor Selection

Once the resistor values are chosen it is necessary to back calculate the nominal detector thresholds.

To do this the following equations are provided for two variables:

$$R_{\Sigma} = R_{IN1} + R_{IN2} + R_{DIFF}$$

$$R_{REF} = R1 + R2 + R3 + R4 + R5$$

where R_{Σ} is the sum of the resistive interface network and R_{REF} is the sum of the resistor divider network on the reference voltage output.

The following values are also needed to perform the threshold calculations. They are:

- V_{REF} = 1.5V
- $R_{IN1} = R_{IN2}$ = 2 x 10MΩ = 20MΩ
- R_{DIFF} = 806kΩ
- G=2.5 (Single ended gain of input amplifier)

which gives:

- R_{Σ} = 40.806MΩ and
- R_{REF} = 270.1kΩ

The threshold equations are:

1. $$V_{L1} = \frac{V_{REF} \cdot R_{\Sigma} \cdot R1}{G \cdot R_{DIFF} \cdot R_{REF}}$$

2. $$V_{H1} = \frac{V_{REF} \cdot R_{\Sigma} \cdot (R1 + R2)}{G \cdot R_{DIFF} \cdot R_{REF}}$$

3. $$V_{L2} = \frac{V_{REF} \cdot R_{\Sigma} \cdot (R1 + R2 + R3)}{G \cdot R_{DIFF} \cdot R_{REF}}$$

4. $$V_{H2} = \frac{V_{REF} \cdot R_{\Sigma} \cdot (R1 + R2 + R3 + R4)}{G \cdot R_{DIFF} \cdot R_{REF}}$$

Using the selected standard 1% resistor values, and back calculating to the threshold voltages produces these results:

- V_{L1} = 3.00280V
- V_{H1} = 5.00467V
- V_{L2} = 11.9662V
- V_{H2} = 14.9690V

As can be seen, the error from using standard value resistors is less than 0.1% for V_{L1} and V_{H1} and is less than 0.3% for V_{L2} and V_{H2}.

3.4 High Voltage Detection Designs

Designs that require higher detection levels greater than approximately 17V will necessitate a different voltage divider ratio to accommodate the operational range of the CPC5712's internal circuitry. Changes to the input resistor divider network are restricted to the high impedance resistors from the tip and ring leads to the IN+ and IN- inputs. Changing the differential input resistor value from 806kΩ is not recommended as this will introduce offset errors. The degree of offset error caused by changing this component's value is not measured and therefore not calculable.

The design procedure for higher voltage detect levels is the same as presented above. Remember to begin with the equations shown in **Section 2.5 "Detector Threshold Operation" on page 6** and use the updated value for the "A" term based on the new input resistor values.

4. Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC5712U	MSL 1

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Reflow Profile

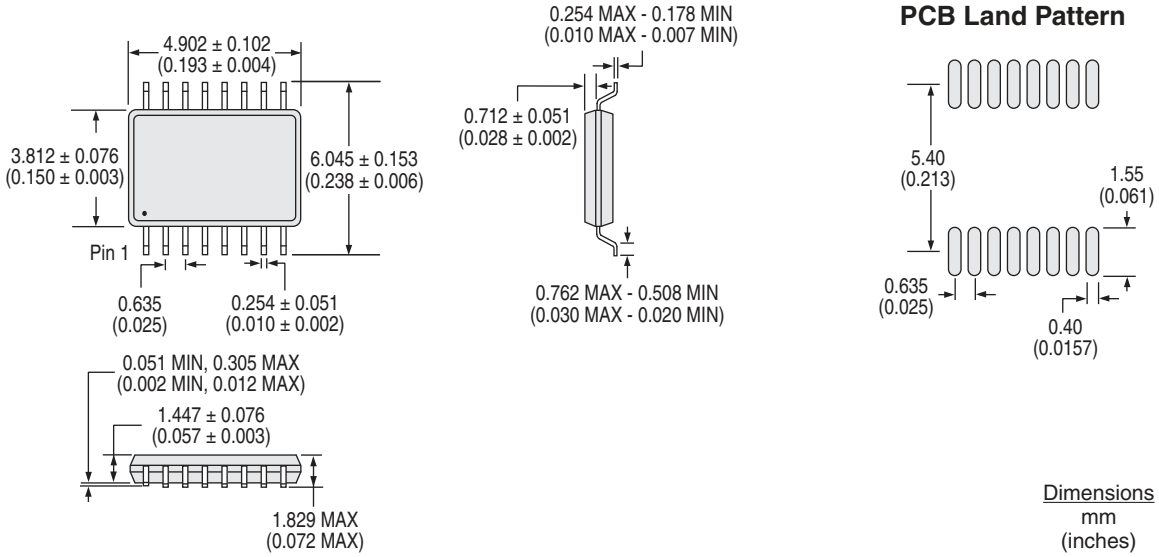
This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC5712U	260°C for 30 seconds

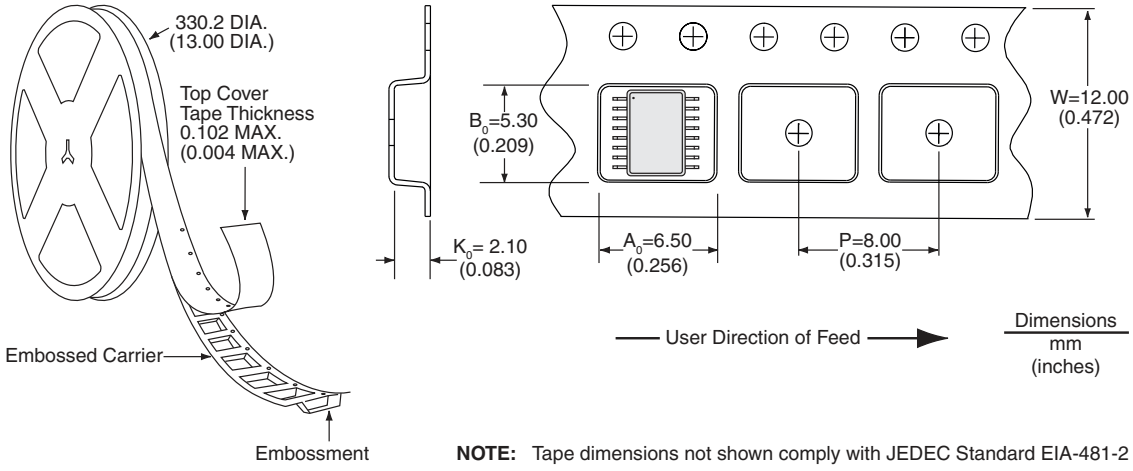
4.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

4.5 CPC5712U 16-Pin SOP Package



4.6 CPC5712UTR Tape and Reel Packaging



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit www.ixysic.com

Specification: DS-CPC5712-R02

12/22/2012