MPQ9846

36V, 0.6A, Low I_Q, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ9846 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves 0.6A of continuous output current, with excellent load and line regulation over a wide 3.3V to 36V input supply range. The switching frequency can be programmed or synchronized to an external clock in the range of 350kHz to 2.5MHz. The synchronous operation and ultra-low 14µA sleep mode quiescent current provide high efficiency over the output current load range. This allows the MPQ9846 to be used in a variety of step-down applications, automotive input environments, and battery-powered applications.

Peak current mode operation provides fast transient response and eases loop stabilization. The excellent low-dropout performance allows the MPQ9846 to be used in high duty cycle applications.

Full protection features include over-current protection (OCP), short-circuit protection (SCP), and thermal shutdown. An open-drain power good (PG) signal indicates when the output is within 10% of its nominal voltage. The MPQ9846 is available in a space-saving QFN-16 (3mmx4mm) package.

FEATURES

- 2µA Low Shutdown Supply Current
- 14µA No-Load Quiescent Current
- Internal 125mΩ High-Side and 115mΩ Low-Side MOSFET
- 350kHz to 2.5MHz Configurable Switching Frequency
- Power Good (PG) Output
- External Soft Start (SS)
- 80ns Minimum On Time
- AAM at Light Load
- Low-Dropout Mode
- Hiccup Over-Current Protection (OCP)
- Available in a QFN-16 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Infotainment
- Clusters
- Advanced Driver Assistance Systems
- Industrial Power Systems

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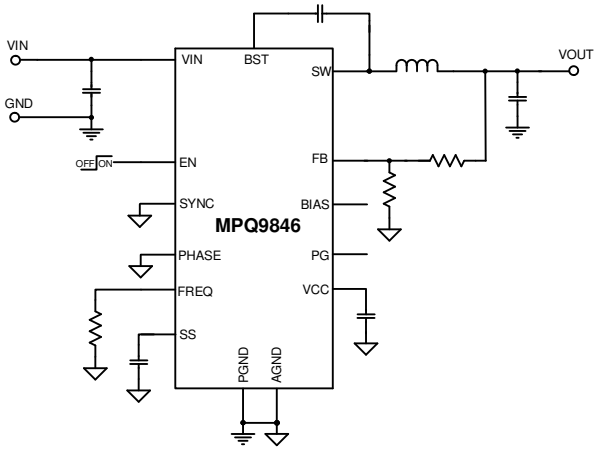
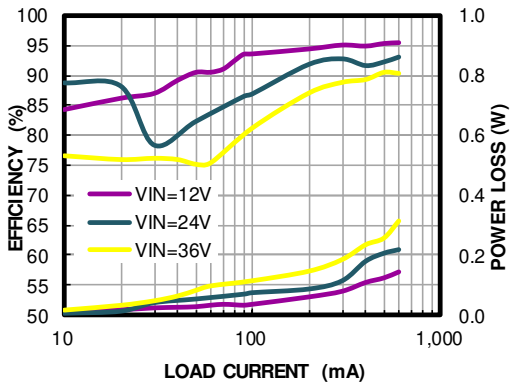
TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 500kHz, L = 10µH, AAM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ9846GL-AEC1	QFN-16 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ9846GL–AEC1–Z).

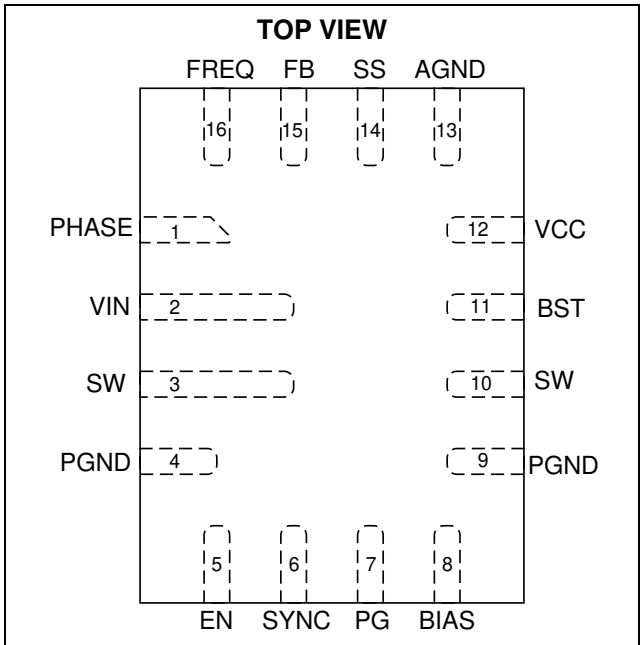
** Moisture Sensitivity Level Rating.

TOP MARKING

MPYW
9846
LLL

MP: MPS prefix
Y: Year code
W: Week code
9846: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	PHASE	**Selectable in-phase or 180° out-of-phase of SYNC input.** Pull PHASE high to be in-phase. Pull PHASE low to be 180° out-of-phase. It is recommend to connect this pin to ground if not used.
2	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries, as well as the power switch connected to SW. Place a decoupling capacitor to ground close to VIN to minimize switching spikes.
3, 10	SW	**Switch node.** SW is the output of the internal power switch. Pin 3 and pin 10 are internally connected.
4, 9	PGND	**Power ground.** PGND is the reference ground of the power device, and requires careful consideration during PCB layout design. For the best results, connect PGND with copper pours and vias.
5	EN	**Enable.** Pull EN below the specified threshold to shut down the chip. Pull EN above the specified threshold to enable the chip.
6	SYNC	**Synchronize.** Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz greater than the R_{FREQ} set frequency. Connect SYNC to GND if this pin is not used.
7	PG	**Power good output.** The output of PG is an open drain, and goes high if the output voltage is within ±10% of the nominal voltage. Float PG if it is not used.
8	BIAS	**Bias input.** Connect BIAS to an external power supply (5V to 18V) to reduce power dissipation and increase efficiency. If not in use, float BIAS or connect it to ground.
11	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
12	VCC	**Bias supply.** VCC supplies power to the internal control circuit and gate drivers. A minimum 1µF decoupling capacitor to ground must be placed near VCC.
13	AGND	**Analog ground.** AGND is the reference ground of the logic circuit.
14	SS	**Optional external soft-start time setting.** Connect an external capacitor between this pin and GND to externally set the soft-start time. The MPQ9846 sources 10µA from SS to the soft-start capacitor during start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up. Floating this pin activates the internal 0.7ms soft-start setting.
15	FB	**Feedback input.** Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
16	FREQ	**Switching frequency program.** Connect a resistor from FREQ to ground to set the switching frequency.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{INx}) .....-0.3V to +40V
Switch voltage (V_{SWx}) ... -0.3V to VIN $_{(MAX)}$ + 0.3V
BST voltage (V_{BSTx}) ..... $V_{SW\ (MAX)}$ + 6.5V
EN voltage (V_{ENx}) .....-0.3V to +40V
BIAS voltage .....-0.3V to +20V
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (5)
QFN-16 (3mmx4mm) 2.9W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) .....±2kV
Charged device model (CDM).....±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) .....3.3V to 36V
Operating junction temp (T_J) (3).....
.....-40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx4mm)		
JESD51-7 (4)	48	11 °C/W
EVQ9846-L-00A (5)	43	5 °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Mission profiles requiring operation above 125°C T_J may be Supported. Contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on the MPS standard EVB for the MPQ9846, 64mmx64mm, 4-layer, 2oz. PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, no switching, T_J = 25°C		14	21	µA
		V_{FB} = 0.85V, no load, no switching			29	
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		2	6	µA
VIN under-voltage lockout rising threshold	$INUV_{RISING}$		2.3	2.8	3.2	V
VIN under-voltage lockout hysteresis threshold	$INUV_{HYS}$			150		mV
EN rising threshold	V_{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V_{EN_HYS}			120		mV
Feedback reference voltage	V_{REF}		784	800	816	mV
		T_J = 25°C	792	800	808	mV
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		125	165	mΩ
LS switch on resistance	R_{ON_LS}			115	155	mΩ
Switching frequency	f_{SW}	R_{FREQ} = 180kΩ, or from sync clock	400	475	550	kHz
		R_{FREQ} = 82kΩ, or from sync clock	850	1000	1150	kHz
		R_{FREQ} = 27kΩ, or from sync clock	2250	2500	2750	kHz
Minimum on time (6)	t_{ON_MIN}			80		ns
SYNC input low voltage	V_{SYNC_LOW}				0.4	V
SYNC input high voltage	V_{SYNC_HIGH}		1.8			V
Current limit	I_{LIMIT_HS}	Duty cycle = 40%	1.0	1.2	1.4	A
Low-side valley current limit	I_{LIMIT_LS}	V_{OUT} = 3.3V, L = 4.7µH	0.55	0.75	0.95	A
ZCD current	I_{ZCD}			0.05		A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
Soft-start current	I_{SS}	V_{SS} = 0.8V	5	10	15	µA
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3.5	%
Thermal shutdown (6)	T_{SD}			170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			20		°C
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	79	84	89	%
		V_{FB} rising	113.5	118.5	123.5	%
PG deglitch timer	$t_{PG\_DEGLITCH}$	PG from low to high		30		µs
		PG from high to low		50		µs
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V

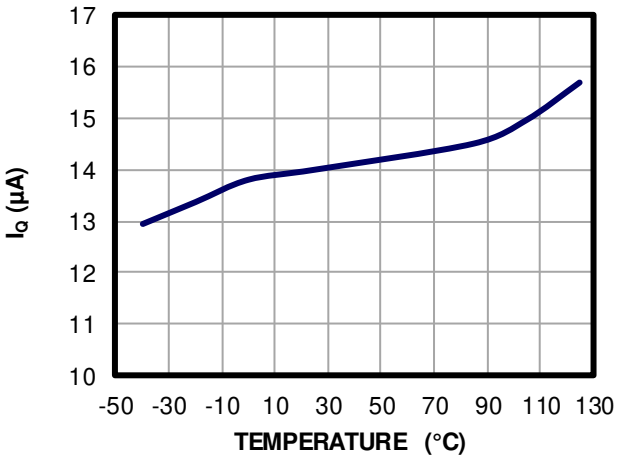
Note:

6) Not tested in production. Guaranteed by design and characterization.

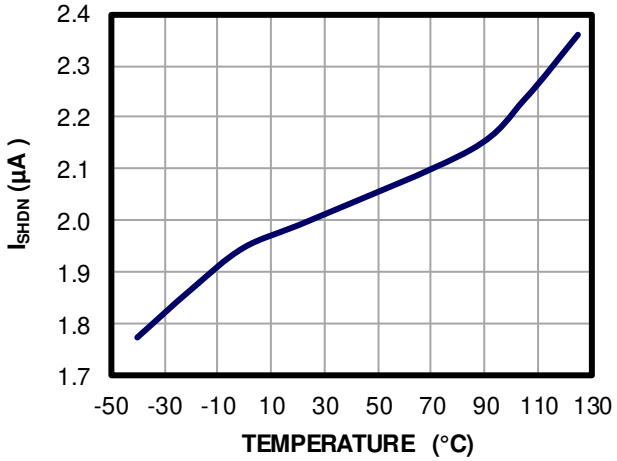
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

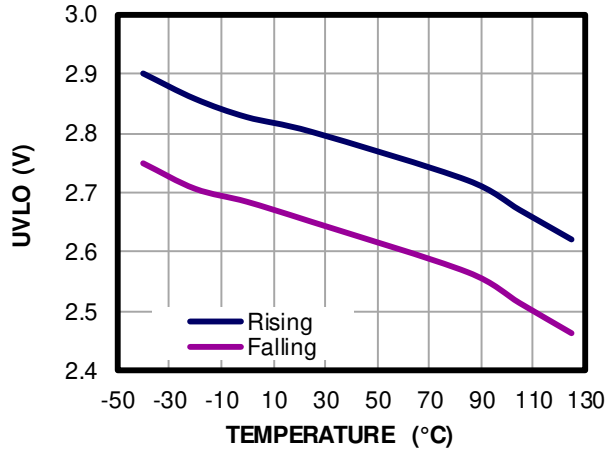
Quiescent Current vs. Temperature



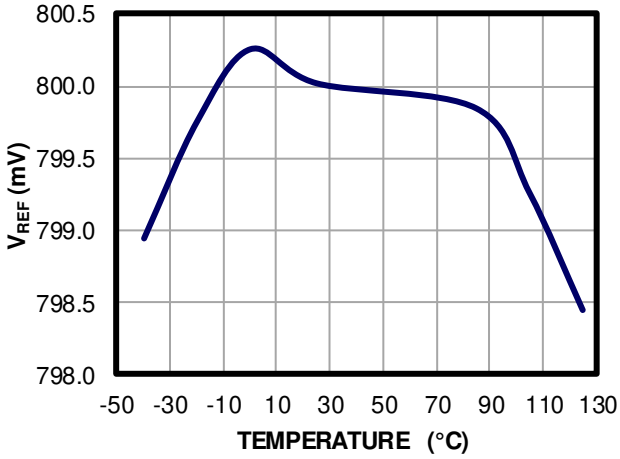
Shutdown Current vs. Temperature



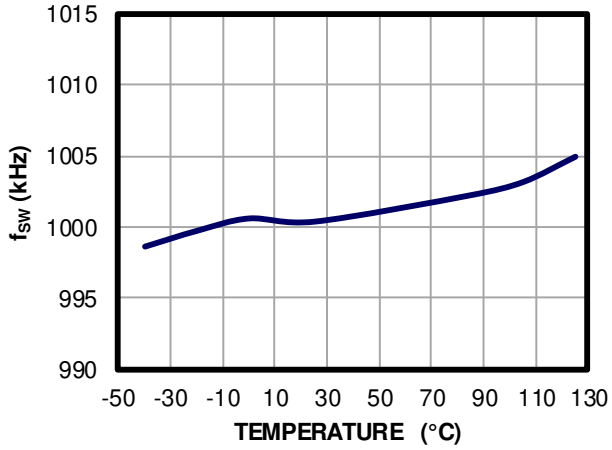
VIN UVLO Threshold vs. Temperature



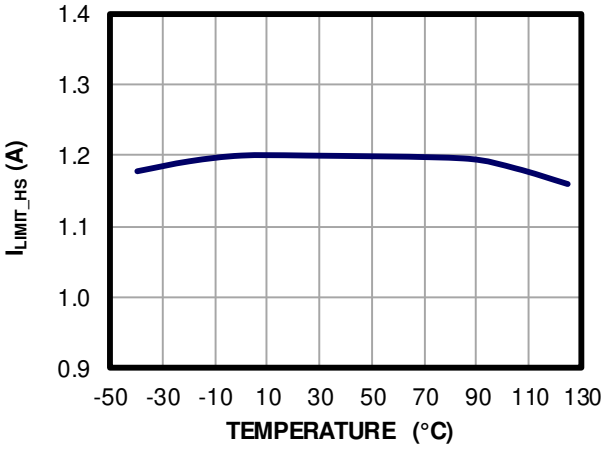
Feedback Reference vs. Temperature



Switching Frequency vs. Temperature



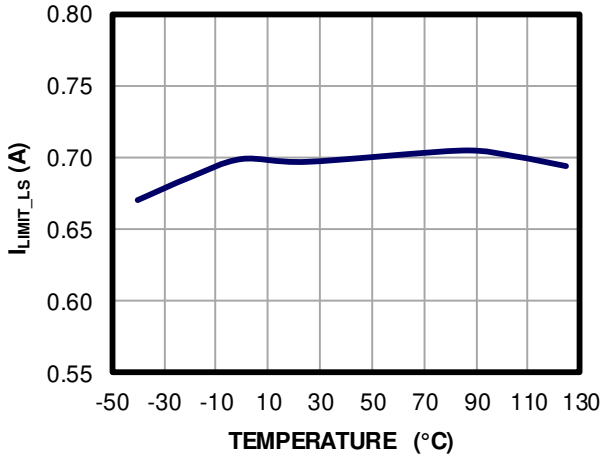
Current Limit vs. Temperature



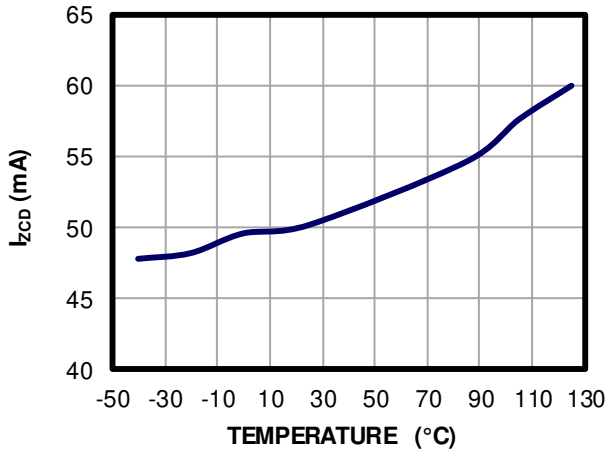
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

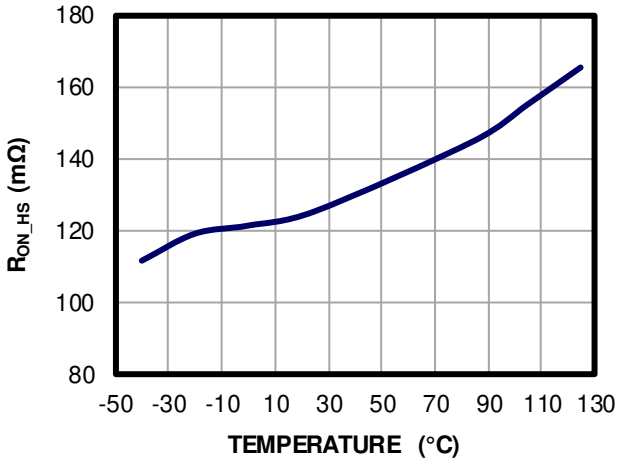
Valley Current Limit vs. Temperature



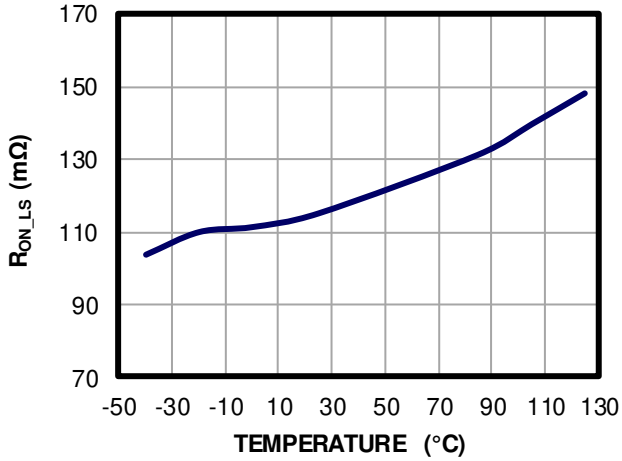
ZCD Current vs. Temperature



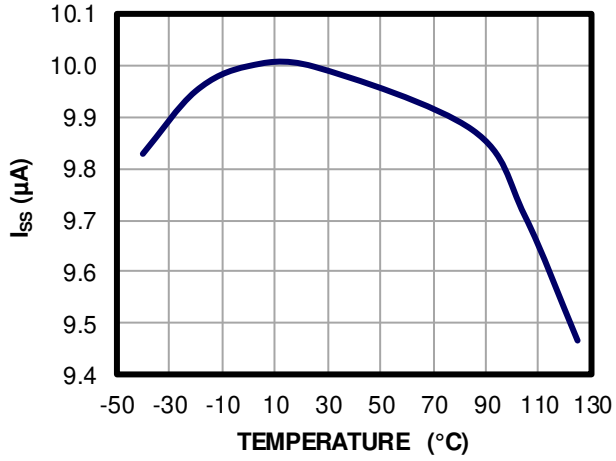
HS-FET On Resistance vs. Temperature



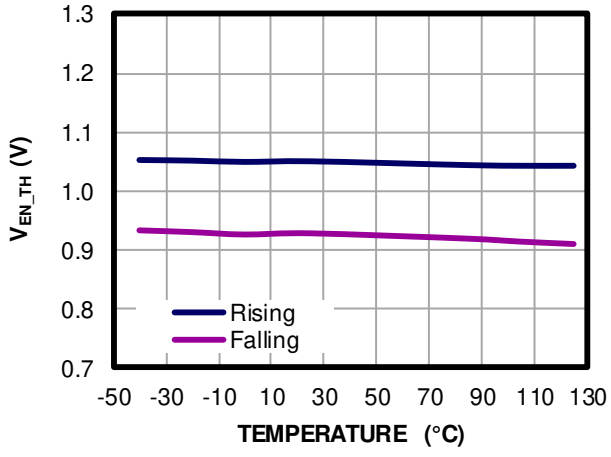
LS-FET On Resistance vs. Temperature



Soft-Start Current vs. Temperature



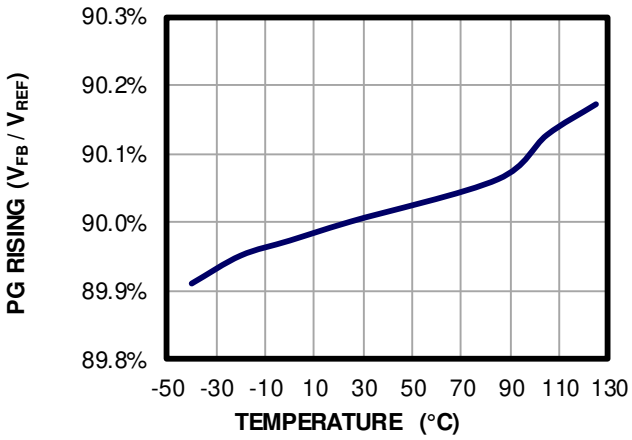
EN Threshold vs. Temperature



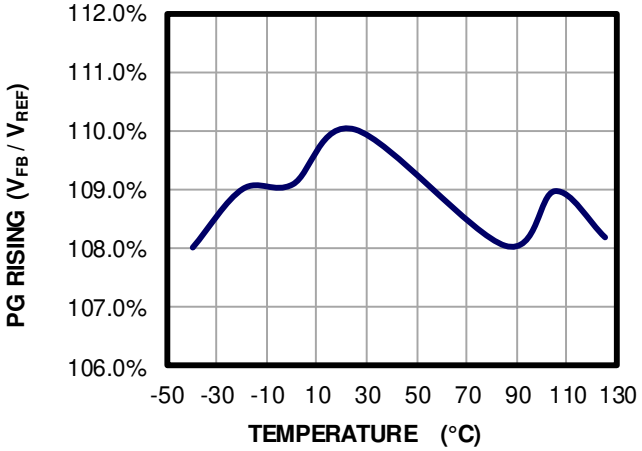
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

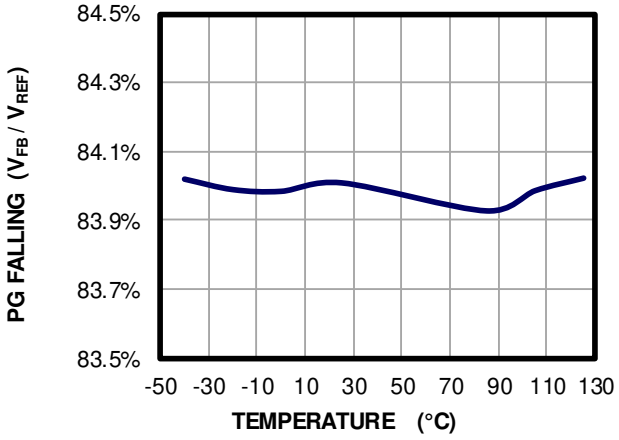
PG Rising Threshold (V_{FB} Rising) vs. Temperature



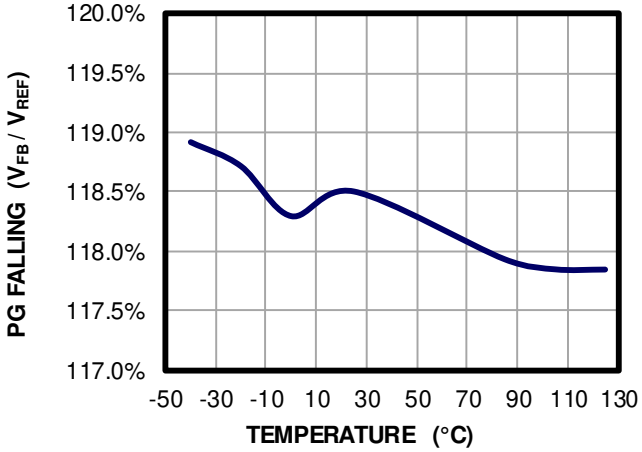
PG Rising Threshold (V_{FB} Falling) vs. Temperature



PG Falling Threshold (V_{FB} Falling) vs. Temperature



PG Falling Threshold (V_{FB} Rising) vs. Temperature

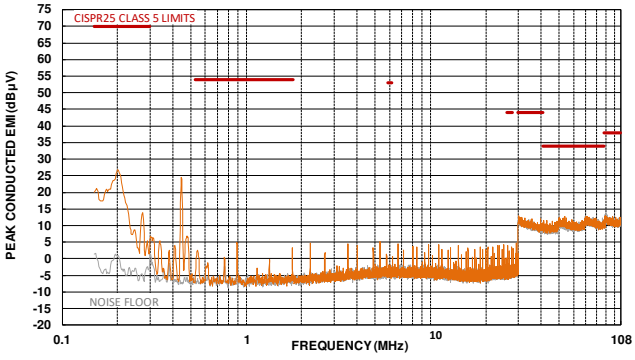


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, I_O = 0.6A, L = 10µH, f_{SW} = 450kHz, with EMI filters, T_A = 25°C, unless otherwise noted. (7)

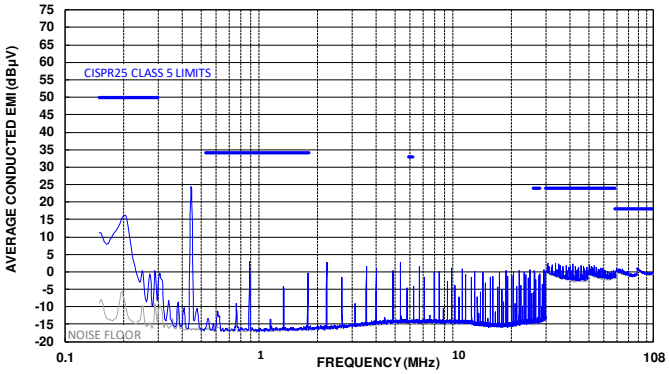
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



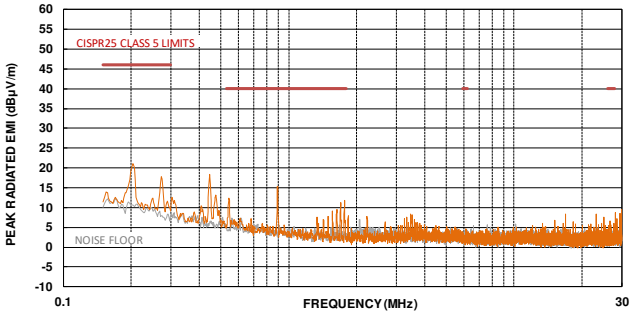
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



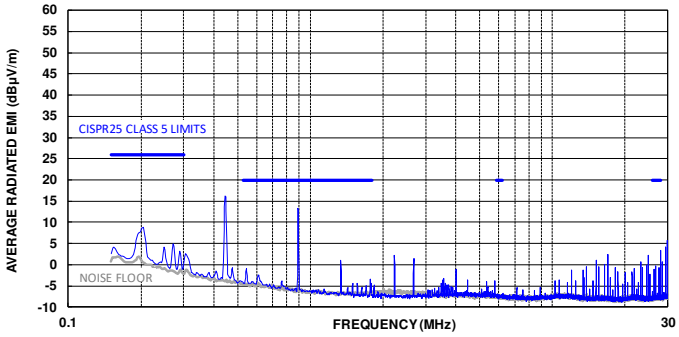
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



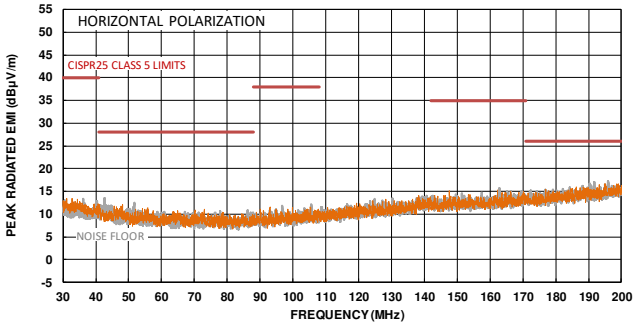
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



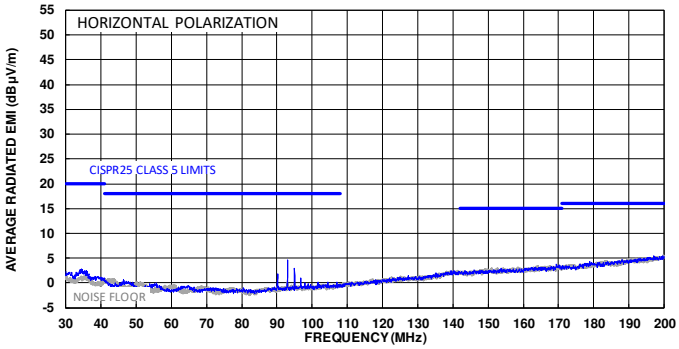
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

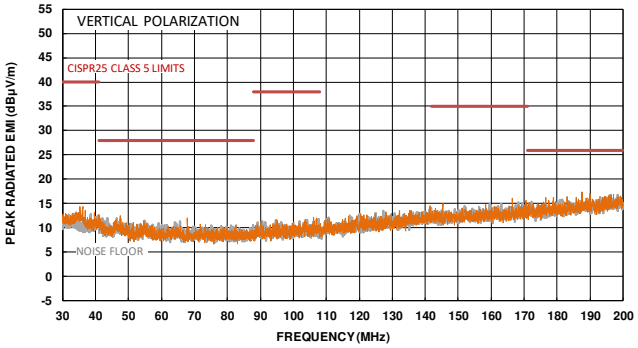


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, I_O = 0.6A, L = 10µH, f_{SW} = 450kHz, with EMI filters, T_A = 25°C, unless otherwise noted. (7)

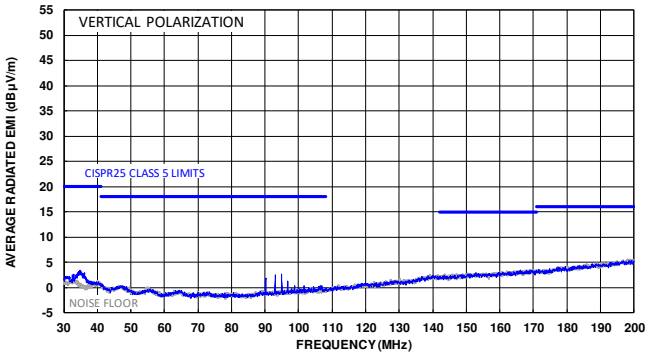
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



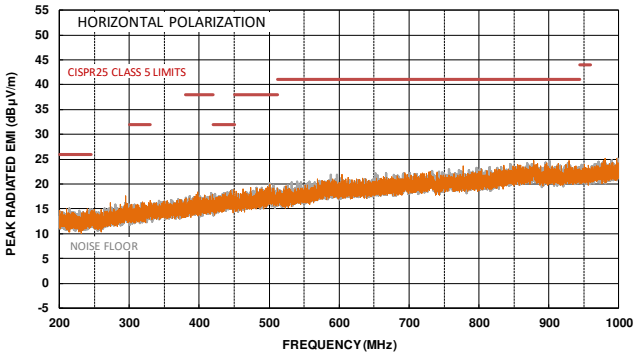
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



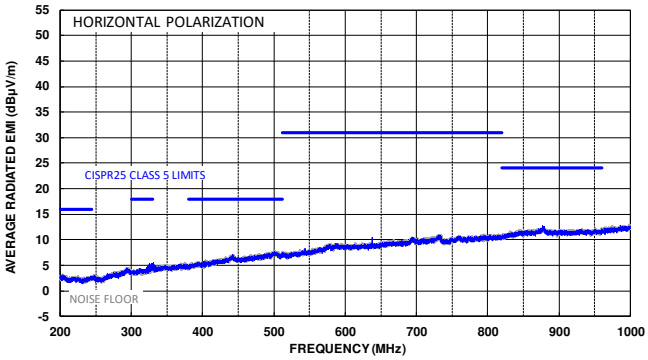
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



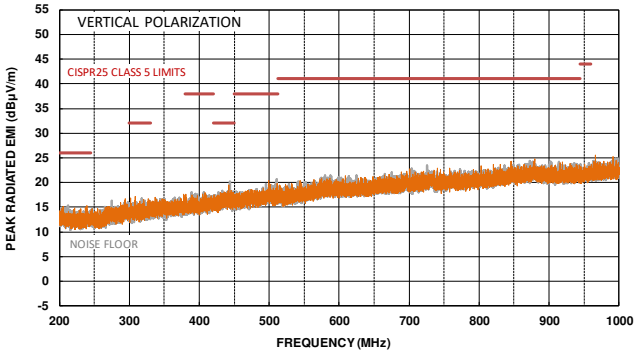
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



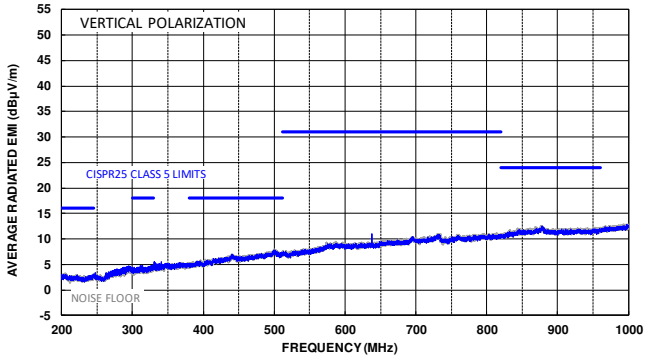
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical,200MHz to 1GHz



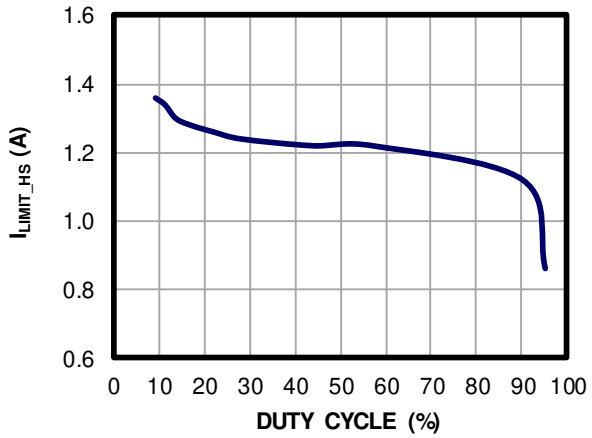
Note:

7) The EMC test results are based on the application circuit's evaluation board (EVQ9846-L-00A) with EMI filters (see Figure 15 on page 33).

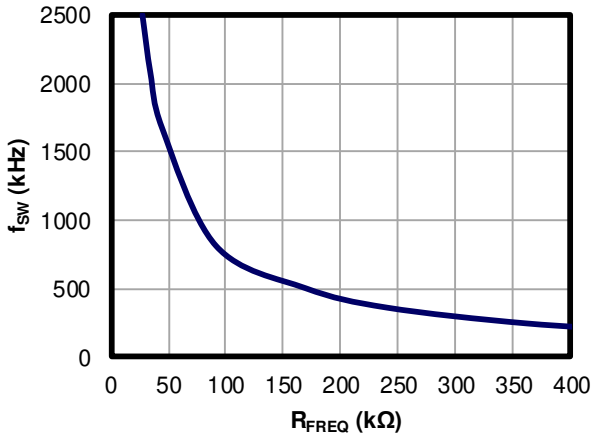
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

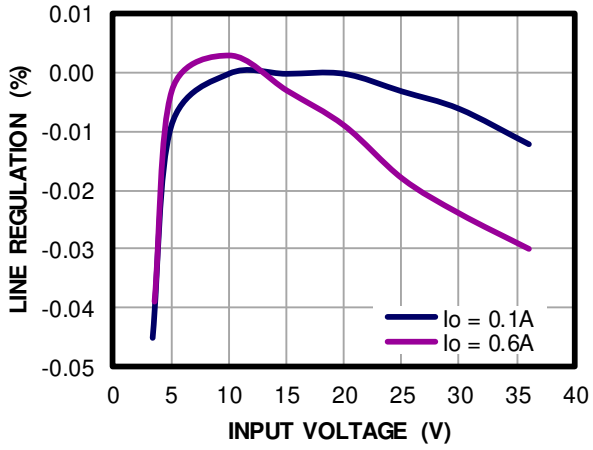
Current Limit vs. Duty Cycle



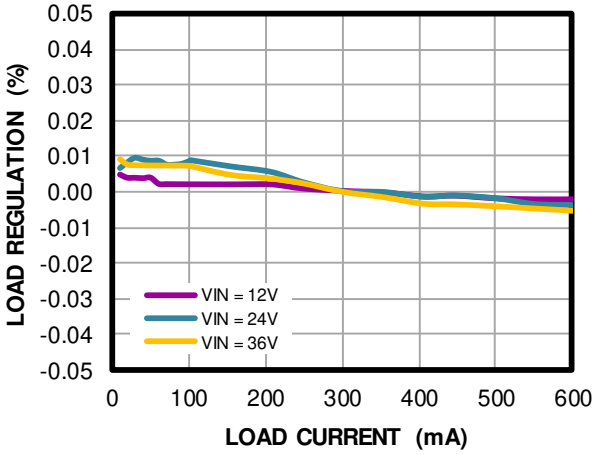
Switching Frequency vs. R_{FREQ}



Line Regulation

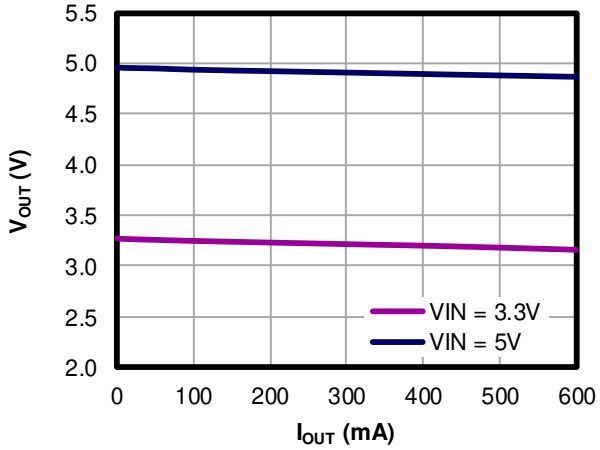


Load Regulation

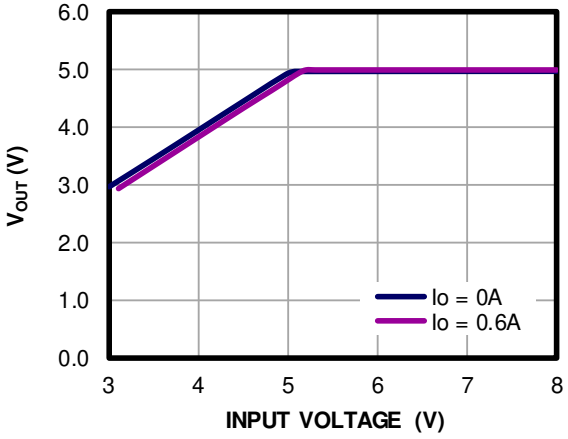


Output Voltage vs. Load Current Dropout Performance

(Set nominal V_{OUT} > V_{IN})



Dropout Performance

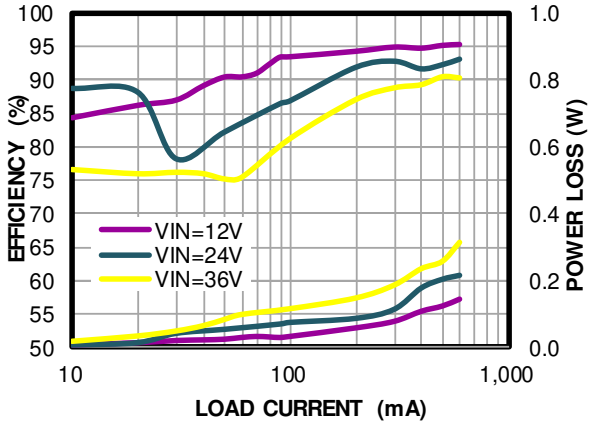


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

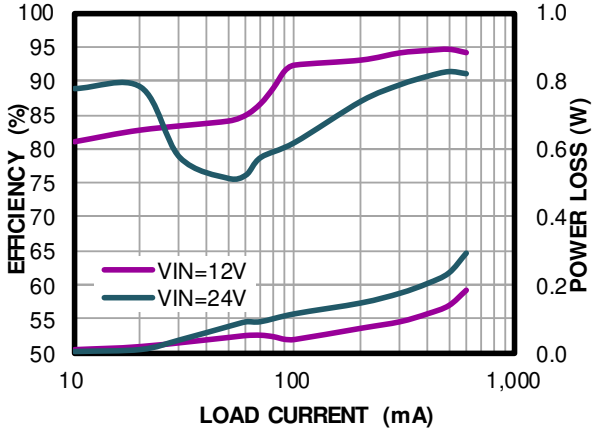
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 5V, f_{SW} = 500kHz



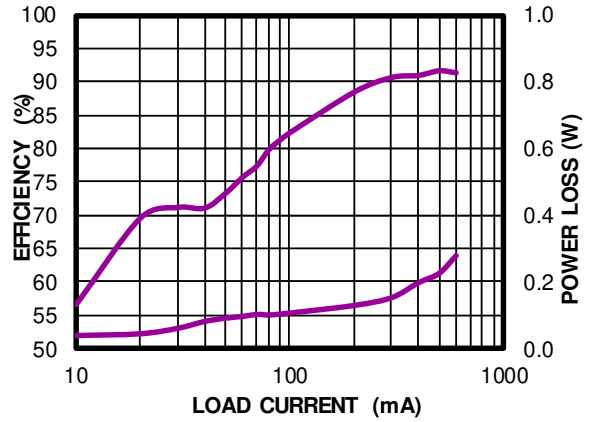
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 5V, f_{SW} = 1MHz



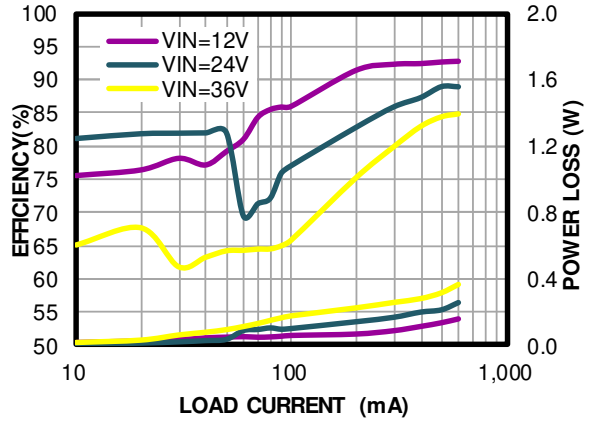
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 5V, f_{SW} = 2.2MHz, V_{IN} = 12V



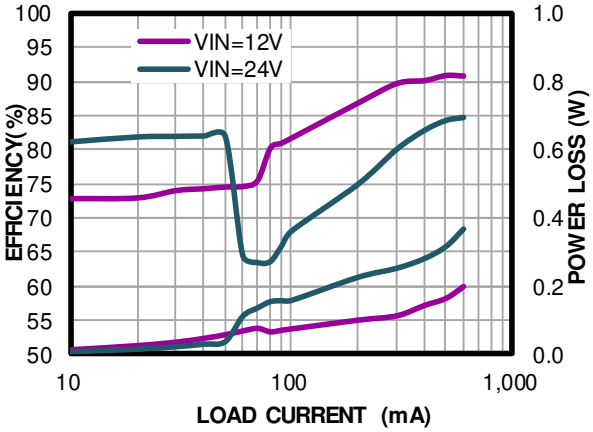
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 3.3V, f_{SW} = 500kHz



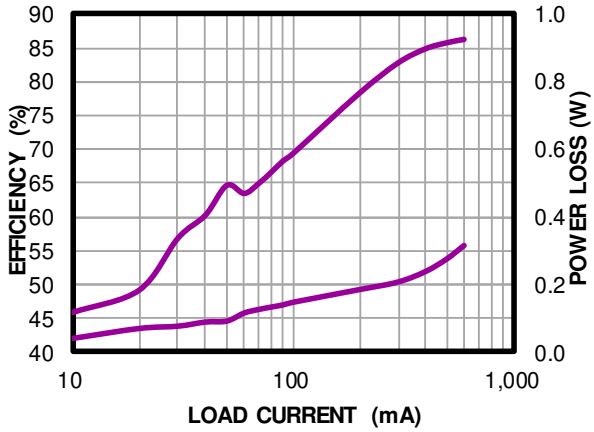
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 3.3V, f_{SW} = 1MHz



Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{IN} = 12V

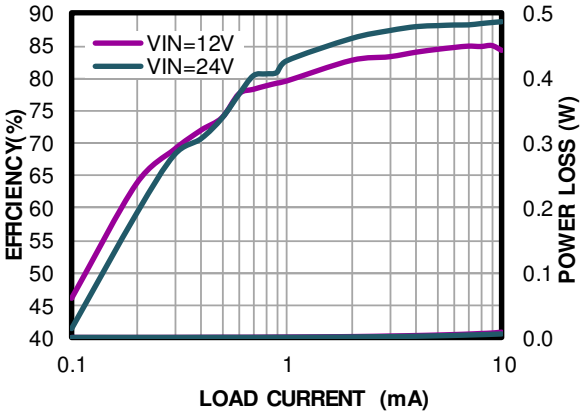


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

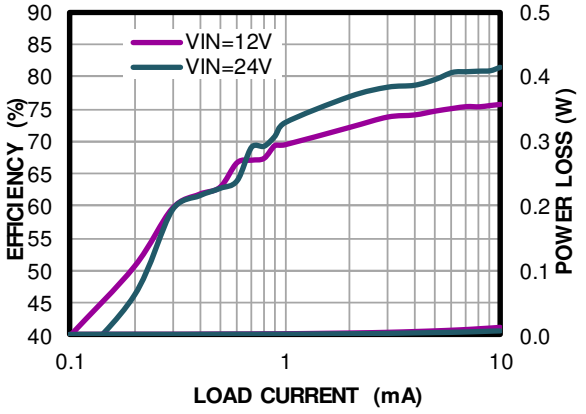
Efficiency vs. Load Current (Extreme Light Load) vs. Power Loss

V_{OUT} = 5v, f_{SW} = 500kHz



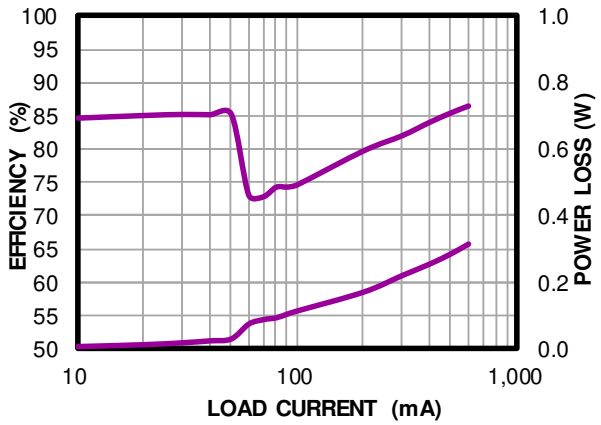
Efficiency vs. Load Current (Extreme Light Load) vs. Power Loss

V_{OUT} = 3.3V, f_{SW} = 500kHz



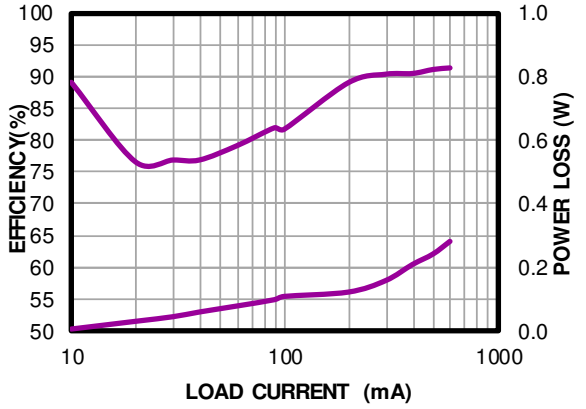
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 2.2µH, V_{IN} = 12V



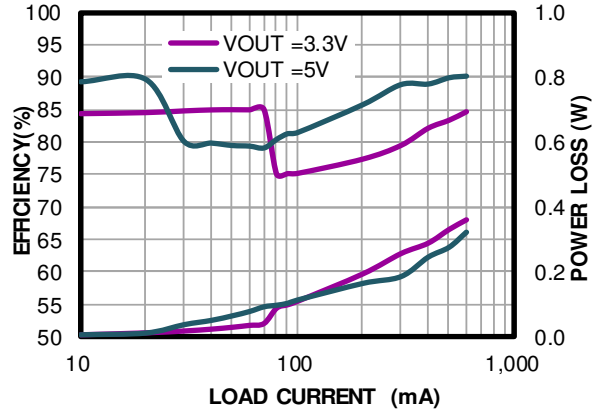
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, V_{IN} = 12V



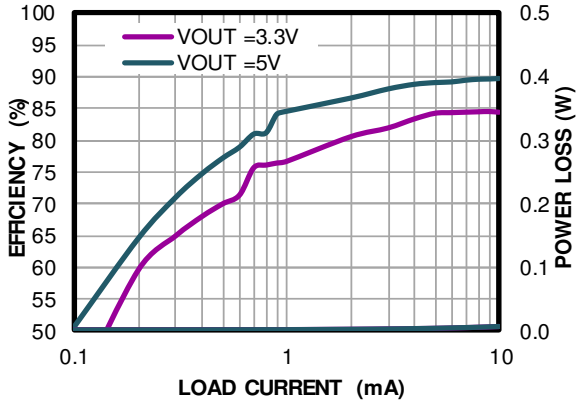
Efficiency vs. Load Current vs. Power Loss

V_{IN} = 14V, f_{SW} = 2.2MHz, L = 2.2µH



Efficiency vs. Load Current (Extreme Light Load) vs. Power Loss

V_{IN} = 14V, f_{SW} = 2.2MHz, L = 2.2µH

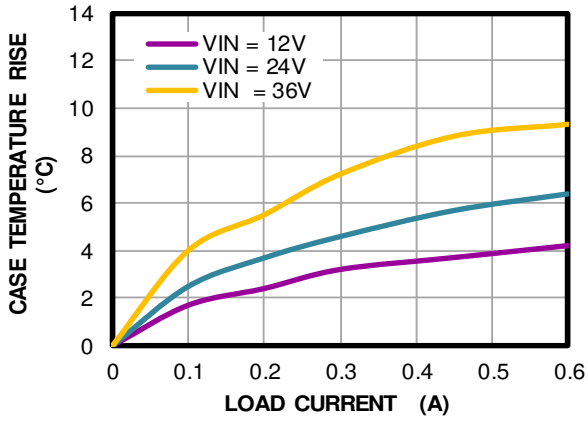


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

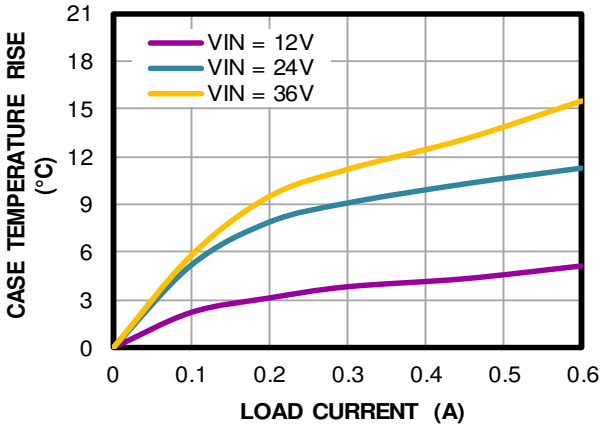
Case Temperature Rise vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 500kHz



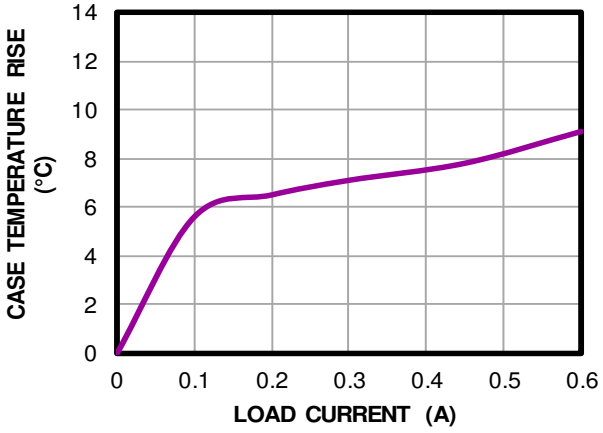
Case Temperature Rise vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 1MHz



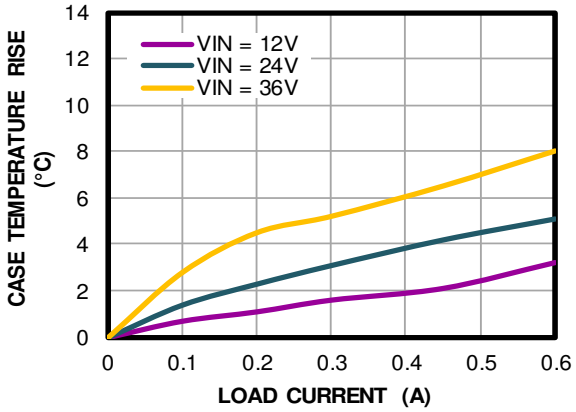
Case Temperature Rise vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{IN} = 12V



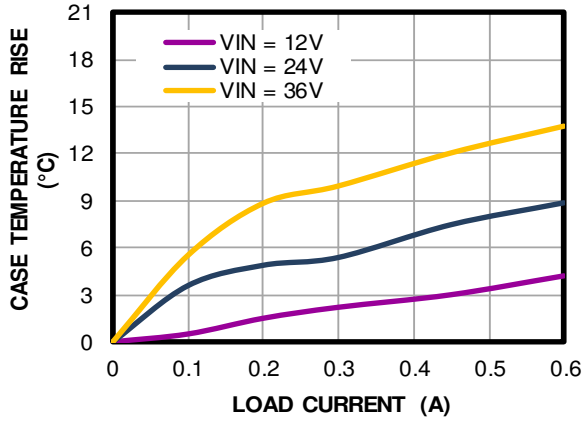
Case Temperature Rise vs. Load Current

V_{OUT} = 5V, f_{SW} = 500kHz



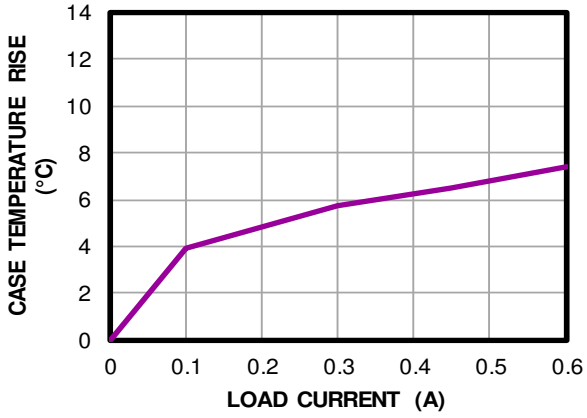
Case Temperature Rise vs. Load Current

V_{OUT} = 5V, f_{SW} = 1MHz



Case Temperature Rise vs. Load Current

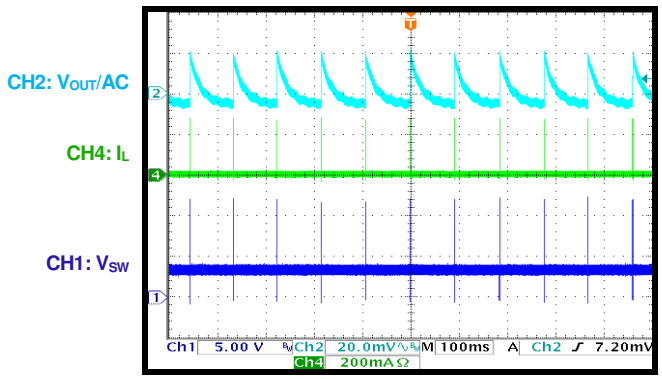
V_{OUT} = 5V, f_{SW} = 2.2MHz, V_{IN} = 12V



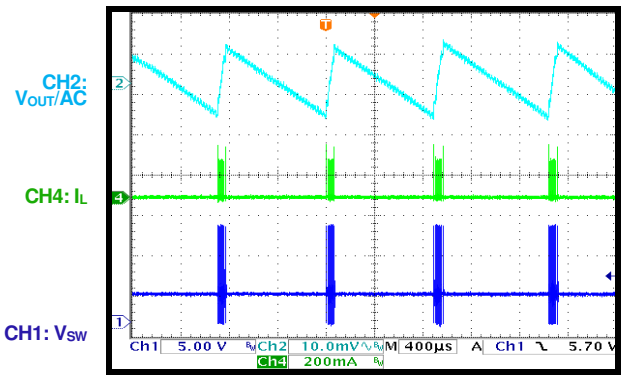
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

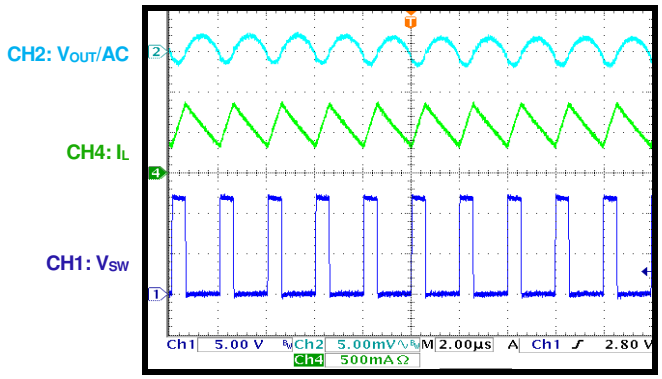
Steady State
I_{OUT} = 0A, AAM mode



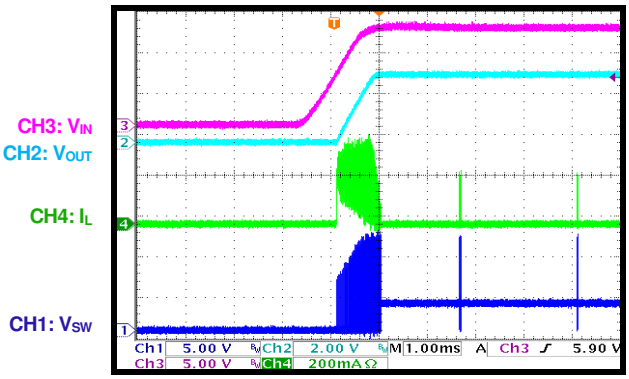
Steady State
I_{OUT} = 1mA, AAM mode



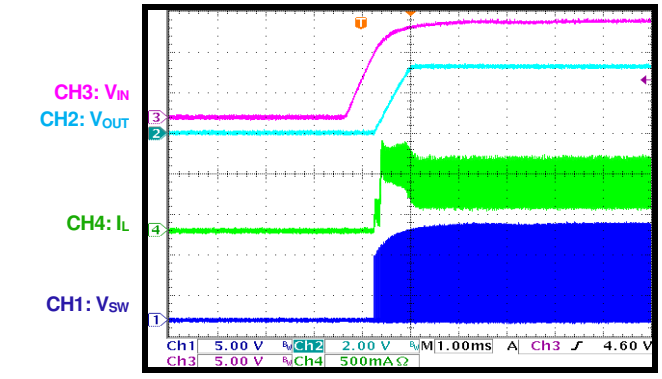
Steady State
I_{OUT} = 0.6A



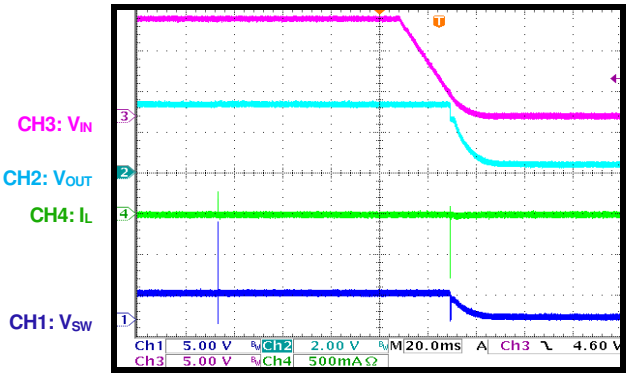
Start-Up through VIN
I_{OUT} = 0A



Start-Up through VIN
I_{OUT} = 0.6A



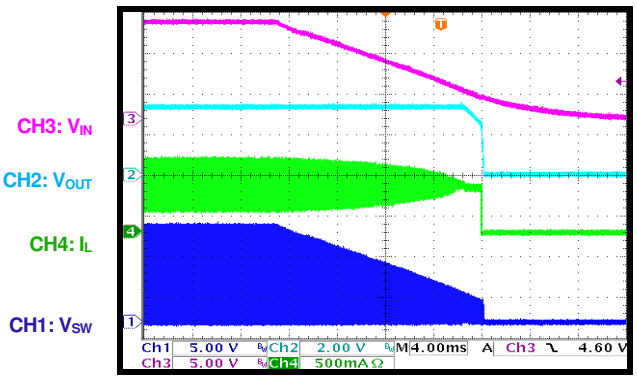
Shutdown through VIN
I_{OUT} = 0A



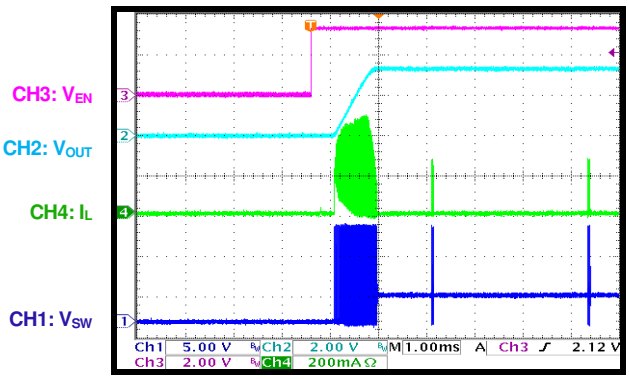
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

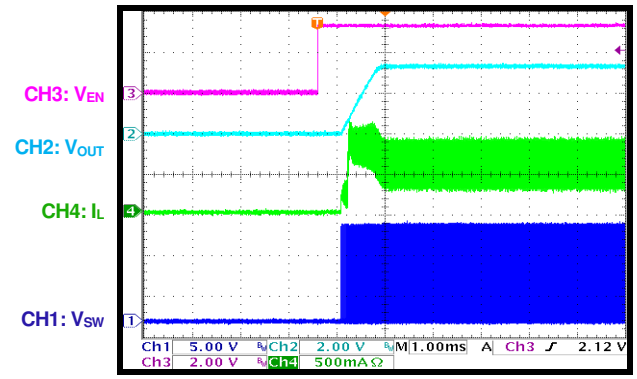
Shutdown through VIN
I_{OUT} = 0.6A



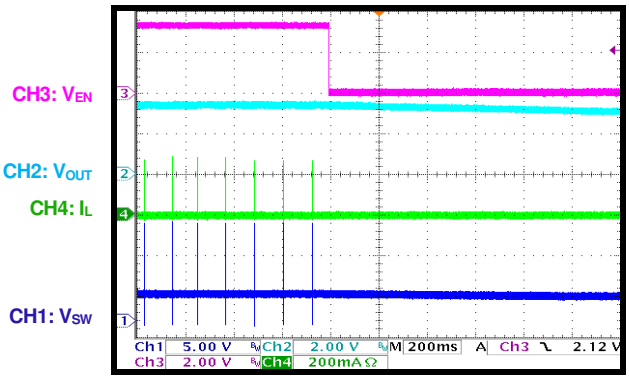
Start-Up through EN
I_{OUT} = 0A



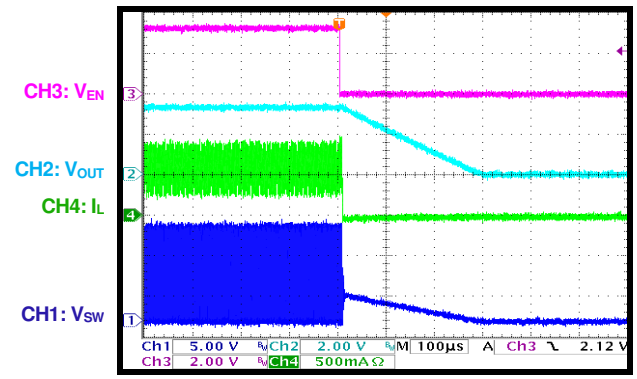
Start-Up through EN
I_{OUT} = 0.6A



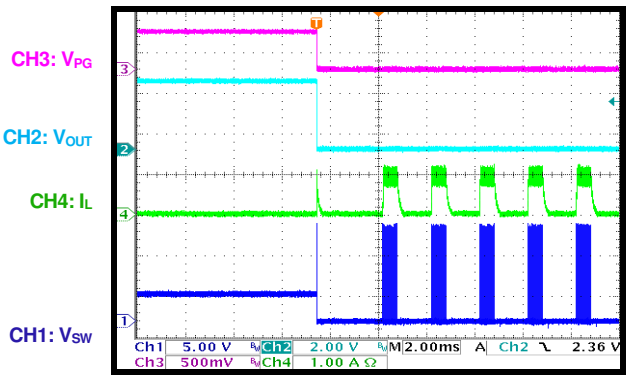
Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 0.6A



SCP Entry
I_{OUT} = 0A to short circuit

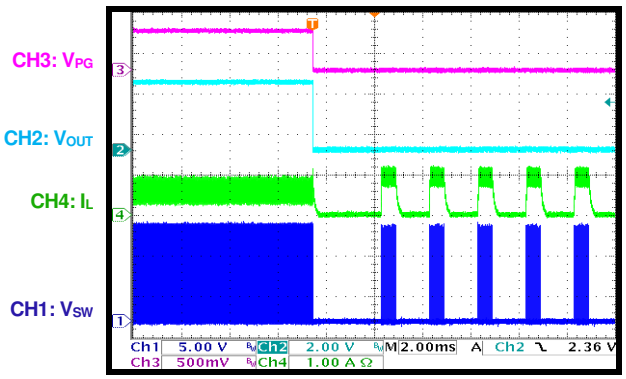


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

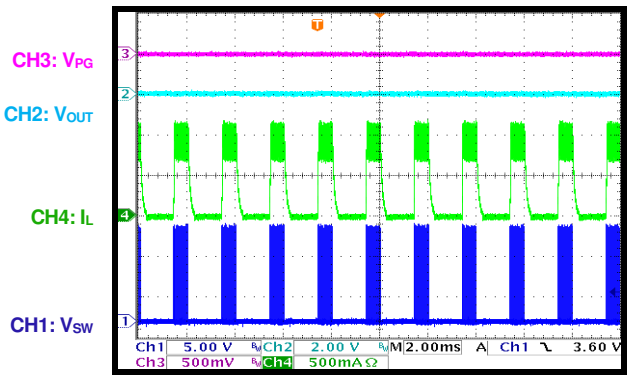
V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

SCP Entry

I_{OUT} = 0.6A to short circuit

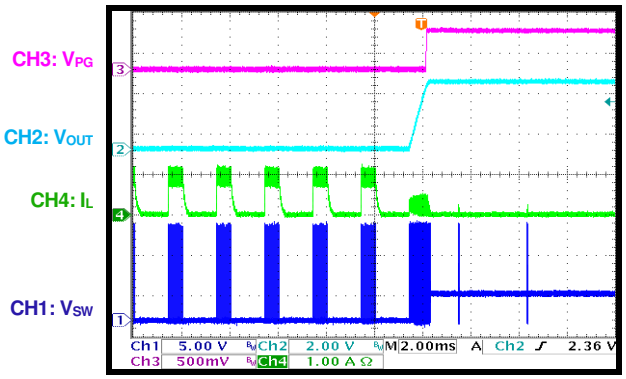


SCP Steady State



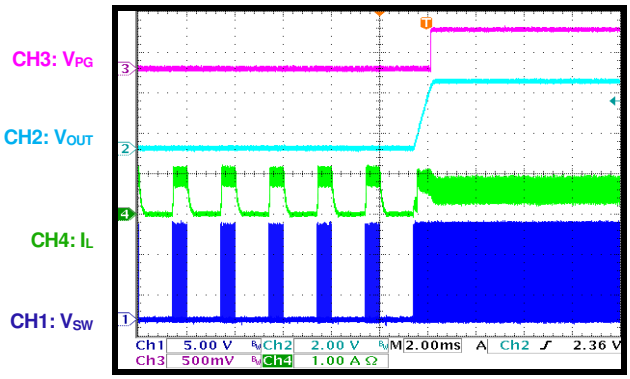
SCP Recovery

Short circuit to I_{OUT} = 0A



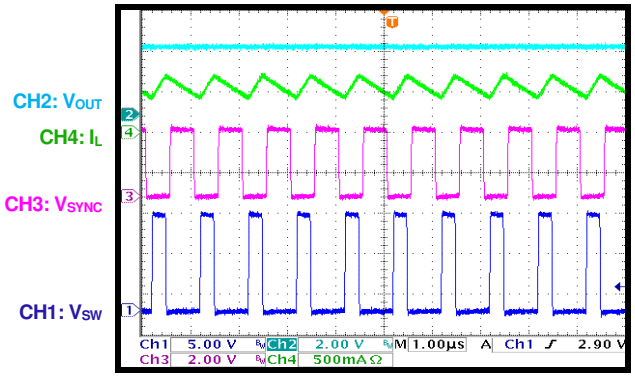
SCP Recovery

Short circuit to I_{OUT} = 0.6A



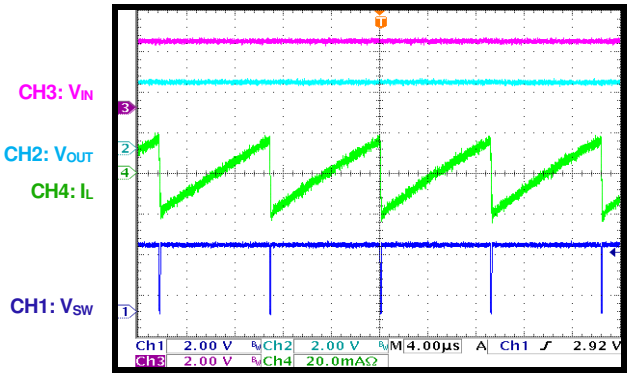
SYNC Operation (In-Phase)

Drive PHASE low, 180° out-of-phase,
I_{OUT} = 0.6A



Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A

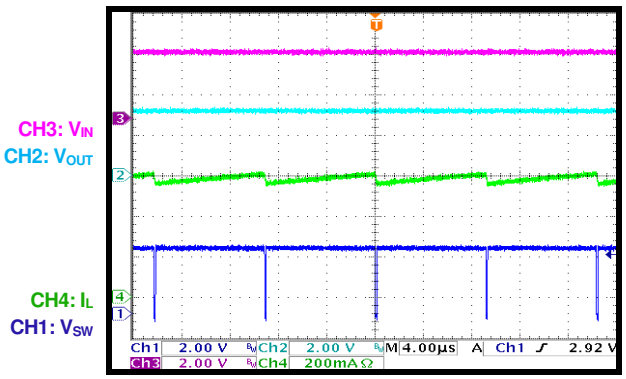


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

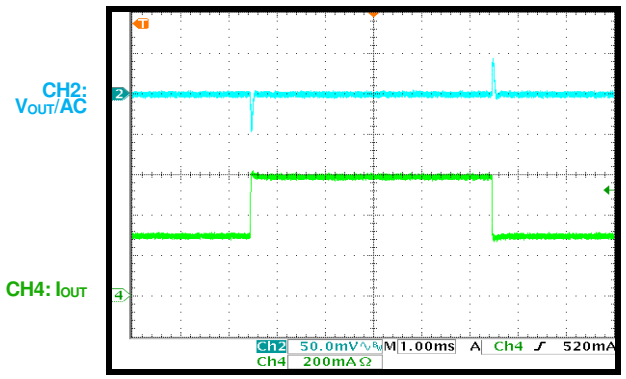
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0.6A



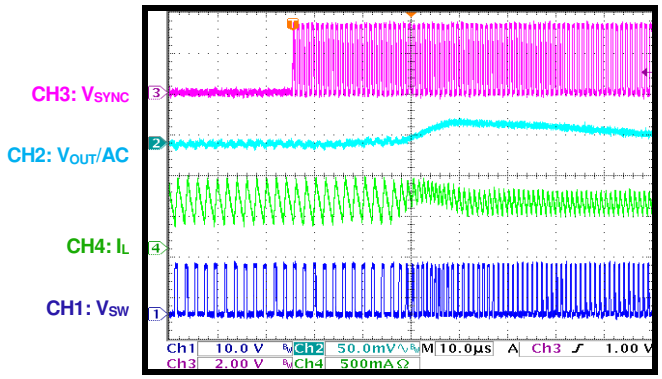
Load Transient

I_{OUT} = 0.3A to 0.6A, 1.6A/µs



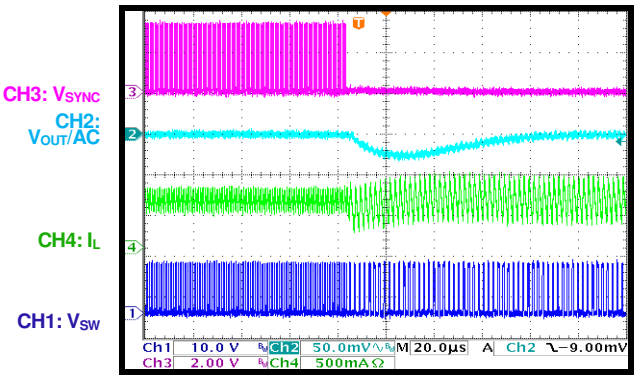
Sync In Transient

I_{OUT} = 0.6A, SYNC = 1MHz



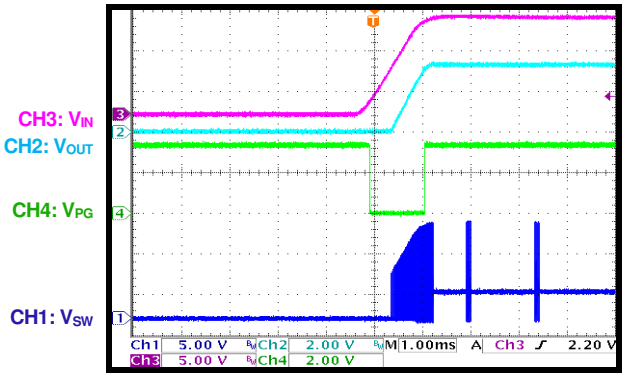
Sync Out Transient

I_{OUT} = 0.6A, SYNC = 1MHz



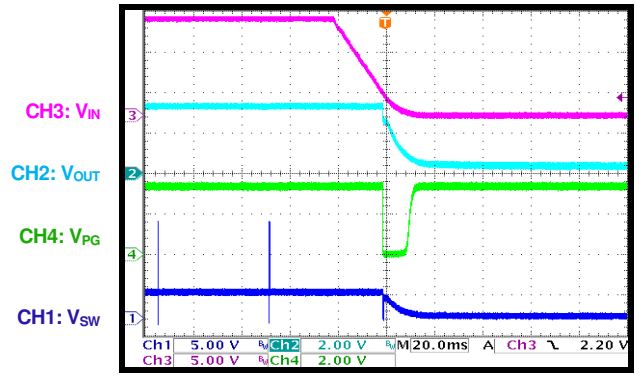
PG in Start-Up through VIN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor



PG in Shutdown through VIN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor

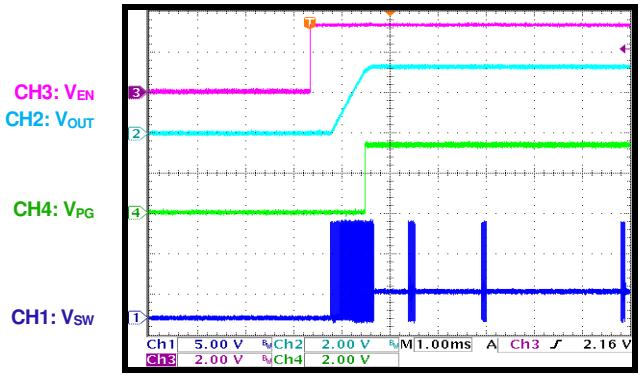


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

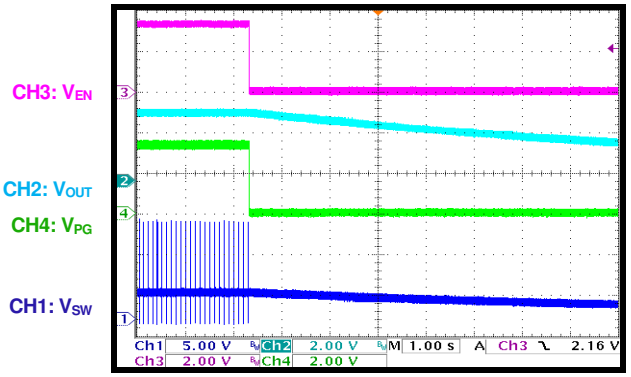
PG in Start-Up through EN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor



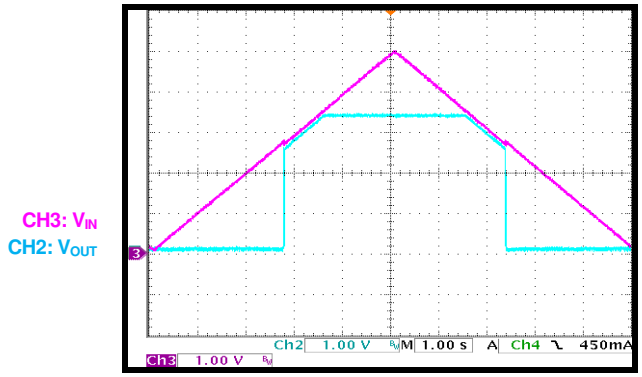
PG in Start-Up through EN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor



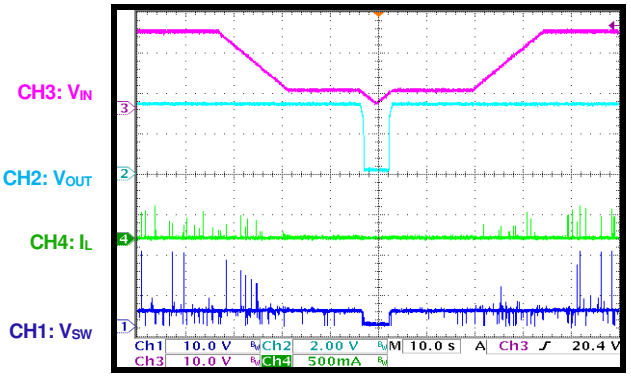
V_{IN} Ramp Up and Down

I_{OUT} = 0.6A



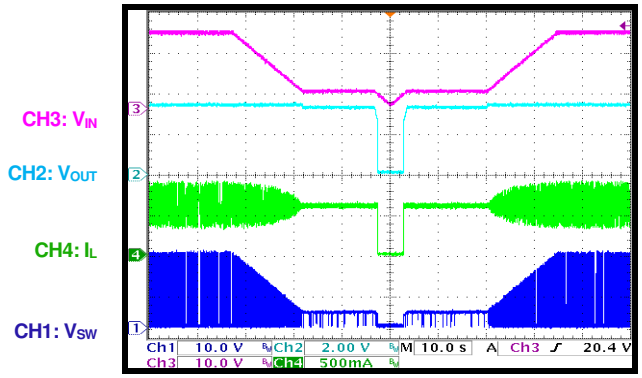
V_{IN} Ramp Up and Down

V_{IN} = 18V to 3.3V to 0V, I_{OUT} = 1mA



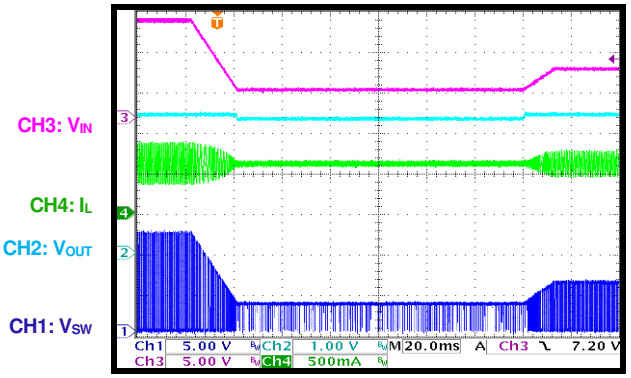
V_{IN} Ramp Up and Down

V_{IN} = 18V to 3.3V to 0V, I_{OUT} = 0.6A



Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 0.6A

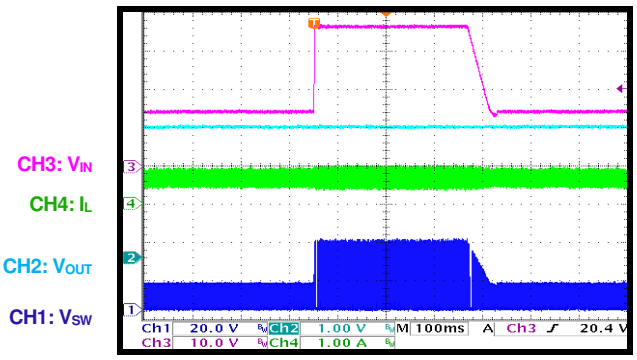


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, AAM, T_A = 25°C, unless otherwise noted.

Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 0.6A



FUNCTIONAL BLOCK DIAGRAM

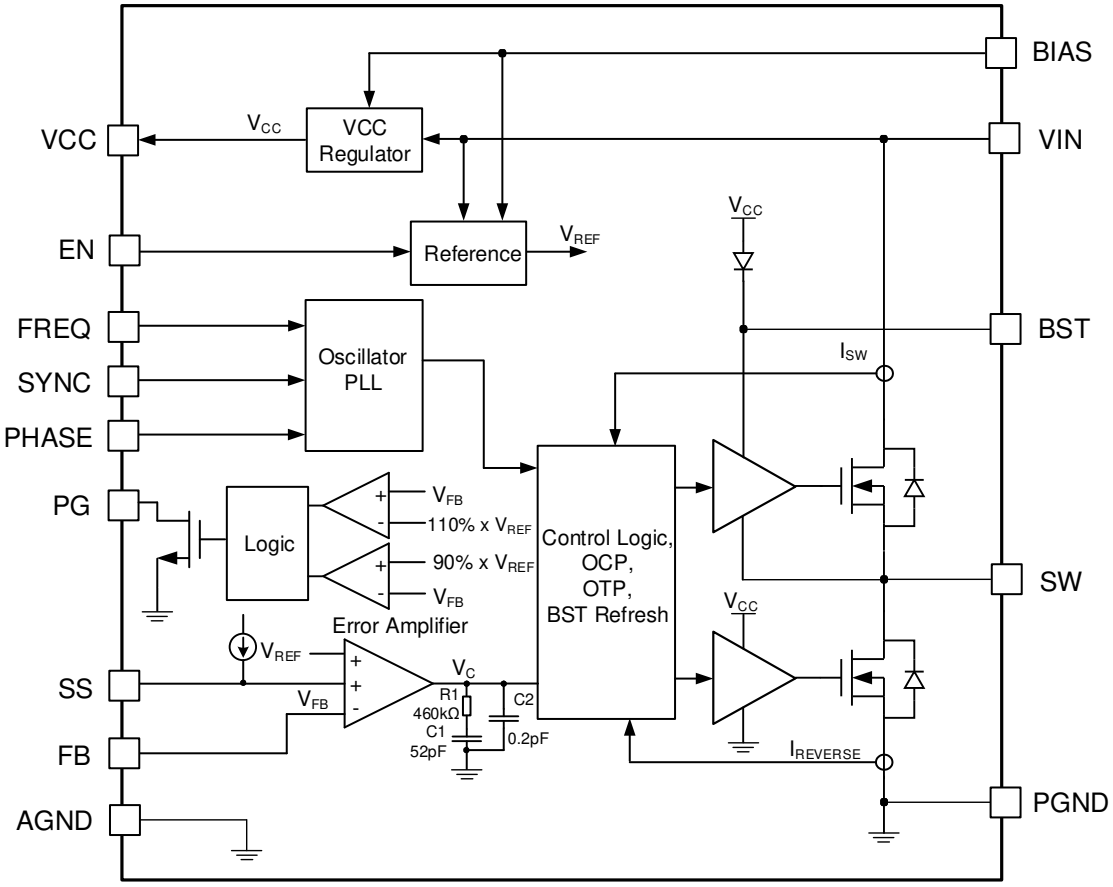


Figure 1: Functional Block Diagram

OPERATION

The MPQ9846 is a synchronous, step-down switching regulator with integrated, internal high-side and low-side power MOSFETs. The MPQ9846 provides 0.6A of highly efficient output current with current mode control.

The device features a wide input voltage range, configurable 350kHz to 2.5MHz switching frequency, external soft start, and precision current limit. Its very low operational quiescent current makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ9846 operates in a fixed-frequency, peak current control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). If the current in the HS-FET does not reach V_{COMP} within one PWM period, the HS-FET remains on, and saves a turn-off operation.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately, and remains on until the next cycle begins. For each turn-on and turn-off in a switching cycle, the HS-FET turns on and off with minimum on and off time limits.

Advanced Asynchronous Mode (AAM)

The MPQ9846 employs advanced asynchronous mode (AAM) to optimize efficiency during light-load or no-load conditions. AAM is enabled by connecting SYNC to a low-level voltage (below 2V) before start-up. SYNC can be used to synchronize switching after start-up.

In AAM, the MPQ9846 first enters nonsynchronous operation while the inductor current approaches zero at light load. If the load further decreases or there is no load, V_{COMP} drops below the AAM voltage (V_{AAM}) and the MPQ9846 enters power-save mode (PSM). The chip enters sleep mode and consumes a very low quiescent current to further improve light-load efficiency.

In PSM, the internal clock is reset when V_{COMP} crosses V_{AAM}, and the crossover time is used as the benchmark of the next clock. When the load increases, and the DC value of V_{COMP} exceeds V_{AAM}, the MPQ9846 adopts discontinuous conduction mode (DCM) or continuous conduction mode (CCM), which both have a constant switching frequency.

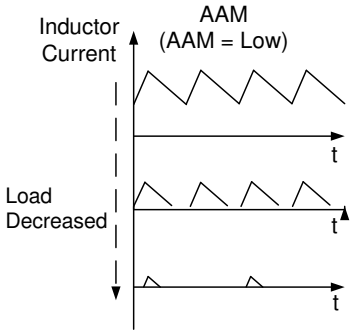


Figure 2: AAM at Different Loads

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage with the internal reference (about 0.8V), and outputs a current proportional to the difference between the two values. This output current charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Bootstrap Charging

The 0.1µF to 1µF bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below regulation, a PMOS pass transistor connected from VIN to BST turns on. The charging current path is from VIN to BST to SW. An external circuit should provide enough voltage headroom to facilitate charging.

When the HS-FET is on, VIN is about equal to SW, so the bootstrap capacitor cannot be charged. During higher duty cycle operation, the time period available for bootstrap charging is shortened, so the bootstrap capacitor may not charge sufficiently. If the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, additional

external circuitry can be used to ensure that the bootstrap voltage is within the normal operation range.

Low-Dropout Operation (BST Refresh)

To improve dropout, the MPQ9846 is designed to operate at close to 100% duty cycle while the BST-to-SW voltage exceeds 2.5V. When the voltage from BST-to-SW drops below 2.5V, the HS-FET turns off using an under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM or PSM, the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. This makes the effective duty cycle of the switching regulator high.

The effective duty cycle during the dropout of the regulator is mainly influenced by: voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

In low-dropout mode, V_{OUT} cannot be regulated at its set voltage. Instead, V_{COMP} ramps up continuously until it is clamped at a high-level voltage. If V_{IN} rises at an extremely fast rate, and the device skips out during low-dropout mode, VCOMP may not respond within the limited time offered by the loop bandwidth, and V_{COMP} generates overshoot on V_{OUT}. Adjusting the loop response faster or using greater capacitance on COUT can reduce the overshoot.

Internal Regulator

Most of the internal circuitry is powered by the 2.6V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When V_{IN} exceeds 3V, the output of the regulator is in full regulation. When V_{IN} is below 3V, the output degrades.

For better thermal performance, connect BIAS to an external 5V source. VCC and the internal circuit are powered by BIAS. Since there is an internal diode between BIAS and the internal circuit, float BIAS or connect BIAS to GND if it is not being used.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off by either the external logic H/L signal or by configuring the VIN under-voltage lockout (UVLO) threshold (see Figure 3).

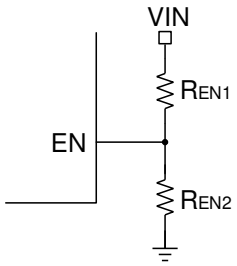


Figure 3: Enable Divider Circuit

When EN is pulled below its threshold voltage, the MPQ9846 is forced into the lowest shutdown current mode. Pulling EN above the EN threshold voltage turns the MPQ9846 on. With a high enough V_{IN}, the MPQ9846 can be enabled and disabled by EN. With the internal current source, this circuit can generate a configurable VIN UVLO and hysteresis. Do not float EN.

Configurable Frequency (FREQ)

The MPQ9846 oscillating frequency can be configured either via an external resistor (R_{FREQ}) from FREQ to GND, or via a logic-level SYNC signal from the SYNC pin. The value of (R_{FREQ}) can be calculated with Equation (1):

$$R_{FREQ}(k\Omega) = \frac{170000}{f_{SW}^{1.11}(kHz)} \quad (1)$$

Through FREQ/SYNC, the chip can be synchronized to an external clock ranging from 350kHz to 2.5MHz.

SYNC and PHASE

Using the SYNC pin, the internal oscillator frequency can be synchronized to an external clock ranging from 350kHz to 2.5MHz. The external clock should be at least 250kHz greater than the R_{FREQ} set frequency. Ensure that the high amplitude of the SYNC clock exceeds 1.8V, and that the low amplitude is below 0.4V.

There is no pulse width requirement, but there is always parasitic capacitance on the pad. If the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. It is recommended to make the pulse width longer than 100ns.

PHASE is used when two or more MPQ9846 devices are in parallel and using the same SYNC clock. Pulling PHASE high forces the MPQ9846s to operate in-phase with the SYNC clock. Pulling PHASE low forces the devices to operate 180° out-of-phase with the SYNC clock.

By setting different voltages for PHASE, two devices can operate 180° out-of-phase to reduce the total input current ripple. This allows a smaller input bypass capacitor to be used (see Figure 4). The PHASE rising threshold is about 2.5V with a 400mV hysteresis.

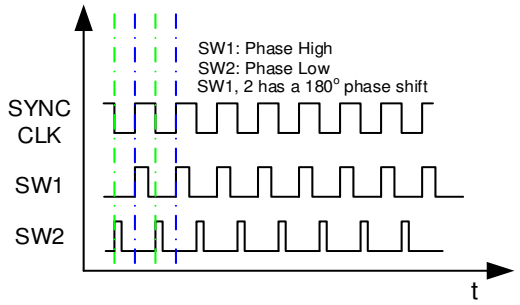


Figure 4: In-Phase and 180° Out-of-Phase

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, an internal current source begins charging the external soft-start capacitor.

The internal SS voltage (V_{SSI}) rises with the SS voltage (V_{SS}). However, when compared to V_{SS}, V_{SSI} has a 0.5V offset and a delay. When V_{SS} is below 0.5V, V_{SSI} is 0V. V_{SSI} rises from 0V to 0.8V when V_{SS} rises from 0.5V to 1.6V. At this time, the error amplifier uses V_{SSI} as the reference, meaning the output voltage ramps up from 0V to the regulated value while V_{SSI} rises. When V_{SS} reaches 1.6V, V_{SSI} is 0.8V. This overrides the internal V_{REF}, so the error amplifier uses the internal V_{REF} as the reference.

The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{C_{ss}(nF) \times 1.1V}{I_{ss}(\mu A)} \quad (2)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 10μA SS charge current.

There is also an internal, fixed 0.7ms soft start. The final SS time is determined by whichever of the two following times is longer: 0.7ms, or the external SS setting time.

SS can be used for tracking and sequencing.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} - 150mV during start-up, the output has a pre-biased voltage, and neither the HS-FET nor LS-FET turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent thermal runaway. When the silicon die temperature exceeds its upper threshold (about 170°C), the power MOSFETs shut down. When the temperature drops below its lower threshold (about 150°C), thermal shutdown is removed and the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. The current is then fed to the high-speed current comparator for current mode control. The current comparator uses this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the power switch current with V_{COMP}. When the sensed current exceeds V_{COMP}, the comparator output goes low to turn off the HS-FET. The maximum current of the internal power MOSFET is cycle-by-cycle internally limited.

Hiccup Protection

When the output is shorted to ground and the output voltage drops below 55% of its nominal output, the IC shuts down momentarily and begins discharging the soft-start (SS) capacitor. The IC restarts with a full soft start when the SS capacitor is fully discharged. This hiccup process repeats until the fault is removed.

Start-Up and Shutdown

If both VIN and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer keeps the power MOSFET off for about 50µs to blank any start-up glitches. When the soft-start (SS) block is enabled, the SS output is held low to ensure that the rest of the circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN going low, VIN going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ9846 includes an open-drain power good (PG) output that indicates whether the regulator output is within ±10% of its nominal output range. When the output voltage moves outside of this range, the PG output is pulled to ground.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 5).

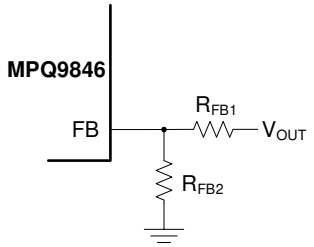


Figure 5: Feedback Network

Choose R_{FB1} to be about 40kΩ. R_{FB2} can then be calculated with Equation (3):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	41.2 (1%)	13 (1%)
5	68.1 (1%)	13 (1%)

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductor value is to make inductor ripple current about 30% of the maximum load current. The inductance value can then be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be about 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (5):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (7):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For the best results, use low-ESR capacitors to maintain a low output voltage ripple. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ9846 can be optimized for a wide range of capacitance and ESR values.

VIN Under-Voltage Lockout (UVLO) Setting

The MPQ9846 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 2.8V, while the falling threshold is about 2.65V. For applications that require a higher UVLO point, place an external resistor divider between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 6).

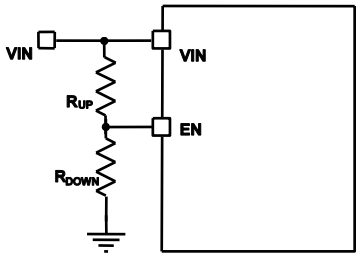


Figure 6: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (12) and Equation (13), respectively:

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (12)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (13)$$

Where V_{EN_RISING} is 1.05V, and $V_{EN\_FALLING}$ is 0.93V.

External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can power the external bootstrap diode. VCC or VOUT is recommended to be the power supply in the circuit (see Figure 7).

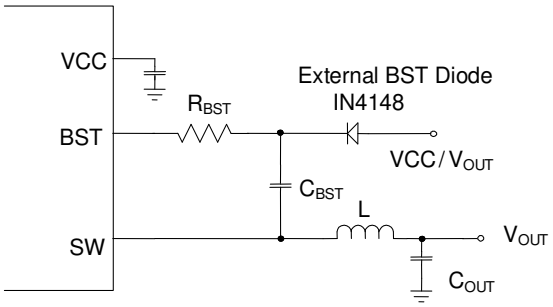


Figure 7: External Bootstrap Diode and Resistor

The recommended external BST diode is IN4148, and the recommended BST capacitor value is between 0.1µF and 1µF.

A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and help prevent voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high V_{IN}. A higher resistance is better at reducing SW spikes but compromises efficiency. To make a tradeoff between EMI and efficiency, it is recommended to keep R_{BST} below 20Ω.

Hot-Plug Application

In a hot-plug application, the VIN pin of the IC may turn on and off frequently before the power supply can establish a connection with the IC. In applications where the input power turns on and off frequently, the BST capacitor may have a residual voltage when the IC is turned on. This may turn on high-side MOSFET (HS-FET) for a short time before VCC can rise high enough, which causes an unexpected overshoot on VOUT.

To protect VIN, hot-plug applications are not recommended. If a hot-plug application must be initiated, use a small BST capacitor (e.g. 47nF), a large VCC capacitor (e.g. 4.7µF), and a large PG resistor (e.g. 1MΩ) to reduce the overshoot risk. Contact an MPS FAE to confirm the design.

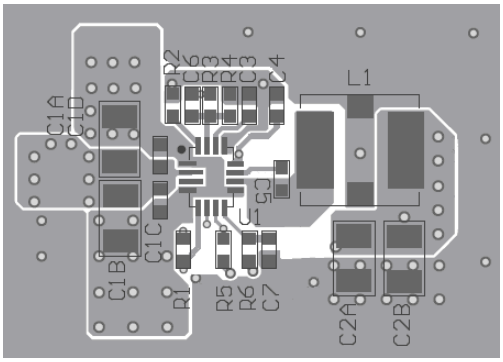
PCB Layout Guidelines (8)

Efficient PCB layout is critical for stable operation, especially regarding the input capacitor placement. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 8 and follow the guidelines below:

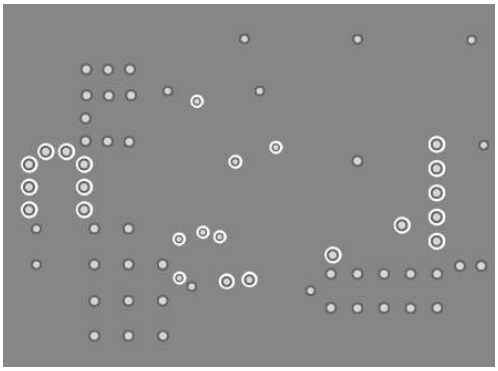
1. Use a large ground plane to connect directly to PGND.
2. Connect PHASE to GND for a symmetric input structure if in-phase operation is not used.
3. Both SW pins (pin 3 and pin 10) are internally connected. It is safe for them to be connected on the layout or not connected.
4. Leave SW (pin 3) floating for a shorter PGND (pin 4) and PHASE trace, and a smaller input hot loop.
5. Add vias near PGND if the bottom layer is a ground plane.
6. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
7. Place the ceramic input capacitors as close as possible to VIN and PGND to minimize high-frequency noise. This is especially important for the small package size (0603) input bypass capacitor.
8. Keep the connection between the input capacitor and VIN as short and wide as possible.
9. Place the VCC capacitor as close as possible to VCC and GND.
10. Route SW and BST away from sensitive analog areas, such as FB.
11. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
12. Use multiple vias to connect the power planes to the internal layers.

Note:

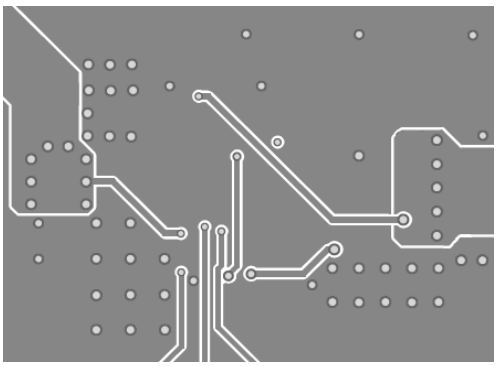
8) The recommended PCB layout is based on Figure 9.



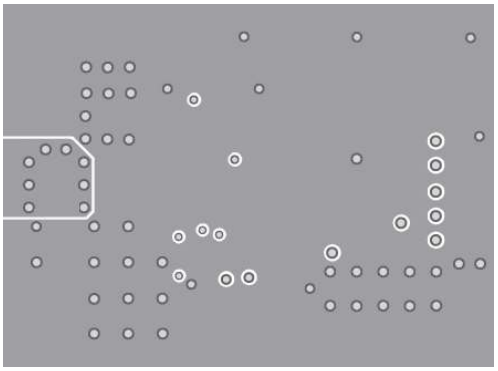
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

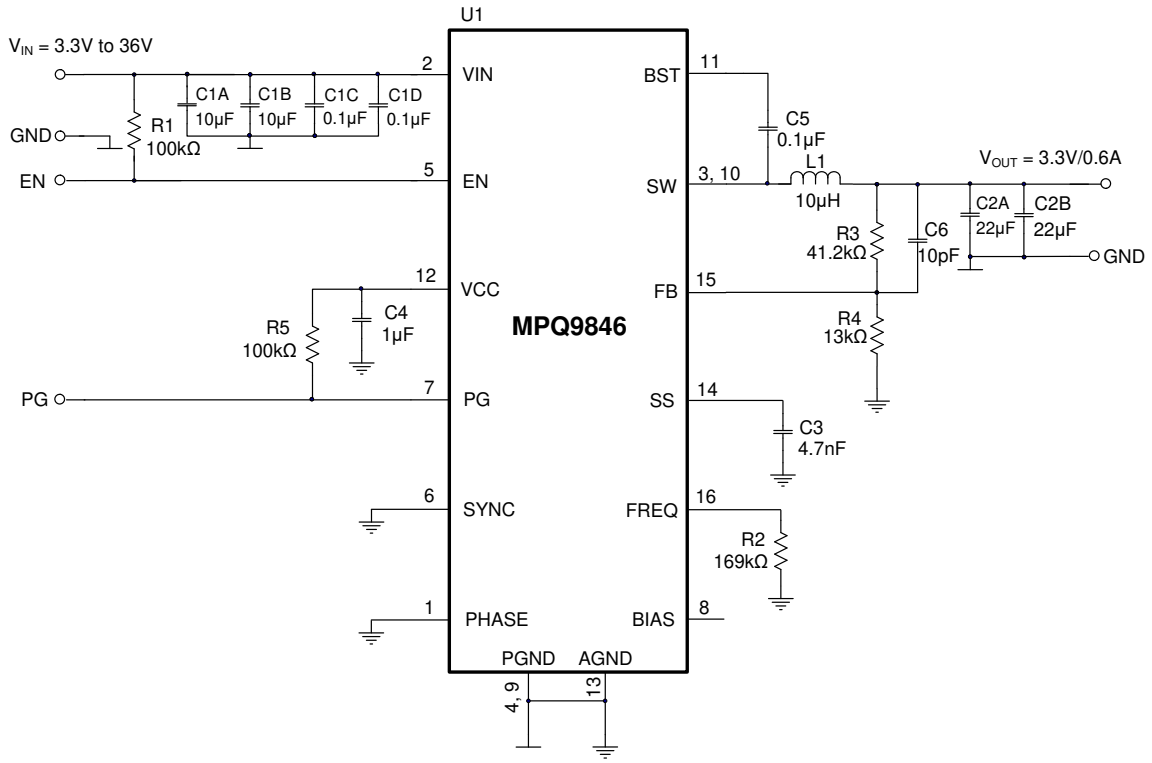


Figure 9: V_{OUT} = 3.3V, f_{SW} = 500kHz

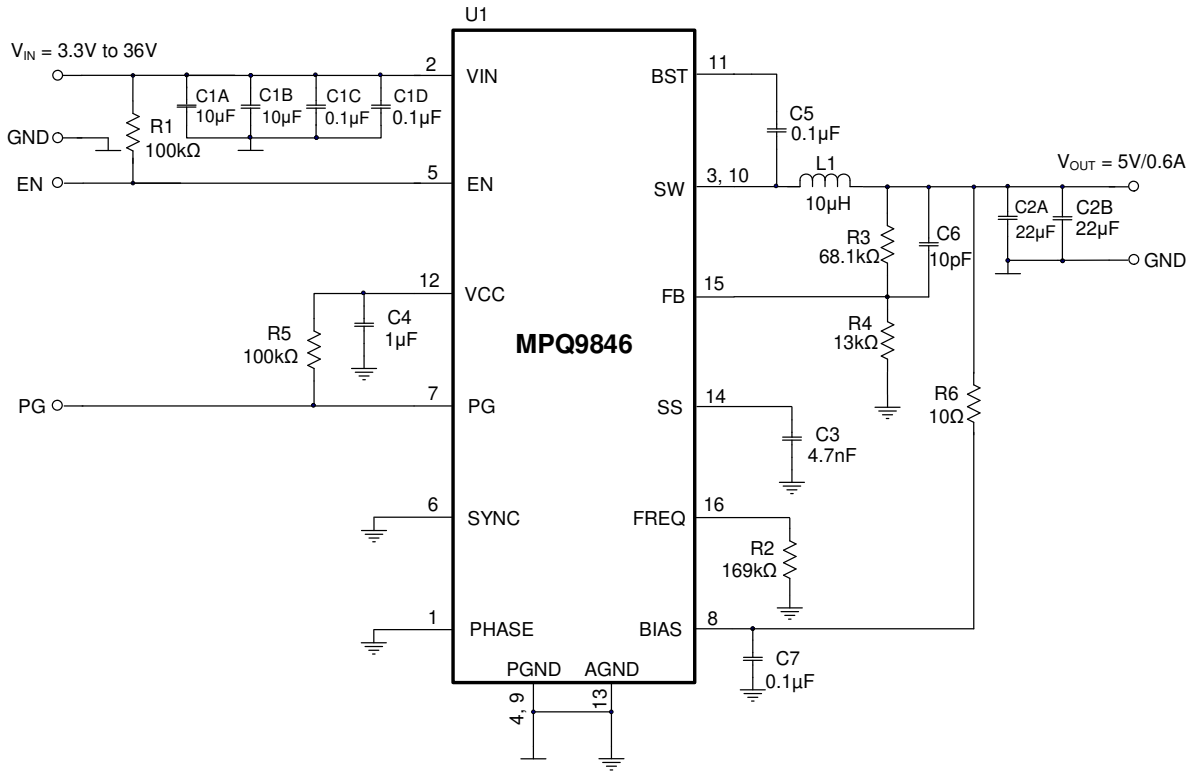


Figure 10: V_{OUT} = 5V, f_{SW} = 500kHz

TYPICAL APPLICATION CIRCUITS *(continued)*

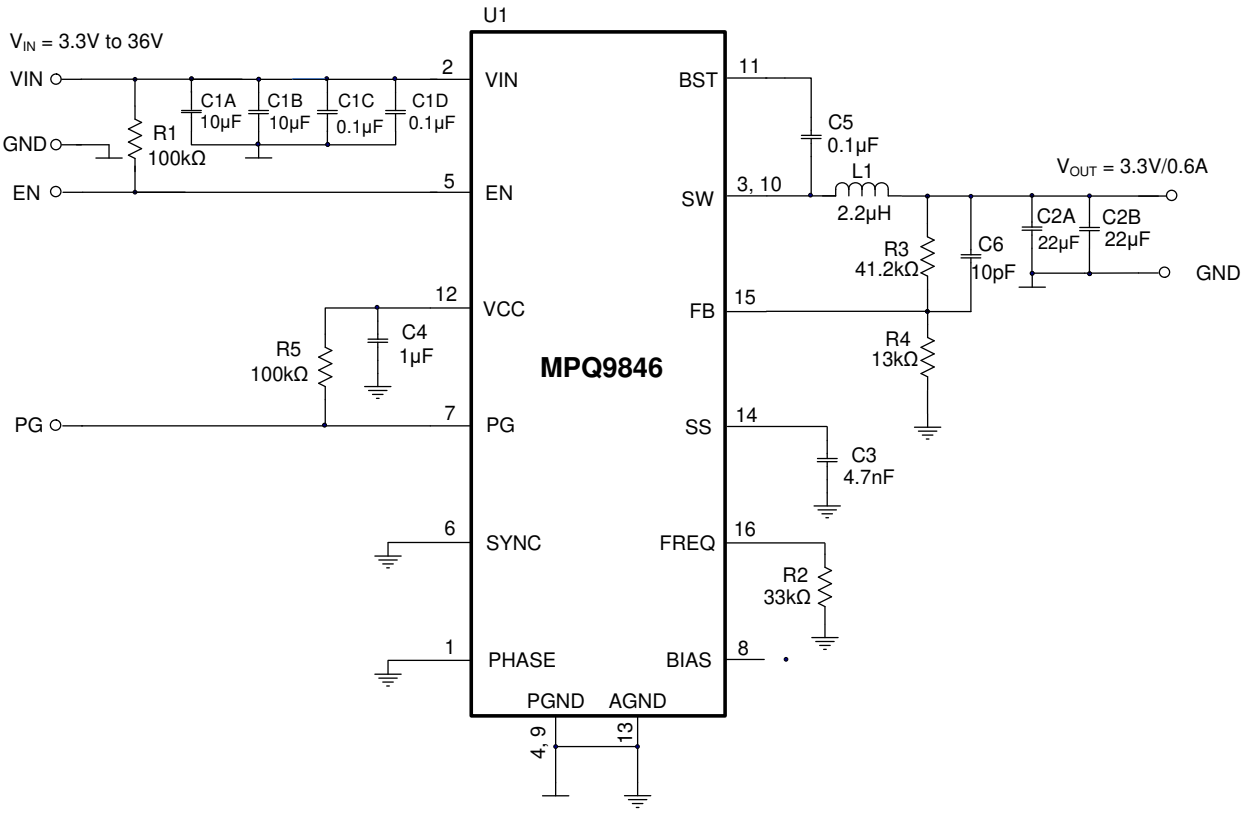


Figure 11: V_{OUT} = 3.3V, f_{SW} = 2.2MHz

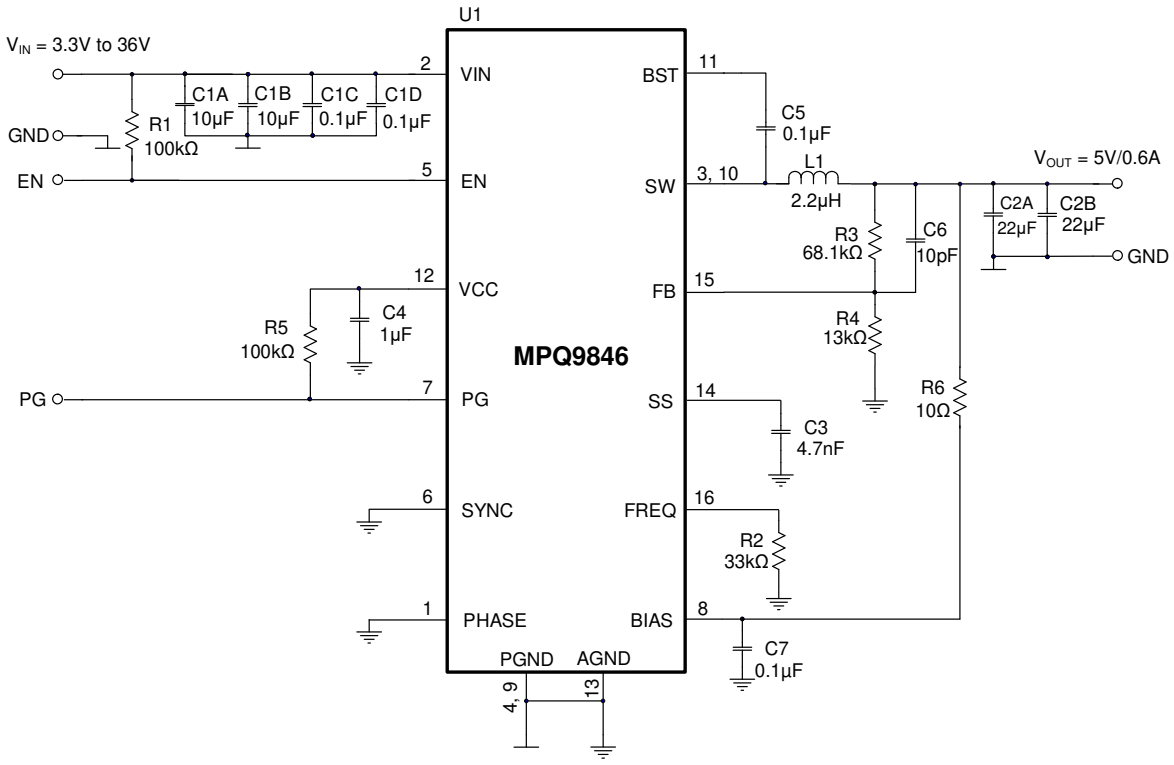


Figure 12: V_{OUT} = 5V, f_{SW} = 2.2MHz

TYPICAL APPLICATION CIRCUITS *(continued)*

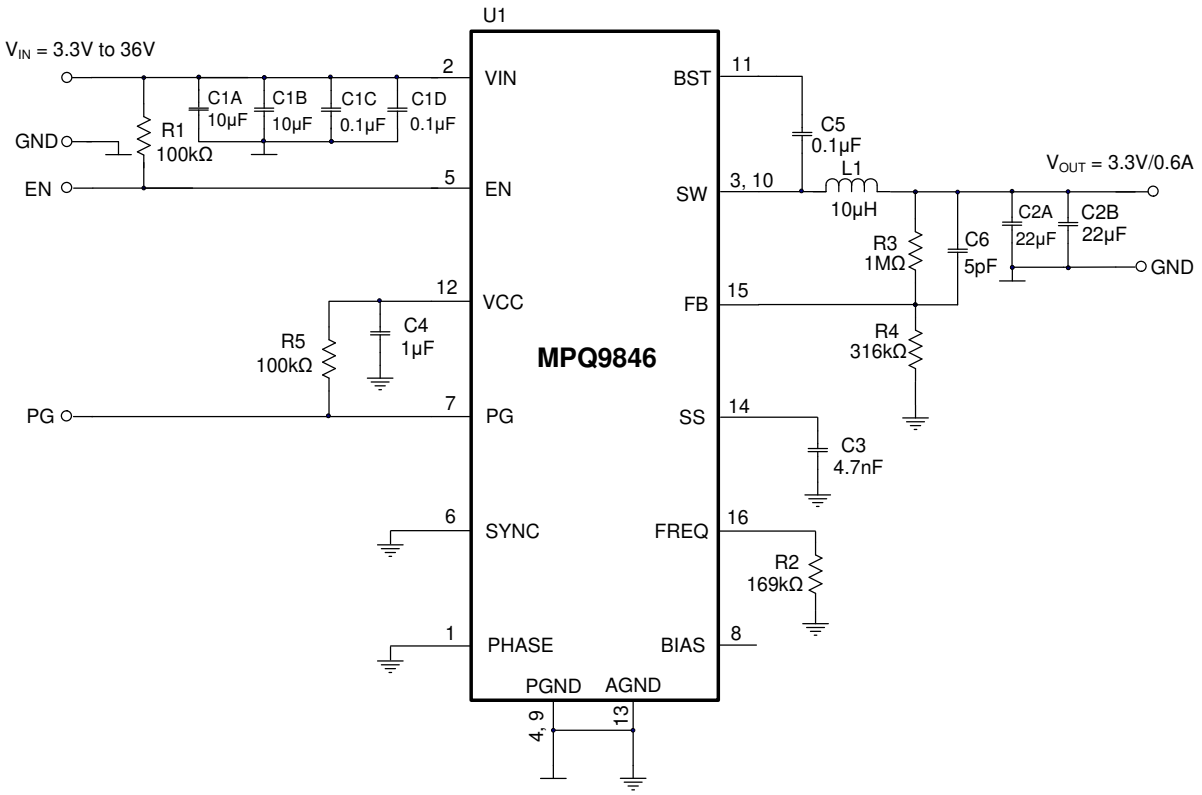


Figure 13: V_{OUT} = 3.3V, f_{SW} = 500kHz for Large FB Resistor Divider Application

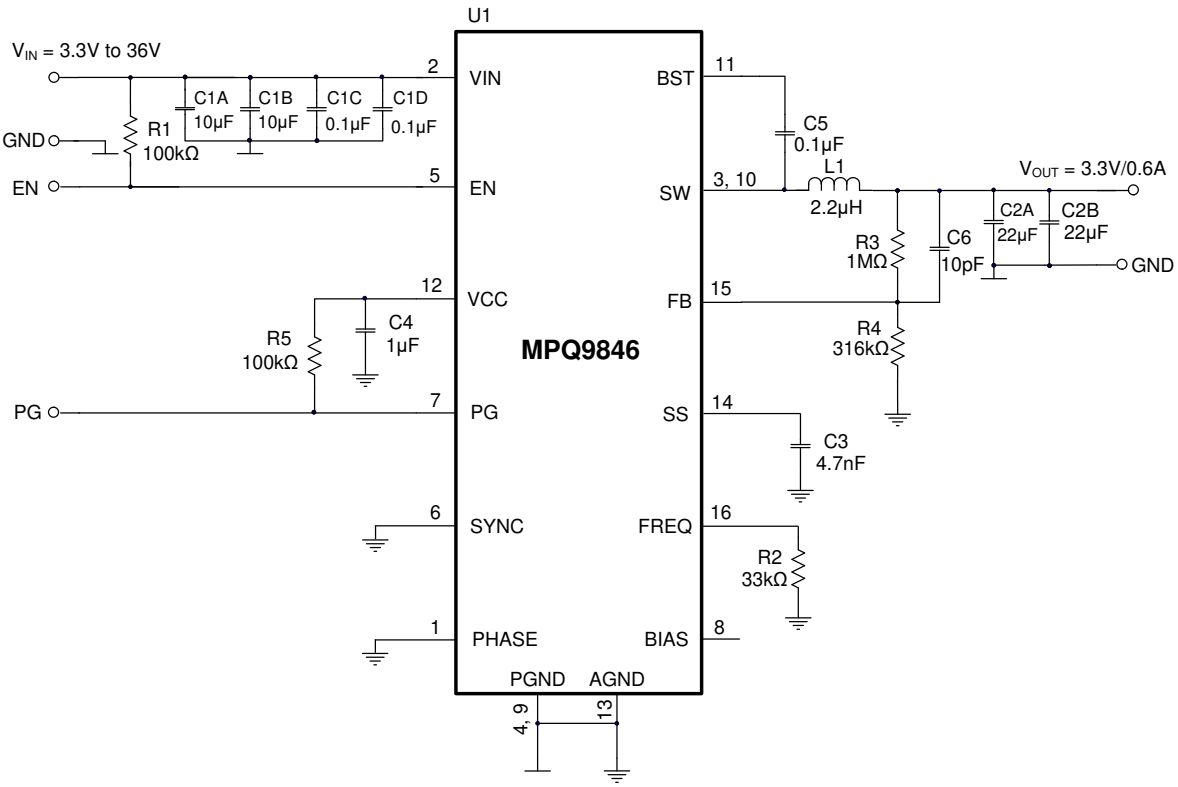


Figure 14: V_{OUT} = 3.3V, f_{SW} = 2.2MHz for Large FB Resistor Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

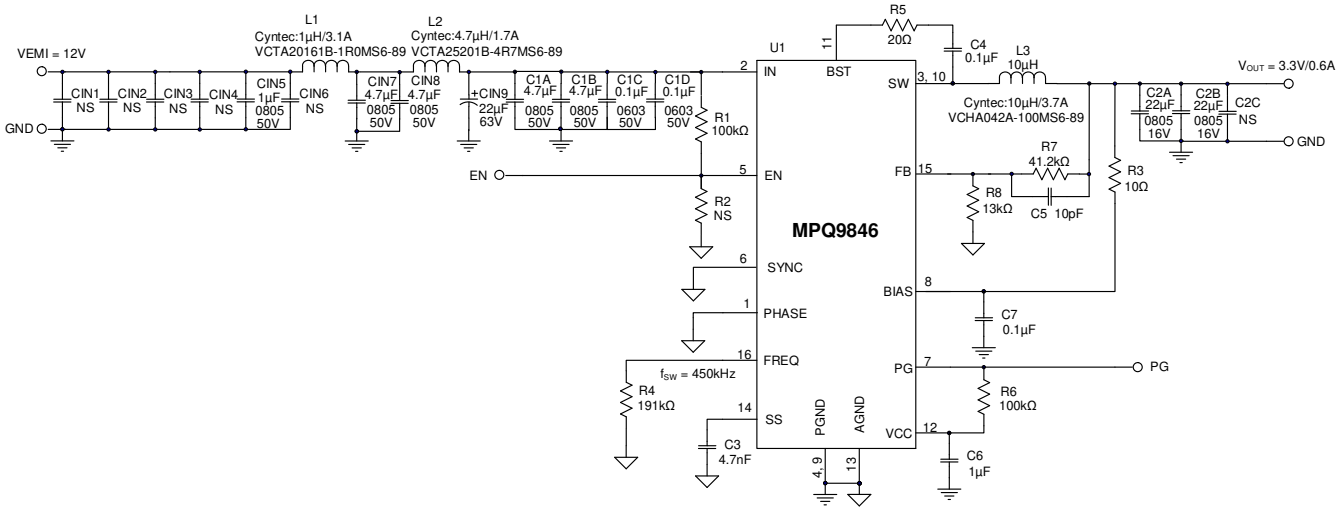
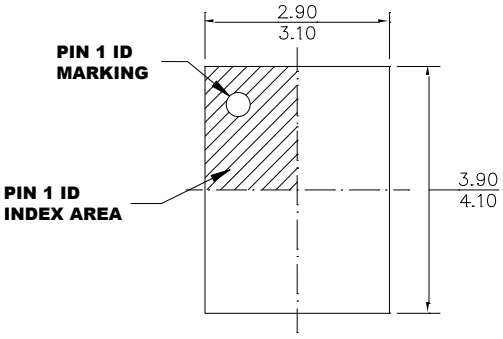


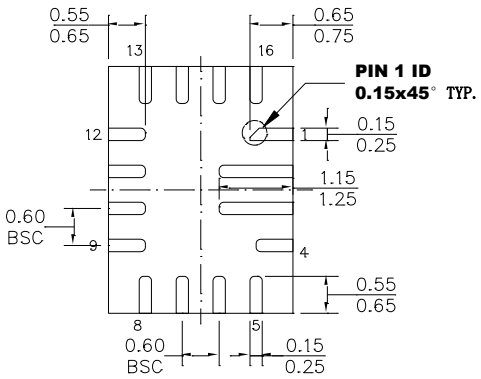
Figure 15: Application Circuit with EMI Filter when V_{OUT} = 3.3V/0.6A, f_{SW} = 450kHz

PACKAGE INFORMATION

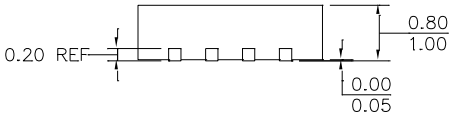
QFN-16 (3mmx4mm)



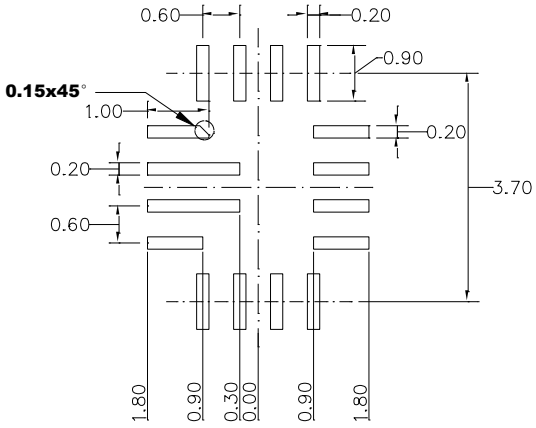
TOP VIEW



BOTTOM VIEW



SIDE VIEW

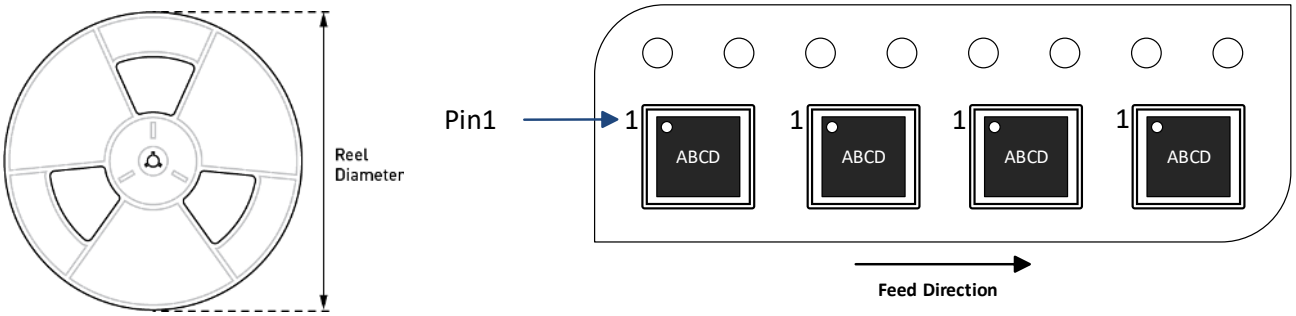


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ9846GL-AEC1–Z	QFN-16 (3mmx4mm)	5000	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	4/28/2020	Initial Release	-