ADS7066EVM-PDK Evaluation Module

The ADS7066 Evaluation Module (EVM) Performance Demonstration Kit (PDK) allows users to evaluate the functionality of Texas Instruments' ADS7066 16-bit, eight-channel programmable successive approximation register (SAR) analog-to-digital converter (ADC). The ADS7066 device showcases eight inputs, each configurable to an analog input, digital output, or digital input. The device supports an internal reference as well as operation with an external reference. This user's guide describes both the hardware platform showcasing the ADS7066 device and the graphical user interface (GUI) software used to configure the various modes of operation of this device. It includes complete circuit descriptions, schematic diagrams, and a bill of materials. The EVM-PDK eases the evaluation of the ADS7066 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface.

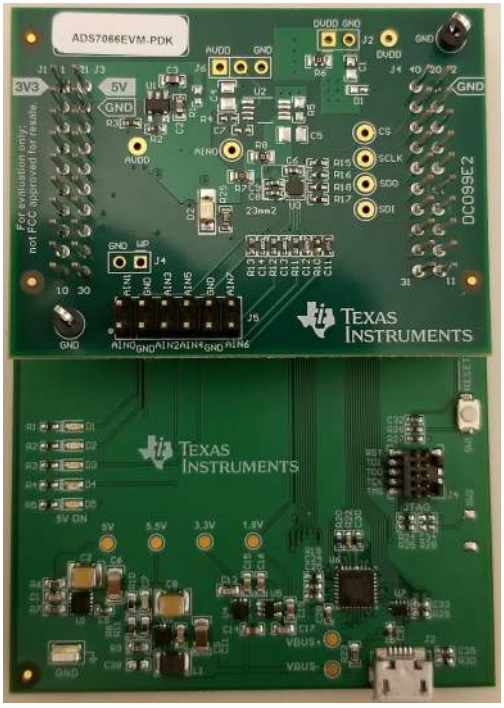

Figure 1. ADS7066EVM-PDK Assembled

The following related documents are available through the Texas Instruments website at www.ti.com.

Table 1. Related Documentation

Device	Literature Number
ADS7066	SBAS928
REF6025	SBOS708B
OPA325	SBOS637D
TPS78001	SBVS083E

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1 Introduction

The ADS7066 EVM is a fully-assembled evaluation platform designed to highlight the ADS7066 features and various modes of operation that make this device suitable for ultra-low-power, small-size sensor monitor applications.

The accompanying Precision ADC Motherboard (PAMBoard) development kit is used as a USB-to-PC GUI communication bridge. This kit also serves as an example implementation of a master microcontroller (MCU) to communicate with the ADS7066 device through a serial-peripheral interface (SPI).

NOTE: The ADS7066 EVM requires an external master controller to evaluate the ADS7066 device.

The PAMBoard is controlled by commands received from the ADS7066 GUI, and returns data to the GUI for display and analysis. If the PAMBoard is not used, the EVM plug-in module format allows for an alternative external host to communicate with the ADS7066 by easily connecting through a pin header.

The ADS7066 device incorporates all required circuitry and components with the following features:

- ADS7066 small WCSP footprint, eight-channel ADC
- Analog input driving a circuit available on channel 0
- Onboard reference, REF6025, to provide low-noise 2.5-V voltage and set the full scale range
- External power-supply connection available to provide DVDD power supply instead of the USB power
- Adjustable linear regulator, TPS78001, to generate stable output voltage to AVDD from the 5-V USB power from the PAMBoard
- SPI for communication and configuration of modes

Figure 2 shows the ADS7066EVM architecture, identifying the key components and blocks previously listed.

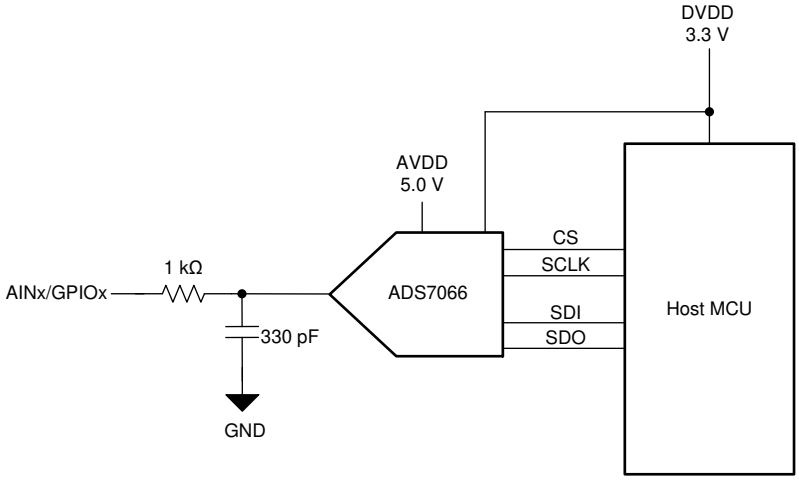

Figure 2. Channel 1 to Channel 6 Hardware Block Diagram

2 ADS7066EVM Overview

This section describes various onboard components that are used to interface the analog input, general-purpose inputs/outputs (GPIOs), digital interface, and provide power supply to the ADS7066 device. Figure 3 shows an ADS7066 board overview.

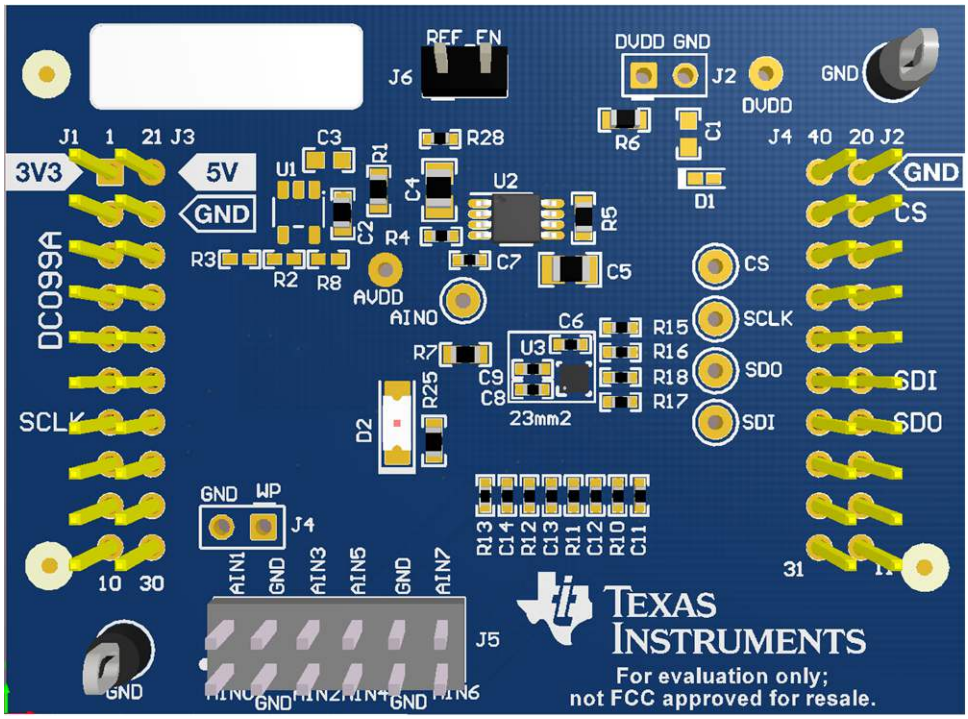

Figure 3. ADS7066 EVM Board

2.1 Connector for Channels

The ADS7066 device is designed for easy interface to an external, analog single-ended source, or to GPIOs through a 100-mil header. Connector J5 provides a connection to the device channels. Table 2 lists the channel connections. The ADS7066 channel AIN0 has a buffered operational amplifier, TLV9061, to drive the analog input. This is further explained in Section 4. Channels AIN1 through AIN6 have a resistor and capacitor filter circuit to condition the analog input, as Figure 2 shows. Channel 7 is hardware-configured to demonstrate GPIO functionality. GPIO7 has a resistor and light-emitting diode (LED) to visibly demonstrate and monitor digital output channel state.

Table 2. Channel Connections

J5 Connector Pin	Description
J5:1	Single-ended analog input with buffer
J5:2	Single-ended analog input or GPIO for channel 1 of the ADC
J5:5	Single-ended analog input or GPIO for channel 2 of the ADC
J5:6	Single-ended analog input or GPIO for channel 3 of the ADC
J5:7	Single-ended analog input or GPIO for channel 4 of the ADC
J5:8	Single-ended analog input or GPIO for channel 5 of the ADC
J5:11	Single-ended analog input or GPIO for channel 6 of the ADC
J5:12	LED GPO for channel 7 of the ADC
J5:3 and J5:4; J5:9 and J5:10	EVM ground

2.2 Digital Interface

As noted in Section 1, the ADS7066 interfaces with the PAMBoard, which in turn communicates with the computer over the USB. The two devices on the EVM that communicate over SPI are the ADS7066 ADC (U3) and the electrically erasable programmable read-only memory (EEPROM) (U4). The EEPROM is preprogrammed with the information required to configure and initialize the ADS7066 platform. Once the hardware is initialized, the EEPROM is no longer used.

2.3 ADS7066 PAMBoard Interface

The ADS7066 supports the digital SPI and functional modes as detailed in the *ADS7066 Small, 8-Channel, 16-Bit SAR ADC With GPIOs Data Sheet*. The PAMBoard is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

2.4 Power Supplies

The device supports a wide range of operation on its analog supply. The AVDD can operate from 3 V to 5.5 V. The DVDD operates from 1.65 V to 5.5 V, independent of the AVDD supply. A voltage regulator available on the PAMBoard is used to supply 5V to AVDD, the DVDD is also provided by the PAMBoard at 3.3V. There is an unpopulated option to use a low-dropout (LDO) regulator, for the TPS78001 for AVDD. There is an onboard option to use an external power supply for DVDD through J2.

3 ADS7066 EVM Initial Setup

The instructions to set up the ADS7066 for evaluation follow:

3.1 EVM Plug-In Hardware Setup Instructions

The EVM and PAMboard come packaged separately. For correct functionality, the boards need to be installed properly.

To install the EVM to the PAMboard, stack the ADS7066EVM-PDK board on the PAMBoard. Make sure the 20-pin connector (J1, J3) on the ADS7066 is mapped to left connector on the PAMBoard, and the EVM connector (J4, J2) is mapped to right connector on the PAMBoard. The silk screen on the ADS7066 must match with the PAMBoard. Figure 4 shows the correct installation. The board headers must be flush. Make sure the USB is not plugged in during this installation.

Connect the PAMBoard micro USB data port to an available USB port on the PC.

Figure 4. ADS7066EVM Lined up With PAMBoard (Left View)

3.2 The ADS7066 GUI Online and TI Cloud Agent Application Installation

The following steps describe the ADS7066 GUI software installation:

1. Plug in the included micro USB to USB cable to the PAMBoard and a USB port on the computer, respectively.
2. On the ADS7066EVM-PDK landing page, the software is available through a web-based GUI. Connecting to the GUI may require login to a user account for access.
3. First-time users may be prompted to download and install the browser extension for Firefox™ or Chrome™ and the TI Cloud Agent Application as Figure 5 shows. Do so if need be, this is a one time download.
4. Refresh the GUI, if need be, and the GUI should connect to the hardware. A green signal will be displayed, and at the left bottom, *Hardware Connected* shows.

Figure 5. Browser Extension and TI Cloud Agent Installation

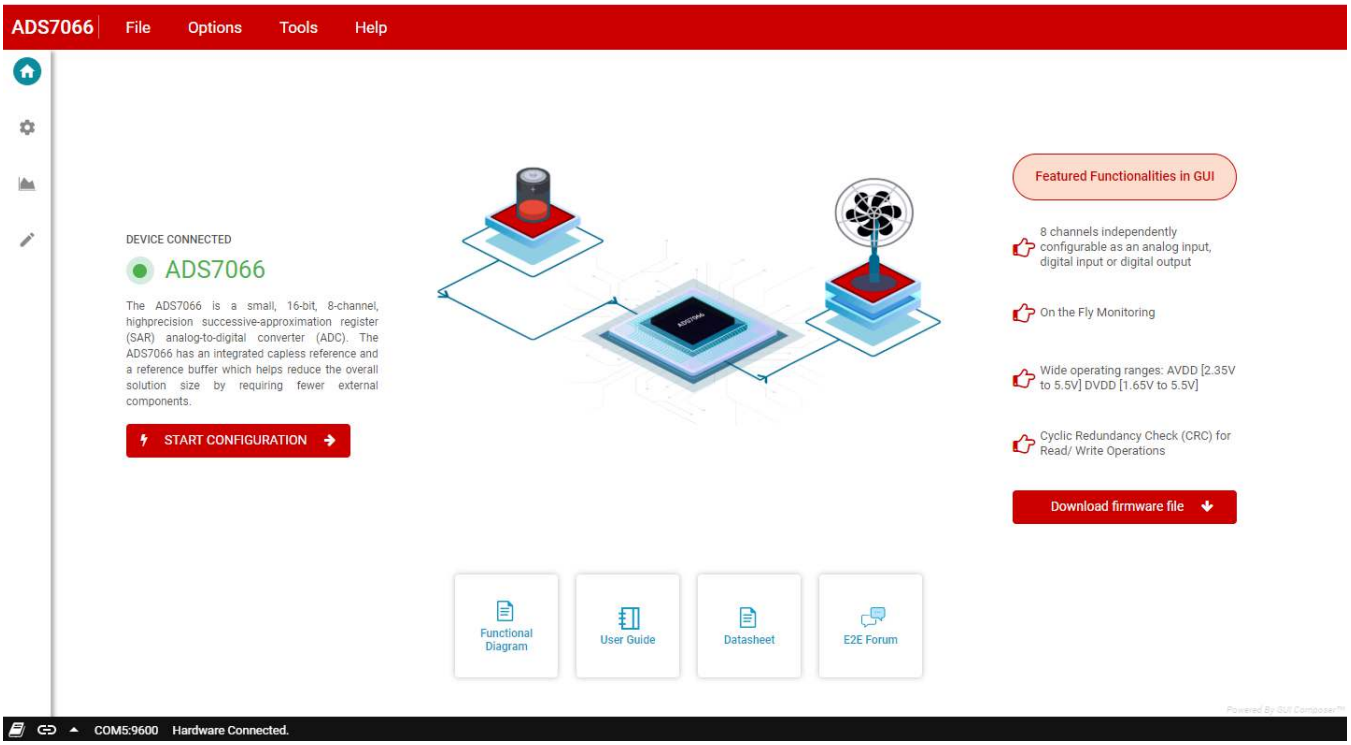

Figure 6. Hardware Connected Successfully to GUI

3.3 ADS7066 GUI Description

3.3.1 GUI Description

Figure 7 shows the GUI landing. This page provides a high-level overview of the ADS7066 device. The left corner (highlighted by the green rectangle) shows the tabs to navigate through the GUI: home, function configurations, data capture, and register map. When the ADS7066 is stacked on the PAMBoard and connected to the PC via the micro USB cable, the GUI detects the EVM module by reading the onboard EEPROM. When detected and connected, the GUI indicates this status as *Connected*. At the bottom left corner of the GUI, there is an option to connect and disconnect the hardware from the GUI.

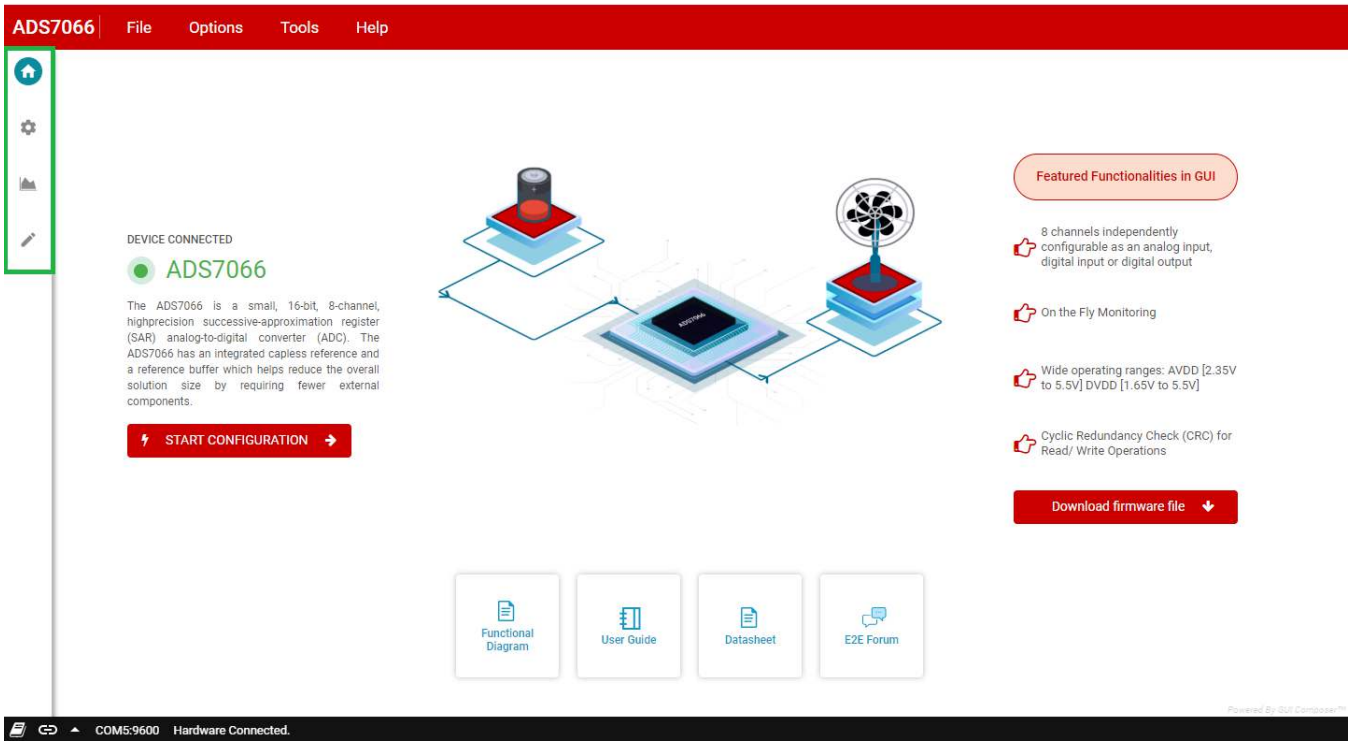

Figure 7. ADS7066 GUI Landing Page

3.3.2 Functional Configuration Tab

As Figure 8 shows, the ADS7066 device configuration tab has two sections. The left-most section lists the multiple functions the user can configure. These options enable the user to navigate through the various functions of the ADS7066 in a structure and clear manner. The main section displays the configuration options for each function.

The Device Configurations available are: Mode Configuration, Channel Selection, Averager, and Cyclic Redundancy Check (CRC)

3.3.2.1 Mode Configuration

The ADS7066 can operate in three sampling modes. The mode configuration tab (Figure 8) allows the user to select the device mode of operation.

The ADS7066 device has the following sampling modes:

- **Manual Mode:** Allows the external host processor to directly request and control when data is sampled. The host provides SPI frames to control conversions and the captured data are returned over the SPI bus after each conversion.
- **Auto-Sequence Mode:** The host can configure the device to scan through the enabled analog input channels. The host must provide continuous clocks (SCLK) to the device to scan through the channels and to read the data from the device. The MUX automatically switches through the predetermined channel sequence, and the data conversion results are sent through the data bus.
- **On-the-Fly Mode:** The first 5 bits of SDI select the first channel to be sampled before the CS rising edge. There is no latency between channel selection and ADC output data since the ADC samples the next channel on the rising edge of CS.

The device powers up in manual mode and can be configured into any of the functional modes by writing the configuration registers for the desired mode.

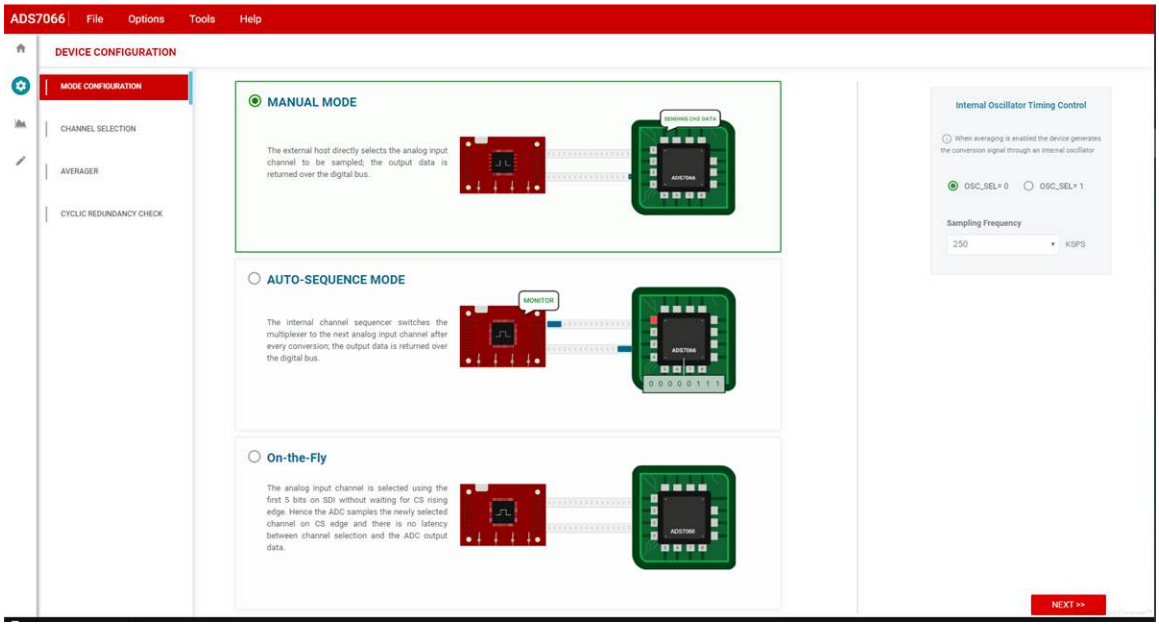

Figure 8. ADS7066 Device Configuration Tab Displaying Mode Configuration

3.3.2.2 Channel Selection

The channel selection configuration option allows the user to configure each of the 8 channels. The default configuration is analog input, but through the drop-down options, each channel can be configured as a digital input or output. If using Auto Sequence mode, individual channels can be selected to be included in the sequence, by checking *Select for Auto-Seq*. The EVM hardware has channel 7 hardwired as a digital output with an LED connected to channel 7 to visually display a high or low digital output state.

To configure for a digital pin, change the *Pin-Config* drop down and select Digital. A second drop down option will appear in line with the channel, *I/O Config*. This drop down option allows to select Input or Output functionality. If output functionality is selected, as shown for channel 7 in Figure 9, configuration options will appear in line with the channel. User will be able to select the *Pin Value* as high or low, and the *Pin Type* as open drain or push pull. The EVM has an LED connected to channel 7 to display this functionality; changing the *Pin Value* on channel 7 will turn on or off the LED (D2)

Through this document, as an example, channel 0 to 5 will be selected as analog inputs, channel 6 as a digital input, and channel 7 as a digital output.

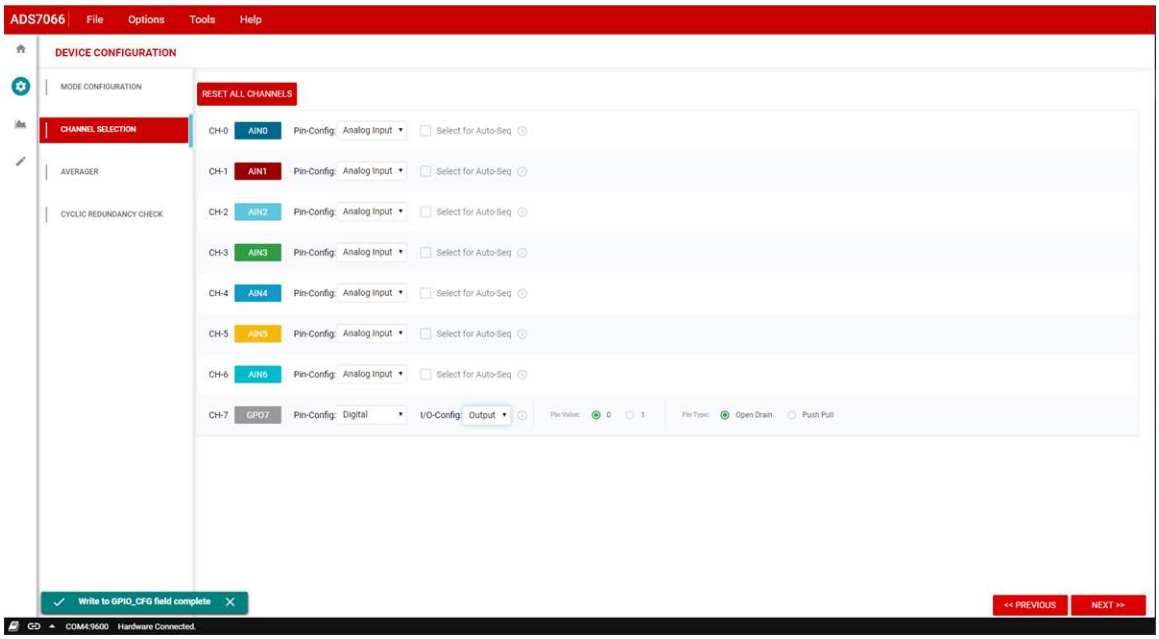

Figure 9. Digital Input or Output Configurations

3.3.2.3 Averaging Function

Within the averaging function page, as Figure 10 shows, the oversampling ratio can be selected through the drop-down option. The oversampling ratio applies to all analog input channels enabled.

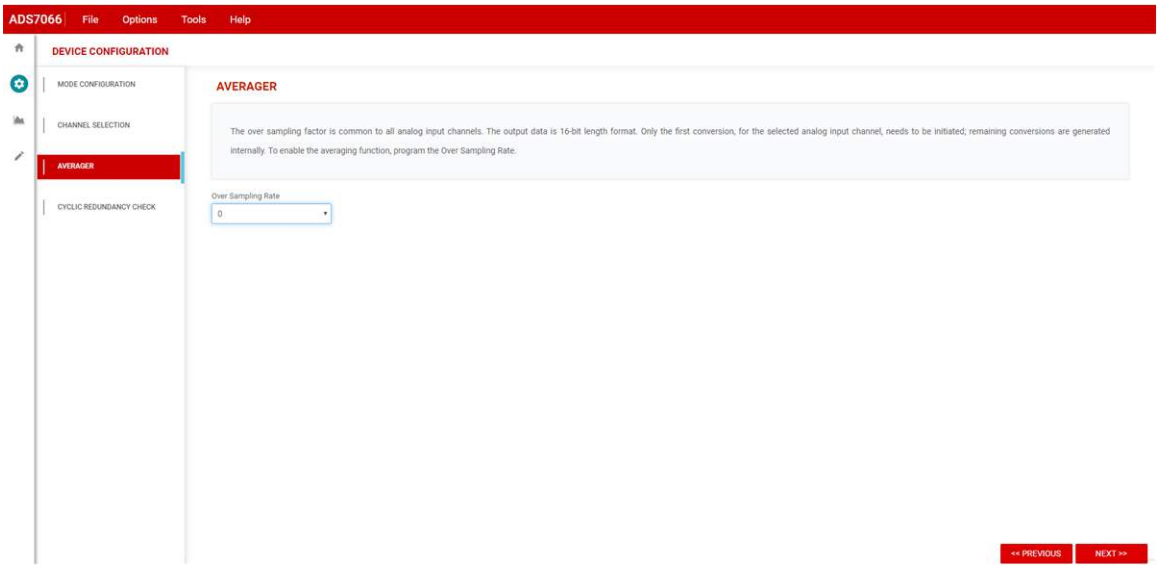

Figure 10. Averaging Page

3.3.2.4 Cyclic Redundancy Check (CRC)

The ADS7066 device supports CRC to check the integrity of data transfer. When CRC is enabled, an 8-bit output is appended to the end of the data transfer. The polynomial is calculated on the CRC-8-ATM as shown in the page.

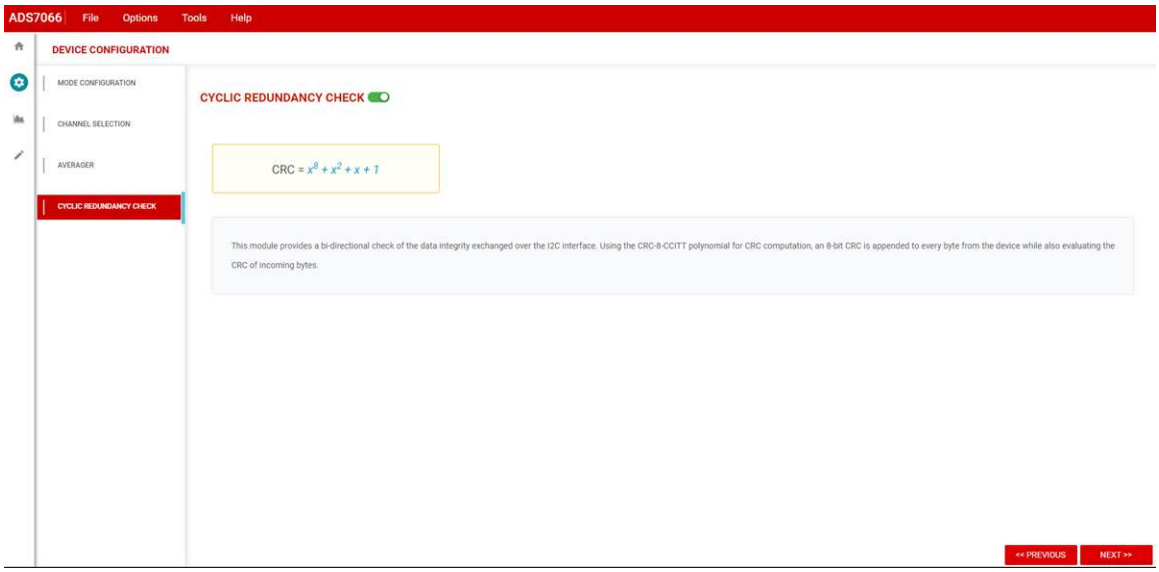

Figure 11. CRC Function Polynomial

3.3.3 Data Capture Tab

The data capture tab displays the conversion results of the sampled data of the enabled channels. As Figure 12 shows, clicking the red **Capture** button commences a sample data set. This page also displays the sampling mode configuration used to capture the data. There is also a checkmark option to repeatedly capture the sample size selected. This tab features two pages to display both the analog input and the digital inputs:

- **Analog Inputs:** The sample and conversion results for each enabled analog input is displayed in this page. The results can be displayed in three methods: time domain, Fast Fourier transform (FFT), and histogram.
- **Digital Inputs:** The enabled digital input channels are displayed in this page.

See Section 3.3.3.1 for more information on capturing data.

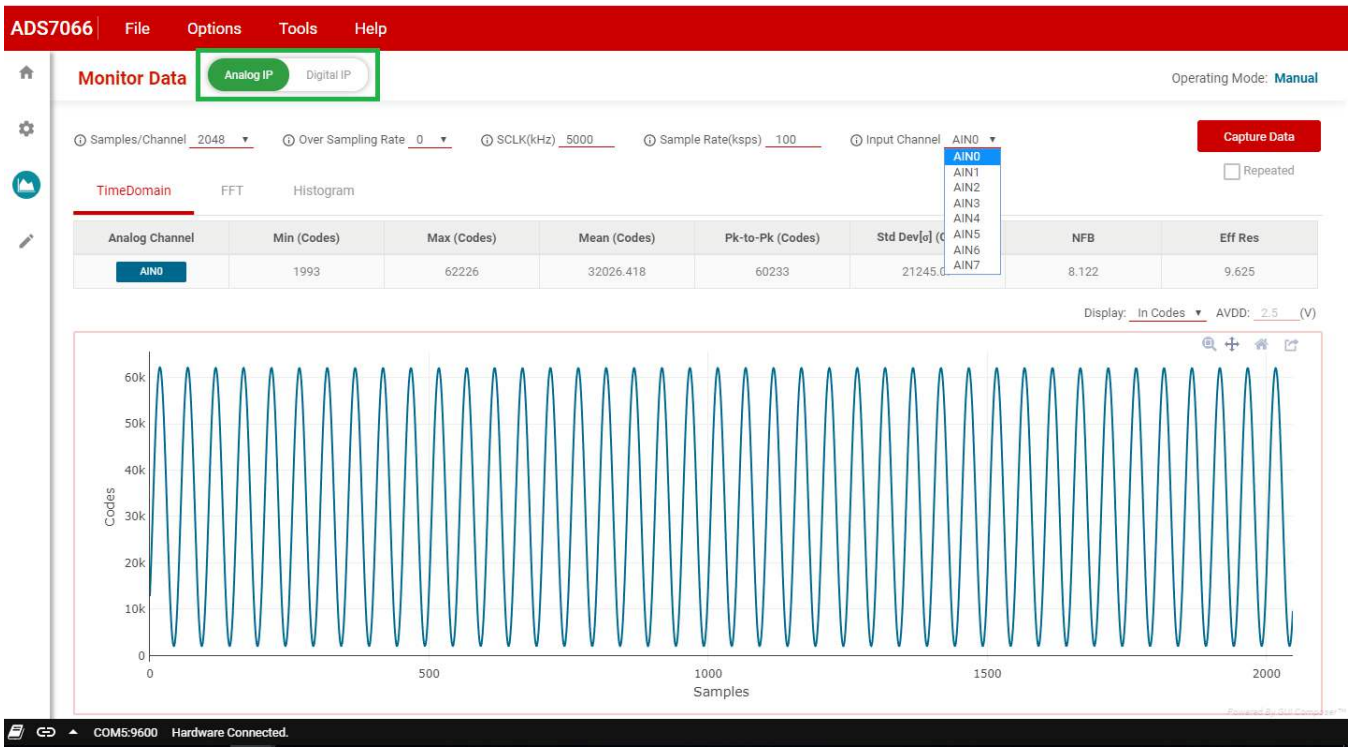

Figure 12. ADS7066 Data Capture Tab

3.3.3.1 Analog Input Data Capture Features

This section describes the features available in the *Analog IP* data capture display of the GUI. This page auto updates to reflect the inputs in Section 3.3.2.2 based on the channel-specific configuration and displays the configuration.

The analog input page provides an interface to the conversion results of the analog input channels. Analog data is captured, as shown in Figure 13, by clicking on the **Capture Data** button. The analog inputs page also provides user options for the following:

- Number of samples per the enabled analog input channels
- A drop-down option for increasing the oversampling rate
- A drop-down option to change the SCLK frequency
- A drop-down option for entering the desired sampling rate
- A drop-down option for selecting input channel displayed when in manual mode. When in Autosequence, all channel selected would be displayed simultaneously

The *Analog IP* also displays a table with helpful attributes of the sampled data. The minimum and maximum sample code are displayed, followed by the peak-to-peak range of the sampled data. The standard deviation in codes, noise-free bits (NFB), and the effective resolution are also automatically displayed after every data capture.

Within the *Analog IP* page, the captured samples can be displayed in three different formats:

- Time Domain
- Fast Fourier Transform (FFT)
- Histogram

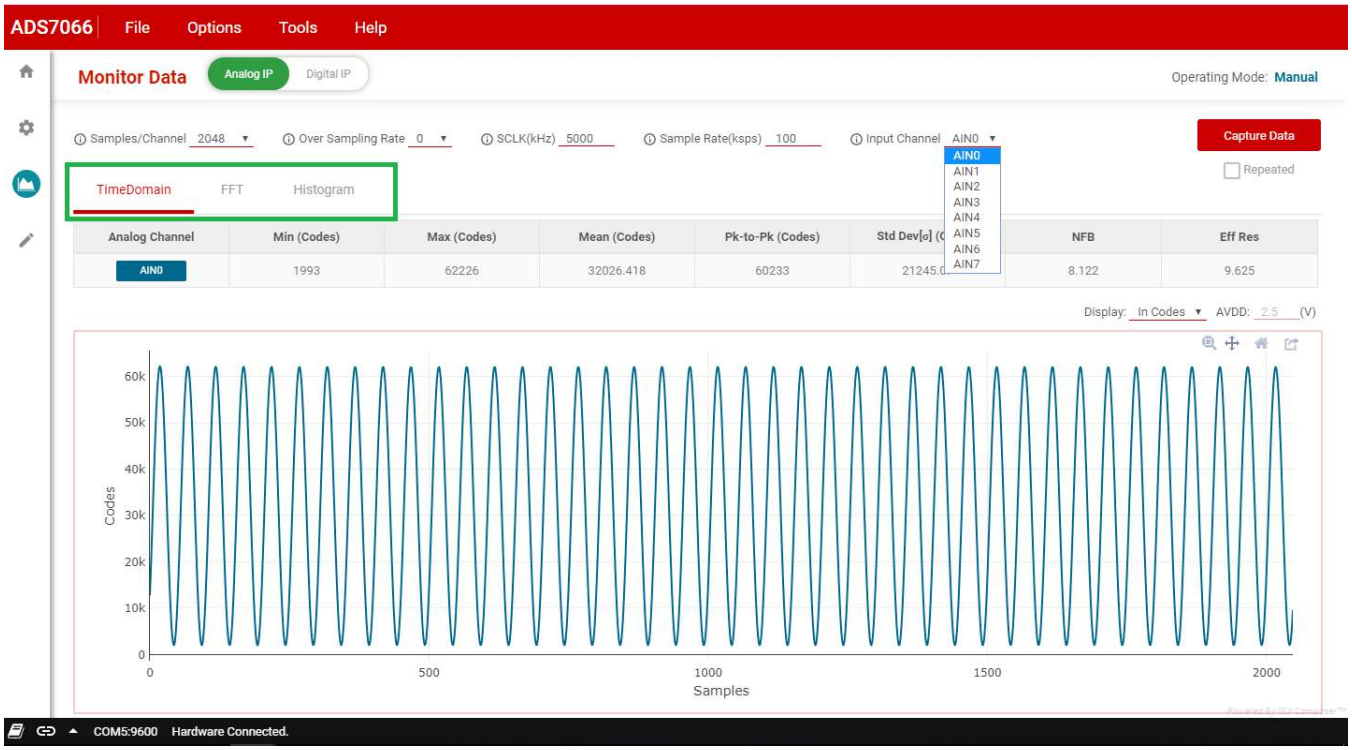

Figure 13. Analog IP Data Capture Tab Options

3.3.3.1.1 Time Domain Display

The time domain graph displays the conversion results of an analog input channel of the sampled data set. The data captured is displayed as code value vs sample number. The number of samples can be increased in the *Samples/Channel* drop-down menu. The data can also be displayed in the volt equivalent of sample captured instead of the code value, based in the AVDD.

When in manual mode, the graph can only display one analog input conversion results at a time; the drop-down option *Input Channel* allows changing which channel is displayed. When the device is operating in auto-sequence mode, all the analog input channels selected will be displayed on the graph.

The data can also be exported by clicking the last icon at the right corner of the graph display.

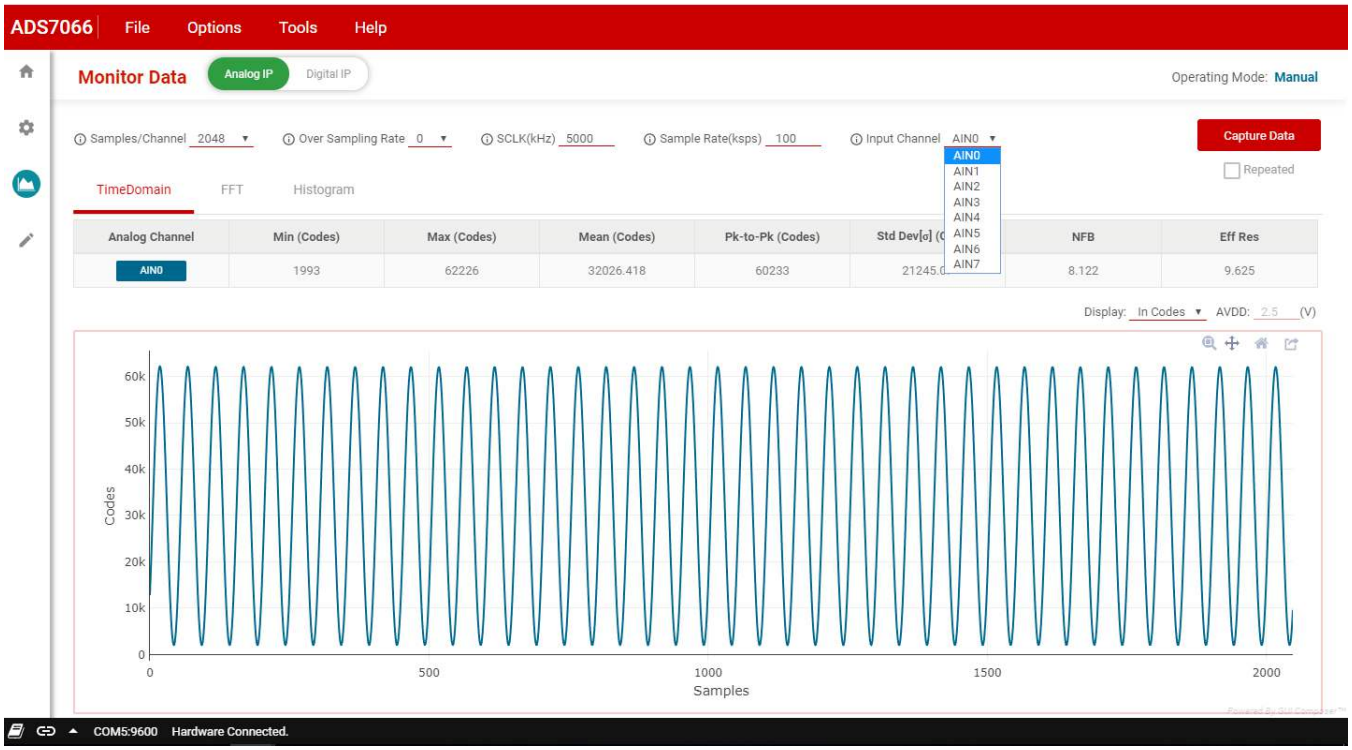

Figure 14. Time Domain Display

3.3.3.1.2 FFT

The *Analog IP* can display the FFT of the data captured. This will only display data if the analog input is AC.

The FFT tab displays a table with the fundamental frequency of the input, followed by the noise floor level, SNR, SFDR, THD, and SINAD. The effective number of bits (ENOB) and the number harmonics shown is also displayed in the table.

NOTE: This image was taken using a incomplete version of the GUI. The device and EVM can perform to data sheet specifications. The latest GUI version available will show correct performance results

Figure 15. FFT Display

3.3.3.1.3 Histogram Graph Display

The conversion results can also be shown as a histogram through the histogram tab (shown in Figure 16) within the *Analog IP* page.

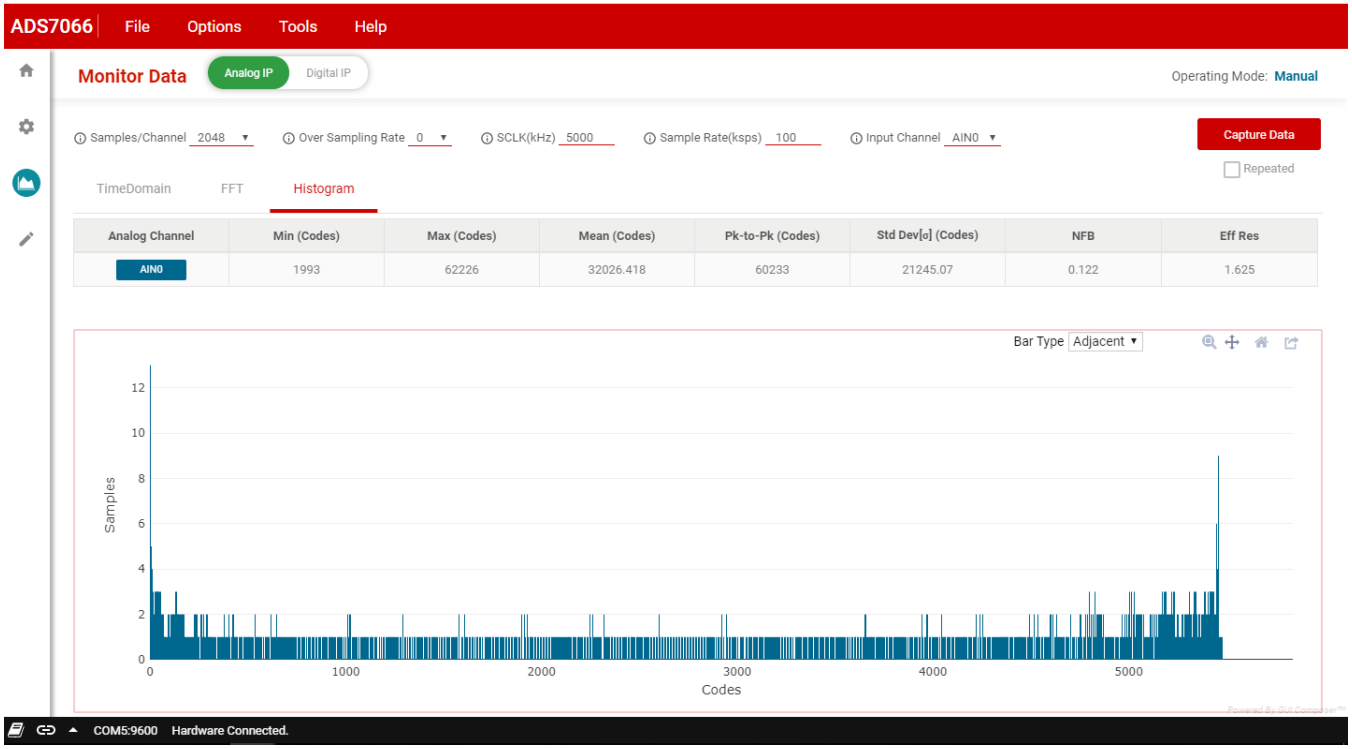

Figure 16. Histogram Graph Display

3.3.4 Digital Input Page

The digital input page displays the enabled digital input channels as configured in Figure 9. As an example channel 6 was configured as a digital input. All digital input channels enabled will be displayed on this page and indicate the present logic state, respectively.

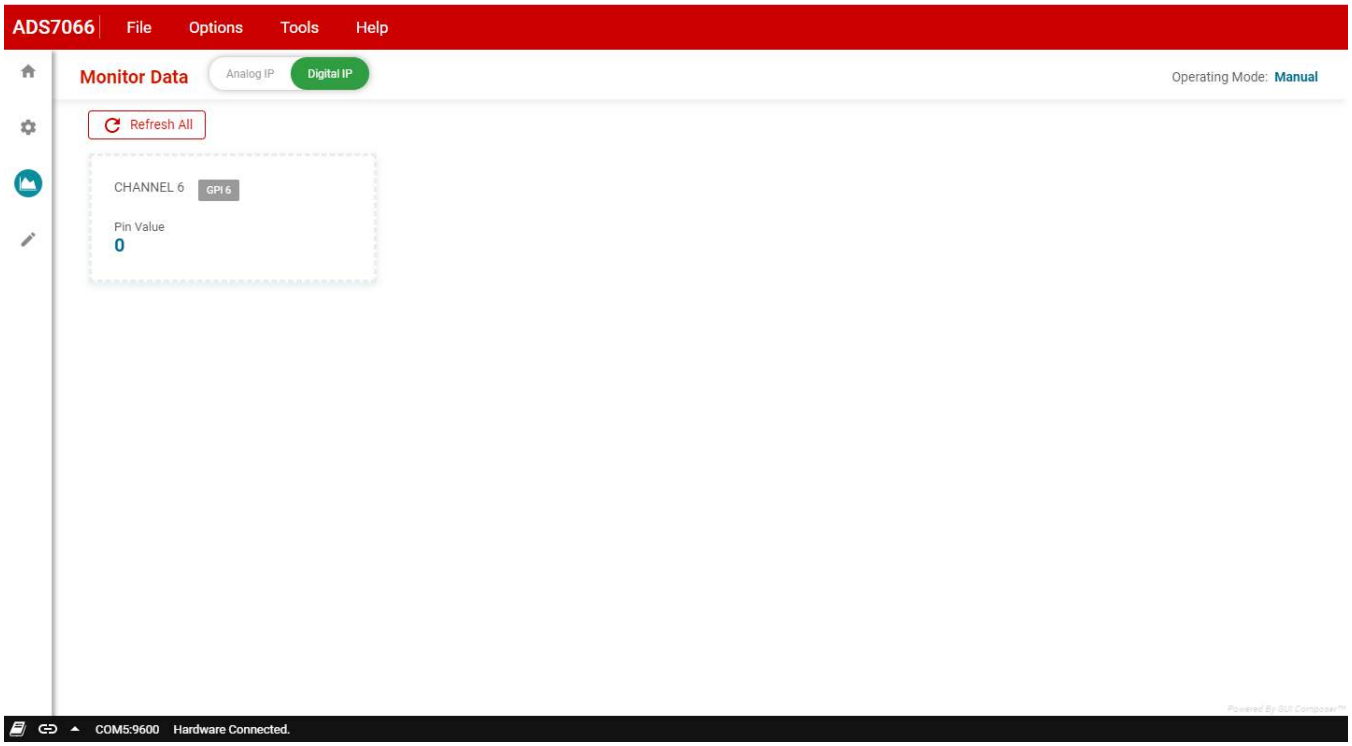

Figure 17. Digital Input Page Display

3.4 Register Map

Figure 18 shows the register map for the ADS7066 device. On the top right corner are options to read registers individually or read all the registers, or write an individual register. Users can choose to have the register values modified in the GUI to be written on the device instantaneously by selecting the *Immediate Write* option or later using the *Deferred Write* drop-down option. In the field view, the registers are broken down into the configurable bits it controls. When making changes in the *Field View*, the bit being changed is highlighted in yellow in the register map.

The register settings can also be saved in an external file to be loaded back into the GUI through the *File → Save Registers* menu selection. This allows for different setting configurations to be saved and easily implemented into the GUI by loading it back through the *File → Load Registers* menu item.

The register configurations can also be saved as a comma-separated values (CSV) file containing the register address and content as configured in the GUI. This allows the user to configure the device easily through the GUI as desired, and then export the respective register addresses and content to reference when creating firmware.

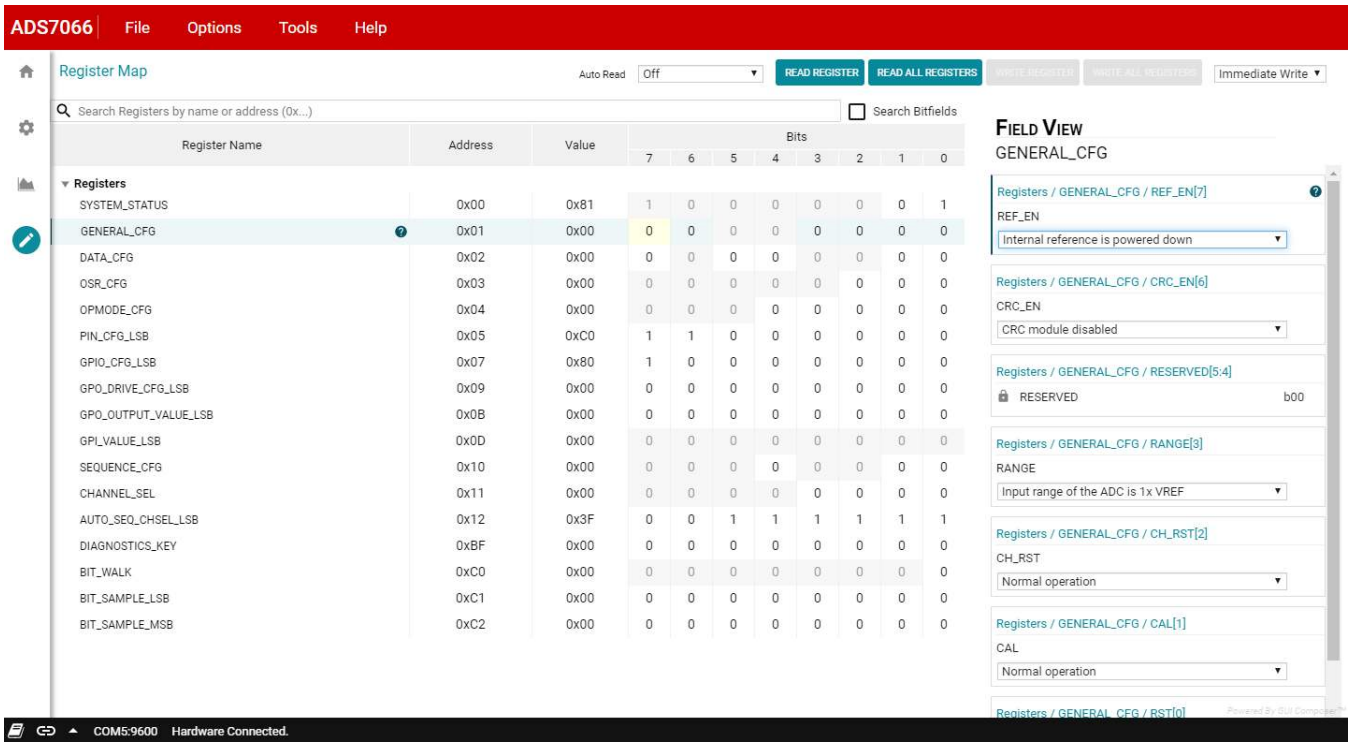

Figure 18. ADS7066 Register Map Page

4 Input Signal-Conditioning Block on the ADS7066EVM

For applications where the input signal requires additional conditioning before the ADC input, the ADS7066EVM has an onboard signal-conditioning path on channel 0. The input signal header, J5 is connected to the amplifier input, OPA325. By default, this signal-conditioning block is populated on the evaluation board as a non-inverting buffer using the OPA325 device. The board has a provision to bypass the operational amplifier (U5) based on the signal conditioning requirement. To bypass this block, remove the R21 0-Ω resistor and populate R26. See Section 5.3 for more details.

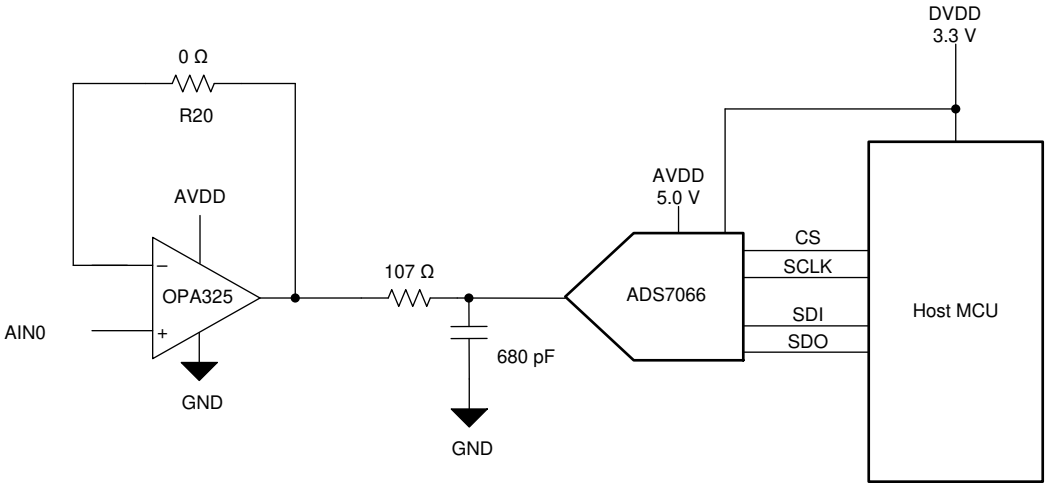

Figure 19. Channel 0 Input Signal Conditioning Block

5 Bill of Materials, Printed Circuit Board Layout, and Schematics

This section contains the ADS7066 bill of materials (BOM), printed circuit board (PCB) layout, and schematics.

5.1 Bill of Materials

Table 3 lists the bill of materials (BOM) for the ADS7066EVM.

Table 3. Bill of Materials

Designator	Quantity	Description	Manufacturer Part Number	Manufacturer
C2	1	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	C0603C105K3RACTU	Kemet
C4	1	CAP, CERM, 10 µF, 10 V, ±20%, X7R, 0805	C0805C106M8RACTU	Kemet
C5,	1	CAP, CERM, 47 µF, 10 V, ±20%, X5R, 0805	GRM21BR61A476ME15L	MuRata
C6, C7, C8, C9	4	CAP, CERM, 1 µF, 6.3 V, ±20%, X7R, 0402	GRM155R70J105MA12D	MuRata
C10, C11, C12, C13, C14, C15	6	CAP, CERM, 330 pF, 50 V, ±1%, C0G/NP0, 0402	GRM1555C1H331FA01J	MuRata
C16, C18	2	CAP, CERM, 0.1 µF, 25 V, ±10%, X5R, 0603	CL10A104KA8NNNC	Samsung Electro-Mechanics
C17	1	CAP, CERM, 680 pF, 25 V, ±5%, C0G/NP0, 0402	GRM1555C1E681JA01D	MuRata
D2	1	LED, Red, SMD	LTST-C150CKT	Lite-On
J1, J3	2	Receptacle, 2.54 mm, 10 × 2, Tin, TH	SSQ-110-03-T-D	Samtec
J5	1	Header, 100 mil, 6 × 2, Tin, TH	PEC06DAAN	Sullins Connector Solutions
J6	1	Header, 100 mil, 2x1, Tin, TH	SSQ-110-03-T-D	Samtec
R1, R6,R7	3	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R4	1	RES, 0.22, 1%, 0.125 W, AEC-Q200 Grade 0, 0402	ERJ-2BQFR22X	Panasonic
R5, R20, R21	3	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R9, R10, R11, R12, R13, R14	6	RES, 1.00 kΩ, 1%, 0.1 W, 0402	ERJ-2RKF1001X	Panasonic
R15, R16, R17, R18, R28	5	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402100KFKED	Vishay-Dale
R23, R24	2	RES, 10.0 kΩ, 1%, 0.063 W, 0402	RC0402FR-0710KL	Yageo America
R25	1	RES, 2.20 kΩ, 1%, 0.1 W, 0603	RC0603FR-072K2L	Yageo
R27	1	RES, 1.00 M, 1%, 0.1 W, 0402	ERJ-2RKF1004X	Panasonic
R29	1	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040249R9FKED	Vishay-Dale
TP4, TP5	2	Test Point, Multipurpose, Black, TH	5011	Keystone
U2	1	5 ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	REF6025IDGKR	Texas Instruments
U3	1	Small, 8-Channel, 12-bit ADC with I2C Interface, GPIOs and CRC, RTE0016C_WF (WQFN-16)	ADS7066RTE	Texas Instruments
U4	1	I2C BUS EEPROM (2-Wire), TSSOP-B8	BR24G32FVT-3AGE2	Texas Instruments
U5	1	CMOS Amplifier 1 Circuit Rail-to-Rail SOT-23-5	OPA325IDBVR	Texas Instruments

5.2 PCB Layout

Figure 20 through Figure 22 illustrate the EVM PCB layouts.

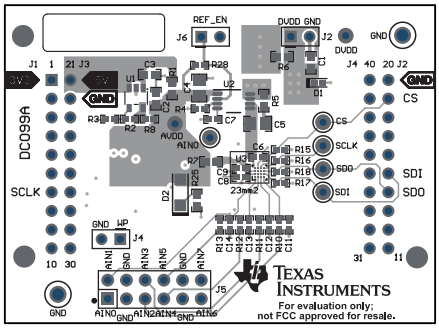

Figure 20. ADS7066 EVM PCB Top Layer

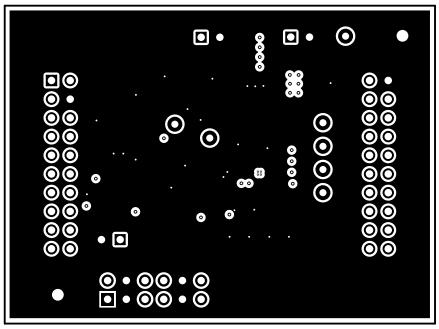

Figure 21. ADS7066 EVM PCB Ground Layer

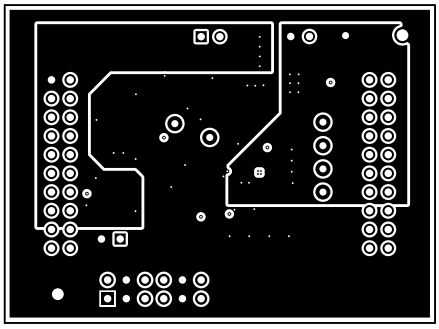

Figure 22. ADS7066 EVM PCB Power Plane Layer

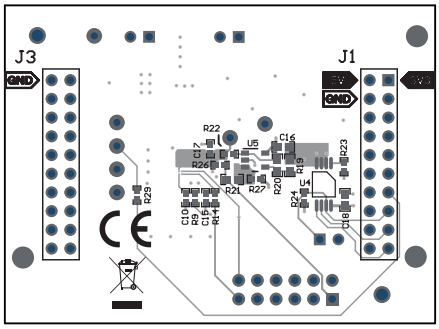

Figure 23. ADS7066 EVM PCB Bottom Layer

5.3 Schematics

Figure 24 illustrates the ADS7066 EVM schematics.

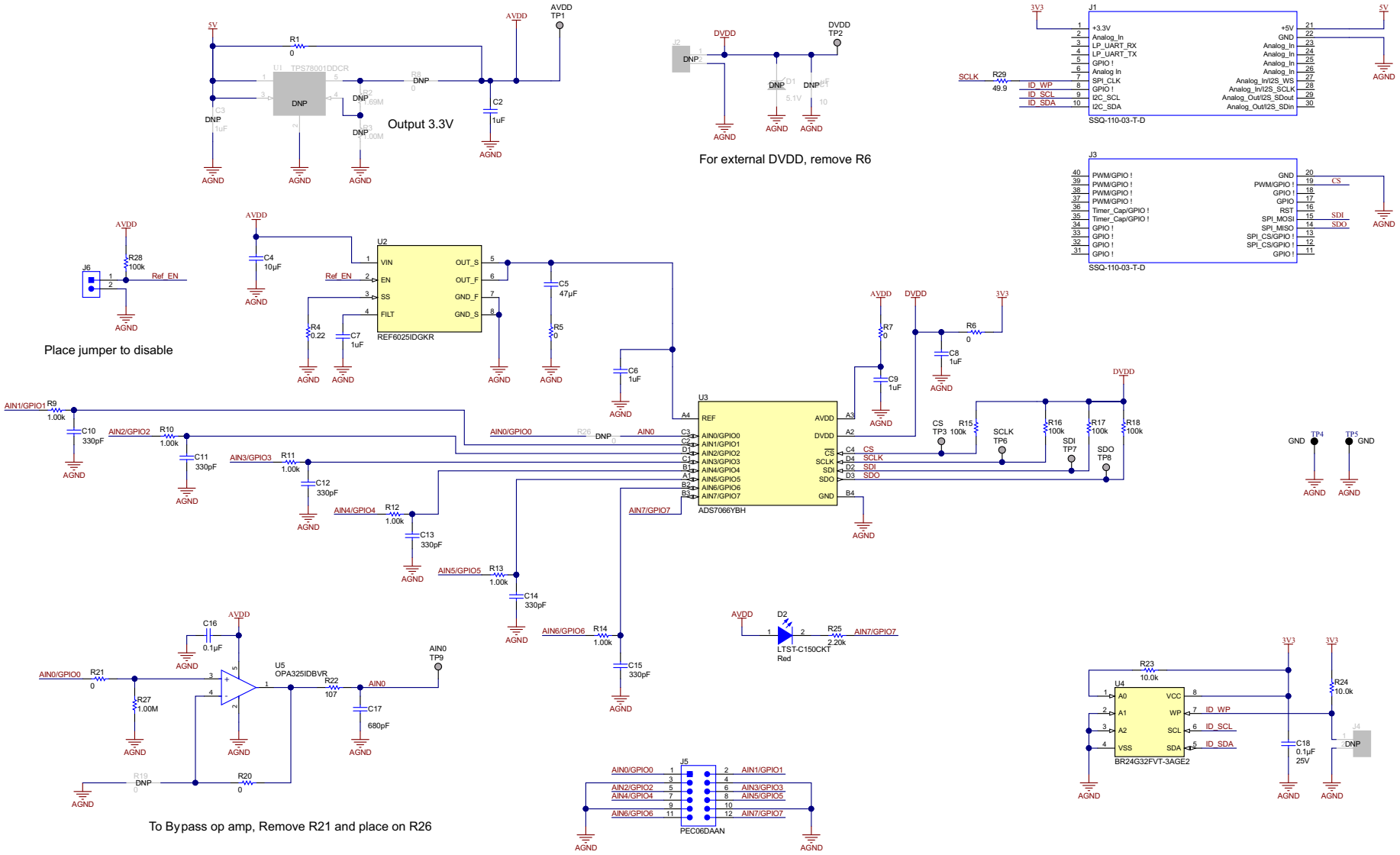

Figure 24. ADS7066 EVM Schematic Diagram

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2020) to A Revision	Page
• Updated many portions of EVM user's guide for release to market.	1

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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