

Vishay Siliconix

# Dual P-Channel 20-V (D-S) MOSFET

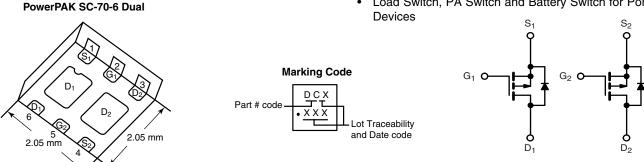
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
	0.094 at V <sub>GS</sub> = - 4.5 V	- 4.5 <sup>a</sup>			
- 20	0.131 at V <sub>GS</sub> = - 2.5 V	- 4.5 <sup>a</sup>	4.9 nC		
	0.185 at V <sub>GS</sub> = - 1.8 V	- 4.5 <sup>a</sup>			

### **FEATURES**

- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
  - Low On-Resistance

#### **APPLICATIONS**

Load Switch, PA Switch and Battery Switch for Portable Devices



Ordering Information: SiA911DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET P-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 20	V	
Gate-Source Voltage		V <sub>GS</sub>	± 8		
	T <sub>C</sub> = 25 °C		- 4.5 <sup>a</sup>		
Continuous Drain Current ( $T_1 = 150 \ ^{\circ}C$ )	T <sub>C</sub> = 70 °C	1-	- 4.5 <sup>a</sup>		
Continuous Drain Current (1j = 150°C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 3.6 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		- 2.9 <sup>b, c</sup>	A	
Pulsed Drain Current		I <sub>DM</sub>	- 8		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	- 4.5 <sup>a</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	15	- 1.6 <sup>b, c</sup>		
	T <sub>C</sub> = 25 °C		6.5		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	PD	5	w	
	T <sub>A</sub> = 25 °C		1.9 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		1.2 <sup>b, c</sup>	7	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	℃	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260		

### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	52	65	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	12.5	16		

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 110 °C/W.



COMPLIANT

d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static									
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = -250 \mu\text{A}$	- 20			V			
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 16.2		mV/°C			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	i <sub>D</sub> = - 230 μA		2.1					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	- 0.4		- 1	V			
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V$ , $V_{GS} = \pm 8 V$			± 100	nA			
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	<u> </u>			
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 \text{ °C}$			- 10	μΑ			
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \!\leq\! 5$ V, $V_{GS}$ = - 4.5 V	8			Α			
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 2.8 A		0.078	0.094	1			
	R <sub>DS(on)</sub>	$V_{GS} = -2.5 \text{ V}, I_D = -2.3 \text{ A}$			0.131	Ω			
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 0.54 A		0.153	0.185	1			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 2.8 A		7		S			
Dynamic <sup>b</sup>									
Input Capacitance	C <sub>iss</sub>			355		pF			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		75					
Reverse Transfer Capacitance	C <sub>rss</sub>	20 30		50					
· · · · · · · · · · · · · · · · · · ·		V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 4.5 A		8.5	12.8	-			
Total Gate Charge	Q <sub>g</sub> Q <sub>gs</sub>			4.9	7.4	nC			
Gate-Source Charge		$V_{DS}$ = - 10 V, $V_{GS}$ = - 4.5 V, $I_{D}$ = - 4.5 A		0.75					
Gate-Drain Charge	Q <sub>gd</sub>			1.2					
Gate Resistance	R <sub>g</sub>	f = 1 MHz		8		Ω			
Turn-On Delay Time	t <sub>d(on)</sub>			10	15				
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_{L}$ = 2.2 $\Omega$		35	55	- ns			
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 4.5 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 $\Omega$		40	60				
Fall Time	t <sub>f</sub>			50	75				
Turn-On Delay Time	t <sub>d(on)</sub>			5	10				
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_{L}$ = 2.2 $\Omega$		10	15				
Turn-Off Delay Time	t <sub>d(off)</sub>	${ m I}_{ m D}\cong$ - 4.5 A, ${ m V}_{ m GEN}$ = - 8 V, ${ m R}_{ m g}$ = 1 $\Omega$		20	30				
Fall Time	t <sub>f</sub>			10	15				
Drain-Source Body Diode Characterist	cs			•	I				
Continuous Source-Drain Diode Current	ا <sub>S</sub>	T <sub>C</sub> = 25 °C			- 4.5	A			
Pulse Diode Forward Current	I <sub>SM</sub>				8				
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 4.5 A, V <sub>GS</sub> = 0 V		- 0.85	- 1.2	V			
Body Diode Reverse Recovery Time	t <sub>rr</sub>			30	60	ns			
Body Diode Reverse Recovery Charge	everse Becovery Charge Q			13	26	nC			
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -4.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$		10		ns			
Reverse Recovery Rise Time	t <sub>b</sub>			15					

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

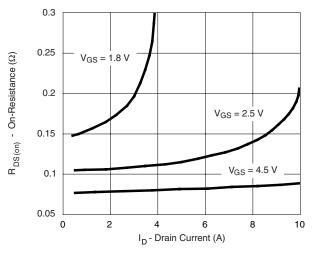
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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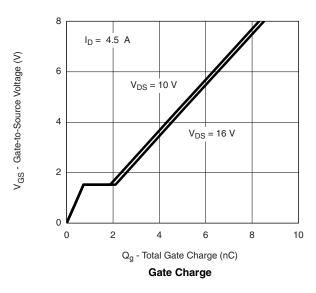
#### 10 8 V<sub>GS</sub> = 2.5 thru 5 V I<sub>D</sub> - Drain Current (A) 6 2 V 4 1.5 V 2 0 0.0 0.4 0.8 1.2 1.6 2.0 V<sub>DS</sub> - Drain-to-Source Voltage (V) **Output Characteristics**

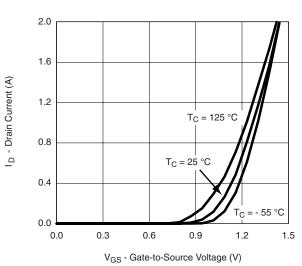
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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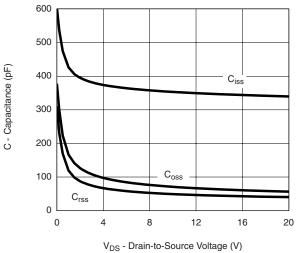


**On-Resistance vs. Drain Current and Gate Voltage** 

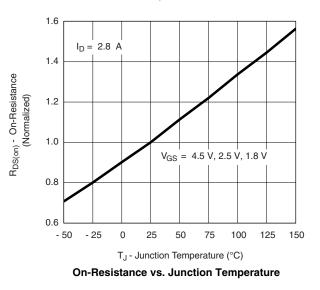




**Transfer Characteristics** 



Capacitance



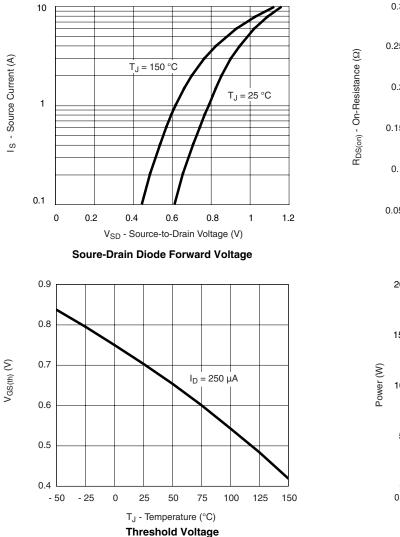
Document Number: 74329 S-80437-Rev. C, 03-Mar-08

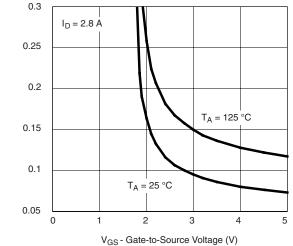
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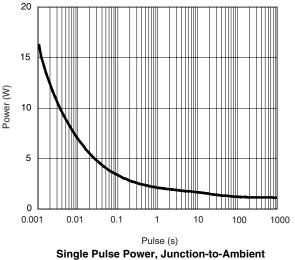
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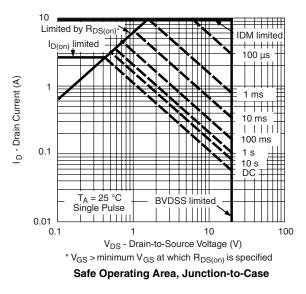
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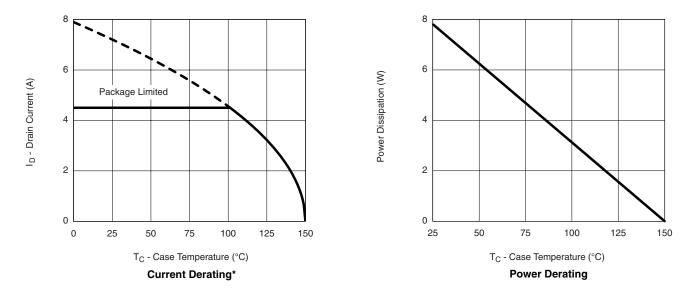
On-Resistance vs. Gate-to-Source Voltage







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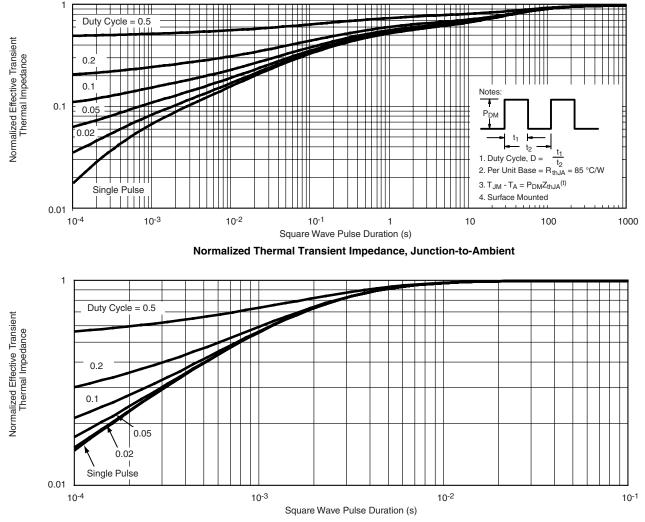
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?74329.



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