Figure 2. Serial Bus Timing Diagram

## SPI TIMING CHARACTERISTICS ([ADM1278-2](ADM1278-2))

Table 5.

| Parameter | Description | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| $t_S$[1] | $\overline{SPI\_SS}$ falling edge to MCLK rising edge setup time | 50 | | | ns | |
| $t_{HIGH}$[1] | MCLK high time | 180 | | | ns | |
| $t_{LOW}$[1] | MCLK low time | 180 | | | ns | |
| $t_{CLK}$[1] | MCLK cycle time | 1 | | | µs | |
| $t_H$[1] | Hold time between $\overline{SPI\_SS}$ and MCLK | 1 | | | µs | |
| $t_V$ | Hold time between new data valid and MCLK falling edge | 110 | | 260 | ns | Track capacitance = 120 pF; $I_{OL}$ = 4 mA |
| $t_{ON}$ | $\overline{SPI\_SS}$ falling edge to MDAT active time | 130 | | 240 | ns | Track capacitance = 120 pF; $I_{OL}$ = 4 mA |
| $t_{OFF}$ | Bus relinquish time after $\overline{SPI\_SS}$ rising edge | 130 | | 280 | ns | Track capacitance = 120 pF; $I_{OL}$ = 4 mA |

[1] Guaranteed by design, but not production tested.
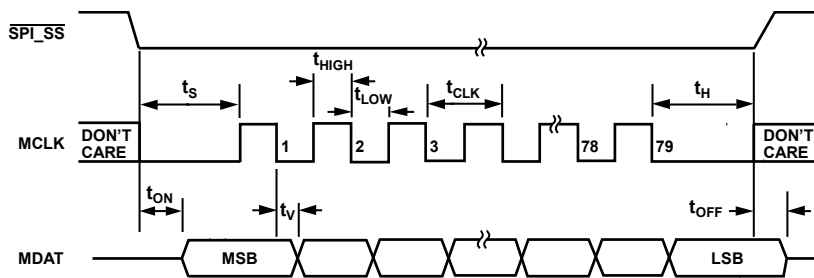


Figure 3. SPI Timing Diagram

series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the device. The effect of any filter resistance seen in series with the remote sensor is automatically cancelled from the temperature result.

The construction of a filter allows the ADM1278 and the remote temperature sensor to operate in noisy environments. Figure 59 shows a low-pass R-C-R filter with the following values: R = 100 Ω and C = 1 nF. This filtering reduces both common-mode noise and differential noise.
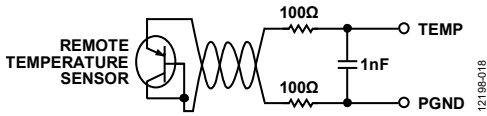


Figure 59. Filter Between Remote Sensor and ADM1278

## SPI INTERFACE

The serial peripheral interface (SPI) allows the user to output a stream of raw data from the ADC as soon as new data is available, removing the bandwidth limitations of the PMBus interface for data readback. The PMBus remains as an active data bus and all configuration and register access must still be completed over the PMBus interface. However, the SPI interface can be used at the same time to serially output the ADC monitoring data. It is a 3-pin serial interface capable of operating at speeds of up to 1 MHz.

The SPI pins are only available on the ADM1278-2 model. If the ADM1278-2 model is used but the SPI pins are not required, tie the SPI input pins ($\overline{SPI\_SS}$, MCLK) to VCAP and the SPI output pin (MDAT) can be left floating or tied to GND.

$\overline{SPI\_SS}$ is the slave select pin, and when it is held low, the MCLK pin can be used to clock data out on the MDAT serial output pin. The $\overline{SPI\_SS}$ pin is also used to frame the output data. The SPI pins are compatible with SPI Mode 0 (CPOL = CPHA =

0), but it is also possible to launch and capture data on the same clock edge for extra timing margin if required.

The interface has the following characteristics:

- MDAT is driven by the ADM1278 (master input, slave output). $\overline{SPI\_SS}$ and MCLK are driven by the user, for example, a baseboard management controller (BMC).
- No header or ID information required. The 80-bit data format is fixed regardless of ADC sampling selection (see Figure 60).
- The falling edge of $\overline{SPI\_SS}$ activates the serial interface, at which point MCLK can be used to clock out data on MDAT. The time between $\overline{SPI\_SS}$ falling edges must be greater than or equal to the maximum ADC sampling time to avoid duplicate data.
- Select single shot mode to allow the falling edge of $\overline{SPI\_SS}$ to trigger ADC sampling (ADC convert start signal).
- Maximum clock speed (MCLK) is approximately 1 MHz.
- The output stream can be stopped at any point in the output frame via a rising edge on the $\overline{SPI\_SS}$ pin.
- The MSB of each sample is output first.
- The output data line is high impedance when not transmitting.

For example, if configuring the SPI interface to read back ADC current samples (16 bits), 15 MCLK falling edges are required to clock out all of the bits after the initial falling edge on $\overline{SPI\_SS}$. These bits can be clocked out at 1 MHz; therefore, with an ADC sample time of approximately 165 μs, the latency between sample and data is 181 μs. See Figure 3 for SPI timing information.

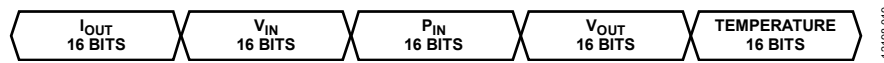Note that the MDAT output samples are offset by one sample from the ADC.
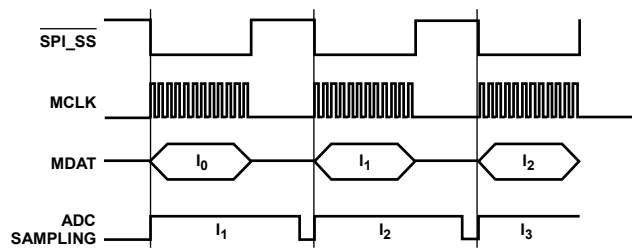


Figure 60. Output Data Format



Figure 61. Streaming Current Data Only

## V<sub>OUT</sub> MEASUREMENT

The VOUT pin measures the output voltage after the FET. This voltage is used by the device to determine the $V_{DS}$ of the MOSFET for foldback operation. Add a 1 kΩ resistor in series between the source of the FET and the VOUT pin. This resistor provides some separation between the ADM1278 and the FET source during a fault condition; thus, ADM1278 operation is not affected.

The VOUT pin on the ADM1278 can also be used to provide an alternate voltage for the power monitor to measure. The user can choose to measure the input voltage at the HS+ pin and/or the output voltage at the VOUT pin.

## FET HEALTH

The ADM1278 provides a comprehensive method of detecting a faulty pass MOSFET. When a faulty FET is detected, the following occurs:

- PWRGD is deasserted.
- FAULT is asserted and latched low.
- FET health PMBus status bits are asserted and latched.

This detection feature ensures that any downstream dc-to-dc converters are disabled, limiting the power dissipation in any faulty or overheating FETs until the user clears the fault, which can be critical to avoid any catastrophic events due to faulty FETs.

A gate to source or gate to drain short is a common type of FET failure. This type of failure is detected by the ADM1278 at any time during operation.

A less common failure is a drain to source short. This normally occurs due to a board manufacturing defect such as a solder short. This type of failure is detected during the initial power-on reset cycle after power-up or after a 10 second autoretry attempt.

There is also an option to disable FET health detection via the PMBus.

## POWER THROTTLING

The ADM1278 provides a number of methods for initiating power throttling of a processor. The simplest method is to configure one of the alert pins for HS_INLIM_ENx (Alert 1 and Alert 2 configuration registers, Bit 4). A latched alert is then generated within a few microseconds after the circuit breaker threshold is exceeded (that is, when the TIMER pin starts ramping). This signal throttles the processor in an attempt to reduce the system current level below the circuit breaker threshold before the TIMER regulation period expires.

The CSOUT pin can be used for the purposes of power throttling as well. The response time of the CSOUT pin to a V<sub>SENSE</sub> step of 10 mV is approximately 10 μs. The CSOUT pin can then be fed into a comparator (via a resistor divider) to set a programmable analog threshold for the system current. The output of the comparator can be used to throttle the processor after the configured threshold has been exceeded. The advantage of using the CSOUT pin is that the threshold for

power throttling can be configured independently of the active hot swap current limit. However, the accuracy of the CSOUT pin has to be taken into account when setting the power throttling threshold.

The latest Intel®processors have a fast processor hot (fast PROCHOT) input/output pin that can be used for power throttling. Asserting this pin initiates a deep throttle of the processor. This is usually used as a last attempt at throttling to avoid a card shutting down when all else has failed. The HS_INLIM_FAULT alert signal or the CSOUT pin can be used to drive this fast PROCHOT pin to achieve power throttling.

## POWER MONITOR

The ADM1278 features an integrated ADC that accurately measures the current sense voltage, the input voltage, and optionally, the output voltage and temperature at an external transistor. The measured input voltage and current being delivered to the load are multiplied together to give a power value that can be read back. Each power value is also added to an energy accumulator that can be read back to allow an external device to calculate the energy consumption of the load.

The ADM1278 reports the measured current, input voltage, output voltage, and temperature. The PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE commands can be used to read the highest readings since the value was last cleared.

An averaging function is provided for voltage, current, and power that allows a number of samples to be averaged together by the ADM1278. This function reduces the need for postprocessing of sampled data by the host processor. The number of samples that can be averaged is $2^N$, where N is in the range of 0 to 7.

The power monitor current sense amplifier is bipolar and measures both positive and negative currents. The power monitor amplifier has an input range of ±25 mV.

The two basic modes of operation for the power monitor are single shot and continuous. In single shot mode, the ADC samples the input voltage and current a number of times, depending on the averaging value selected by the user. The ADM1278 returns a single value corresponding to the average voltage and current measured. When configured for continuous mode, the power monitor continuously samples the voltage and current, making the most recent sample available to be read.

The single shot mode can be triggered in a number of ways. The simplest method is by selecting the single shot mode using the PMON_CONFIG command and writing to the convert bit using the PMON_CONTROL command. The convert bit can also be written as part of a PMBus group command. Using a group command allows multiple devices to be written to as part of the same I²C bus transaction, with all devices executing the command when the stop condition appears on the bus. In this way, several devices can be triggered to sample at the same time.

# PMBUS INTERFACE

The I²C bus is a common, simple serial bus used by many devices to communicate. It defines the electrical specifications, the bus timing, the physical layer, and some basic protocol rules.

SMBus is based on I²C and aims to provide a more robust and fault tolerant bus. Functions such as bus timeout and packet error checking are added to help achieve this robustness, together with more specific definitions of the bus messages used to read and write data to devices on the bus.

PMBus is layered on top of SMBus and, in turn, on I²C. Using the SMBus defined bus messages, PMBus defines a set of standard commands that can be used to control a device that is part of a power chain.

The ADM1278 command set is based on the *PMBus™ Power System Management Protocol Specification*, Part I and Part II, Revision 1.2. This version of the standard is intended to provide a common set of commands for communicating with dc-to-dc type devices. However, many of the standard PMBus commands can be mapped directly to the functions of a hot swap controller.

Part I and Part II of the PMBus standard describe the basic commands and their use in a typical PMBus setup. The following sections describe how the PMBus standard and the ADM1278 specific commands are used.

## DEVICE ADDRESSING

The ADM1278 is available in three A grade models: the ADM1278-1, ADM1278-2, and ADM1278-3. There is also an AA grade version of the ADM1278-1 with improved power monitoring accuracy and a B grade version with lower power monitoring accuracy.

The PMBus device address is seven bits in size. There are no default addresses for any of the models; any device can be programmed to any of 16 possible addresses. Two quad level ADRx pins map to the 16 possible device addresses.

**Table 10. ADRx Pin Connections**

| ADRx State | ADRx Pin Connection |
|---|---|
| Low | Connect to GND |
| Resistor | 150 kΩ resistor to GND |
| High-Z | No connection (floating) |
| High | Connect to VCAP |

**Table 11. PMBus Address Decode (7-Bit Address)**

| ADR2 State | ADR1 State | Device Address (Hex) |
|---|---|---|
| Low | Low | 0x10 |
| Low | Resistor | 0x11 |
| Low | High-Z | 0x12 |
| Low | High | 0x13 |
| Resistor | Low | 0x40 |
| Resistor | Resistor | 0x41 |
| Resistor | High-Z | 0x42 |
| Resistor | High | 0x43 |
| High-Z | Low | 0x44 |
| High-Z | Resistor | 0x45 |
| High-Z | High-Z | 0x46 |
| High-Z | High | 0x47 |
| High | Low | 0x50 |
| High | Resistor | 0x51 |
| High | High-Z | 0x52 |
| High | High | 0x53 |

## SMBUS PROTOCOL USAGE

All I²C transactions on the ADM1278 are performed using SMBus defined bus protocols. The following SMBus protocols are implemented by the ADM1278:

- Send byte
- Receive byte
- Write byte
- Read byte
- Write word
- Read word
- Block read

## PACKET ERROR CHECKING

The ADM1278 PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the ADM1278 during a read transaction or sent by the bus host to the ADM1278 during a write transaction. The ADM1278 supports the use of PEC with all the SMBus protocols that it implements.

The use of the PEC byte is optional. The bus host can decide whether to use the PEC byte with the ADM1278 on a message by message basis. There is no need to enable or disable PEC in the ADM1278.

The PEC byte is used by the bus host or the ADM1278 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the ADM1278 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag.

Within a group command, the host can choose whether to send a PEC byte as part of the message to the ADM1278.

## PARTIAL TRANSACTIONS ON I²C BUS

If there is a partial transaction on the I²C bus (for example, spurious data interpreted as a start command), the ADM1278 I²C bus is not locked up, thinking it is in the middle of an I²C transaction. A new start command is recognized even in the middle of another transaction.

## SMBUS MESSAGE FORMATS

Figure 62 to Figure 70 show all the SMBus protocols supported by the ADM1278, along with the PEC variant. In these figures, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the ADM1278 is driving the bus.

Figure 62 to Figure 70 use the following abbreviations:

- S is the start condition.
- Sr is the repeated start condition.
- P is the stop condition.
- R is the read bit.
- $\overline{W}$ is the write bit.
- A is the acknowledge bit (0).
- $\overline{A}$ is the acknowledge bit (1).

A, the acknowledge bit, is typically active low (Logic 0) when the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by $\overline{A}$.



NOTES
1. THE SEND BYTE AND SEND BYTE WITH PEC PROTOCOLS ARE ONLY PERMITTED FOR USE WITH THE CLEAR_FAULTS COMMAND AND THE POWER_CYCLE COMMAND. THE SEND BYTE MUST NOT BE USED FOR ANY OTHER COMMANDS.
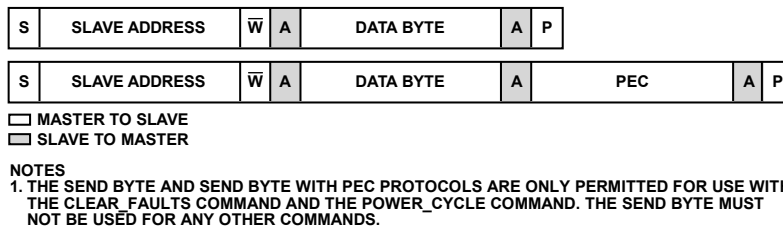
*Figure 62. Send Byte and Send Byte with PEC*
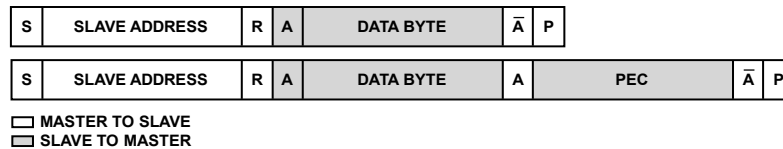


*Figure 63. Receive Byte and Receive Byte with PEC*
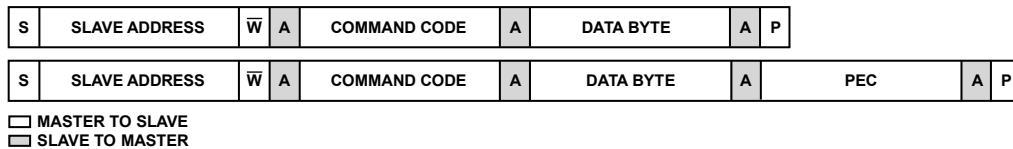


*Figure 64. Write Byte and Write Byte with PEC*
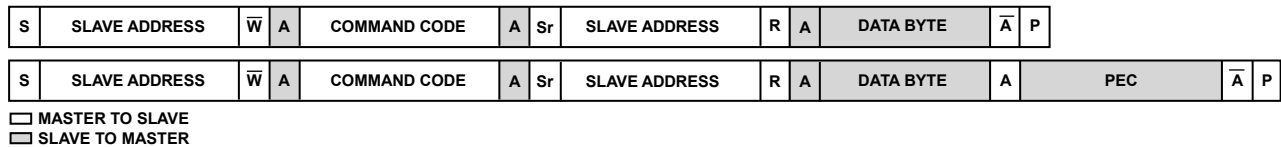


*Figure 65. Read Byte and Read Byte with PEC*
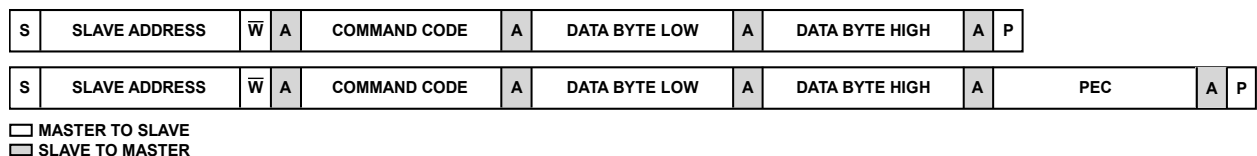


*Figure 66. Write Word and Write Word with PEC*

| S | SLAVE ADDRESS | W̄ | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | R | A | DATA BYTE LOW | A | ●●● |

| DATA BYTE HIGH | Ā | P |

| S | SLAVE ADDRESS | W̄ | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | R | A | DATA BYTE LOW | A | ●●● |

| DATA BYTE HIGH | A | PEC | Ā | P |

☐ MASTER TO SLAVE
☐ SLAVE TO MASTER
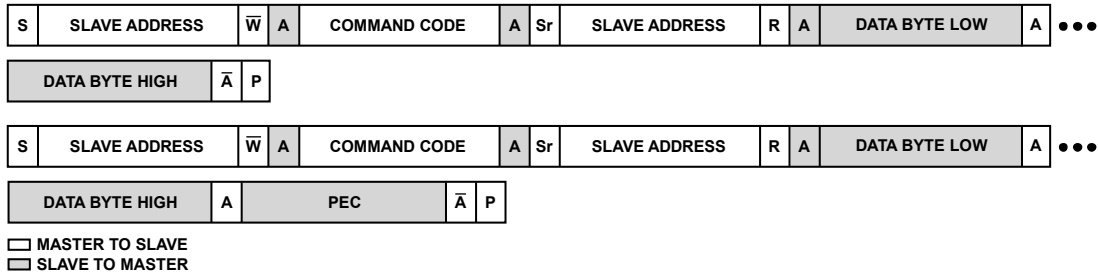
*Figure 67. Read Word and Read Word with PEC*

| S | SLAVE ADDRESS | W̄ | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | R | A | BYTE COUNT = N | A | ●●● |

| DATA BYTE 1 | A | DATA BYTE 2 | A | ●●● | DATA BYTE N | Ā | P |

| S | SLAVE ADDRESS | W̄ | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | R | A | BYTE COUNT = N | A | ●●● |

| DATA BYTE 1 | A | DATA BYTE 2 | A | ●●● | DATA BYTE N | A | PEC | Ā | P |

☐ MASTER TO SLAVE
☐ SLAVE TO MASTER
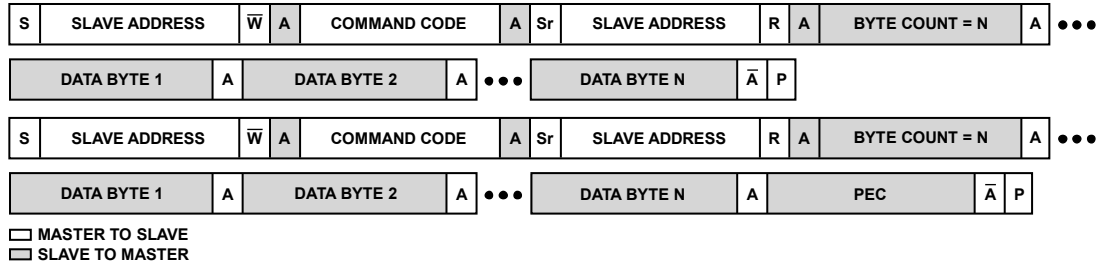
*Figure 68. Block Read and Block Read with PEC*

ONE OR MORE DATA BYTES

| S | DEVICE 1 ADDRESS | W̄ | A | COMMAND CODE 1 | A | LOW DATA BYTE | A | ●●● | HIGH DATA BYTE | A | ●●● |

ONE OR MORE DATA BYTES

| Sr | DEVICE 2 ADDRESS | W̄ | A | COMMAND CODE 2 | A | LOW DATA BYTE | A | ●●● | HIGH DATA BYTE | A | ●●● |

ONE OR MORE DATA BYTES

| Sr | DEVICE N ADDRESS | W̄ | A | COMMAND CODE N | A | LOW DATA BYTE | A | ●●● | HIGH DATA BYTE | A | P |

☐ MASTER TO SLAVE
☐ SLAVE TO MASTER

*Figure 69. Group Command*

ONE OR MORE DATA BYTES

| S | DEVICE 1 ADDRESS | W̄ | A | COMMAND CODE 1 | A | LOW DATA BYTE | A | ●●● | HIGH DATA BYTE | A | PEC 1 | A | ●●● |

ONE OR MORE DATA BYTES

| Sr | DEVICE 2 ADDRESS | W̄ | A | COMMAND CODE 2 | A | LOW DATA BYTE | A | ●●● | HIGH DATA BYTE | A | PEC 2 | A | ●●● |

ONE OR MORE DATA BYTES

| Sr | DEVICE N ADDRESS | W̄ | A | COMMAND CODE N | A | LOW DATA BYTE | A | ●●● | HIGH DATA BYTE | A | PEC N | A | P |

☐ MASTER TO SLAVE
☐ SLAVE TO MASTER

*Figure 70. Group Command with PEC*

## GROUP COMMANDS

The PMBus standard defines what are known as group commands. Group commands are single bus transactions that send commands or data to more than one device at the same time. Each device is addressed separately, using its own address; there is no special group command address. A group command transaction can contain only write commands that send data to a device. It is not possible to use a group command to read data from devices.

From an I²C protocol point of view, a normal write command consists of the following:

- I²C start condition.
- Slave address bits and a write bit (followed by an acknowledge from the slave device).
- One or more data bytes (each of which is followed by an acknowledge from the slave device).
- I²C stop condition to end the transaction.

A group command differs from a nongroup command in that after the data is written to one slave device, a repeated start condition is placed on the bus followed by the address of the next slave device and data. This continues until all of the devices have been written to, at which point the stop condition is placed on the bus by the master device.

The format of a group command and a group command with PEC is shown in Figure 69 and Figure 70, respectively.

Each device that is written to as part of the group command does not immediately execute the command written. The device must wait until the stop condition appears on the bus. At that point, all devices execute their commands at the same time.

Using a group command, it is possible, for example, to turn multiple PMBus devices on or off simultaneously. In the case of the ADM1278, it is also possible to issue a power monitor command that initiates a conversion, causing multiple ADM1278 devices to sample together at the same time.

## HOT SWAP CONTROL COMMANDS
### OPERATION Command

The GATE pin that drives the FET is controlled by a dedicated hot swap state machine. The UV and OV input pins, the TIMER, PWG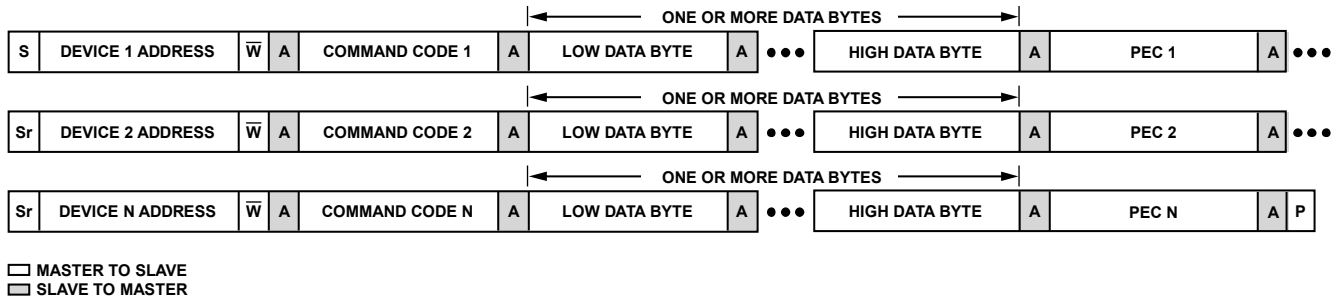IN, and ENABLE pins, and the current sense all feed into the state machine, and they control when and how strongly the gate is turned off.

It is also possible to control the hot swap GATE output using commands over the PMBus interface. The OPERATION command can be used to request the hot swap output to turn on. However, if the UV pin indicates that the input supply is less than required, the hot swap output is not turned on, even if the OPERATION command requests that the output be enabled.

If the OPERATION command is used to disable the hot swap output, the GATE pin is held low, even if all hot swap state machine control inputs indicate that it can be enabled.

The default state of Bit 7 (also named the ON bit) of the OPERATION command is 1; therefore, the hot swap output is always enabled when the ADM1278 emerges from UVLO. If the on bit is never changed, the UV input or the ENABLE/ENABLE input is the hot swap master on/off control signal.

If the on bit is set to 0 while the UV signal is high, the hot swap output is turned off. If the UV signal is low or if the OV signal is high, the hot swap output is already off and the status of the on bit has no effect.

If the on bit is set to 1, the hot swap output is requested to turn on. If the UV signal is low or if the OV signal is high, setting the on bit to 1 has no effect, and the hot swap output remains off.

It is possible to determine at any time whether the hot swap output is enabled using the STATUS_BYTE or the STATUS_WORD command (see the Status Commands section).

The OPERATION command can also clear any latched faults in the status registers. To clear latched faults, set the on bit to 0 and then reset it to 1. This also clears the latched FAULT pin.

### DEVICE_CONFIG Command

The DEVICE_CONFIG command configures certain settings within the ADM1278, for example, enabling or disabling FET health detection, general-purpose output pin configuration, and modifying the duration of the severe overcurrent settings.

### POWER_CYCLE Command

The POWER_CYCLE command can be used to request that the ADM1278 be turned off for approximately five seconds and then turned back on. This command is useful if the processor that controls the ADM1278 is also powered off when the ADM1278 is turned off. This command allows the processor to request that the ADM1278 turn off and on again as part of a single command.

## ADM1278 INFORMATION COMMANDS
### CAPABILITY Command

The CAPABILITY command can be used by host processors to determine the I²C bus features that are supported by the ADM1278. The features that can be reported include the maximum bus speed, whether the device supports the packet error checking (PEC) byte, and the SMBAlert reporting function.

### PMBUS_REVISION Command

The PMBUS_REVISION command reports the version of Part I and Part II of the PMBus standard.

### MFR_ID, MFR_MODEL, and MFR_REVISION Commands

The MFR_ID, MFR_MODEL, and MFR_REVISION commands return ASCII strings that can be used to facilitate detection and identification of the ADM1278 on the bus.

These commands are read using the SMBus block read message type. This message type requires that the ADM1278 return a byte count corresponding to the length of the string data that is to be read back.

# STATUS COMMANDS

The ADM1278 provides a number of status bits to report faults and warnings from the hot swap controller and the power monitor. These status bits are located in six different registers that are arranged in a hierarchy. The STATUS_BYTE and STATUS_WORD commands provide 8 bits and 16 bits of high level information, respectively. The STATUS_BYTE and STATUS_WORD commands contain the most important status bits, as well as pointer bits that indicate whether any of the five other status registers need to be read for more detailed status information.

In the ADM1278, a particular distinction is made between faults and warnings. A fault is always generated by the hot swap controller and is typically defined by hardware component values. Events that can generate a fault are

- Overcurrent condition that causes the hot swap timer to time out
- Overvoltage condition on the OV pin
- Undervoltage condition on the UV pin
- Overtemperature condition
- FET health issue detected

When a fault occurs, the hot swap controller always takes some action, usually to turn off the GATE pin, which is driving the FET. The $\overline{FAULT}$ pin is asserted, and the PWRGD pin is deasserted. A fault can also generate an SMBAlert on the GPO2/$\overline{ALERT2}$ pin.

All warnings in the ADM1278 are generated by the power monitor, which samples the voltage, current, and temperature and then compares these measurements to the threshold values set by the various limit commands. A warning has no effect on the hot swap controller, but it may generate an SMBAlert on one or both of the GPOx/$\overline{ALERTx}$ output pins.

When a status bit is set, it always means that the status condition—fault or warning—is active or was active at some point in the past. When a fault or warning bit is set, it is latched until it is explicitly cleared using either the OPERATION or the CLEAR_FAULTS command. Some other status bits are live, that is, they always reflect a status condition and are never latched.

## STATUS_BYTE and STATUS_WORD Commands

The STATUS_BYTE and STATUS_WORD commands obtain a snapshot of the overall device status. These commands indicate whether it is necessary to read more detailed information using the other status commands.

The low byte of the word returned by the STATUS_WORD command is the same byte returned by the STATUS_BYTE command. The high byte of the word returned by the STATUS_WORD command provides a number of bits that determine which of the other status commands needs to be issued to obtain all active status bits. The status bits for FET health and power good are also found in the high byte of STATUS_WORD.

## STATUS_INPUT Command

The STATUS_INPUT command returns a number of bits relating to voltage faults and warnings on the input supply as well as the overpower warning.

## STATUS_VOUT Command

The STATUS_VOUT command returns a number of bits relating to voltage warnings on the output supply.

## STATUS_IOUT Command

The STATUS_IOUT command returns a number of bits relating to current faults and warnings on the output supply.

## STATUS_TEMPERATURE Command

The STATUS_TEMPERATURE command returns a number of bits relating to temperature faults and warnings at the external transistor.

## STATUS_MFR_SPECIFIC Command

The STATUS_MFR_SPECIFIC command is a standard PMBus command, but the contents of the byte returned are specific to the ADM1278.

## CLEAR_FAULTS Command

The CLEAR_FAULTS command clears fault and warnings bits when they are set. Fault and warnings bits are latched when they are set. In this way, a host can read the bits any time after the fault or warning condition occurs and determine which problem actually occurred.

If the CLEAR_FAULTS command is issued and the fault or warning condition is no longer active, the status bit is cleared. If the condition is still active—for example, if an input voltage is below the undervoltage threshold of the UV pin—the CLEAR_FAULTS command attempts to clear the status bit, but that status bit is immediately set again.

# GPO AND ALERT PIN SETUP COMMANDS

Two multipurpose pins are provided on the ADM1278: GPO1/$\overline{ALERT1}$/CONV and GPO2/$\overline{ALERT2}$.

These pins can be configured over the PMBus in one of three output modes, as follows:

- General-purpose digital output
- Output for generating an SMBAlert when one or more fault/warning status bits become active in the PMBus status registers
- Digital comparator

In digital comparator mode, the current, voltage, power and temperature warning thresholds are compared to the values read or calculated by the ADM1278. The comparison result sets the output high or low according to whether the value is greater or less than the warning threshold that has been set.

For an example of how to configure these pins to generate an SMBAlert and how to respond and clear the condition, see the Example Use of SMBus ARA section.

### ALERT1_CONFIG and ALERT2_CONFIG Commands

Using combinations of bit masks, the ALERT1_CONFIG and ALERT2_CONFIG commands select the status bits that, when set, generate an SMBAlert signal to a processor, or control the digital comparator mode. Pin 13 and Pin 14 (GPO1/$\overline{\text{ALERT1}}$/ CONV and GPO2/$\overline{\text{ALERT2}}$) must be configured in SMBAlert or digital comparator mode in the DEVICE_CONFIG register.

When Pin 13 or Pin 14 is configured in GPO mode, the pin is under software control. If this mode is set, the SMBAlert masking bits are ignored.

## POWER MONITOR COMMANDS

The ADM1278 provides a high accuracy, 12-bit current, voltage, and temperature power monitor. The power monitor can be configured in a number of different modes of operation and can run in either continuous mode or single shot mode with different sample averaging options.

The power monitor can measure the following quantities:

- Input voltage ($V_{IN}$)
- Output voltage ($V_{OUT}$)
- Output current ($I_{OUT}$)
- External temperature

The following quantities are then calculated:

- Input power ($P_{IN}$)
- Input energy ($E_{IN}$)

### PMON_CONFIG Command

The power monitor can run in a variety of modes. The PMON_CONFIG command sets up the power monitor.

The settings that can be configured are as follows:

- Single shot or continuous sampling
- $V_{IN}$/$V_{OUT}$/temperature sampling enable/disable
- Current and voltage sample averaging
- Power sample averaging
- Simultaneous sampling enable/disable
- Temperature sensor filter enable/disable

Modifying the power monitor settings while the power monitor is sampling is not recommended. To ensure correct operation of the device and to avoid any potential spurious data or the generation of status alerts, stop the power monitor before any of these settings are changed.

### PMON_CONTROL Command

Power monitor sampling can be initiated via hardware or via software using the PMON_CONTROL command. This command can be used with single shot or continuous mode.

### READ_VIN, READ_VOUT, and READ_IOUT Commands

The ADM1278 power monitor always measures the voltage developed across the sense resistor to provide a current measurement. The input voltage measurement from the HS+ pin is also enabled by default. The output voltage present on the VOUT pin is available if enabled with the PMON_CONFIG command.

### READ_TEMPERATURE_1 Command

Temperature measurement at an external transistor can also be enabled with the PMON_CONFIG command. If enabled, the temperature sensor takes over the ADC for 64 μs (typical) every 6 ms and returns a measurement every 12 ms.

### READ_PIN, READ_PIN_EXT, READ_EIN, and READ_EIN_EXT Commands

The 12-bit input voltage ($V_{IN}$) and 12-bit current ($I_{OUT}$) measurement values are multiplied by the ADM1278 to give the input power value. This is accomplished by using fixed point arithmetic, and produces a 24-bit value. It is assumed that the numbers are in the 12.0 format, meaning that there is no fractional part. Note that only positive $I_{OUT}$ values are used to avoid returning a negative power.

This 24-bit value can be read from the ADM1278 using the READ_PIN_EXT command, where the most significant bit (MSB) is always a zero because PIN_EXT is a twos complement binary value that is always positive.

The 16 most significant bits of the 24-bit value are used as the value for $P_{IN}$. The MSB of the 16-bit $P_{IN}$ word is always zero, because $P_{IN}$ is a twos complement binary value that is always positive.

Each time a power calculation is completed, the 24-bit power value is added to a 24-bit energy accumulator register. This is a twos complement representation as well; therefore, the MSB is always zero. Each time this energy accumulator register rolls over from 0x7FFFFF to 0x000000, a 16-bit rollover counter is incremented. The rollover counter is straight binary, with a maximum value of 0xFFFF before it rolls over.

A 24-bit straight binary power sample counter is also incremented by 1 each time a power value is calculated and added to the energy accumulator.

These registers can be read back using one of two commands, depending on the level of accuracy required for the energy accumulator and the desire to limit the frequency of reads from the ADM1278.

A bus host can read these values, and by calculating the delta in the energy accumulated, the delta in the number of samples, and the time delta since the last read, the host can calculate the average power since the last read, as well as the energy consumed since then.

The time delta is calculated by the bus host based on when it sends its commands to read from the device, and is not provided by the ADM1278.

To avoid loss of data, the bus host must read at a rate that ensures the rollover counter does not wrap around more than once, and if the counter does wrap around, that the next value read for $P_{IN}$ is less than the previous one.

The READ_EIN command returns the top 16 bits of the energy accumulator, the lower 8 bits of the rollover counter, and the full 24 bits of the sample counter.

The READ_EIN_EXT command returns the full 24 bits of the energy accumulator, the full 16 bits of the rollover counter, and the full 24 bits of the sample counter. The use of the longer rollover counter means that the time interval between reads of the device can be increased from seconds to minutes without losing any data.

### PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE Commands

In addition to the standard PMBus commands for reading voltage and current, the ADM1278 provides commands that can report the maximum peak voltage, current, power, or temperature value since the peak value was last cleared.

The peak values are updated only after the power monitor has sampled and averaged the current and voltage measurements. Individual peak values are cleared by writing a 0 value with the corresponding command.

## WARNING LIMIT SETUP COMMANDS

The ADM1278 power monitor can monitor a number of different warning conditions simultaneously and report any current, voltage, power, or temperature values that exceed the user defined thresholds using the status commands.

All comparisons performed by the power monitor require the measured value to be strictly greater or less than the threshold value.

At power-up, all threshold limits are set to either minimum scale (for undervoltage or undercurrent conditions) or to maximum scale (for overvoltage, overcurrent, overpower, or overtemperature conditions). This effectively disables the generation of any status warnings by default; warning bits are not set in the status registers until the user explicitly sets the threshold values.

### VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT Commands

The VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT commands set the OV and UV thresholds on the input voltage, as measured at the HS+ pin.

### VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT Commands

The VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT commands set the OV and UV thresholds on the output voltage, as measured at the VOUT pin.

### IOUT_OC_WARN_LIMIT Command

The IOUT_OC_WARN_LIMIT command sets the OC threshold for the current flowing through the sense resistor.

### OT_WARN_LIMIT Command

The OT_WARN_LIMIT command sets the overtemperature threshold for the temperature measured at the external transistor.

### PIN_OP_WARN_LIMIT Command

The PIN_OP_WARN_LIMIT command sets the overpower threshold for the power delivered to the load.

## PMBUS DIRECT FORMAT CONVERSION

The ADM1278 uses the PMBus direct format to represent real-world quantities such as voltage, current, and power values. A direct format number takes the form of a 2-byte, twos complement, binary integer value.

It is possible to convert between direct format value and real-world quantities using the following equations. Equation 1 converts from real-world quantities to PMBus direct values, and Equation 2 converts PMBus direct format values to real-world values.

$$Y = (mX + b) \times 10^R \qquad (1)$$

$$X = 1/m \times (Y \times 10^{-R} - b) \qquad (2)$$

where:
$Y$ is the value in PMBus direct format.
$X$ is the real-world value.
$m$ is the slope coefficient, a 2-byte, twos complement integer.
$b$ is the offset, a 2-byte, twos complement integer.
$R$ is a scaling exponent, a 1-byte, twos complement integer.

The same equations are used for voltage, current, power, and temperature conversions, the only difference being the values of the m, b, and R coefficients that are used. Table 12 lists all the coefficients required for the ADM1278. The current and power coefficients shown are dependent on the value of the external sense resistor used in a given application. This means that an additional calculation must be performed to take the sense resistor value into account to obtain the coefficients for a specific sense resistor value.

The sense resistor value used in the calculations to obtain the coefficients is expressed in milliohms. The m coefficients are defined as 2-byte, twos complement numbers in the PMBus standard; therefore, the maximum positive value that can be represented is 32,767. If the m value is greater than that, and is to be stored in PMBus standard form, then divide the m coefficients by 10, and increase the R coefficient by a value of 1. For example, if a 10 mΩ sense resistor is used, the m coefficient for power is 6123, and the R coefficient is −1.

Example 1: IOUT_OC_WARN_LIMIT requires a current-limit value expressed in direct format.

If the required current limit is 10 A and the sense resistor is 2 mΩ, the first step is to determine the voltage coefficient. This is simply m = 800 × 2, giving 1600.

Using Equation 1, and expressing X, in units of amperes,

$Y = ((1600 \times 10) + 20{,}475) \times 10^{-1}$

$Y = 3647.5 = 3648$ (rounded up to integer form)

Writing a value of 3648 with the IOUT_OC_WARN_LIMIT command sets an overcurrent warning at 10 A.

Example 2: the READ_IOUT command returns a direct format value of 3339 representing the current flowing through a sense resistor of 1 mΩ.

To convert this value to the current flowing, use Equation 2, with m = 800 × 1.

$X = 1/800 \times (3339 \times 10^1 - 20{,}475)$

$X = 16.14$ A

This means that, when READ_IOUT returns a value of 3339, 16.14 A is flowing in the sense resistor.

Note that the same calculations that are used to convert power values also apply to the energy accumulator value returned by the READ_EIN command because the energy accumulator is a summation of multiple power values.

The READ_PIN_EXT and READ_EIN_EXT commands return 24-bit extended precision versions of the 16-bit values returned by READ_PIN and READ_EIN. The direct format values must be divided by 256 prior to being converted with the coefficients shown in Table 12.

Example 3: The PIN_OP_WARN_LIMIT command requires a power limit value expressed in direct format.

If the required power limit is 350 W and the sense resistor is 1 mΩ, the first step is to determine the m coefficient, that is, m = 6123 × 1, which is 6123.

Using Equation 1,

$Y = ((6123 \times 350) \times 10^{-2}$

$Y = 21{,}430.5 = 21{,}431$ (rounded up to integer form)

Writing a value of 21,431 with the PIN_OP_WARN_LIMIT command sets an overpower warning at 350 W.

## VOLTAGE AND CURRENT CONVERSION USING LSB VALUES

The direct format voltage and current values returned by the READ_VIN, READ_VOUT, and READ_IOUT commands and the corresponding peak versions are the data output directly by the ADM1278 ADC. Because the voltages and currents are 12-bit ADC output codes, they can also be converted to real-world values when there is knowledge of the size of the LSB on the ADC.

The m, b, and R coefficients defined for the PMBus conversion are required to be whole integers by the standard and have, therefore, been rounded slightly. Using this alternative method, with the exact LSB values, can provide somewhat more accurate numerical conversions.

To convert an ADC code to current in amperes, use the following formulas:

$V_{SENSE\_MO} = LSB_{CURRENT} \times (I_{ADC} - 2048)$

$I_{OUT} = V_{SENSE\_MO}/(R_{SENSE} \times 0.001)$

where:
$V_{SENSE\_MO} = (V_{MO+}) - (V_{MO-})$.
$LSB_{CURRENT} = 12.51$ μV.
$I_{ADC}$ is the 12-bit ADC code.
$I_{OUT}$ is the measured current value in amperes.
$R_{SENSE}$ is the value of the sense resistor in milliohms.

To convert an ADC code to a voltage, use the following formula:

$V_M = LSB_{VOLTAGE} \times (V_{ADC} + 0.5)$

where:
$V_M$ is the measured value in volts.
$LSB_{VOLTAGE} = 5.104$ mV.
$V_{ADC}$ is the 12-bit ADC code.

To convert a current in amperes to a 12-bit value, use the following formula (round the result to the nearest integer):

$V_{SENSE\_MO} = I_A \times R_{SENSE} \times 0.001$

$I_{CODE} = 2048 + (V_{SENSE\_MO}/LSB_{CURRENT})$

where:
$V_{SENSE\_MO} = (V_{MO+}) - (V_{MO-})$.
$I_A$ is the current value in amperes.
$R_{SENSE}$ is the value of the sense resistor in milliohms.
$I_{CODE}$ is the 12-bit ADC code.
$LSB_{CURRENT} = 12.51$ μV.

To convert a voltage to a 12-bit value, the following formula can be used (round the result to the nearest integer):

$V_{CODE} = (V_A/LSB_{VOLTAGE}) - 0.5$

where:
$V_{CODE}$ is the 12-bit ADC code.
$V_A$ is the voltage value in volts.
$LSB_{VOLTAGE} = 5.104$ mV.

**Table 12. PMBus Conversion to Real-World Coefficients**

| Coefficient | Voltage (V) | Current (A) | Power (W) | Temperature (°C) |
|---|---|---|---|---|
| m | +19,599 | +800 × R$_{SENSE}$ (in mΩ) | +6123 × R$_{SENSE}$ (in mΩ) | +42 |
| b | 0 | +20,475 | 0 | +31,880 |
| R | −2 | −1 | −2 | −1 |

# ALERT PIN BEHAVIOR

The ADM1278 provides a very flexible alert system, whereby one or more fault/warning conditions can be indicated to an external device.

## FAULTS AND WARNINGS

A PMBus fault on the ADM1278 is typically generated due to an analog event (the exception being a temperature fault) and causes a change in state in the hot swap output, turning it off. The defined fault sources are as follows:

- Undervoltage (UV) event detected on the UV pin.
- Overvoltage (OV) event detected on the OV pin.
- Overcurrent (OC) event that causes a hot swap timeout.
- Overtemperature (OT) event detected at the external transistor.
- Fault detected with the pass MOSFET.

Faults are continuously monitored, and, as long as power is applied to the device, they cannot be disabled. When a fault occurs, a corresponding status bit is set in one or more STATUS_xxx registers.

A value of 1 in a status register bit field always indicates a fault or warning condition. Fault and warning bits in the status registers are latched when set to 1. To clear a latched bit to 0—provided that the fault condition is no longer active—use the CLEAR_FAULTS command or use the OPERATION command to turn the hot swap output off and then on again.

A warning is less severe than a fault and never causes a change in the state of the hot swap controller. The sources of a warning are defined as follows:

- CML: a communications error occurred on the I²C bus.
- HS_INLIM_FAULT: the circuit breaker threshold was tripped and the TIMER pin started ramping, but did not necessarily shut the system down.
- $I_{OUT}$ OC warning from the ADC.
- $V_{IN}$ UV warning from the ADC.
- $V_{IN}$ OV warning from the ADC.
- $V_{OUT}$ UV warning from the ADC.
- $V_{OUT}$ OV warning from the ADC.
- $P_{IN}$ overpower (OP) warning from the $V_{IN} \times I_{OUT}$ calculation.
- OT warning from the ADC.
- Hysteretic output warning from the ADC.

## GENERATING AN ALERT

A host device can periodically poll the ADM1278 using the status commands to determine whether a fault/warning is active. However, this polling is very inefficient in terms of software and processor resources. The ADM1278 has two output pins (GPO1/$\overline{ALERT1}$/CONV and GPO2/$\overline{ALERT2}$) that can be used to generate interrupts to a host processor.

By default at power-up, the open-drain GPO1/$\overline{ALERT1}$ /CONV and GPO2/$\overline{ALERT2}$ outputs are high impedance; therefore, the pins can be pulled high through a resistor. The GPO1/$\overline{ALERT1}$/ CONV and GPO2/$\overline{ALERT2}$ pins are disabled by default on the ADM1278.

Any one or more of the faults and warnings listed in the Faults and Warnings section can be enabled and cause an alert, making the corresponding GPO1/$\overline{ALERT1}$/CONV or GPO2/$\overline{ALERT2}$ pin active. By default, the active state of the GPO1/$\overline{ALERT1}$/ CONV and GPO2/$\overline{ALERT2}$ pins are low.

For example, to use GPO2/$\overline{ALERT2}$ to monitor the $V_{OUT}$ UV warning from the ADC, the followings steps must be performed:

1. Set a threshold level with the VOUT_UV_WARN_LIMIT command.
2. Set the VOUT_UV_WARN_EN2 bit in the ALERT2_CONFIG register.
3. Start the power monitor sampling on $V_{OUT}$ (ensure the power monitor is configured to sample $V_{OUT}$ in the PMON_CONFIG register).

If a $V_{OUT}$ sample is taken that is below the configured $V_{OUT}$ UV value, the GPO2/$\overline{ALERT2}$ pin is pulled low, signaling an interrupt to a processor.

## HANDLING/CLEARING AN ALERT

When faults/warnings are configured on the GPO1/$\overline{ALERT1}$/ CONV or GPO2/$\overline{ALERT2}$ pins, the pin becomes active to signal an interrupt to the processor. (The pin is active low, unless inversion is enabled.) The GPO1/$\overline{ALERT1}$ /CONV or GPO2/$\overline{ALERT2}$ signal performs the functions of an SMBAlert.

Note that the GPO1/$\overline{ALERT1}$/CONV and GPO2/$\overline{ALERT2}$ pins can become active independently but they are always made inactive together.

A processor can respond to the interrupt in one of two ways, depending on whether there is a single or multiple devices on the bus.

### Single Device on Bus

When there is only one device on the bus, the processor simply reads the status bytes and issues a CLEAR_FAULTS command to clear all the status bits, which causes the deassertion of the GPO1/$\overline{ALERT1}$/CONV or GPO2/$\overline{ALERT2}$ line. If there is a persistent fault (for example, an undervoltage on the input), the status bits remain set after the CLEAR_ FAULTS command is executed because the fault has not been removed. However, the GPO1/ $\overline{ALERT1}$/CONV or GPO2/$\overline{ALERT2}$ line is not pulled low unless a new fault or warning becomes active. If the cause of the SMBAlert is a power monitor generated warning and the power monitor is running continuously, the next sample generates a new SMBAlert after the CLEAR_FAULTS command is issued.

### Multiple Devices on Bus

When there are several devices on the bus, the processor issues an SMBus alert response address (ARA) command to find out which device asserted the SMBAlert line. The processor reads the status bytes from that device and issues a CLEAR_FAULTS command.

## SMBUS ALERT RESPONSE ADDRESS

The SMBus ARA is a special address that can be used by the bus host to locate any devices that need to communicate with the bus host. A host typically uses a hardware interrupt pin to monitor the SMBus alert pins of multiple devices. When the host interrupt occurs, the host issues a message on the bus using the SMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have an SMB alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active SMBAlert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its SMBus alert signal. If the host sees that the SMBus alert signal is still low, it continues to read addresses until all devices that need to communicate have successfully transmitted their addresses.

## EXAMPLE USE OF SMBUS ARA

The full sequence of steps that occurs when an SMBAlert is generated and cleared is as follows:

1. A fault or warning is enabled using the ALERT2_CONFIG command, and the corresponding status bit for the fault or warning changes from 0 to 1, indicating that the fault or warning has just become active.
2. The GPO2/$\overline{ALERT2}$ pin becomes active (set low) to signal that an SMBAlert is active.
3. The host processor issues an SMBus ARA command to determine which device has an active alert.
4. If there are no other active alerts from devices with lower I2C addresses, this device makes the GPO2/$\overline{ALERT2}$ pin inactive (set high) during the no acknowledge bit period after it sends its address to the host processor.
5. If the GPO2/$\overline{ALERT2}$ pin stays low, the host processor must continue to issue SMBus ARA commands to devices to determine the addresses of all devices that require a status check.
6. The ADM1278 continues to operate with the GPO2/$\overline{ALERT2}$ pin inactive and the contents of the status bytes unchanged until the host reads the status bytes and clears them, or until a new fault occurs. That is, if a status bit for a fault/warning that is enabled on the GPO2/$\overline{ALERT2}$ pin and that was not already active (equal to 1) changes from 0 to 1, a new alert is generated, causing the GPO2/$\overline{ALERT2}$ pin to become active again.

## DIGITAL COMPARATOR MODE

The GPO1/$\overline{ALERT1}$/CONV and GPO2/$\overline{ALERT2}$ pins can be configured to indicate if a user defined threshold for voltage, current, or power is being exceeded. In this mode, the output pin is live and is not latched when a warning threshold is exceeded. In effect, the pin acts as a digital comparator, where the threshold is set using the warning limit threshold commands.

The ALERTx_CONFIG command is used, as for the SMBAlert configuration, to select the specific warning threshold to be monitored. The GPO1/ALERT1/CONV or GPO2/ALERT2 pin then indicates if the measured value is above or below the threshold.

## TYPICAL APPLICATION CIRCUITS



Figure 71. ADM1278-1 Typical Application Circuit

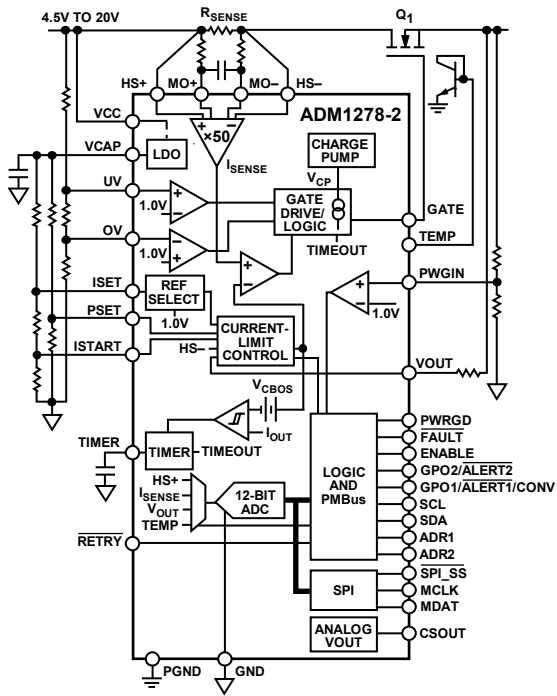*Figure 72. ADM1278-2 Typical Application Circuit*



*Figure 73. ADM1278-3 Typical Application Circuit*

# PMBUS COMMAND REFERENCE

Register addresses are in hexadecimal format.

**Table 13. PMBus Command Summary**

| Address | Name | SMBus Transaction Type | Number of Data Bytes | Reset |
|---------|------|------------------------|----------------------|-------|
| 0x01 | OPERATION | Read/write byte | 1 | 0x80 |
| 0x03 | CLEAR_FAULTS | Send byte[1] | 0 | Not applicable |
| 0x19 | CAPABILITY | Read byte | 1 | 0xB0 |
| 0x42 | VOUT_OV_WARN_LIMIT | Read/write word | 2 | 0x0FFF |
| 0x43 | VOUT_UV_WARN_LIMIT | Read/write word | 2 | 0x0000 |
| 0x4A | IOUT_OC_WARN_LIMIT | Read/write word | 2 | 0x0FFF |
| 0x4F | OT_FAULT_LIMIT | Read/write word | 2 | 0x0FFF |
| 0x51 | OT_WARN_LIMIT | Read/write word | 2 | 0x0FFF |
| 0x57 | VIN_OV_WARN_LIMIT | Read/write word | 2 | 0x0FFF |
| 0x58 | VIN_UV_WARN_LIMIT | Read/write word | 2 | 0x0000 |
| 0x6B | PIN_OP_WARN_LIMIT | Read/write word | 2 | 0x7FFF |
| 0x78 | STATUS_BYTE | Read byte | 1 | 0x00 |
| 0x79 | STATUS_WORD | Read word | 2 | 0x0000 |
| 0x7A | STATUS_VOUT | Read byte | 1 | 0x00 |
| 0x7B | STATUS_IOUT | Read byte | 1 | 0x00 |
| 0x7C | STATUS_INPUT | Read byte | 1 | 0x00 |
| 0x7D | STATUS_TEMPERATURE | Read byte | 1 | 0x00 |
| 0x80 | STATUS_MFR_SPECIFIC | Read byte | 1 | 0x00 |
| 0x86 | READ_EIN | Block read | 6 | 0x000000000000 |
| 0x88 | READ_VIN | Read word | 2 | 0x0000 |
| 0x8B | READ_VOUT | Read word | 2 | 0x0000 |
| 0x8C | READ_IOUT | Read word | 2 | 0x0000 |
| 0x8D | READ_TEMPERATURE_1 | Read word | 2 | 0x0000 |
| 0x97 | READ_PIN | Read word | 2 | 0x0000 |
| 0x98 | PMBUS_REVISION | Read byte | 1 | 0x22 |
| 0x99 | MFR_ID | Block read | 3 | ASCII = ADI |
| 0x9A | MFR_MODEL | Block read | 10 | ASCII = ADM1278-xy |
| 0x9B | MFR_REVISION | Block read | 1 | 0x33 |
| 0x9D | MFR_DATE | Block read | 6 | ASCII = YYMMDD |
| 0xD0 | PEAK_IOUT | Read/write word | 2 | 0x0000 |
| 0xD1 | PEAK_VIN | Read/write word | 2 | 0x0000 |
| 0xD2 | PEAK_VOUT | Read/write word | 2 | 0x0000 |
| 0xD3 | PMON_CONTROL | Read/write byte | 1 | 0x01 |
| 0xD4 | PMON_CONFIG | Read/write word | 2 | 0x0714 |
| 0xD5 | ALERT1_CONFIG | Read/write word | 2 | 0x0000 |
| 0xD6 | ALERT2_CONFIG | Read/write word | 2 | 0x0000 |
| 0xD7 | PEAK_TEMPERATURE | Read/write word | 2 | 0x0000 |
| 0xD8 | DEVICE_CONFIG | Read/write word | 2 | 0x000D |
| 0xD9 | POWER_CYCLE | Send byte[1] | 0 | Not applicable |
| 0xDA | PEAK_PIN | Read/write word | 2 | 0x0000 |
| 0xDB | READ_PIN_EXT | Block read | 3 | 0x000000 |
| 0xDC | READ_EIN_EXT | Block read | 8 | 0x0000000000000000 |
| 0xF2 | HYSTERESIS_LOW | Read/write word | 2 | 0x0000 |
| 0xF3 | HYSTERESIS_HIGH | Read/write word | 2 | 0xFFFF |
| 0xF4 | STATUS_HYSTERESIS | Read byte | 1 | 0x00 |
| 0xF6 | STRT_UP_IOUT_LIM | Read/write word | 2 | 0x000F |

[1] The send byte protocol is only permitted for the CLEAR_FAULTS command and the POWER_CYCLE command. Do not use the send byte protocol for any other commands.

# REGISTER DETAILS

## OPERATION REGISTER

**Address: 0x01, Reset: 0x80, Name: OPERATION**

This command requests the hot swap turn on and turn off. When turning the hot swap on, it clears status bits for any faults or warnings that are not active.

**Table 14. Bit Descriptions for OPERATION**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | ON | | Hot swap enable. | 0x1 | RW |
| | | 0 | Hot swap output disabled. | | |
| | | 1 | Hot swap output enabled. | | |
| [6:0] | RESERVED | | Always reads as 0000000. | 0x00 | RESERVED |

## CLEAR FAULTS REGISTER

**Address: 0x03, Send Byte, No Data, Name: CLEAR_FAULTS**

This command clears fault and warning bits in all the status registers. Any faults that are still active are not cleared and remain set. Any warnings and the OT_FAULT that are generated by the power monitor are cleared, but may be asserted again if they remain active following the next power monitor conversion cycle.

This command does not require any data.

## PMBUS CAPABILITY REGISTER

**Address: 0x19, Reset: 0xB0, Name: CAPABILITY**

Allows the host system to determine the SMBus interface capabilities of the device.

**Table 15. Bit Descriptions for CAPABILITY**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | PEC_SUPPORT | | Packet error correction (PEC) support. | 0x1 | R |
| | | 1 | Always reads as 1. PEC is supported. | | |
| [6:5] | MAX_BUS_SPEED | | Maximum bus interface speed. | 0x1 | R |
| | | 01 | Always reads as 01. Maximum supported bus speed is 400 kHz. | | |
| 4 | SMBALERT_SUPPORT | | SMBAlert support. | 0x1 | R |
| | | 1 | Always reads as 1. Device supports SMBAlert and ARA. | | |
| [3:0] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |

## V$_{OUT}$ OV WARNING LIMIT REGISTER

**Address: 0x42, Reset: 0x0FFF, Name: VOUT_OV_WARN_LIMIT**

This register sets the overvoltage warning limit for the voltage measured on the VOUT pin.

**Table 16. Bit Descriptions for VOUT_OV_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | VOUT_OV_WARN_LIMIT | | Overvoltage warning threshold for the VOUT pin measurement, expressed in direct format. | 0xFFF | RW |

## V<sub>OUT</sub> UV WARNING LIMIT REGISTER

**Address: 0x43, Reset: 0x0000, Name: VOUT_UV_WARN_LIMIT**

This register sets the undervoltage warning limit for the voltage measured on the VOUT pin.

**Table 17. Bit Descriptions for VOUT_UV_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | VOUT_UV_WARN_LIMIT | | Undervoltage warning threshold for the VOUT pin measurement, expressed in direct format. | 0x000 | RW |

## I<sub>OUT</sub> OC WARNING LIMIT REGISTER

**Address: 0x4A, Reset: 0x0FFF, Name: IOUT_OC_WARN_LIMIT**

This register sets the overcurrent warning limit for the current measured between the MO+ and the MO− pins.

**Table 18. Bit Descriptions for IOUT_OC_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | IOUT_OC_WARN_LIMIT | | Overcurrent warning threshold for the $I_{OUT}$ measurement, expressed in direct format. | 0xFFF | RW |

## OT FAULT LIMIT REGISTER

**Address: 0x4F, Reset: 0x0FFF, Name: OT_FAULT_LIMIT**

This register sets the overtemperature fault limit for the temperature measured on the TEMP pin.

**Table 19. Bit Descriptions for OT_FAULT_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | OT_FAULT_LIMIT | | Overtemperature fault threshold for the TEMP pin measurement, expressed in direct format. | 0xFFF | RW |

## OT WARNING LIMIT REGISTER

**Address: 0x51, Reset: 0x0FFF, Name: OT_WARN_LIMIT**

This register sets the overtemperature warning limit for the temperature measured on the TEMP pin.

**Table 20. Bit Descriptions for OT_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | OT_WARN_LIMIT | | Overtemperature warning threshold for the TEMP pin measurement, expressed in direct format. | 0xFFF | RW |

## V<sub>IN</sub> OV WARNING LIMIT REGISTER

**Address: 0x57, Reset: 0x0FFF, Name: VIN_OV_WARN_LIMIT**

This register sets the overvoltage warning limit for the voltage measured on the HS+ pin.

**Table 21. Bit Descriptions for VIN_OV_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | VIN_OV_WARN_LIMIT | | Overvoltage warning threshold for the HS+ pin measurement, expressed in direct format. | 0xFFF | RW |

## V$_{IN}$ UV WARNING LIMIT REGISTER

**Address: 0x58, Reset: 0x0000, Name: VIN_UV_WARN_LIMIT**

This register sets the undervoltage warning limit for the voltage measured on the HS+ pin.

**Table 22. Bit Descriptions for VIN_UV_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | VIN_UV_WARN_LIMIT | | Undervoltage warning threshold for the HS+ pin measurement, expressed in direct format. | 0x000 | RW |

## P$_{IN}$ OP WARNING LIMIT REGISTER

**Address: 0x6B, Reset: 0x7FFF, Name: PIN_OP_WARN_LIMIT**

This register sets the overpower warning limit for the power calculated based on $V_{IN} \times I_{OUT}$.

**Table 23. Bit Descriptions for PIN_OP_WARN_LIMIT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 15 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |
| [14:0] | PIN_OP_WARN_LIMIT | | Overpower warning threshold for the $V_{IN} \times I_{OUT}$ power calculation, expressed in direct format. | 0x7FFF | RW |

## STATUS BYTE REGISTER

**Address: 0x78, Reset: 0x00, Name: STATUS_BYTE**

Provides status information for critical faults and certain top-level status commands in the device. This is also the lower byte returned by STATUS_WORD. A bit set to 1 indicates that a fault or warning has occurred.

**Table 24. Bit Descriptions for STATUS_BYTE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |
| 6 | HOTSWAP_OFF | | Hot swap gate is off. This bit is live. | 0x0 | R |
| | | 0 | The hot swap gate drive output is enabled. | | |
| | | 1 | The hot swap gate drive output is disabled, and the GATE pin is pulled down. This can be due to, for example, an overcurrent fault that causes the device to latch off, an undervoltage condition on the UV pin, or the use of the OPERATION command to turn the output off. | | |
| 5 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |
| 4 | IOUT_OC_FAULT | | I$_{OUT}$ overcurrent fault. This bit is latched. | 0x0 | R |
| | | 0 | No overcurrent output fault detected. | | |
| | | 1 | The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down. | | |
| 3 | VIN_UV_FAULT | | V$_{IN}$ fault. This bit is latched. | 0x0 | R |
| | | 0 | No undervoltage input fault detected on the UV pin. | | |
| | | 1 | An undervoltage input fault was detected on the UV pin. | | |
| 2 | TEMP_FAULT | | Temperature fault or warning. This bit is live. | 0x0 | R |
| | | 0 | There are no active status bits to be read by STATUS_TEMPERATURE. | | |
| | | 1 | There are one or more active status bits to be read by STATUS_TEMPERATURE. | | |
| 1 | CML_FAULT | | CML fault. This bit is latched. | 0x0 | R |
| | | 0 | No communications error detected on the I²C/PMBus interface. | | |
| | | 1 | An error was detected on the I²C/PMBus interface. Errors detected include an unsupported command, invalid PEC byte, and | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| | | | incorrectly structured message. | | |
| 0 | NONEABOVE_STATUS | | None of the above. This bit is live. | 0x0 | R |
| | | 0 | No other active status bit reported by any other status command. | | |
| | | 1 | Active status bits are waiting to be read by one or more status commands. | | |

## STATUS WORD REGISTER

**Address: 0x79, Reset: 0x0000, Name: STATUS_WORD**

Provides status information for critical faults and all top-level status commands in the device. The lower byte is also returned by STATUS_BYTE.

**Table 25. Bit Descriptions for STATUS_WORD**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 15 | VOUT_STATUS | | $V_{OUT}$ warning. This bit is live. | 0x0 | R |
| | | 0 | There are no active status bits to be read by the STATUS_VOUT register. | | |
| | | 1 | There are one or more active status bits to be read by STATUS_VOUT. | | |
| 14 | IOUT_STATUS | | $I_{OUT}$ fault or warning. This bit is live. | 0x0 | R |
| | | 0 | There are no active status bits to be read by the STATUS_IOUT register. | | |
| | | 1 | There are one or more active status bits to be read by the STATUS_IOUT register. | | |
| 13 | INPUT_STATUS | | Input warning. This bit is live. | 0x0 | R |
| | | 0 | There are no active status bits to be read by the STATUS_INPUT register. | | |
| | | 1 | There are one or more active status bits to be read by STATUS_INPUT. | | |
| 12 | MFR_STATUS | | Manufacture specific fault or warning. This bit is live. | 0x0 | R |
| | | 0 | There are no active status bits to be read by the STATUS_MFR_SPECIFIC register. | | |
| | | 1 | There are one or more active status bits to be read by STATUS_MFR_SPECIFIC register. | | |
| 11 | PGB_STATUS | | Power is not good. This bit is live. | 0x0 | R |
| | | 0 | Output power is good. The voltage on the PWGIN pin is above the threshold. | | |
| | | 1 | Output power is bad. The voltage on the PWGIN pin is below the threshold. | | |
| [10:9] | RESERVED | | | 0x0 | RESERVED |
| 8 | FET_HEALTH_FAULT | | FET health fault. This bit is latched. | 0x0 | R |
| | | 0 | No FET faults have been detected. | | |
| | | 1 | A fault condition has been detected on the FET. | | |
| 7 | RESERVED | | Always set to 0. | 0x0 | RESERVED |
| 6 | HOTSWAP_OFF | | Duplicate of corresponding bit in the STATUS_BYTE register. | 0x0 | R |
| 5 | RESERVED | | Always set to 0. | 0x0 | RESERVED |
| 4 | IOUT_OC_FAULT | | Duplicate of corresponding bit in the STATUS_BYTE register. | 0x0 | R |
| 3 | VIN_UV_FAULT | | Duplicate of corresponding bit in the STATUS_BYTE register. | 0x0 | R |
| 2 | TEMP_FAULT | | Duplicate of corresponding bit in the STATUS_BYTE register. | 0x0 | R |
| 1 | CML_FAULT | | Duplicate of corresponding bit in the STATUS_BYTE register. | 0x0 | R |
| 0 | NONEABOVE_STATUS | | Duplicate of corresponding bit in the STATUS_BYTE register. | 0x0 | R |

## V<sub>OUT</sub> STATUS REGISTER

**Address: 0x7A, Reset: 0x00, Name: STATUS_VOUT**

Provides status information for warnings related to V<sub>OUT</sub>.

**Table 26. Bit Descriptions for STATUS_VOUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |
| 6 | VOUT_OV_WARN | | V<sub>OUT</sub> Overvoltage Warning. | 0x0 | R |
| | | 0 | No overvoltage condition on the output supply detected by the power monitor. | | |
| | | 1 | An overvoltage condition on the output supply was detected by the power monitor. This bit is latched. | | |
| 5 | VOUT_UV_WARN | | V<sub>OUT</sub> UV warning. | 0x0 | R |
| | | 0 | No undervoltage condition on the output supply detected by the power monitor. | | |
| | | 1 | An undervoltage condition on the output supply was detected by the power monitor. This bit is latched. | | |
| [4:0] | RESERVED | | Always reads as 00000. | 0x00 | RESERVED |

## I<sub>OUT</sub> STATUS REGISTER

**Address: 0x7B, Reset: 0x00, Name: STATUS_IOUT**

Provides status information for faults and warnings related to I<sub>OUT</sub>.

**Table 27. Bit Descriptions for STATUS_IOUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | IOUT_OC_FAULT | | I<sub>OUT</sub> overcurrent fault. | 0x0 | R |
| | | 0 | No overcurrent output fault detected. | | |
| | | 1 | The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down. This bit is latched. | | |
| 6 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |
| 5 | IOUT_OC_WARN | | I<sub>OUT</sub> overcurrent warning. | 0x0 | R |
| | | 0 | No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command. | | |
| | | 1 | An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command. This bit is latched. | | |
| [4:0] | RESERVED | | Always reads as 00000. | 0x00 | RESERVED |

## INPUT STATUS REGISTER

**Address: 0x7C, Reset: 0x00, Name: STATUS_INPUT**

Provides status information for faults and warnings related to V<sub>IN</sub> and P<sub>IN</sub>.

**Table 28. Bit Descriptions for STATUS_INPUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | VIN_OV_FAULT | | V<sub>IN</sub> overvoltage fault. | 0x0 | R |
| | | 0 | No overvoltage detected on the OV pin. | | |
| | | 1 | An overvoltage was detected on the OV pin. This bit is latched. | | |
| 6 | VIN_OV_WARN | | V<sub>IN</sub> overvoltage warning fault. | 0x0 | R |
| | | 0 | No overvoltage condition on the input supply detected by the power monitor. | | |
| | | 1 | An overvoltage condition on the input supply was detected by the power monitor. This bit is latched. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 5 | VIN_UV_WARN | | V<sub>IN</sub> undervoltage warning. | 0x0 | R |
| | | 0 | No undervoltage condition on the input supply detected by the power monitor. | | |
| | | 1 | An undervoltage condition on the input supply was detected by the power monitor. This bit is latched. | | |
| 4 | VIN_UV_FAULT | | V<sub>IN</sub> undervoltage fault. | 0x0 | R |
| | | 0 | No undervoltage detected on the UV pin. | | |
| | | 1 | An undervoltage was detected on the UV pin. This bit is latched. | | |
| [3:1] | RESERVED | | Always reads as 000. | 0x0 | RESERVED |
| 0 | PIN_OP_WARN | | P<sub>IN</sub> overpower warning. | 0x0 | R |
| | | 0 | No overpower condition on the input supply detected by the power monitor. | | |
| | | 1 | An overpower condition on the input supply was detected by the power monitor. This bit is latched. | | |

## TEMPERATURE STATUS REGISTER

**Address: 0x7D, Reset: 0x00, Name: STATUS_TEMPERATURE**

Provides status information for faults and warnings related to temperature.

**Table 29. Bit Descriptions for STATUS_TEMPERATURE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | OT_FAULT | | Overtemperature fault. | 0x0 | R |
| | | 0 | No overtemperature fault detected by the ADC. | | |
| | | 1 | An overtemperature fault was detected by the ADC. This bit is latched. | | |
| 6 | OT_WARNING | | Overtemperature warning. | 0x0 | R |
| | | 0 | No overtemperature warning detected by the ADC. | | |
| | | 1 | An overtemperature warning was detected by the ADC. This bit is latched. | | |
| [5:0] | RESERVED | | Always reads as 000000. | 0x0 | RESERVED |

## MANUFACTURER SPECIFIC STATUS REGISTER

**Address: 0x80, Reset: 0x00, Name: STATUS_MFR_SPECIFIC**

Provides status information for manufacturer specific faults and warnings.

**Table 30. Bit Descriptions for STATUS_MFR_SPECIFIC**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | FET_HEALTH_FAULT | | FET health fault. | 0x0 | R |
| | | 0 | No FET health problems have been detected. | | |
| | | 1 | An FET health fault has been detected. This bit is latched. | | |
| 6 | UV_CMP_OUT | | UV input comparator fault output. | 0x0 | R |
| | | 0 | Input voltage to UV pin is above threshold. | | |
| | | 1 | Input voltage to UV pin is below threshold. This bit is live. | | |
| 5 | OV_CMP_OUT | | OV input comparator fault output. | 0x0 | R |
| | | 0 | Input voltage to OV pin is below threshold. | | |
| | | 1 | Input voltage to OV pin is above threshold. This bit is live. | | |
| 4 | SEVERE_OC_FAULT | | Severe overcurrent fault. | 0x0 | R |
| | | 0 | A severe overcurrent has not been detected by the hot swap. | | |
| | | 1 | A severe overcurrent has been detected by the hot swap. This bit is latched. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 3 | HS_INLIM_FAULT | | Hot swap in limit fault. | 0x0 | R |
| | | 0 | The hot swap has not actively limited the current into the load. | | |
| | | 1 | The hot swap has actively limited current into the load. This bit differs from the IOUT_OC_FAULT bit in that the HS_INLIM_FAULT bit is set immediately, whereas the IOUT_OC_FAULT bit is not set unless the time limit set by the capacitor on the TIMER pin elapses. This bit is latched. | | |
| [2:0] | HS_SHUTDOWN_CAUSE | | Cause of last hot swap shutdown. This bit is latched until the status registers are cleared. | 0x0 | R |
| | | 000 | The hot swap is either enabled and working correctly, or has been shut down using the OPERATION command. | | |
| | | 001 | An OT_FAULT condition occurred that caused the hot swap to shut down. | | |
| | | 010 | An IOUT_OC_FAULT condition occurred that caused the hot swap to shut down. | | |
| | | 011 | An FET_HEALTH_FAULT condition occurred that caused the hot swap to shut down. | | |
| | | 100 | A VIN_UV_FAULT condition occurred that caused the hot swap to shut down. | | |
| | | 110 | A VIN_OV_FAULT condition occurred that caused the hot swap to shut down. | | |

## READ E$_{IN}$ REGISTER

**Address: 0x86, Reset: 0x000000000000, Name: READ_EIN**

Read the energy metering registers in a single operation to ensure time consistent data.

**Table 31. Bit Descriptions for READ_EIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [47:24] | SAMPLE_COUNT | | This is the total number of P$_{IN}$ samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 5 is the high byte, Byte 4 is the middle byte, and Byte 3 is the low byte. | 0x000000 | R |
| [23:16] | ROLLOVER_COUNT | | Number of times that the energy count has rolled over from 0x7FFF to 0x0000. This is an unsigned 8-bit binary value. | 0x00 | R |
| [15:0] | ENERGY_COUNT | | Energy accumulator value in PMBus direct format. Byte 1 is the high byte, and Byte 0 is the low byte. Internally, the energy accumulator is a 24-bit value, but only the most significant 16 bits are returned with this command. Use the READ_EIN_EXT register to access the nontruncated version. | 0x0000 | R |

## READ V$_{IN}$ REGISTER

**Address: 0x88, Reset: 0x0000, Name: READ_VIN**

Reads the input voltage, V$_{IN}$, from the device.

**Table 32. Bit Descriptions for READ_VIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | READ_VIN | | Input voltage from the HS+ pin measurement after averaging, expressed in direct format. | 0x000 | R |

## READ V$_{OUT}$ REGISTER

**Address: 0x8B, Reset: 0x0000, Name: READ_VOUT**

Reads the output voltage, V$_{OUT}$, from the device.

**Table 33. Bit Descriptions for READ_VOUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | READ_VOUT | | Input voltage from the VOUT pin measurement after averaging, expressed in direct format. | 0x000 | R |

## READ I$_{OUT}$ REGISTER

**Address: 0x8C, Reset: 0x0000, Name: READ_IOUT**

Reads the output current, I$_{OUT}$, from the device.

**Table 34. Bit Descriptions for READ_IOUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | READ_IOUT | | Output current derived from MO+/MO− sense pin voltage measurement after averaging, expressed in direct format. | 0x000 | R |

## READ TEMPERATURE 1 REGISTER

**Address: 0x8D, Reset: 0x0000, Name: READ_TEMPERATURE_1**

Reads the temperature measured by the device.

**Table 35. Bit Descriptions for READ_TEMPERATURE_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | READ_TEMPERATURE_1 | | Temperature from the TEMP pin measurement after averaging, expressed in direct format. | 0x000 | R |

## READ P$_{IN}$ REGISTER

**Address: 0x97, Reset: 0x0000, Name: READ_PIN**

Reads the calculated input power, P$_{IN}$, from the device.

**Table 36. Bit Descriptions for READ_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:0] | READ_PIN | | Input power calculation, using V$_{IN}$ × I$_{OUT}$, after averaging, expressed in PMBus direct format. P$_{IN}$ values are calculated for each V$_{IN}$ × I$_{OUT}$ sample, all P$_{IN}$ values are then averaged before the value is returned to the READ_PIN register. | 0x0000 | R |

## PMBUS REVISION REGISTER

**Address: 0x98, Reset: 0x22, Name: PMBUS_REVISION**

Allows the system to read the PMBus revision that the device supports.

**Table 37. Bit Descriptions for PMBUS_REVISION**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | PMBUS_P1_REVISION | | PMBus Part I Support. | 0x2 | R |
| | | 0010 | Revision 1.2. | | |
| [3:0] | PMBUS_P2_REVISION | | PMBus Part II Support. | 0x2 | R |
| | | 0010 | Revision 1.2. | | |

## MANUFACTURER ID REGISTER

**Address: 0x99, Reset: ASCII = ADI, Name: MFR_ID**

Returns a string identifying the Manufacturer of the device.

**Table 38. Bit Descriptions for MFR_ID**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [23:0] | MFR_ID | | String identifying manufacturer as Analog Devices (ADI). | 0x494441 | R |

## MANUFACTURER MODEL REGISTER

**Address: 0x9A, Reset: ASCII = ADM1278-xy, Name: MFR_MODEL**

Returns a string identifying the specific model of the device.

**Table 39. Bit Descriptions for MFR_MODEL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [79:0] | MFR_MODEL | | String identifying model as ADM1278-xy, where xy identifies the particular model type. Note that the ADM1278-1AA model is identified as ADM1278-1A in the MFR_MODEL register. | 0x41312D383732314D4441 | R |

## MANUFACTURER REVISION REGISTER

**Address: 0x9B, Reset: 0x33, Name: MFR_REVISION**

Returns a string identifying the hardware revision of the device.

**Table 40. Bit Descriptions for MFR_REVISION**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | MFR_REVISION | | String identifying hardware revision as, for example, 3. | 0x33 | R |

## MANUFACTURER DATE REGISTER

**Address: 0x9D, Reset: ASCII = YYMMDD, Name: MFR_DATE**

Returns a string identifying the production test date of the device.

**Table 41. Bit Descriptions for MFR_DATE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [47:0] | DATE | | String identifying test date, in the form of YYMMDD. | 0x313338303231 | R |

## PEAK $I_{OUT}$ REGISTER

**Address: 0xD0, Reset: 0x0000, Name: PEAK_IOUT**

Reports the peak output current, $I_{OUT}$. Writing 0x0000 with this command resets the peak value.

**Table 42. Bit Descriptions for PEAK_IOUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | PEAK_IOUT | | Peak output current measurement, $I_{OUT}$, expressed in direct format. | 0x000 | R |

## PEAK V$_{IN}$ REGISTER

**Address: 0xD1, Reset: 0x0000, Name: PEAK_VIN**

Reports the peak input voltage, V$_{IN}$. Writing 0x0000 with this command resets the peak value.

**Table 43. Bit Descriptions for PEAK_VIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | PEAK_VIN | | Peak input voltage measurement, V$_{IN}$, expressed in direct format. | 0x000 | R |

## PEAK V$_{OUT}$ REGISTER

**Address: 0xD2, Reset: 0x0000, Name: PEAK_VOUT**

Reports the peak output voltage, V$_{OUT}$. Writing 0x0000 with this command resets the peak value.

**Table 44. Bit Descriptions for PEAK_VOUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | PEAK_VOUT | | Peak output voltage measurement, V$_{OUT}$, expressed in direct format. | 0x000 | R |

## POWER MONITOR CONTROL REGISTER

**Address: 0xD3, Reset: 0x01, Name: PMON_CONTROL**

This command starts and stops the power monitor.

**Table 45. Bit Descriptions for PMON_CONTROL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:1] | RESERVED | | Always reads as 0000000. | 0x00 | RESERVED |
| 0 | CONVERT | | Conversion enable. | 0x1 | RW |
| | | 0 | Power monitor is not running. | | |
| | | 1 | Power monitor is sampling. Default. In single shot mode, this bit clears itself after one complete cycle. In continuous mode, this bit must be written to 0 to stop sampling. A rising edge on the conversion input (CONV function of Pin 13) or a falling edge on $\overline{SPI\_SS}$ sets this bit to 1. During sampling, additional conversion edges on these pins are ignored. | | |

## POWER MONITOR CONFIGURATION REGISTER

**Address: 0xD4, Reset: 0x0714, Name: PMON_CONFIG**

This command configures the power monitor. Different combinations of channels can be included in the rotational sampling, and averaging can be set for different measurements.

**Table 46. Bit Descriptions for PMON_CONFIG**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 15 | TSFILT | | Temperature sensor filter enable. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. Data sheet specifications are with the temperature sensor filter disabled. | | |
| 14 | SIMULTANEOUS | | Simultaneous sampling. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. Power monitoring accuracy is reduced. Data sheet specifications are with simultaneous sampling disabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [13:11] | PWR_AVG | | $P_{IN}$ averaging. | 0x0 | RW |
| | | 000 | Disables sample averaging for power. | | |
| | | 001 | Sets sample averaging for power to two samples. | | |
| | | 010 | Sets sample averaging for power to four samples. | | |
| | | 011 | Sets sample averaging for power to eight samples. | | |
| | | 100 | Sets sample averaging for power to 16 samples. | | |
| | | 101 | Sets sample averaging for power to 32 samples. | | |
| | | 110 | Sets sample averaging for power to 64 samples. | | |
| | | 111 | Sets sample averaging for power to 128 samples. | | |
| [10:8] | VI_AVG | | $V_{IN}/V_{OUT}/I_{OUT}$ averaging. | 0x7 | RW |
| | | 000 | Disables sample averaging for current and voltage. | | |
| | | 001 | Sets sample averaging for current and voltage to two samples. | | |
| | | 010 | Sets sample averaging for current and voltage to four samples. | | |
| | | 011 | Sets sample averaging for current and voltage to eight samples. | | |
| | | 100 | Sets sample averaging for current and voltage to 16 samples. | | |
| | | 101 | Sets sample averaging for current and voltage to 32 samples. | | |
| | | 110 | Sets sample averaging for current and voltage to 64 samples. | | |
| | | 111 | Sets sample averaging for current and voltage to 128 samples. | | |
| [7:5] | RESERVED | | Always reads as 000. | 0x0 | RESERVED |
| 4 | PMON_MODE | | Conversion mode. | 0x1 | RW |
| | | 0 | Single shot sampling. | | |
| | | 1 | Continuous sampling. | | |
| 3 | TEMP1_EN | | Enable temperature sampling. | 0x0 | RW |
| | | 0 | Temperature sampling disabled. | | |
| | | 1 | Temperature sampling enabled. | | |
| 2 | VIN_EN | | Enable $V_{IN}$ sampling. | 0x1 | RW |
| | | 0 | $V_{IN}$ sampling disabled. | | |
| | | 1 | $V_{IN}$ sampling enabled. | | |
| 1 | VOUT_EN | | Enable $V_{OUT}$ sampling. | 0x0 | RW |
| | | 0 | $V_{OUT}$ sampling disabled. | | |
| | | 1 | $V_{OUT}$ sampling enabled. | | |
| 0 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |

## ALERT 1 CONFIGURATION REGISTER

**Address: 0xD5, Reset: 0x0000, Name: ALERT1_CONFIG**

This commands allows different combinations of faults and warnings to be configured on the GPO1 output of the GPO1/$\overline{ALERT1}$/ CONV pin. The pin can operate in different modes, configured using the DEVICE_CONFIG command.

**Table 47. Bit Descriptions for ALERT1_CONFIG**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 15 | FET_HEALTH_FAULT_EN1 | | FET health fault enable. | 0x0 | RW |
| 14 | IOUT_OC_FAULT_EN1 | | $I_{OUT}$ overcurrent fault enable. | 0x0 | RW |
| 13 | VIN_OV_FAULT_EN1 | | $V_{IN}$ overvoltage fault enable. | 0x0 | RW |
| 12 | VIN_UV_FAULT_EN1 | | $V_{IN}$ undervoltage fault enable. | 0x0 | RW |
| 11 | CML_ERROR_EN1 | | Communications error enable. | 0x0 | RW |
| 10 | IOUT_OC_WARN_EN1 | | $I_{OUT}$ overcurrent warning enable. | 0x0 | RW |
| 9 | HYSTERETIC_EN1 | | Hysteretic output enable. | 0x0 | RW |
| 8 | VIN_OV_WARN_EN1 | | $V_{IN}$ overvoltage warning enable. | 0x0 | RW |
| 7 | VIN_UV_WARN_EN1 | | $V_{IN}$ undervoltage warning enable. | 0x0 | RW |
| 6 | VOUT_OV_WARN_EN1 | | $V_{OUT}$ overvoltage warning enable. | 0x0 | RW |
| 5 | VOUT_UV_WARN_EN1 | | $V_{OUT}$ undervoltage warning enable. | 0x0 | RW |
| 4 | HS_INLIM_EN1 | | Hot swap in-limit enable. | 0x0 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 3 | PIN_OP_WARN_EN1 | | $P_{IN}$ overpower warning enable. | 0x0 | RW |
| 2 | OT_FAULT_EN1 | | Overtemperature fault enable. | 0x0 | RW |
| 1 | OT_WARN_EN1 | | Overtemperature warning enable. | 0x0 | RW |
| 0 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |

## ALERT 2 CONFIGURATION REGISTER

**Address: 0xD6, Reset: 0x0000, Name: ALERT2_CONFIG**

This commands allows different combinations of faults and warnings to be configured on the GPO2 output of the GPO2/$\overline{ALERT2}$ pin. The pin can operate in different modes, configured using the DEVICE_CONFIG command.

**Table 48. Bit Descriptions for ALERT2_CONFIG**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 15 | FET_HEALTH_FAULT_EN2 | | FET health fault enable. | 0x0 | RW |
| 14 | IOUT_OC_FAULT_EN2 | | $I_{OUT}$ overcurrent fault enable. | 0x0 | RW |
| 13 | VIN_OV_FAULT_EN2 | | $V_{IN}$ overvoltage fault enable. | 0x0 | RW |
| 12 | VIN_UV_FAULT_EN2 | | $V_{IN}$ undervoltage fault enable. | 0x0 | RW |
| 11 | CML_ERROR_EN2 | | Communications error enable. | 0x0 | RW |
| 10 | IOUT_OC_WARN_EN2 | | $I_{OUT}$ overcurrent warning enable. | 0x0 | RW |
| 9 | HYSTERETIC_EN2 | | Hysteretic output enable. | 0x0 | RW |
| 8 | VIN_OV_WARN_EN2 | | $V_{IN}$ overvoltage warning enable. | 0x0 | RW |
| 7 | VIN_UV_WARN_EN2 | | $V_{IN}$ undervoltage warning enable. | 0x0 | RW |
| 6 | VOUT_OV_WARN_EN2 | | $V_{OUT}$ overvoltage warning enable. | 0x0 | RW |
| 5 | VOUT_UV_WARN_EN2 | | $V_{OUT}$ undervoltage warning enable. | 0x0 | RW |
| 4 | HS_INLIM_EN2 | | Hot swap in-limit enable. | 0x0 | RW |
| 3 | PIN_OP_WARN_EN2 | | $P_{IN}$ overpower warning enable. | 0x0 | RW |
| 2 | OT_FAULT_EN2 | | Overtemperature fault enable. | 0x0 | RW |
| 1 | OT_WARN_EN2 | | Overtemperature warning enable. | 0x0 | RW |
| 0 | RESERVED | | Always reads as 0. | 0x0 | RESERVED |

## PEAK TEMPERATURE REGISTER

**Address: 0xD7, Reset: 0x0000, Name: PEAK_TEMPERATURE**

Reports the peak measured temperature. Writing 0x0000 with this command resets the peak value.

**Table 49. Bit Descriptions for PEAK_TEMPERATURE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| [11:0] | PEAK_TEMPERATURE | | Peak temperature measurement, expressed in direct format. | 0x000 | R |

## DEVICE CONFIGURATION REGISTER

**Address: 0xD8, Reset: 0x000D, Name: DEVICE_CONFIG**

This command configures the hot swap overcurrent threshold and filtering, and GPO1/GPO2 output modes. Note that dual function pin names are referenced by the relevant function only, for example, GPO2 for the general-purpose output function of the GPO2/$\overline{ALERT2}$ pin (see the Pin Configurations and Function Descriptions section for full pin mnemonics and descriptions).

**Table 50. Bit Descriptions for DEVICE_CONFIG**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:12] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| 11 | FHDIS | | FET health disable. | 0x0 | RW |
| | | 0 | FET health checks enabled. | | |
| | | 1 | FET health checks disabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 10 | PWR_HYST_EN | | When enabled, the general-purpose output alert hysteresis functions refer to power rather than current. The HYSTERETIC_ENx bit also needs to be set in ALERT_CONFIG. | 0x0 | RW |
| | | 0 | Current hysteresis mode. | | |
| | | 1 | Power hysteresis mode. | | |
| [9:8] | GPO2_MODE | | GPO2 configuration mode. | 0x0 | RW |
| | | 00 | Default. GPO2 is configured to generate SMBAlerts. | | |
| | | 01 | GPO2 can be used as a general-purpose digital output pin. Use the GPO2_INVERT bit to change the output state. | | |
| | | 10 | Reserved. | | |
| | | 11 | This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert. | | |
| 7 | GPO2_INVERT | | GPO2 invert mode. | 0x0 | RW |
| | | 0 | In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low. | | |
| | | 1 | In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high. | | |
| [6:5] | GPO1_MODE | | GPO1 configuration mode. | 0x0 | RW |
| | | 00 | Default. GPO1 is configured to generate SMBAlerts. | | |
| | | 01 | GPO1 can be used as a general-purpose digital output pin. Use the GPO1_INVERT bit to change the output state. | | |
| | | 10 | GPO1 is configured as a convert (CONV) input pin. | | |
| | | 11 | This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert. | | |
| 4 | GPO1_INVERT | | GPO1 invert mode. | 0x0 | RW |
| | | 0 | In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low. | | |
| | | 1 | In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high. | | |
| [3:2] | OC_TRIP_SELECT | | Severe overcurrent threshold select. | 0x11 | RW |
| | | 00 | 125%. | | |
| | | 01 | 150%. | | |
| | | 10 | 200%. | | |
| | | 11 | Default, 225%. | | |
| 1 | OC_RETRY_DIS | | Severe OC retry mode. | 0x0 | RW |
| | | 0 | Retry once immediately after severe overcurrent event. | | |
| | | 1 | Latch off after severe overcurrent event. | | |
| 0 | OC_FILT_SELECT | | Severe overcurrent filter select. | 0x1 | RW |
| | | 0 | 200 ns. | | |
| | | 1 | Default, 900 ns. | | |

## POWER CYCLE REGISTER

**Address: 0xD9, Send Byte, No Data, Name: POWER_CYCLE**

This command is provided to allow a processor to request the hot swap to turn off and turn back on again approximately five seconds later. This is useful in the event that the hot swap output is powering the processor.

This command does not require any data.

## PEAK P$_{IN}$ REGISTER

**Address: 0xDA, Reset: 0x0000, Name: PEAK_PIN**

Reports the peak input power, P$_{IN}$. Writing 0x0000 with this command resets the peak value.

**Table 51. Bit Descriptions for PEAK_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:0] | PEAK_PIN | | Peak input power calculation, P$_{IN}$, expressed in direct format. | 0x0000 | R |

## READ P$_{IN}$ (EXTENDED) REGISTER

**Address: 0xDB, Reset: 0x000000, Name: READ_PIN_EXT**

Reads the extended precision version of the calculated input power, P$_{IN}$, from the device.

**Table 52. Bit Descriptions for READ_PIN_EXT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [23:0] | READ_PIN_EXT | | Extended precision version of peak input power calculation, P$_{IN}$, expressed in PMBus direct format. | 0x000000 | R |

## READ E$_{IN}$ (EXTENDED) REGISTER

**Address: 0xDC, Reset: 0x0000000000000000, Name: READ_EIN_EXT**

Read the extended precision energy metering registers in a single operation to ensure time consistent data.

**Table 53. Bit Descriptions for READ_EIN_EXT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [63:40] | SAMPLE_COUNT | | This is the total number of P$_{IN}$ samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 7 is the high byte, Byte 6 is the middle byte, and Byte 5 is the low byte. | 0x000000 | R |
| [39:24] | ROLLOVER_EXT | | Number of times that the energy count has rolled over from 0x7FFFFF to 0x000000. This is an unsigned 16-bit binary value. Byte 4 is the high byte, and Byte 3 is the low byte. | 0x0000 | R |
| [23:0] | ENERGY_EXT | | Extended precision energy accumulator value in PMBus direct format. Byte 2 is the high byte, Byte 1 is the middle byte, and Byte 0 is the low byte. | 0x000000 | R |

## HYSTERESIS LOW LEVEL REGISTER

**Address: 0xF2, Reset: 0x0000, Name: HYSTERESIS_LOW**

This sets the lower threshold used to generate the hysteretic output signal, which can be made available on a general-purpose output pin.

**Table 54. Bit Descriptions for HYSTERESIS_LOW**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:0] | HYSTERESIS_LOW | | Value setting the lower hysteresis threshold, expressed in direct format. | 0x000 | RW |

## HYSTERESIS HIGH LEVEL REGISTER

**Address: 0xF3, Reset: 0xFFFF, Name: HYSTERESIS_HIGH**

This sets the higher threshold used to generate the hysteretic output signal, which can be made available on a general-purpose output pin.

**Table 55. Bit Descriptions for HYSTERESIS_HIGH**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:0] | HYSTERESIS_HIGH | | Value setting the higher hysteresis threshold, expressed in direct format. | 0xFFFF | RW |

## HYSTERESIS STATUS REGISTER

**Address: 0xF4, Reset: 0x00, Name: STATUS_HYSTERESIS**

This status register reports whether the hysteretic comparison is above or below the user defined thresholds, and the IOUT_OC_WARNING status bit as well.

**Table 56. Bit Descriptions for STATUS_HYSTERESIS**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | RESERVED | | Always reads as 0000. | 0x0 | RESERVED |
| 3 | IOUT_OC_WARN | | $I_{OUT}$ overcurrent warning. | 0x0 | R |
| | | 0 | No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command. | | |
| | | 1 | An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command. | | |
| 2 | HYST_STATE | | Hysteretic comparison output. | 0x0 | R |
| | | 0 | Comparison output low. | | |
| | | 1 | Comparison output high. | | |
| 1 | HYST_GT_HIGH | | Hysteretic upper threshold comparison. | 0x0 | R |
| | | 0 | Compared value is below upper threshold. | | |
| | | 1 | Compared value is above upper threshold. | | |
| 0 | HYST_LT_LOW | | Hysteretic lower threshold comparison. | 0x0 | R |
| | | 0 | Compared value is above lower threshold. | | |
| | | 1 | Compared value is below lower threshold. | | |

## START-UP $I_{OUT}$ LIMIT REGISTER

**Address: 0xF6, Reset: 0x000F, Name: STRT_UP_IOUT_LIM**

This sets the current limit initially used while the hot swap is turning on the FET.

**Table 57. Bit Descriptions for STRT_UP_IOUT_LIM**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [15:4] | RESERVED | | Always reads as 0x00. | 0x00 | RESERVED |
| [3:0] | STRT_UP_IOUT_LIM | | Current limit used during startup, expressed in direct format. | 0xF | RW |
| | | 0000 | Current limit equal to (ISTART × 1/16) (hot swap start up current limit level). | | |
| | | 0001 | Current limit equal to (ISTART × 2/16). | | |
| | | … | … | | |
| | | 1110 | Current limit equal to (ISTART × 15/16). | | |
| | | 1111 | Current limit equal to ISTART. | | |

# OUTLINE DIMENSIONS
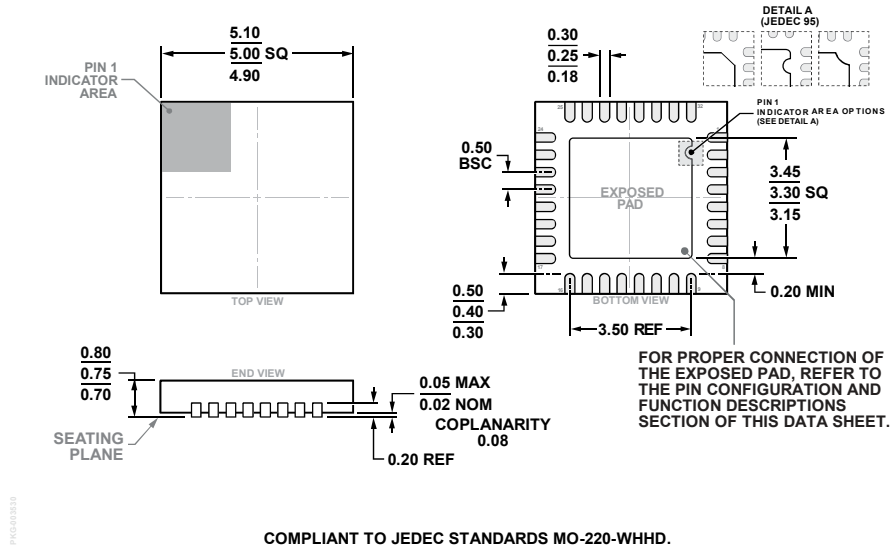


COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

*Figure 74. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.75 mm Package Height*
*(CP-32-13)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADM1278-1AACPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-1AACPZ-RL | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-1ACPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-1ACPZ-RL | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-1BCPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-1BCPZ-RL | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-2ACPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-2ACPZ-RL | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-3ACPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADM1278-3ACPZ-RL | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| EVAL-ADM1278EBZ | | Evaluation Kit | |

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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