

# **BUK7607-30B**

# N-channel TrenchMOS standard level FET Rev. 02 — 21 February 2011

**Product data sheet** 

#### 1. **Product profile**

## 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 1.3 Applications

- 12 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

## 1.4 Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$		-	-	30	V
I <sub>D</sub>	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 3</u>	[1]	-	-	75	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	157	W
Static chara	acteristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 11}}{\text{Figure 12}};$		-	5.9	7	mΩ
Avalanche	ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup} \le 30$ V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	329	mJ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 24 \text{ V}; T_j = 25 \text{ °C};$ see Figure 13		-	12	-	nC

<sup>[1]</sup> Continuous current is limited by package.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol			
1	G	gate		_			
2	D	drain[1]	mb	D			
3	S	source		$G \longrightarrow X$			
mb	D	mounting base; connected to drain		mbb076 S			
			SOT404 (D2PAK)				

<sup>[1]</sup> It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7607-30B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

		9 , (				
Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	30	V
$V_{GS}$	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	$T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	<u>[1]</u>	-	75	Α
		$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 3</u>	[2]	-	108	Α
			[1]	-	75	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; see Figure 3		-	435	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	157	W
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode					
Is	source current	T <sub>mb</sub> = 25 °C	[1]	-	75	Α
			[2]	-	108	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25  ^{\circ}C$		-	435	Α
Avalanche r	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup} \le 30$ V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	329	mJ
	-	-			_	

- [1] Continuous current is limited by package.
- [2] Current is limited by power dissipation chip rating.

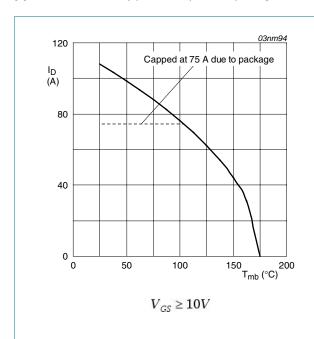


Fig 1. Normalized continuous drain current as a function of mounting base temperature

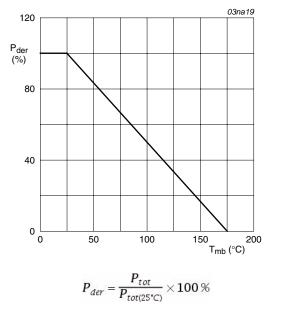
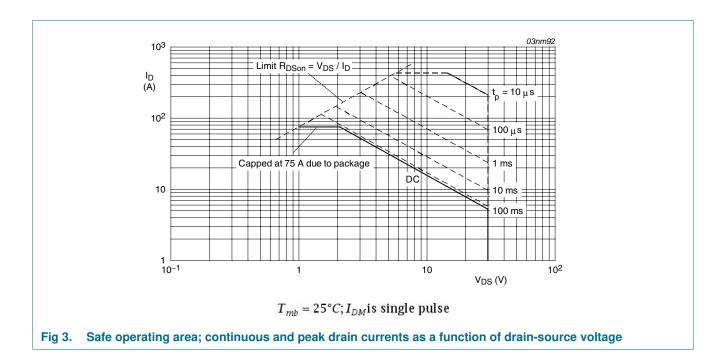


Fig 2. Normalized total power dissipation as a function of mounting base temperature

BUK7607-30B

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## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	-	50	K/W

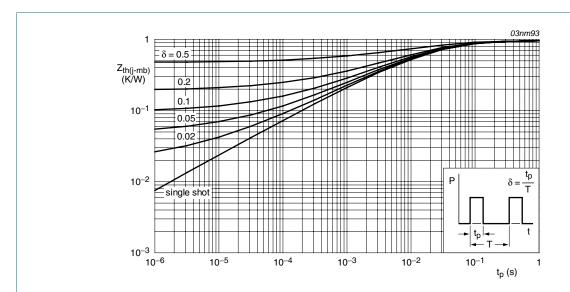


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter Parameter	Conditions	Min	Tyn	Max	Unit
Symbol Static cha	racteristics	Conditions	IVIIII	Тур	IVIAX	Unit
		1 0.25 mA: V 0.V: T 25 °C	30			V
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	27			V
V/	<del>-</del>	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$		<u>-</u> -	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 175 \text{ °C}$ ; see Figure 10	1	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ °C}$ ; see Figure 10	2	3	4	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ °C}$ ; see Figure 10	-	-	4.4	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.02	1	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub> drain-source o resistance	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 11; see Figure 12	-	-	13.3	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 11; see Figure 12	-	5.9	7	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$	-	36	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; see <u>Figure 13</u>	-	9	-	nC
$Q_{GD}$	gate-drain charge		-	12	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	1820	2427	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	632	758	рF
C <sub>rss</sub>	reverse transfer capacitance		-	256	351	рF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$	-	20	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	51	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	51	-	ns
t <sub>f</sub>	fall time		-	44	-	ns
L <sub>D</sub>	internal drain inductance	from drain lead 6 mm from package to centre of die ; $T_j = 25  ^{\circ}\text{C}$	-	4.5	-	nΗ
		from upper edge of drain mounting base to centre of die; $T_j = 25$ °C	-	2.5	-	nΗ
L <sub>S</sub>	internal source inductance	from source lead 6 mm from package to source bond pad ; $T_j = 25  ^{\circ}\text{C}$	-	7.5	-	nΗ
Source-di	rain diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 15	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	46	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ °C}$	-	28	-	nC

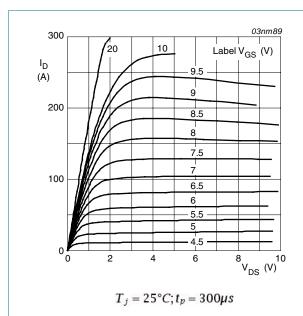


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

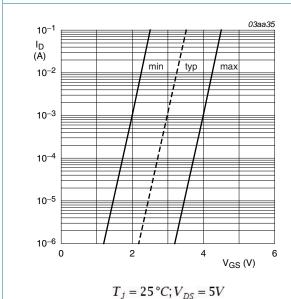


Fig 7. Sub-threshold drain current as a function of gate-source voltage

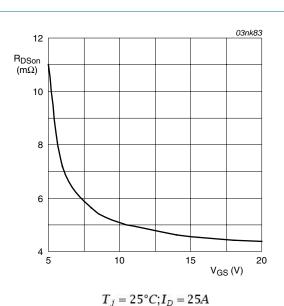


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

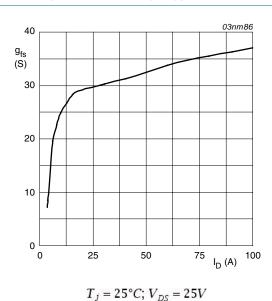


Fig 8. Forward transconductance as a function of drain current; typical values

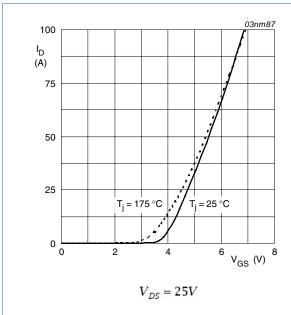


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

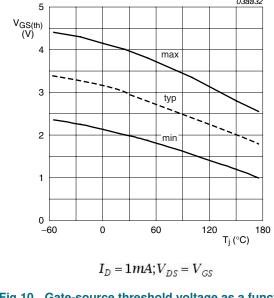


Fig 10. Gate-source threshold voltage as a function of junction temperature

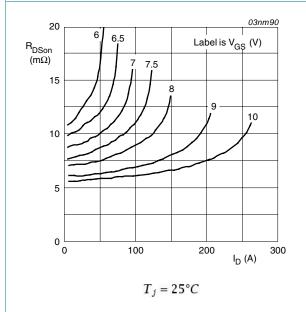


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

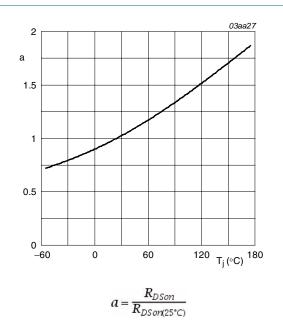


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

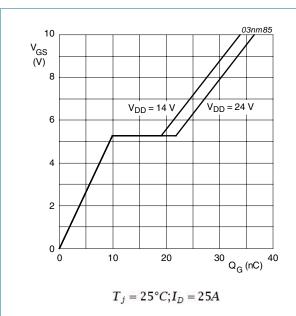


Fig 13. Gate-source voltage as a function of gate charge; typical values

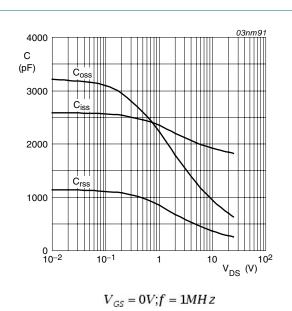


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

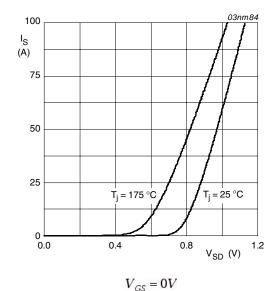


Fig 15. Source current as a function of source-drain voltage; typical values

## 7. Package outline

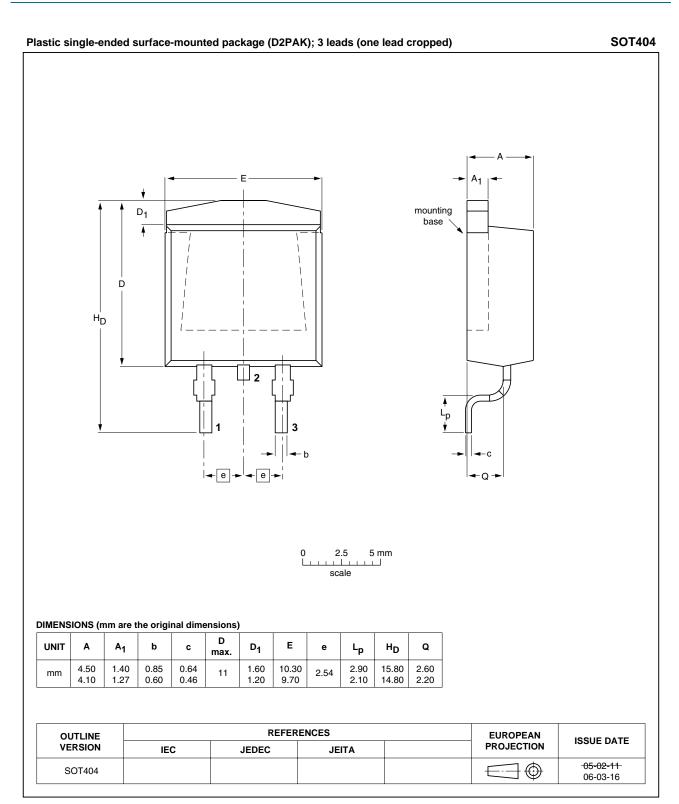


Fig 16. Package outline SOT404 (D2PAK)

## 8. Revision history

## Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BUK7607-30B v.2	20110221	Product data sheet	-	BUK75_7607_30B v.1	
Modifications:	<ul> <li>The format of this of NXP Semicondu</li> </ul>	mat of this data sheet has been redesigned to comply with the new identity guide Semiconductors.			
	<ul> <li>Legal texts have be</li> </ul>	een adapted to the new c	ompany name where app	oropriate.	
	<ul> <li>Type number BUK</li> </ul>	7607-30B separated from	n data sheet BUK75_760	7_30B v.1.	
BUK75_7607_30B v.1	20030407	Product data	-	-	

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#### 9.1 Data sheet status

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# **BUK7607-30B**

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