PESD5V0L1BSF

Ultra low profile bidirectional low capacitance ESD protection diode

Rev. 1 — 18 February 2011 Product data sheet

1. Product profile

1.1 General description

Low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a SOD962 leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Bidirectional ESD protection of one line
- Low diode capacitance C_d = 12 pF
- ESD protection up to ±30 kV according to IEC 61000-4-2
- Ultra small SMD package
- Symmetrical breakdown voltage

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

1.4 Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			–5	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	[1]	9	12	15.4	pF

[1] This parameter is guaranteed by design.

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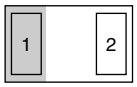
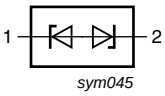
2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode (diode 1)	 Transparent top view	
2	cathode (diode 2)		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0L1BSF	-	leadless ultra small package; 2 terminals; body 0.6 × 0.3 × 0.3 mm	SOD962

4. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0L1BSF	none

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PP}	peak pulse power	t_p = 8/20 μs	[1][2]	-	35	W
I_{PP}	peak pulse current	t_p = 8/20 μs	[1][2]	-	3	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−55	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5; see Figure 1.

[2] Measured from pin 1 to pin 2.

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	-	30	kV
		IEC 61000-4-2 (air discharge)		-	30	kV
		MIL-STD-883 (human body model)		-	30	kV

[1] Measured from pin 1 to pin 2.

[2] Device stressed with ten non-repetitive ESD pulses; see Figure 2.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2, level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

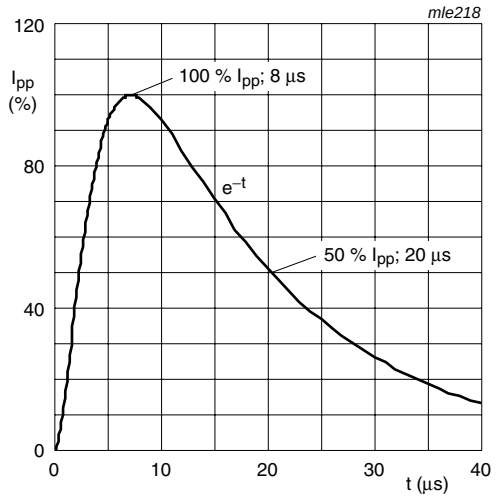


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

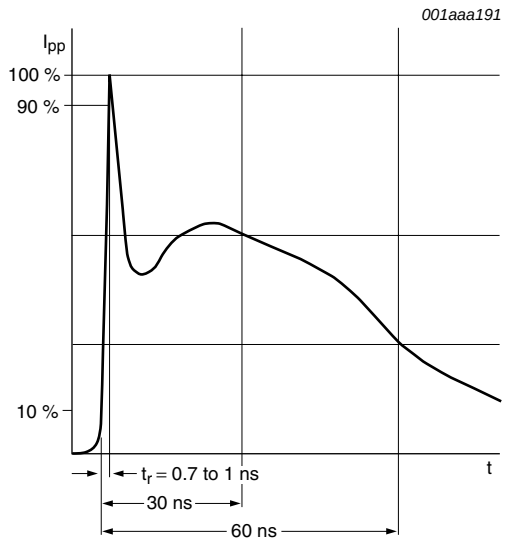


Fig 2. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse standoff voltage			–5	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V		-	1	100	nA
V_{CL}	clamping voltage	I_{PP} = 1 A	[1][2]	-	-	11.5	V
		I_{PP} = 3 A	[1][2]	-	-	13.5	V
V_{BR}	breakdown voltage	I_R = 1 mA	[3]	6	-	10	V
		I_R = −1 mA	[3]	−10	-	−6	V
C_d	diode capacitance	f = 1 MHz	[4]				
		V_R = 0 V		9	12	15.4	pF
		V_R = 2.5 V		-	8.9	11.4	pF
		V_R = 5 V		-	8	10.2	pF
L_S	series inductance		[5]	-	0.05	-	nH
R_{dyn}	dynamic resistance		[6]	-	1	-	Ω

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5; see Figure 1.

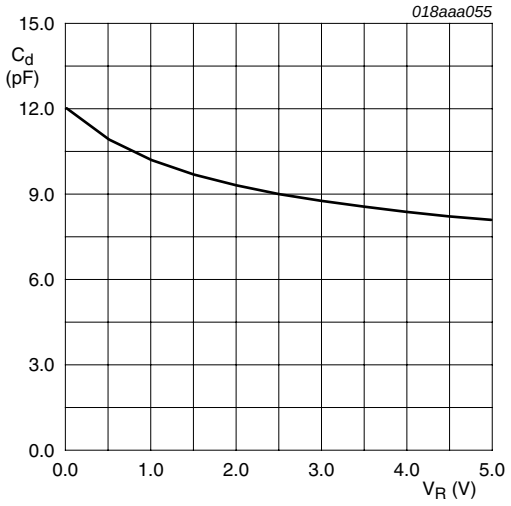
[2] Measured from pin 1 to pin 2.

[3] Breakdown voltage is always symmetrical within the characterized range, which means no difference in breakdown voltage from pin 1 to pin 2 and vice versa.

[4] This parameter is guaranteed by design.

[5] Calculated from S-parameter values.

[6] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANS/IESD STM5.1-2008.



f = 1 MHz; T_{amb} = 25 °C

Fig 3. Diode capacitance as a function of reverse voltage; typical values

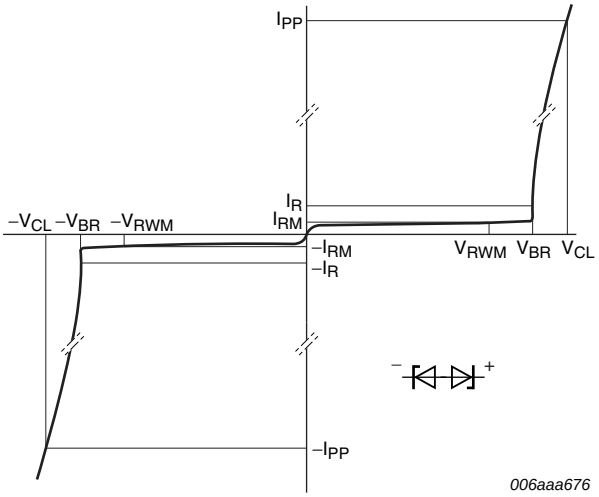


Fig 4. V-I characteristics for a bidirectional ESD protection diode

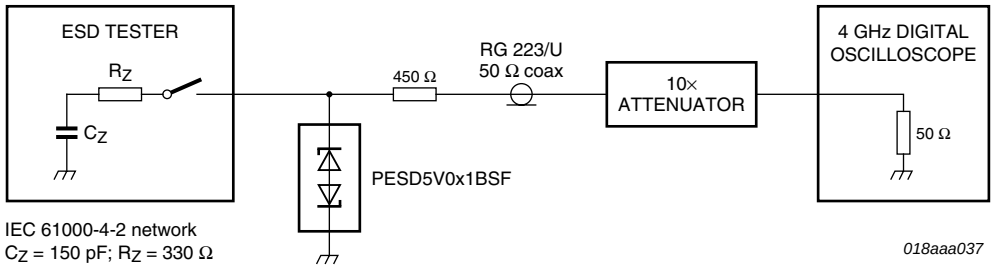
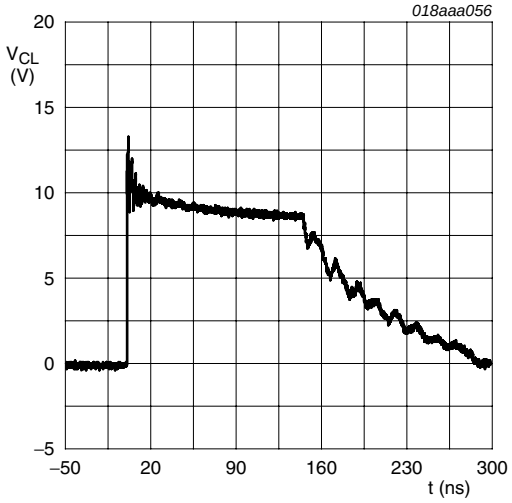
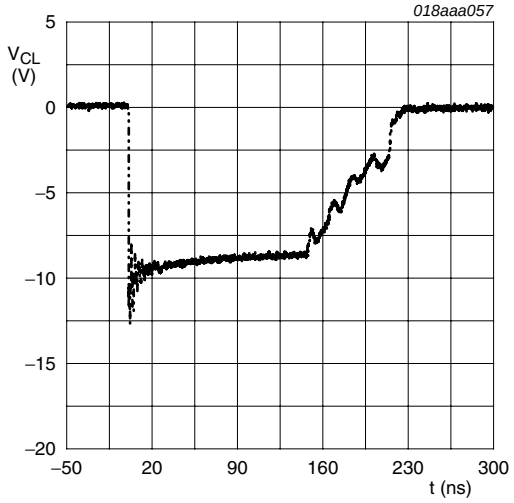


Fig 5. ESD clamping test setup



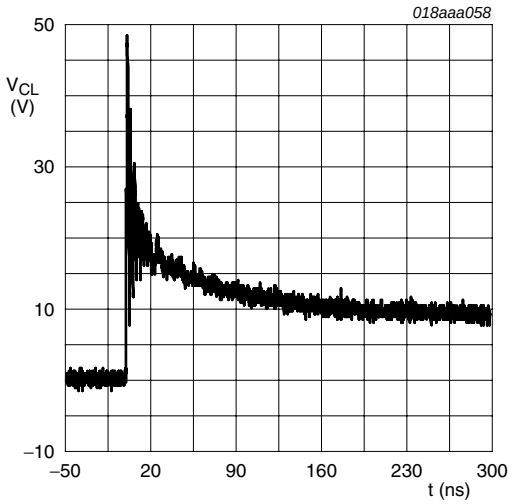
f = 1 MHz; T_{amb} = 25 °C

Fig 6. Clamped +1 kV ESD pulse waveform (IEC 61000-4-2 network)



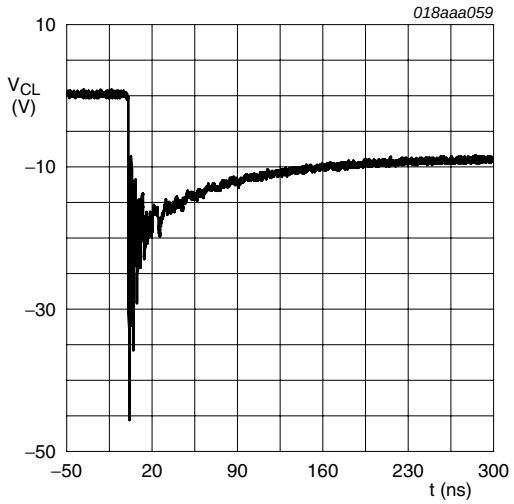
f = 1 MHz; T_{amb} = 25 °C

Fig 7. Clamped −1 kV ESD pulse waveform (IEC 61000-4-2 network)



f = 1 MHz; T_{amb} = 25 °C

Fig 8. Clamped +8 kV ESD pulse waveform (IEC 61000-4-2 network)



f = 1 MHz; T_{amb} = 25 °C

Fig 9. Clamped −8 kV ESD pulse waveform (IEC 61000-4-2 network)

7. Application information

The PESD5V0L1BSF is designed for the protection of one data or signal line from the damage caused by ESD and/or other surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground. It provides protection against surges with up to 35 W per line.

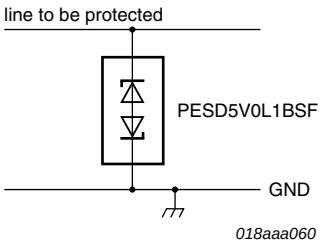


Fig 10. Application diagram

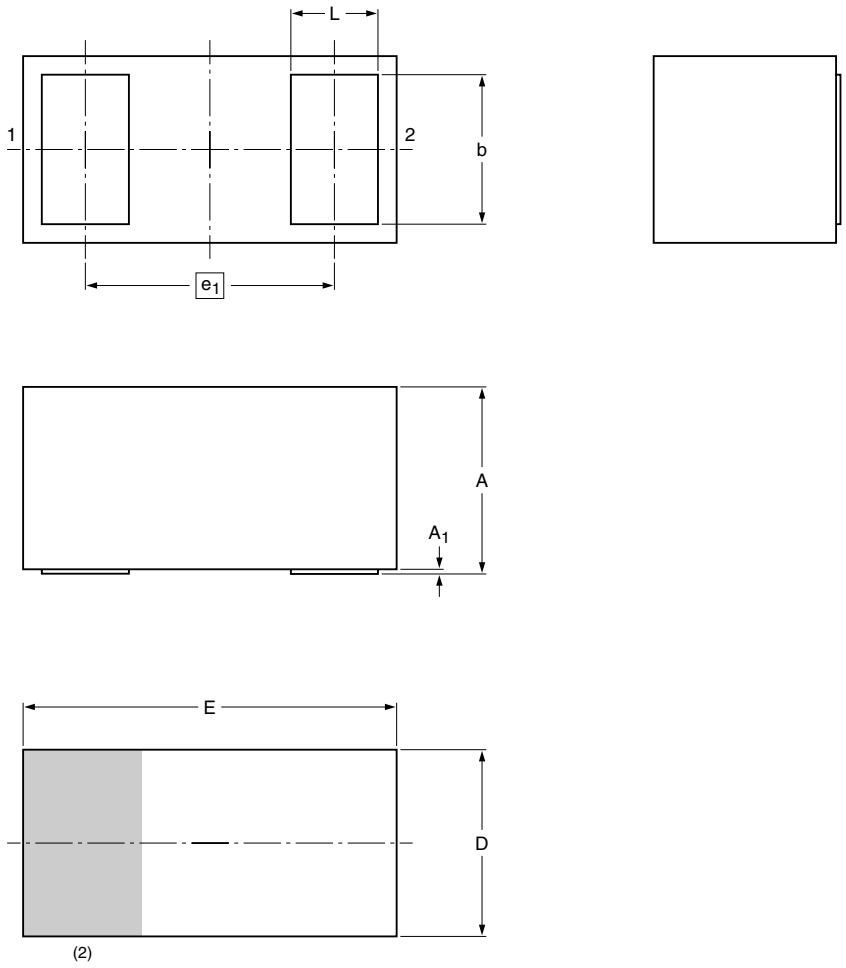
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD and Electrical Fast Transient (EFT). The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible
2. The path length between the device and the protected line should be minimized
3. Avoid running protected conductors in parallel with unprotected conductors
4. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops
5. Minimize the length of the transient return path to ground
6. Avoid using shared transient return paths to a common ground point
7. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962**



Dimensions

Unit		A(1)	A1	b	D	E	e1	L
mm	max	0.32	0.0076	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. Dimension A is including coating foil thickness.
2. The marking bar indicates the cathode.

sod962_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962						~~10-11-03~~ 10-11-11

Fig 11. Package outline PESD5V0L1BSF (SOD962)

9. Packing information

Table 9. Packing methods

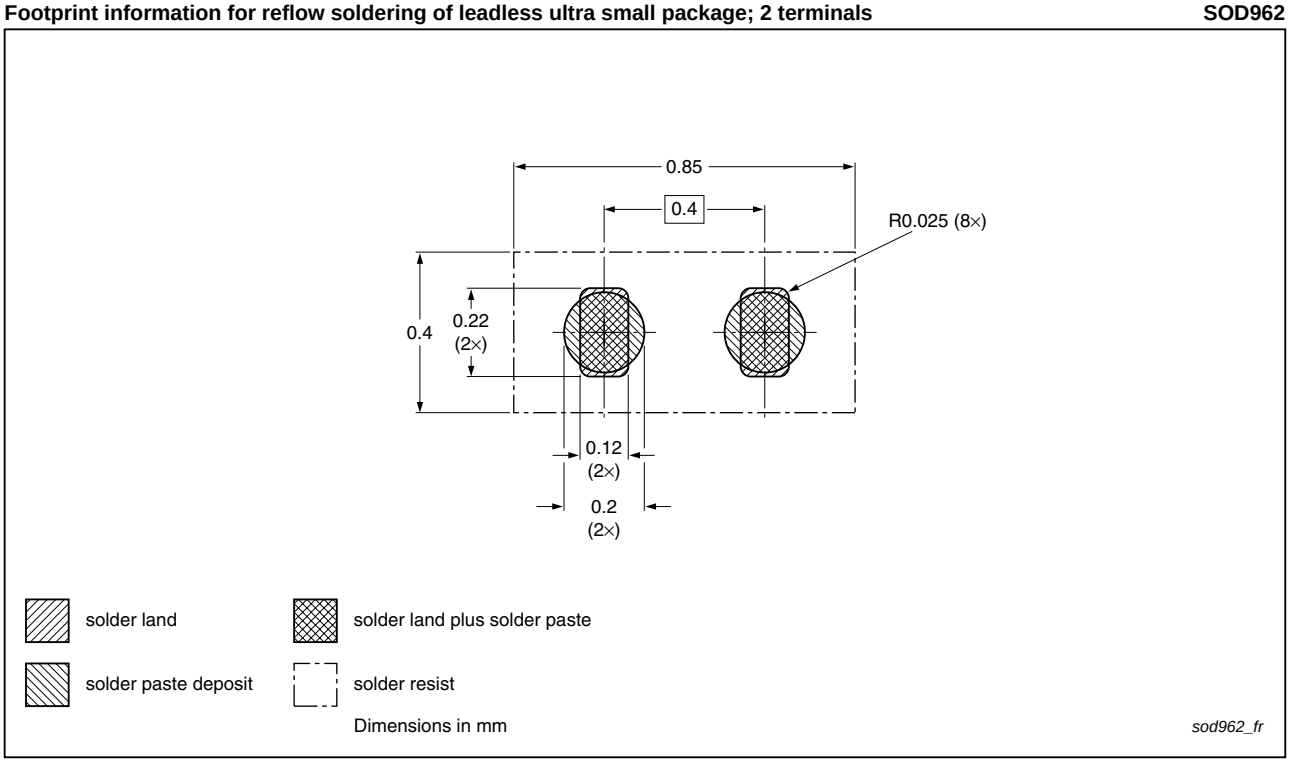
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity
			9000
PESD5V0L1BSF	SOD962	2 mm pitch, 8 mm tape and reel	-315

[1] For further information and the availability of packing methods, see Section 13.

10. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962**



Reflow soldering is the required soldering method.

Fig 12. Required reflow soldering footprint PESD5V0L1BSF (SOD962)

Based on results of board mount testing, Nexperia requires the following soldering guidelines:

1. Soldering footprint as indicated in Figure 12: solder paste has to cover the whole solder land area.
2. Non-solder mask defined (copper-defined) solder lands.
3. Minimum stencil thickness of 100 μm.
4. Paste type 4 or smaller sphere size.
5. Pick and placement accuracy of ±50 μm.

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0L1BSF v.1	20110218	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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