Power Management IC for Automotive

Power Management IC for ADAS Applications

BD39031MUF-C

General Description

BD39031MUF-C is a power management IC with Primary Buck Controller (BUCK1), Dual Secondary Buck Converter (BUCK2/BUCK3), and Secondary Boost Converter (BOOST4). This device contains Reset, Power Good, Watchdog Timer functions, and is suitable for ADAS application such as radar, camera, and LiDAR. In addition, this device contributes to ASIL level improvement of the system by BIST (Built-In Self Test) function and Mutual Monitoring function.

Features

- AEC-Q100 Qualified *(Note 1)*
- Functional Safety Supportive Automotive Products
- Primary Buck Controller for 3.3 V Fixed
- Secondary Buck Converter for 1.2 V Output Fixed
- Secondary Buck Converter for Adjustable Output
- Secondary Boost Converter for 5.0 V Output Fixed
- Enable Input for Each Output
- Two Power Good Functions
- Reset Function for BUCK1
- Adjustable Window Watchdog Timer
- Spread Spectrum
- Over Current Protection
- Over Voltage Protection
- Short Circuit Protection
- Thermal Shut Down Protection
- Thermal Warning Function

(Note 1) Grade 1

Applications

- ADAS Application (Radar Module, Camera Module, LiDAR Module, etc.)
- ADAS ECU

Key Specifications

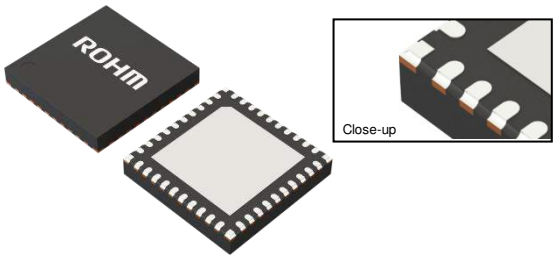
■ Input Voltage Range:	4.0 V to 28 V
■ Output Voltage:	
BUCK1 Voltage	3.3 V
BUCK2 Voltage	1.2 V
BUCK3 Voltage	0.8 V to 2.5 V
BOOST4 Voltage	5.0 V
■ Maximum Output Current:	
BUCK2, BUCK3	2.5 A
BOOST4	0.5 A
■ Switching Frequency:	2.2 MHz (Typ)
■ Standby Current:	0 µA (Typ)
■ Operating Ambient Temperature Range:	-40 °C to +125 °C

Special Characteristics

■ Output Voltage Accuracy:	
BUCK1 VO1 Voltage	±1.5 %
BUCK2 VO2 Voltage	±1.5 %
BUCK3 FB Voltage	±1.5 %
BOOST4 VO4 Voltage	±2.0 %

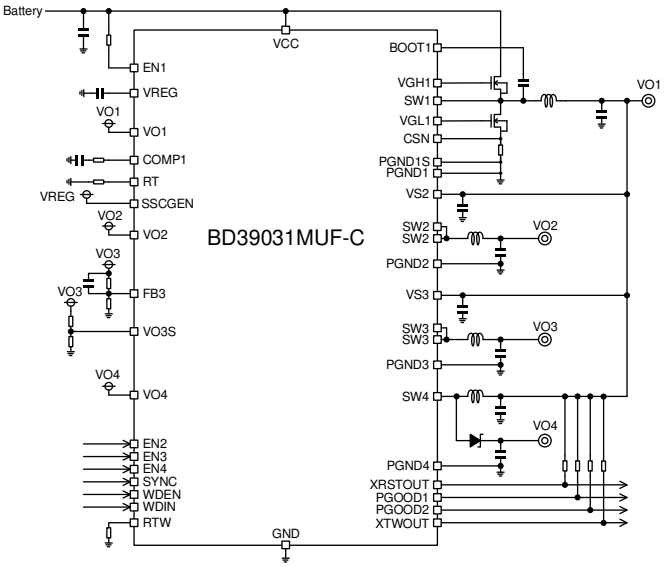
Package

Package	W (Typ) x D (Typ) x H (Max)
VQFN40FV6060	6.0 mm x 6.0 mm x 1.0 mm



VQFN40FV6060
Wettable Flank Package

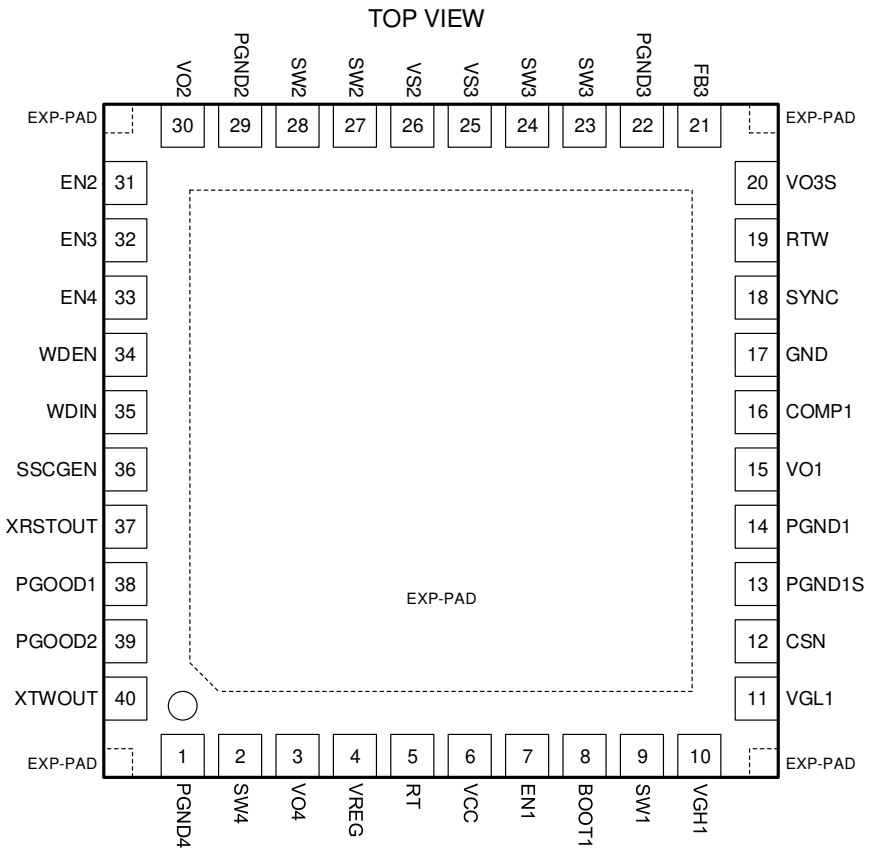
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configurations



Pin Descriptions

Pin No.	Pin Name	Function
1	PGND4	Power ground of BOOST4 converter.
2	SW4	BOOST4 switching node.
3	VO4	BOOST4 feedback pin. Connect to VO4 output voltage.
4	VREG	Internal regulator of 5 V output. Connect output capacitor. Can't be used for external power supply.
5	RT	Switching frequency set pin. Connect resistor between RT and GND.
6	VCC	Power supply.
7	EN1	Enable input for internal reference circuit and BUCK1. Controlled by external microcomputer or pulled up to VCC.
8	BOOT1	BUCK1 power supply for high side FET. Connect capacitor between BOOT1 and SW1.
9	SW1	BUCK1 switching node. (Floating ground for high side FET)
10	VGH1	BUCK1 gate driver for high side FET.
11	VGL1	BUCK1 gate driver for low side FET.
12	CSN	Differential current sense for BUCK1. Connect resistor between CSN and PGND1S.
13	PGND1S	Differential current sense for BUCK1. Connect resistor between CSN and PGND1S.
14	PGND1	Power ground of BUCK1.
15	VO1	BUCK1 feedback pin.
16	COMP1	Error amplifier output for BUCK1 controller.
17	GND	Analog ground.
18	SYNC	Synchronization input pin. This pin can be driven by external clock to set desired switching frequency.
19	RTW	WDT frequency setting pin. Put resistor between the RTW pin and GND.
20	VO3S	BUCK3 input for external sense voltage of VO3.
21	FB3	BUCK3 feedback pin. Input external resistance division between output and GND.
22	PGND3	Power ground for BUCK3.
23	SW3	BUCK3 switching node.
24	SW3	BUCK3 switching node.
25	VS3	Power supply for BUCK3. Connect to VO1 output voltage.
26	VS2	Power supply for BUCK2. Connect to VO1 output voltage.
27	SW2	BUCK2 switching node.
28	SW2	BUCK2 switching node.
29	PGND2	Power ground for BUCK2.
30	VO2	BUCK2 feedback pin.
31	EN2	Enable pin for BUCK2.
32	EN3	Enable pin for BUCK3.
33	EN4	Enable pin for BOOST4.
34	WDEN	Enable pin for WDT.
35	WDIN	Clock input pin for WDT.
36	SSCGEN	Enable pin for Spread Spectrum function. Connect to VREG or GND.
37	XRSTOUT	Reset Nch open drain output pin.
38	PGOOD1	Power Good Nch open drain output pin for BUCK2.
39	PGOOD2	Power Good Nch open drain output pin for all outputs.
40	XTWOUT	Thermal warning Nch open drain output pin.
-	EXP-PAD	The EXP-PAD of the center of product is connected to PCB ground plane. The EXP-PADs on the center and corner of the product are shorted inside the package.

Block Diagrams

<TOP BLOCK>

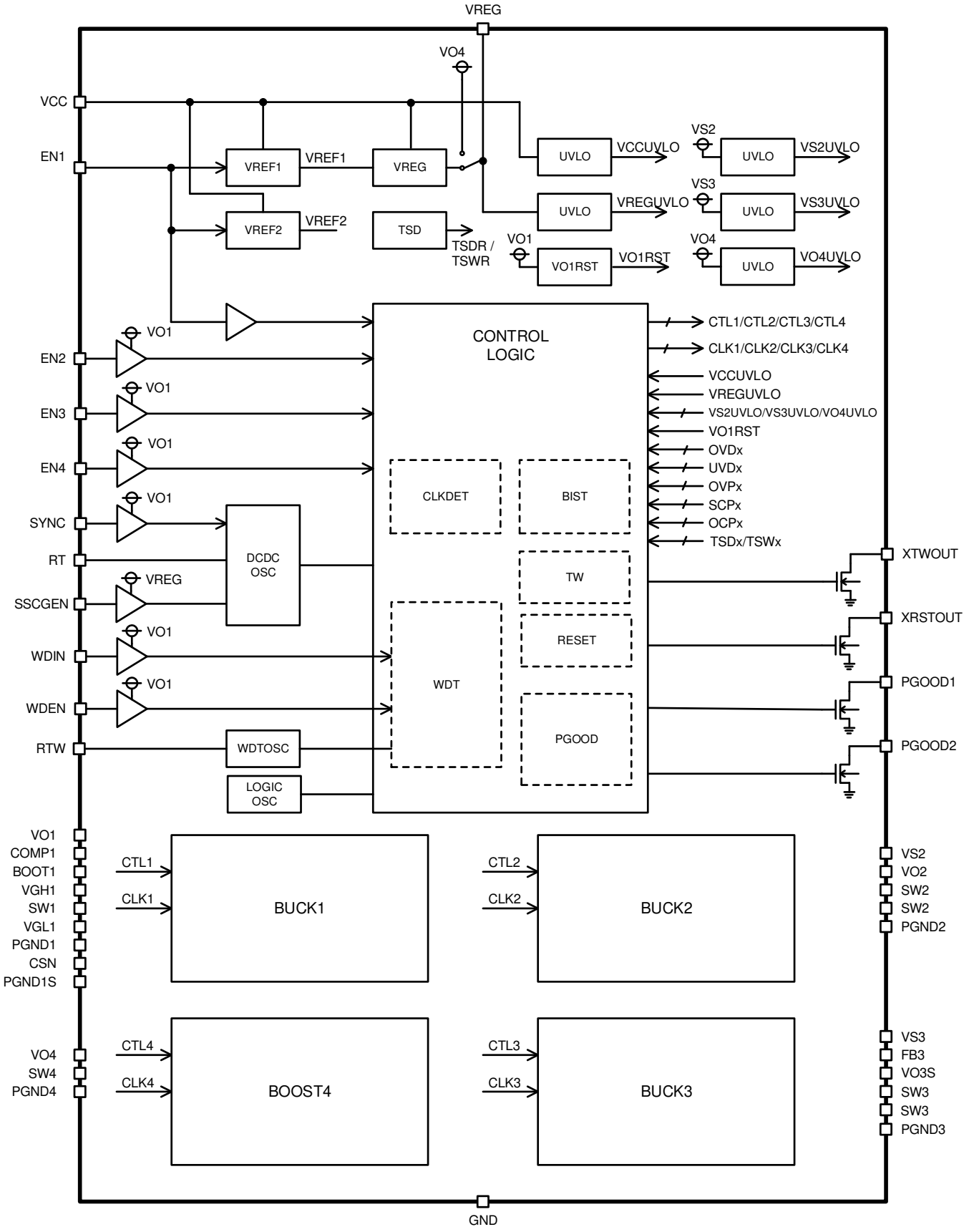


Figure 1. Top Block Diagram

Block Diagrams - continued

<BUCK1>

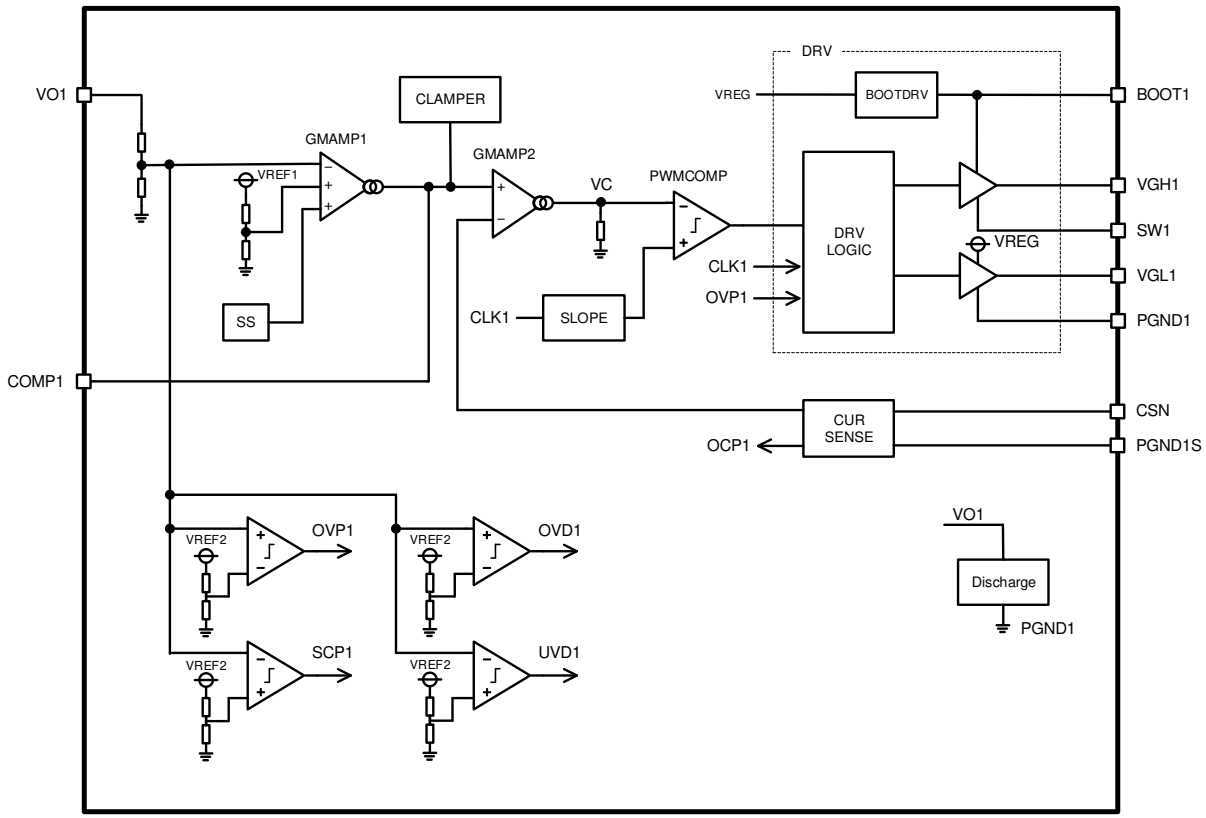


Figure 2. BUCK1 Block Diagram

<BUCK2>

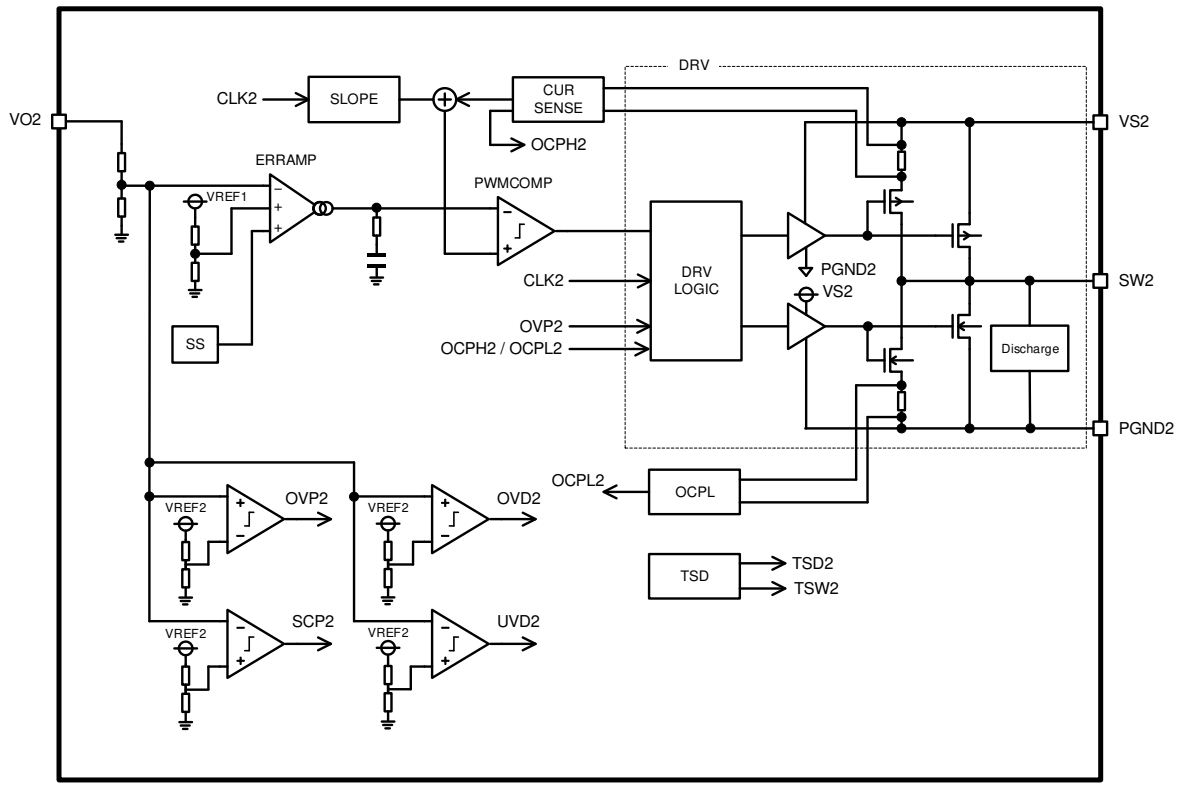


Figure 3. BUCK2 Block Diagram

Block Diagrams - continued

<BUCK3>

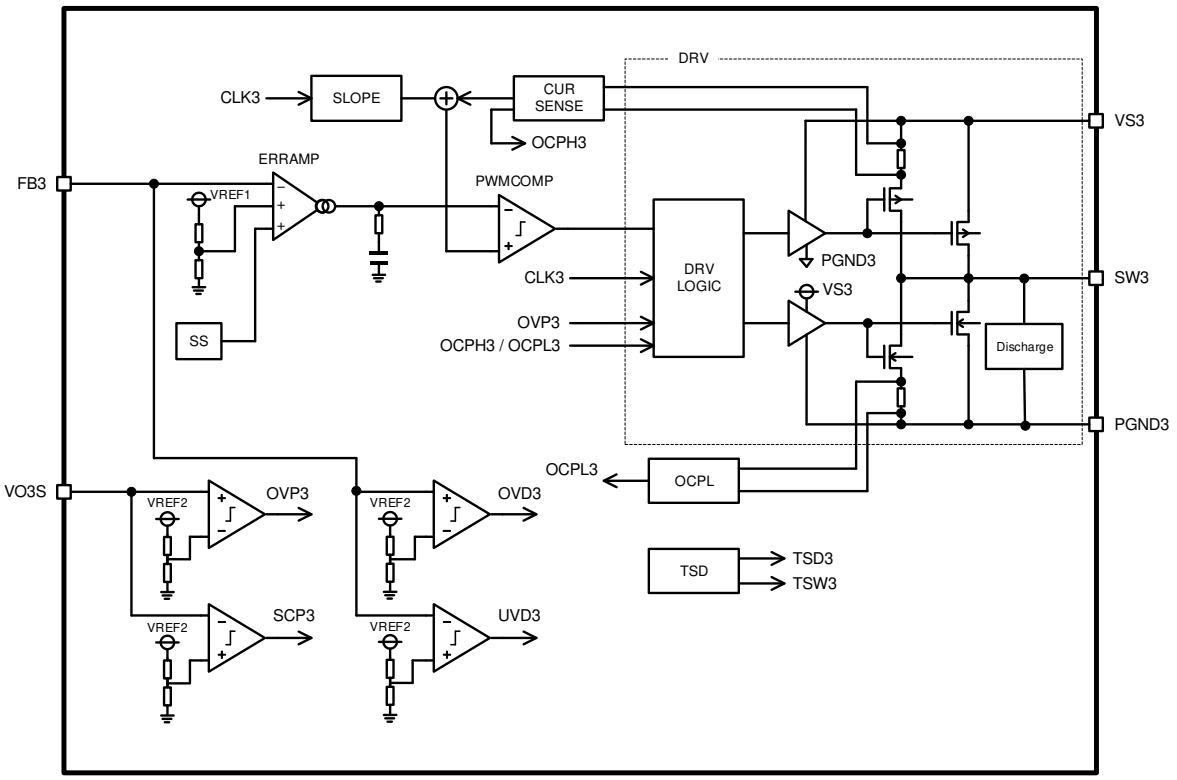


Figure 4. BUCK3 Block Diagram

<BOOST4>

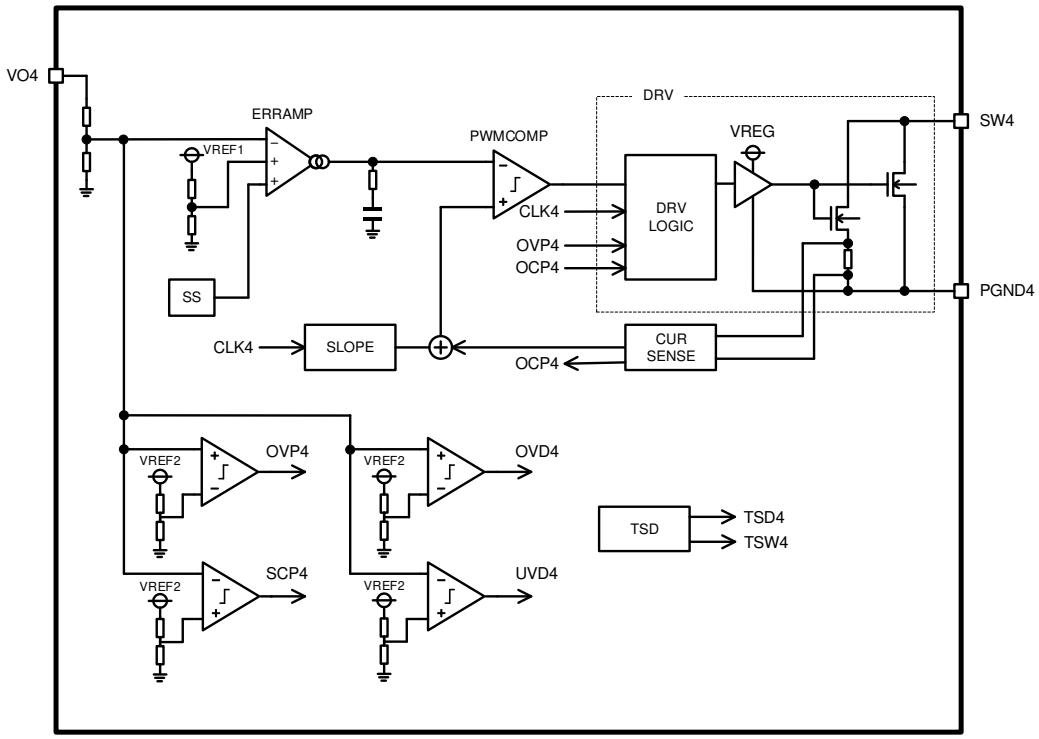


Figure 5. BOOST4 Block Diagram

Description of Blocks

1. TOP BLOCK

Reference Voltage (VREF1, VREF2)

There are 2 reference voltages; VREF1 and VREF2.

VREF1 is used for each regulator control reference voltage and VREF2 is used for each protection function reference voltage.

After VCC input, VREF1 and VREF2 will startup when EN1 is turned to high. VREF1 and VREF2 will stop when EN1 is turned to low.

Internal Regulator (VREG)

VREG is 5 V (Typ) regulator for internal circuit. Needs to connect external capacitor to the VREG pin. After VCC input, VREG will startup when EN1 is turned to high. VREG will stop when EN1 is turned to low. Do not use VREG for any other purposes. Also internal regulator will be switched to VO4 after VO4 output becomes more than 4.5 V (Typ) and soft start of BOOST4 is completed.

Under Voltage Lock-Out (UVLO)

UVLO is under voltage lockout circuit. Prevents internal circuit malfunction when power supply startup or is at lower input voltage. Monitors VCC, VREG, VS2, VS3, and VO4 voltage and activates when each voltage goes under each threshold voltage. When VCCUVLO or VREGUVLO is detected, all the outputs will turn off. When VS2UVLO is detected, BUCK2 will turn off. When VS3UVLO is detected, BUCK3 will turn off. When VO4UVLO is detected, BOOST4 will turn off.

Oscillator (LOGICOSC, WDTOSC, DCDCOSC)

There are 3 types of oscillator. One for Control Logic, the second for Watch Dog Timer and the third for BUCK1, BUCK2, BUCK3 and BOOST4. BUCK3 clock phase is 180 deg shifted from BUCK1, BUCK2 and BOOST4 to reduce switching noise. Connect 9.1 kΩ between RT and GND.

Spread Spectrum Clock Generator (SSCG)

OSC block built in spread spectrum clock generator (SSCG) function. This function activates when the SSCGEN pin is connected to VREG. When the SSCGEN pin is connected to GND, SSCG function is disable. The modulation range of Spread Spectrum is between +6.2% (Typ) and -6.2% (Typ) from the typical frequency. Also, modulation frequency is set to 1.075 kHz (Typ). The modulation range and modulation frequency are fixed.

Synchronization mode (SYNC)

Switching frequency can be synchronized to an external clock signal using the SYNC pin. The SYNC pin allows the operating frequency to be varied above and below the frequency setting. Adjustment range is from +10 % to -10 %. The RT resistor must always be connected to initialize the operating frequency.

Control Logic (CONTROL LOGIC)

This block controls startup/stop sequence, Reset, Power Good, Watch Dog Timer, mutual monitoring function, Built-In Self Test (BIST), and each protection. Control Logic will be active when internal power supply VREGUVLO is released. When VREGUVLO is detected, Control Logic will reset and initialize.

Reset (RESET)

This block informs output voltage for microcomputer which is completely ON by reset signal. Pull up this pin to VO1 or external power supply using resistor. The XRSTOUT pin goes low when internal circuit is in abnormal conditions. The XRSTOUT pin goes high when all the following conditions are satisfied.

a) VO1 voltage is higher than 2.6 V (Typ)
b) BIST result are OK
c) Mutual monitoring result are OK
d) No detection of WDT FAST Timeout / SLOW Timeout

XRSTOUT goes High 10 ms (Typ) after all conditions are satisfied.

Power Good (PGOOD)

This block informs whether each regulator output startups normally or not. Power Good have UVD and OVD for each regulator and asserts it by Power Good pin. Pull up this pin to VO1 or to external power supply using resistor.

This product has 2 Power Good pins. Each pin monitors the following regulator.

- PGOOD1 : Only BUCK2
- PGOOD2 : BUCK1, BUCK2, BUCK3, and BOOST4

PGOOD1, PGOOD2 goes High 10 ms (Typ) after all conditions are satisfied.

TOP BLOCK - continued

Built-In Self Test (BIST)

When VCCUVLO and VREGUVLO are released, and VO1 voltage is higher than 2.6 V (Typ), BIST is performed and self-test for each OVD/UVD and RESET comparators are executed to check if each comparator correctly toggles their high/low output based on input voltage change. Once BIST ends without any error, the XRSTOUT pin becomes high. If an error is found during BIST, the XRSTOUT pin keeps low and BIST is repeated until it passes.

Clock Mutual Detect (CLKDET)

CLKDET block monitors each clock outputted from each OSC blocks mutually. If any one of their frequency exceeds range, XRSTOUT goes low.

Thermal Warning (TW)

This block monitors internal temperature and detect when it reaches 135 degree (Typ). Pull up this pin to VO1 or external power supply using resistor. The XTWOUT pin goes Low when internal temperature is higher than threshold.
The XTWOUT pin goes High when internal temperature is lower than threshold. This block only warns of internal temperature getting high. Hence, all function works normally even with this function detected. Thermal Warning function works when VCCUVLO, VREGUVLO, and Reset function are not detected. When it is not working, the XTWOUT pin is kept at high level.

2. BUCK1 BLOCK

BUCK1 is Primary Buck Controller. It is necessary to connect external MOSEFT. Output voltage is 3.3 V (Typ) fixed.

- GMAMP1 Error amplifier which have reference voltage VREF1 and VO1 divider input.
  Also phase compensation of BUCK1 can be adjust by inserting capacitor and resistor to the COMP1 pin.
- GMAMP2 Error amplifier which have output of GMAMP1 and current sense signal input. This block generates the VC voltage to control duty.
- SS Soft Start (SS) function prevent overshoot of output voltage and rush current by gradually increasing ON duty of switching pulse. Soft start time is fixed internally.
- CLAMPER CLAMPER limits the maximum and minimum value of coil current and works as over current protection. When coil current reaches maximum value, it makes duty small and reduces the output voltage. Similarly, when coil current reaches and minimum value, it increases duty and raise the output voltage.
- CURSENSE Detects the amount of current flowing through the inductance using resistor which is connected between the CSN pin and the PGND1S pin, and feedbacks current sense signal to GMAMP2.
- SLOPE This is the block which makes slope waveform from clock generated at OSC block. This slope waveform is combined with current sense and sends to PWMCOMP.
- PWMCOMP This compares slope waveform including current information with GMAMP2 output, and sends output signal to DRV block.
- DRV BUCK1 Driver block. Drives external FET which is connect to VGH1 and VGL1 by using signal from PWMCOMP.

  Pulse Skip Function

  BUCK1 controller needs on time for low side FET to charge the BOOT1 pin, because high side FET is driven by boot strap. Therefore, it sets minimum off time, and the output voltage is limited by this in the condition where the input and output voltage are close

  As for this countermeasure, DRV skips off pulse when the voltage difference of the input and output becomes small, and continuously turns on high side FET and keeps max duty to rise. The off pulse skip will occer 4 consectutive times as maximum.

Description of Blocks - continued

3. BUCK2 BLOCK

BUCK2 is Secondary Buck converter. Output voltage is 1.2 V (Typ) fixed. EN2 = High turns on BUCK2 and EN2 = Low turns off BUCK2.

- ERRAMP Error Amplifier with reference voltage and VO2 divider input.
  Controls on duty width of switching pulse by internal COMP2 node which is an ERRAMP output.
  Capacitor and resistor for phase compensation are fixed.
- SS Soft Start (SS) function prevent overshoot of output voltage and rush current by gradually increasing on duty of switching pulse. Soft start time is fixed internally.
- SLOPE This is the block which makes slope waveform from clock generated at OSC block. This slope waveform is combined with current sense and is sent to PWMCOMP.
- PWMCOMP This compares slope waveform including current information with ERRAMP output, and sends output signal to DRV block.
- DRV BUCK2 Driver block. Drives internal FET by using signal from PWMCOMP.

4. BUCK3 BLOCK

BUCK3 is Secondary Buck converter. Output voltage can be set by external resistor. EN3 = High turns on BUCK3 and EN3 = Low turns off BUCK3.

- ERRAMP Error Amplifier with reference voltage and FB3 input.
  Controls on duty width of switching pulse by internal COMP3 node which is an ERRAMP output.
  Capacitor and resistor for phase compensation are fixed.
- SS Soft Start (SS) function prevent overshoot of output voltage and rush current by gradually increasing on duty of switching pulse. Soft start time is fixed internally.
- SLOPE This is the block which makes slope waveform from clock generated at OSC block. This slope waveform is combined with current sense and is sent to PWMCOMP.
- PWMCOMP This compares slope waveform including current information with ERRAMP output, and sends output signal to DRV block.
- DRV BUCK3 Driver block. Drives internal FET by using signal from PWMCOMP.

5. BOOST4 BLOCK

BOOST4 is Secondary Boost converter. Output voltage is 5.0 V (Typ) fixed. EN4 = High turns on BOOST4 and EN4 = Low turns off BOOST4.

- ERRAMP Error Amplifier with reference voltage and VO4 divider input.
  Controls on duty width of switching pulse by internal COMP4 node which is an ERRAMP output.
  Capacitor and resistor for phase compensation are fixed.
- SS Soft Start (SS) function prevent overshoot of output voltage and rush current by gradually increasing on duty of switching pulse. Soft start time is fixed internally.
- SLOPE This is the block which makes slope waveform from clock generated at OSC block. This slope waveform is combined with current sense and is sent to PWMCOMP.
- PWMCOMP After compared with slope waveform which has been combined with current sense and ERRAMP output, sends signal to DRV block.
- DRV BOOST4 Driver block. Drives internal FET by using signal from PWMCOMP.

Description of Blocks - continued

6. Detection Function

Over Voltage Detection (OVD)
If output voltage goes higher than threshold voltage, OVD is detected and the PGOOD pin goes down to low. Detection pins are VO1, VO2, FB3, and VO4. If VO2 detects OVD, PGOOD1 goes down to low and if either VO1, VO2, FB3, or VO4 detects OVD, PGOOD2 goes down to low.

Under Voltage Detection (UVD)
If output voltage goes lower than threshold voltage, UVD is detected and the PGOOD pin goes down to low. Detection pins are VO1, VO2, FB3 and VO4. If VO2 detects UVD, PGOOD1 goes down to low and if either VO1, VO2, FB3, or VO4 detects UVD, PGOOD2 goes down to low.

7. Protection Function

Over Voltage Protection (OVP)
If output voltage goes higher than threshold voltage, OVP is detected and switching will turn off. Detection pins are VO1, VO2, VO3S, and VO4. If OVP is detected for continuous 1ms (Typ), switching will turn off and soft start will discharge. After that, output continues to stop for 10 ms (Typ) and re-starts automatically by soft start.

Short Circuit Protection (SCP)
When output voltage is shorted to GND (or when output voltage is lower than SCP threshold voltage) for 1 ms (Typ), switching will turn off and soft start will discharge. After that, output continues to stop for 10 ms (Typ) and re-starts automatically by soft start. Detection pins are VO1, VO2, VO3S, and VO4.
Before each voltage startups, or are in soft start status, SCP function is masked.

Over Current Protection (OCP)
When over current goes through output FET, over current protection will be detected and output pulse width will be limited. For BUCK1, over current protection will be detected when the voltage between CSN and PGND1S goes more than 75 mV (Typ).
For BUCK2 and BUCK3, over current protection will be detected when current goes through more than 3.0 A to integrated FET. For BOOST4, over current protection will be detected when current goes through more than 1.0 A to integrated FET.

When OCP is detected continuously for more than 1 ms (Typ), switching will turn off and soft start will discharge.
However, time counter is not stated until soft start of each output is completed.
After turn off by OCP, output continues to stop for 10 ms (Typ) and re-starts automatically by soft start.

BUCK1 OCP
BUCK1 contains OCP detection function to protect FET. To prevent destruction between source and drain of high side FET, when SW1 voltage falls 0.35 V lower than VCC (Typ), high side FET keeps to turn off.

OCPL2/OCPL3
These OCP watches the negative current of low side FET. This is designed to protect lower FET when output is applied from outside. If OCPL2 or OCPL3 detects, each low side FET will turn off. At the time of BUCK2 and BUCK3 startup, detection level of OCPL2/OCPL3 is at lower setting than normal operation for stable startup of the system.

Protection Function - continued

Protection

The value in this list is typical unless otherwise specified.

Block	Protection	Detect	Release	Detection action
ALL	VCCUVLO	V_{CC} < 3.8 V	V_{CC} > 4.2 V	BUCK1, BUCK2, BUCK3, BOOST4 OFF XRSTOUT = PGOOD1 = PGOOD2 = Low
	VREGUVLO	V_{REG} < 3.5 V	V_{REG} > 3.6 V	BUCK1, BUCK2, BUCK3, BOOST4 OFF Internal OSC OFF XRSTOUT = PGOOD1 = PGOOD2 = Low
	TSD	Tj > 175 °C	-	BUCK1, BUCK2, BUCK3, BOOST4 OFF After 10 ms, re-startup
BUCK1	OVP1	V_{VO1} > 4.25 V	V_{VO1} < 4.0 V	BUCK1 VGH = Low, VGL = Low Detected continuous 1 ms, BUCK1, BUCK2, BUCK3, BOOST4 OFF After 10 ms, re-startup
	SCP1	V_{VO1} < 1.65 V	V_{VO1} > 1.815 V	Detected continuous 1 ms, BUCK1, BUCK2, BUCK3, BOOST4 OFF After 10 ms, re-startup
	OCP1	V_{CSN} - V_{PGND1S} > 75 mV	V_{CSN} - V_{PGND1S} < 75 mV	Pulse width will be limited Detected continuous 1 ms, BUCK1, BUCK2, BUCK3, BOOST4 OFF After 10 ms, re-startup
BUCK2	VS2UVLO	V_{S2} < 2.5 V	V_{S2} > 2.7 V	BUCK2 OFF
	OVP2	V_{VO2} > 1.44 V	V_{VO2} < 1.32 V	SW2 Hiz Detected continuous 1 ms, BUCK2 OFF, After 10 ms, re-startup
	SCP2	V_{VO2} < 0.60 V	V_{VO2} > 0.72 V	Detected continuous 1 ms, BUCK2 OFF, After 10 ms, re-startup
	OCP2	I_{VS2} > 3.0 A (Min)	I_{VS2} < 3.0 A (Min)	Pulse width will be limited Detected continuous 1 ms, BUCK2 OFF, After 10 ms, re-startup
BUCK3	VS3UVLO	V_{S3} < 2.5 V	V_{S3} > 2.7 V	BUCK3 OFF
	OVP3	V_{VO3S} > 0.96 V	V_{VO3S} < 0.88 V	SW3 Hiz Detected continuous 1 ms, BUCK3 OFF, After 10 ms, re-startup
	SCP3	V_{VO3S} < 0.40 V	V_{VO3S} > 0.48 V	Detected continuous 1 ms, BUCK3 OFF, After 10 ms, re-startup
	OCP3	I_{VS3} > 3.0 A (Min)	I_{VS3} < 3.0 A (Min)	Pulse width will be limited Detected continuous 1 ms, BUCK3 OFF, After 10 ms, re-startup
BOOST4	VO4UVLO	V_{VO4} < 1.8 V	V_{VO4} > 2.0 V	BOOST4 OFF
	OVP4	V_{VO4} > 6.5 V	V_{VO4} < 6.25 V	SW4 Hiz Detected continuous 1 ms, BOOST4 OFF, After 10 ms, re-startup
	SCP4	V_{VO4} < 2.5 V	V_{VO4} > 3.0 V	Detected continuous 1 ms, BOOST4 OFF, After 10 ms, re-startup
	OCP4	I_{SW4} > 1.0 A (Min)	I_{SW4} < 1.0 A (Min)	Pulse width will be limited Detected continuous 1 ms, BOOST4 OFF, After 10 ms, re-startup

Description of Blocks - continued

8. Watchdog Timer (WDT)

Watch Dog Timer (WDT) monitors microprocessor's operation by detecting the time between rising edge of WDIN signal. When both WDEN and XRSTOUT are high, WDT is activated. If BIST result is an error, WDT will not work for XRSTOUT is kept low.

As long as the period of WDIN clock is kept within "Trigger Open Window" as in Figure 6., WDT will not detect any error and XRSTOUT will stay at high.

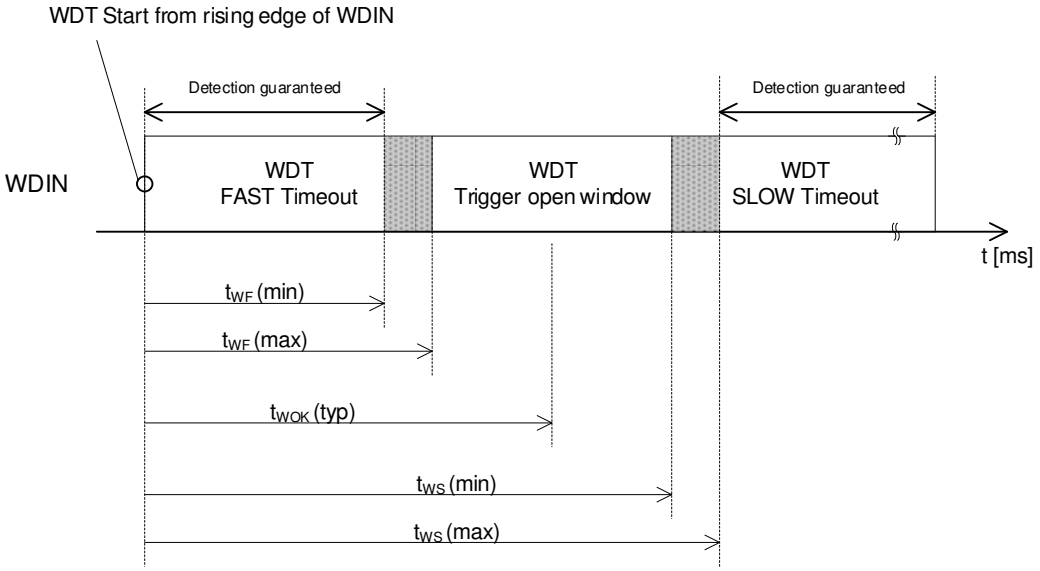


Figure 6. WDT Window Description

Watchdog Timer - continued

WDT FAST Timeout Detection

When WDEN is low, WDT is disabled. During this period WDIN input signal is ignored and XRSTOUT output is not affected. When both WDEN and XRSTOUT are high, WDT is activated. Just after WDT is active during this first period, only SLOW Timeout detection works and FAST Timeout doesn't work. The rising edge of WDIN comes within SLOW Timeout, both FAST Timeout and SLOW Timeout detection start to work. WDT detection monitors the time between this rising edge and the next rising edge. When it detects WDIN rising edge within FAST Timeout (t_{WF}), XRSTOUT becomes low. XRSTOUT goes back to high after 10 ms delay. Then, WDT works after 500 ms delay again. This delay time is implemented as a time for microprocessor to be reset normally and to stabilized. If this time is unnecessary and WDT should be activated as soon as possible, WDEN may be controlled from low to high.

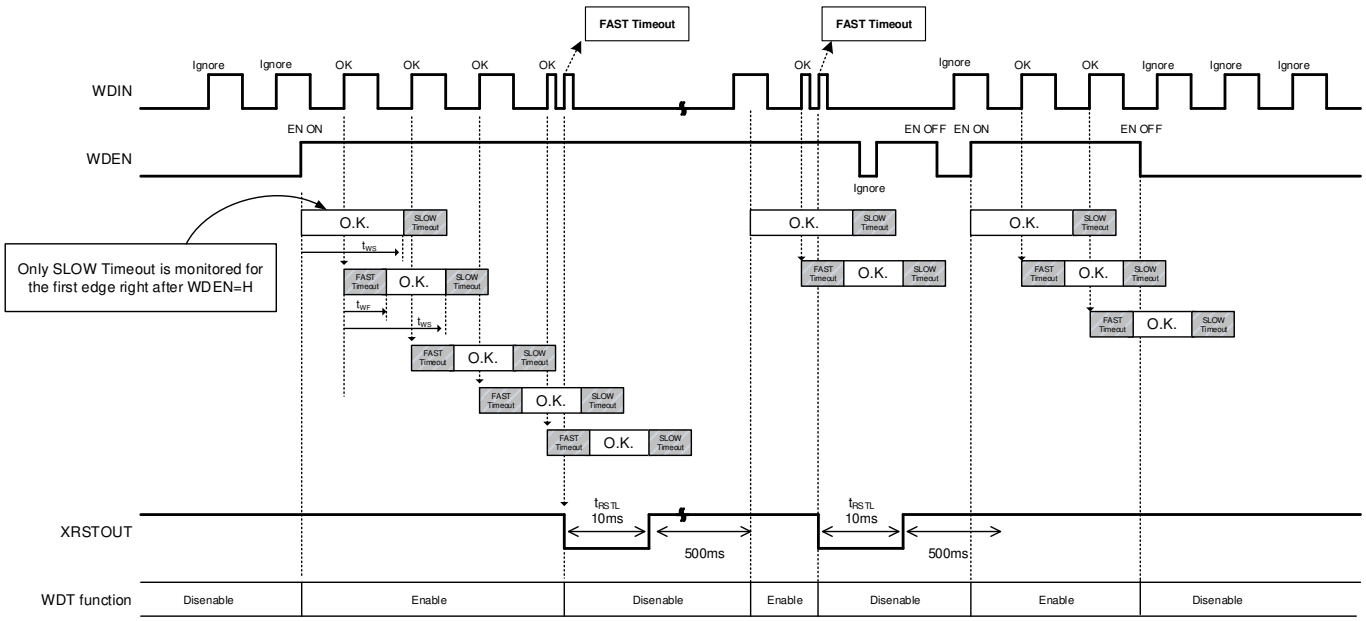


Figure 7. WDT FAST Timeout detection

Watchdog Timer - continued

WDT SLOW Timeout Detection

When WDEN is low, WDT is disabled. During this period WDIN input signal is ignored and XRSTOUT output is not affected. When both WDEN and XRSTOUT are high, WDT is activated. Just after WDT is active during this first period, only SLOW Timeout detection works and FAST Timeout doesn't work. The rising edge of WDIN comes within SLOW Timeout, both FAST Timeout and SLOW Timeout detection start to work. WDT detection monitors the time between this rising edge and the next rising edge. When it can't detect WDIN rising edge within SLOW Timeout (t_{WS}), XRSTOUT becomes low. XRSTOUT goes back to high after 10 ms delay. Then, WDT works after 500 ms delay again. This delay time is implemented as a time for microprocessor to be reset normally and to stabilized. If this time is unnecessary and WDT should be activated as soon as possible, WDEN may be controlled from low to high.

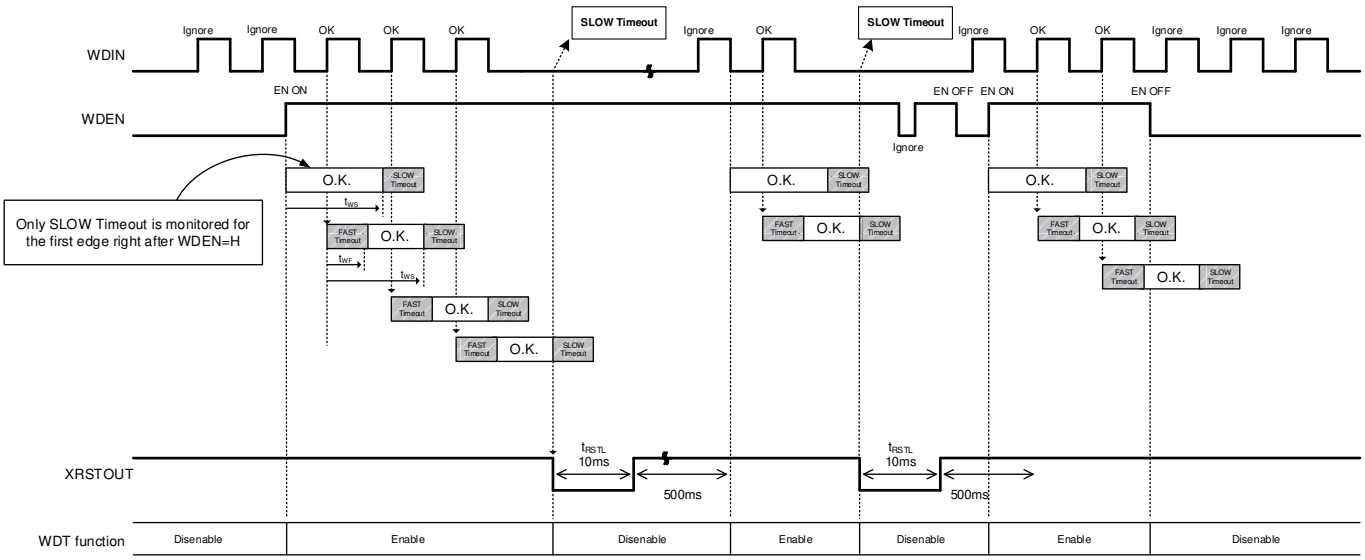


Figure 8. WDT SLOW Timeout Detection

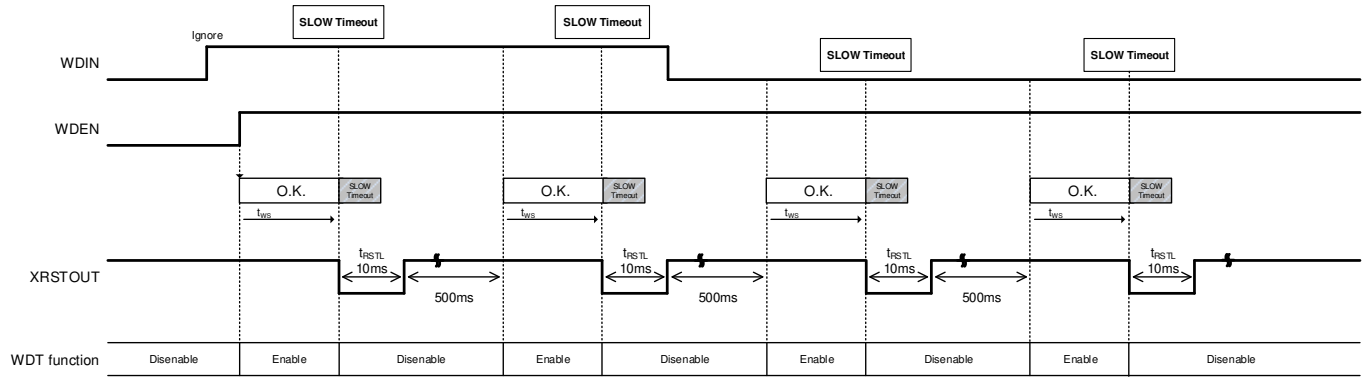


Figure 9. XRSTOUT Behavior with Continuous WDT Timeout Detection

WDT SLOW timeout detection – continued

The window time for detection can be changed by the resistor value between RTW and GND. Following figure shows the detection time determined by R_{RTW} resistor value. Refer to a table of electric characteristic regarding an accuracy. Customer can choose the value ranging from 10 kΩ to 47 kΩ according to their clock frequency. The ratio for detection time is fixed and can be shown like this, FAST Timeout: SLOW Timeout = 1: 4.

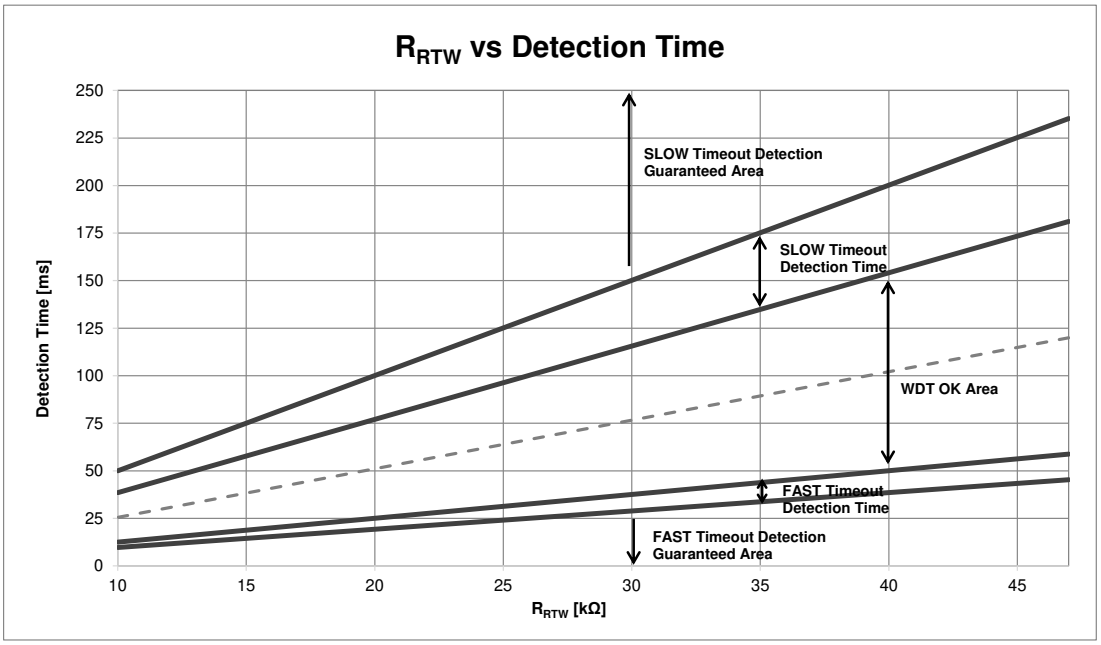


Figure 10. Detection time vs R_{RTW} resistance

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
VCC Voltage	V_{CC}	-0.3 to +42	V
VS2, VS3 Voltage	V_{S2}, V_{S3}	-0.3 to +6	V
EN1 Voltage	V_{EN1}	-0.3 to +42	V
EN2, EN3, EN4 Voltage	V_{EN2}, V_{EN3}, V_{EN4}	-0.3 to +7	V
VO1 Voltage	V_{VO1}	-0.3 to +7	V
VO2 Voltage	V_{VO2}	-0.3 to V_{REG} +0.3	V
FB3 Voltage	V_{FB3}	-0.3 to V_{REG} +0.3	V
VO3S Voltage	V_{VO3S}	-0.3 to V_{REG} +0.3	V
VO4 Voltage	V_{VO4}	-0.3 to +7	V
PGND1S, CSN Voltage	V_{PGND1S}, V_{CSN}	-0.3 to +0.3	V
SYNC Voltage	V_{SYNC}	-0.3 to +6	V
WDEN Voltage	V_{WDEN}	-0.3 to +6	V
WDIN Voltage	V_{WDIN}	-0.3 to +6	V
SSCGEN Voltage	V_{SSCGEN}	-0.3 to V_{REG} +0.3	V
XRSTOUT, PGOOD1, PGOOD2, XTWOUT Voltage	$V_{XRSTOUT}$ V_{PGOOD1} V_{PGOOD2} V_{XTWOUT}	-0.3 to +7	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
VQFN40FV6060				
Junction to Ambient	θ_{JA}	83.7	27.0	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	8.0	4.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage 1 *(Note 6)*	V_{CC}	4	12	28	V
Supply Voltage 2	V_{S2}, V_{S3}	3.0	3.3	5.5	V
VO2/VO3 Output Current	I_{VO2}, I_{VO3}	-	-	2.5 *(Note 7)*	A
SW4 Current	I_{SW4}	-	-	1.0 *(Note 7)*	A
SYNC Input Frequency	f_{SYNC}	1.9	2.2	2.5	MHz
SYNC Input Duty Cycle	D_{SYNC}	40	50	60	%
WDIN Input Frequency	f_{WDIN}	10	-	50	Hz
WDIN Minimum ON Pulse/OFF Pulse	t_{WDP}	-	-	100	µs
VO3 Output Voltage Range	V_{VO3}	0.8	-	2.5	V
Operating Ambient Temperature	Topr	-40	+25	+125	°C

(Note 6) Initial startup is over 4.5 V.
(Note 7) ASO should not be exceeded

Electrical Characteristics
(Unless otherwise specified V_{CC} = 12 V, V_{S2} = V_{S3} = 3.3 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
All						
Standby Current 1	I_{st1}	-	0	10	µA	V_{EN1} = 0 V, Tj = 25 °C
Standby Current 2	I_{st2}	-	-	50	µA	V_{EN1} = 0 V, Tj = 125 °C
Circuit Current	I_{VCC}	-	5	-	mA	V_{EN1} = 12 V, V_{EN2} = V_{EN3} = V_{EN4} = 3.3 V Non-switching current
VREG Output Voltage	V_{REG}	4.6	5.0	5.4	V	I_{VREG} = -10 mA
VCC UVLO Threshold Voltage 1	V_{UVVCC1}	3.6	3.8	4.0	V	VCC voltage sweep down
VCC UVLO Threshold Voltage 2	V_{UVVCC2}	4.0	4.2	4.4	V	VCC voltage sweep up
VCC UVLO Hysteresis	V_{HYSVCC}	-	0.4	-	V	
VREG UVLO Threshold Voltage 1	V_{UVREG1}	3.2	3.5	3.8	V	VREG voltage sweep down
VREG UVLO Threshold Voltage 2	V_{UVREG2}	3.3	3.6	3.9	V	VREG voltage sweep up
VREG UVLO Hysteresis	V_{HYSREG}	-	0.1	-	V	
VREG Switch Over Voltage 1	V_{SWREG1}	4.15	4.5	4.85	V	VO4 voltage sweep up
VREG Switch Over Voltage 2	V_{SWREG2}	4.05	4.4	4.75	V	VO4 voltage sweep down
VREG Switch Hysteresis	V_{HYSSW}	-	0.1	-	V	
VS2/VS3 UVLO Threshold Voltage 1	V_{UVVS21} V_{UVVS31}	2.2	2.5	2.8	V	VS2/VS3 voltage sweep down
VS2/VS3 UVLO Threshold Voltage 2	V_{UVVS22} V_{UVVS32}	2.4	2.7	3.0	V	VS2/VS3 voltage sweep up
VS2/VS3 UVLO Hysteresis	V_{HYSVS2} V_{HYSVS3}	-	0.2	-	V	
VO4 UVLO Threshold Voltage 1	V_{UVVO41}	1.6	1.8	2.0	V	VO4 voltage sweep down
VO4 UVLO Threshold Voltage 2	V_{UVVO42}	1.8	2.0	2.2	V	VO4 voltage sweep up
VO4 UVLO Hysteresis	V_{HYSVO4}	-	0.2	-	V	
Switching Frequency	f_{OSC}	1.9	2.2	2.5	MHz	R_{RT} = 9.1 kΩ V_{SSCGEN} = 0 V

Electrical Characteristics – continued
(Unless otherwise specified V_{CC} = 12 V, V_{S2} = V_{S3} = 3.3 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BUCK1 (Primary Buck Controller)						
VO1 Voltage	V_{VO1}	3.250	3.300	3.350	V	
Soft Start Time1	t_{SS1}	0.75	-	3.0	ms	
VGH1 High Side ON Resistance	$R_{ONVGH1H}$	-	10	20	Ω	I_{VGH1} = -10 mA
VGH1 Low Side ON Resistance	$R_{ONVGH1L}$	-	1.5	4	Ω	I_{VGH1} = +10 mA
VGL1 High Side ON Resistance	$R_{ONVGL1H}$	-	10	25	Ω	I_{VGL1} = -10 mA
VGL1 Low Side ON Resistance	$R_{ONVGL1L}$	-	1.5	4	Ω	I_{VGL1} = +10 mA
Over Current Protection CSN Voltage	V_{CSN}	60	75	90	mV	$V_{CSN} – V_{PGND1S}$
OVP Detect Voltage 1	V_{OVP11}	4.00	4.25	4.50	V	VO1 voltage sweep up
OVP Release Voltage 1	V_{OVP12}	-	4.00	-	V	VO1 voltage sweep down
SCP Detect Voltage 1	V_{SCP11}	1.485	1.650	1.815	V	VO1 voltage sweep down
SCP Release Voltage 1	V_{SCP12}	-	1.815	-	V	VO1 voltage sweep up
OVD Detect Voltage 1	V_{OVD1}	3.365	3.415	3.465	V	VO1 voltage sweep up
UVD Detect Voltage 1	V_{UVD1}	3.135	3.185	3.235	V	VO1 voltage sweep down
OVD/UVD Filter Time 1	t_{FIL1}	50	75	100	µs	
VO1 Discharge Resistor	R_{DIS1}	-	-	500	Ω	Resistance between VO1 and PGND1
BUCK2 (Secondary Buck)						
VO2 Voltage	V_{VO2}	1.182	1.200	1.218	V	
Soft Start Time 2	t_{SS2}	0.6	-	2.4	ms	
SW2 High Side On Resistance	R_{ON2H}	-	75	150	mΩ	I_{SW2} = -50 mA
SW2 Low Side On Resistance	R_{ON2L}	-	75	150	mΩ	I_{SW2} = +50 mA
OVP Detect Voltage 2	V_{OVP21}	1.36	1.44	1.52	V	VO2 voltage sweep up
OVP Release Voltage 2	V_{OVP22}	-	1.32	-	V	VO2 voltage sweep down
SCP Detect Voltage 2	V_{SCP21}	0.54	0.60	0.66	V	VO2 voltage sweep down
SCP Release Voltage 2	V_{SCP22}	-	0.72	-	V	VO2 voltage sweep up
OVD Detect Voltage 2	V_{OVD2}	1.224	1.242	1.260	V	VO2 voltage sweep up
UVD Detect Voltage 2	V_{UVD2}	1.140	1.158	1.176	V	VO2 voltage sweep down
OVD/UVD Filter Time 2	t_{FIL2}	50	75	100	µs	
VO2 Discharge Resistor	R_{DIS2}	-	-	100	Ω	Resistance between SW2 and PGND2
BUCK3 (Secondary Buck)						
FB3 Voltage	V_{FB3}	0.788	0.800	0.812	V	
Soft Start Time 3	t_{SS3}	0.6	-	2.4	ms	
SW3 High Side On Resistance	R_{ON3H}	-	75	150	mΩ	I_{SW3} = -50 mA
SW3 Low Side On Resistance	R_{ON3L}	-	75	150	mΩ	I_{SW3} = +50 mA
OVP Detect Voltage 3	V_{OVP31}	0.90	0.96	1.02	V	VO3S voltage sweep up
OVP Release Voltage 3	V_{OVP32}	-	0.88	-	V	VO3S voltage sweep down
SCP Detect Voltage 3	V_{SCP31}	0.36	0.40	0.44	V	VO3S voltage sweep down
SCP Release Voltage 3	V_{SCP32}	-	0.48	-	V	VO3S voltage sweep up
OVD Detect Voltage 3	V_{OVD3}	0.816	0.828	0.840	V	FB3 voltage sweep up
UVD Detect Voltage 3	V_{UVD3}	0.760	0.772	0.784	V	FB3 voltage sweep down
OVD/UVD Filter Time 3	t_{FIL3}	50	75	100	µs	
VO3 Discharge Resistor	R_{DIS3}	-	-	100	Ω	Resistance between SW3 and PGND3

Electrical Characteristics - continued
(Unless otherwise specified V_{CC} = 12 V, V_{S2} = V_{S3} = 3.3 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BOOST4 (Secondary Boost)						
VO4 Voltage	V_{VO4}	4.90	5.00	5.10	V	
Soft Start Time of BOOST 4	t_{SS4}	1	-	4	ms	
SW4 On Resistance	R_{ON4}	-	200	-	mΩ	I_{SW4} = 50 mA
OVP Detect Voltage 4	V_{OVP41}	6.0	6.5	7.0	V	VO4 voltage sweep up
OVP Release Voltage 4	V_{OVP42}	-	6.25	-	V	VO4 voltage sweep down
SCP Detect Voltage 4	V_{SCP41}	2.25	2.50	2.75	V	VO4 voltage sweep down
SCP Release Voltage 4	V_{SCP42}	-	3.00	-	V	VO4 voltage sweep up
OVD Detect Voltage 4	V_{OVD4}	5.150	5.325	5.500	V	VO4 voltage sweep up
UVD Detect Voltage 4	V_{UVD4}	4.500	4.675	4.850	V	VO4 voltage sweep down
OVD/UVD Filter Time 4	t_{FIL4}	50	75	100	µs	
Enable						
EN1 Low Voltage	V_{ENL1}	-	-	0.8	V	
EN1 High Voltage	V_{ENH1}	2.6	-	-	V	
EN1 Pull down Resistor	R_{EN1}	125	250	375	kΩ	V_{EN1} = 5 V
EN2, EN3, EN4 Low Voltage	V_{ENL2}, V_{ENL3}, V_{ENL4}	-	-	V_{VO1} x 0.2	V	
EN2, EN3, EN4 High Voltage	V_{ENH2}, V_{ENH3}, V_{ENH4}	V_{VO1} x 0.8	-	-	V	
EN2, EN3, EN4 Pull Down Resistor	$R_{EN2/3/4}$	50	100	150	kΩ	
Synchronous						
SYNC Low Voltage	V_{SYNCL}	-	-	V_{VO1} x 0.2	V	
SYNC High Voltage	V_{SYNCH}	V_{VO1} x 0.8	-	-	V	
SYNC Pull down Resistor	R_{SYNC}	50	100	150	kΩ	
SSCGEN						
SSCGEN Low Voltage	$V_{SSCGENL}$	-	-	V_{REG} x 0.2	V	
SSCGEN High Voltage	$V_{SSCGENH}$	V_{REG} x 0.8	-	-	V	
SSCGEN Pull up Resistor	R_{SSCGEN}	50	100	150	kΩ	Between VREG and SSCGEN
RESET						
VO1 Power On Reset Threshold Voltage (Falling)	V_{UVVO11}	2.3	2.4	2.5	V	VO1 voltage sweep down
VO1 Power On Reset Threshold Voltage (Rising)	V_{UVVO12}	2.5	2.6	2.7	V	VO1 voltage sweep up
VO1 Power On Reset Hysteresis	V_{VO1HYS}	-	0.2	-	V	
XRSTOUT On Resistance	R_{ONRST}	-	-	200	Ω	I_{RSTOUT} = 1 mA
XRSTOUT Leak Current	I_{LRST}	-	-	10	µA	V_{RSTOUT} = 5 V
XRSTOUT Low Hold Time	t_{RSTL}	7	10	13	ms	
Power Good						
PGOOD On Resistance	R_{ONPG}	-	-	200	Ω	PGOOD1, PGOOD2 I_{PGOOD1}, I_{PGOOD2} = 1 mA
PGOOD Leak Current	I_{LPG}	-	-	10	µA	PGOOD1, PGOOD2 V_{PGOOD1}, V_{PGOOD2} = 5 V
Power On Delay Time	t_{PG}	7	10	13	ms	PGOOD1, PGOOD2
Thermal Warning						
XTWOUT On Resistance	R_{ONTW}	-	-	200	Ω	I_{XTWOUT} = 1 mA
XTWOUT Leak Current	I_{LTW}	-	-	10	µA	V_{XTWOUT} = 5 V

Electrical Characteristics - continued
(Unless otherwise specified V_{CC} = 12 V, V_{S2} = V_{S3} = 3.3 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Watch Dog Timer						
WDEN Low Level Input Voltage	V_{WDENL}	-	-	V_{VO1} x 0.2	V	
WDEN High Level Input Voltage	V_{WDENH}	V_{VO1} x 0.8	-	-	V	
WDEN Pull Down Resistor	R_{WDEN}	50	100	150	kΩ	
WDIN Low Level Input Voltage	V_{WDINL}	-	-	V_{VO1} x 0.2	V	
WDIN High Level Input Voltage	V_{WDINH}	V_{VO1} x 0.8	-	-	V	
WDIN Pull Up Resistor	R_{WDIN}	50	100	150	kΩ	
WDT OK Time 1	t_{WOK1}	12.5	25.5	38.5	ms	R_{RTW} = 10 kΩ
WDT FAST Timeout Detect 1	t_{WF1}	9.6	11.1	12.5	ms	R_{RTW} = 10 kΩ
WDT SLOW Timeout Detect 1	t_{WS1}	38.5	44.3	50.1	ms	R_{RTW} = 10 kΩ
WDT OK Time 2	t_{WOK2}	33.8	68.9	104.1	ms	R_{RTW} = 27 kΩ
WDT FAST Timeout Detect 2	t_{WF2}	26.0	29.9	33.8	ms	R_{RTW} = 27 kΩ
WDT SLOW Timeout Detect 2	t_{WS2}	104.1	119.6	135.2	ms	R_{RTW} = 27 kΩ
WDT OK Time 3	t_{WOK3}	58.8	120.0	181.1	ms	R_{RTW} = 47 kΩ
WDT FAST Timeout Detect 3	t_{WF3}	45.3	52.1	58.8	ms	R_{RTW} = 47 kΩ
WDT SLOW Timeout Detect 3	t_{WS3}	181.1	208.2	235.3	ms	R_{RTW} = 47 kΩ

Typical Performance Curves

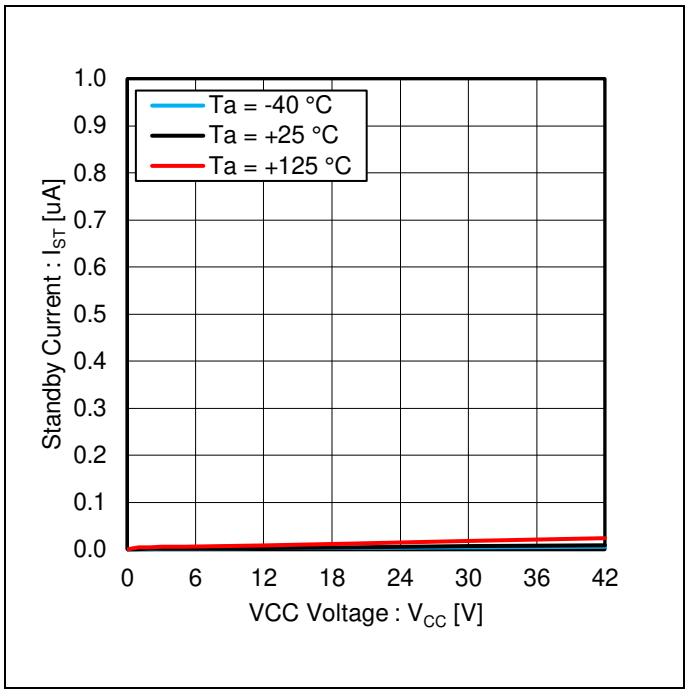


Figure 11. Stand-by Current vs VCC Voltage

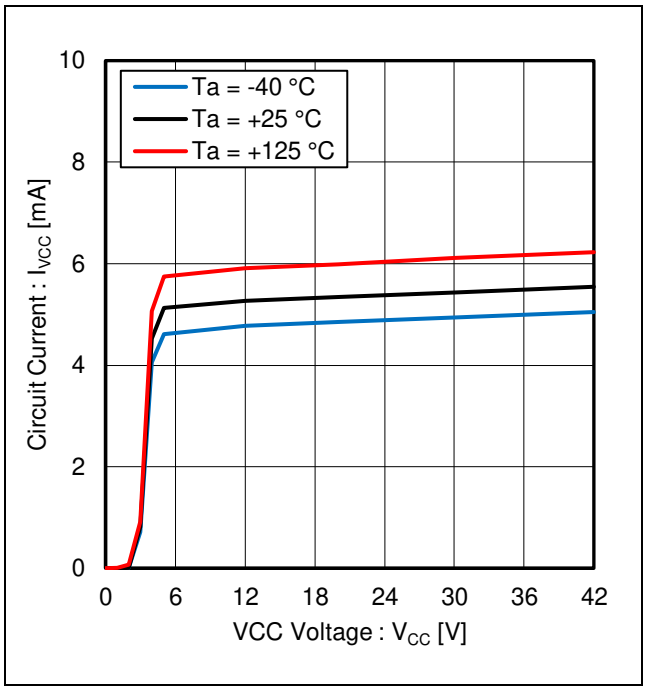


Figure 12. Circuit Current vs VCC Voltage

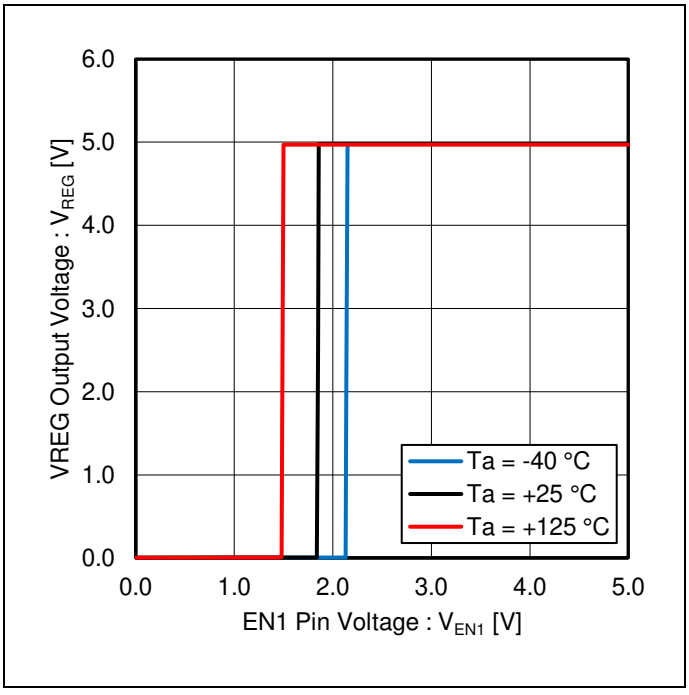


Figure 13. VREG Output Voltage vs the EN1 Pin Voltage ("EN1 Threshold Voltage")

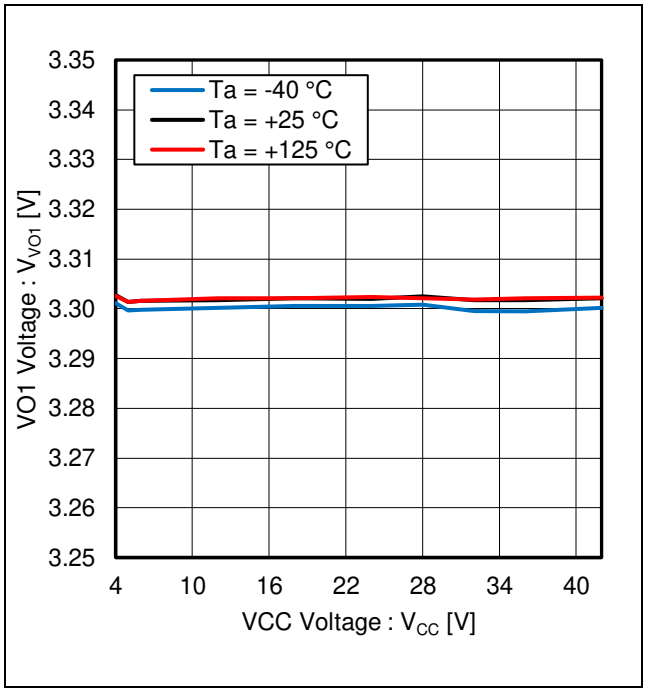


Figure 14. Output Voltage VO1 vs VCC Voltage

Typical Performance Curves - continued

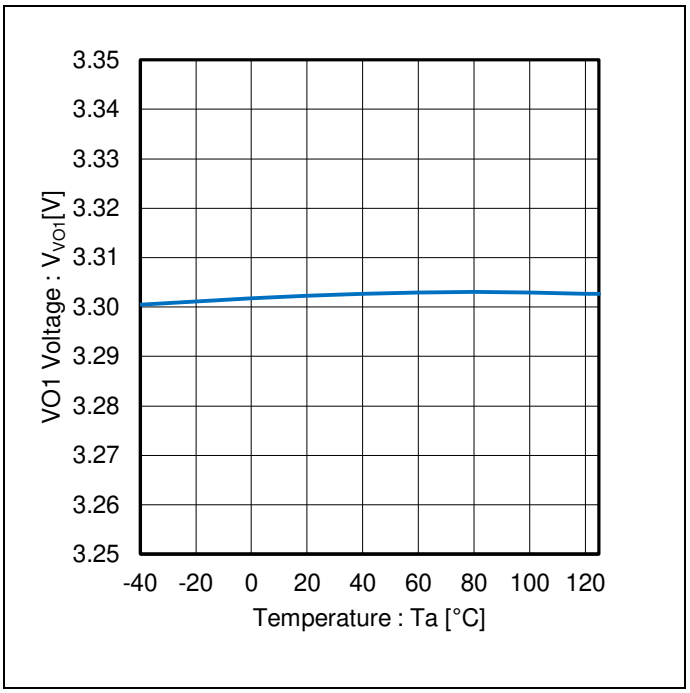


Figure 15. Output Voltage VO1 vs Temperature
(V_{CC} = 12 V)

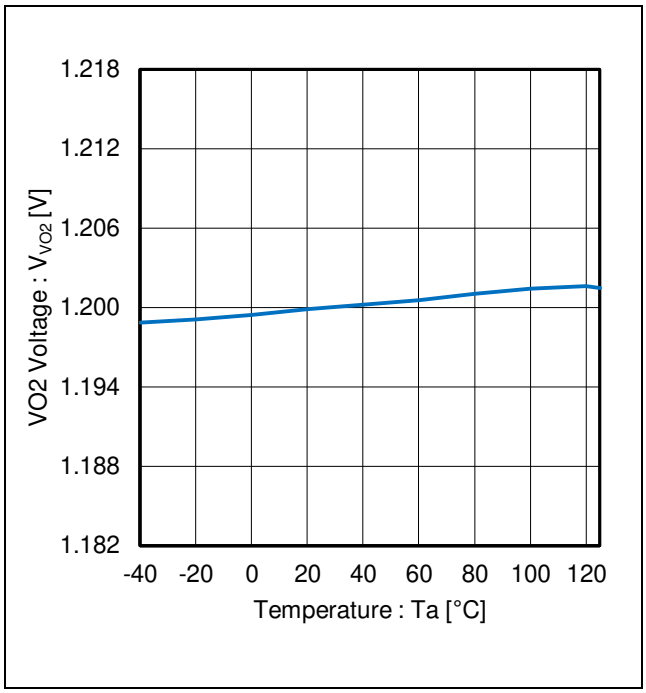


Figure 16. Output Voltage VO2 vs Temperature

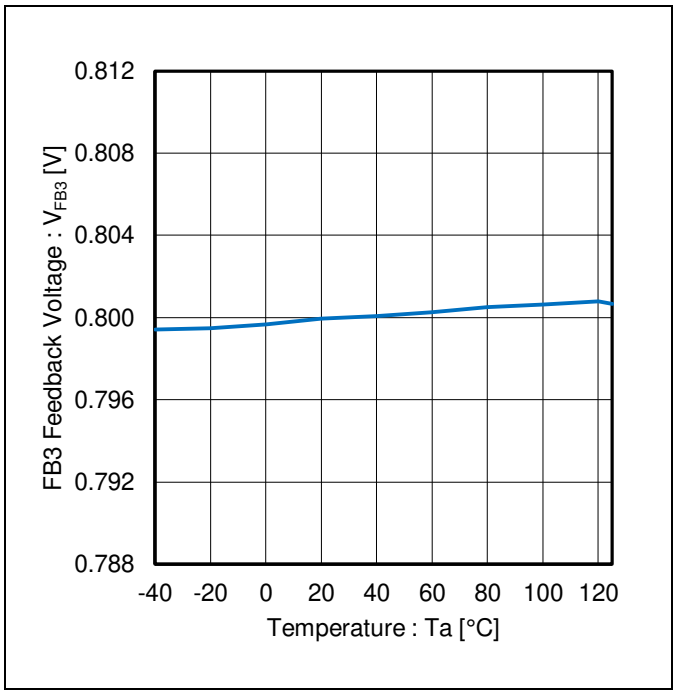


Figure 17. Feedback Voltage FB3 vs Temperature Ta

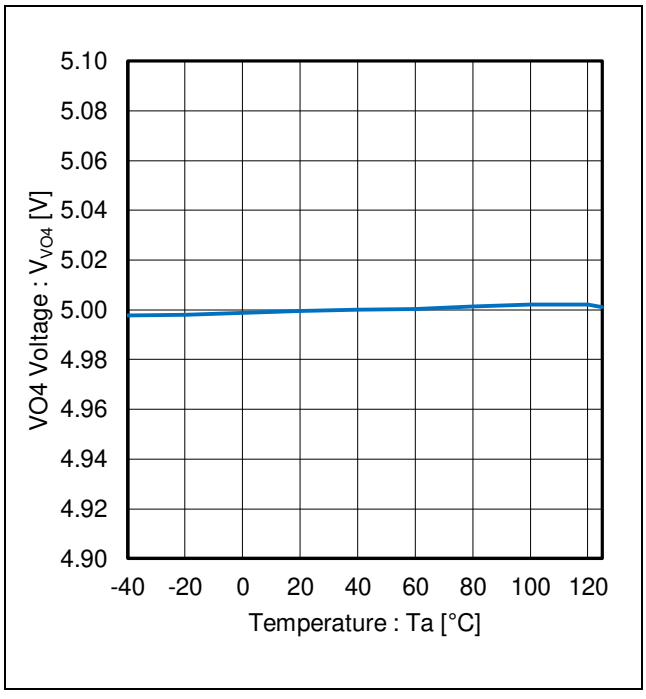


Figure 18. Output Voltage VO4 vs Temperature Ta

Typical Performance Curves - continued

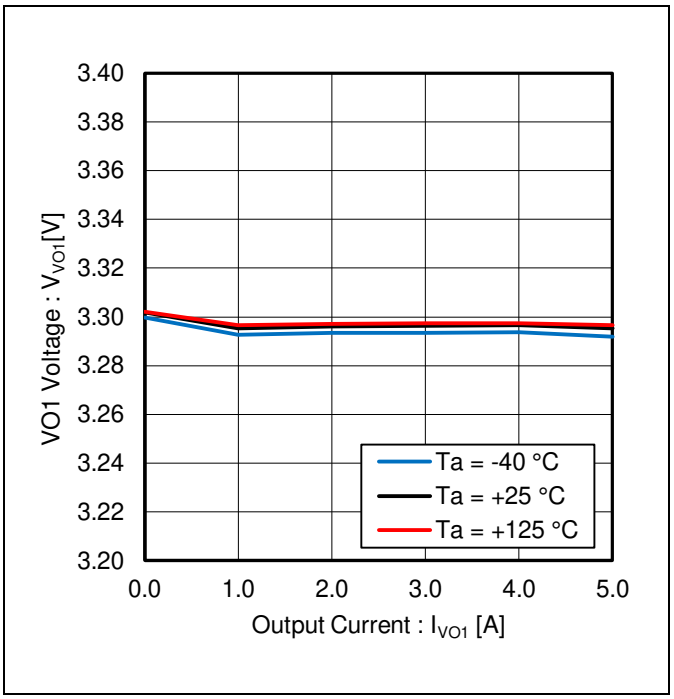


Figure 19. Output Voltage VO1 vs Output Current
("VO1 Load Regulation", V_{CC} = 12 V)

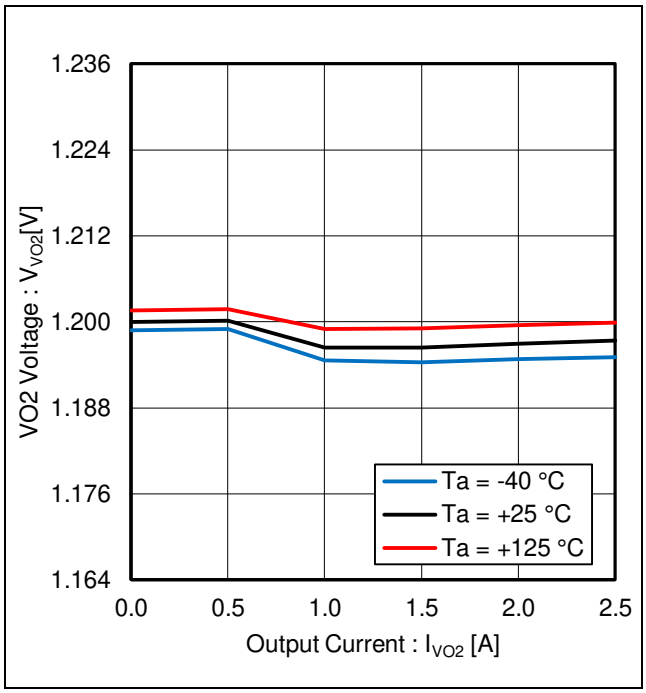


Figure 20. Output Voltage VO2 vs Output Current
("VO2 Load Regulation", V_{S2} = 3.3 V)

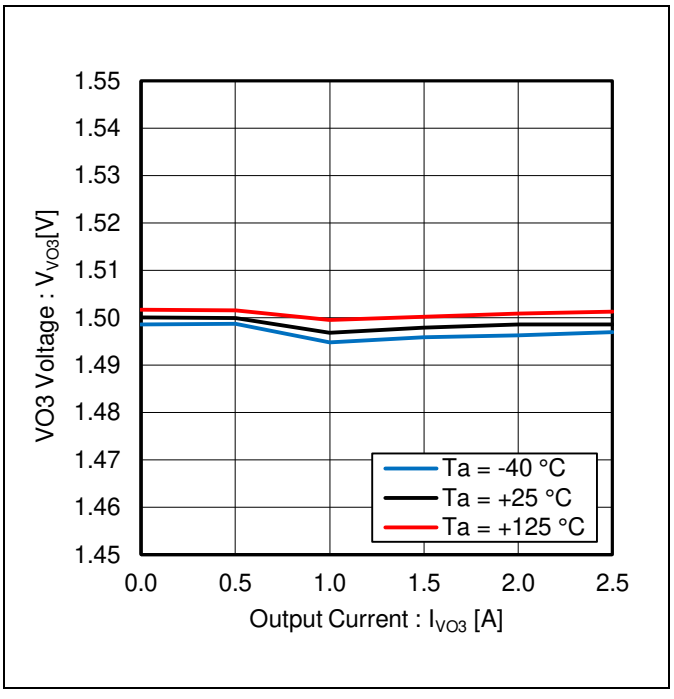


Figure 21. Output Voltage VO3 vs Output Current
("VO3 Load Regulation", V_{S3} = 3.3 V, VO3 = 1.5 V setting)

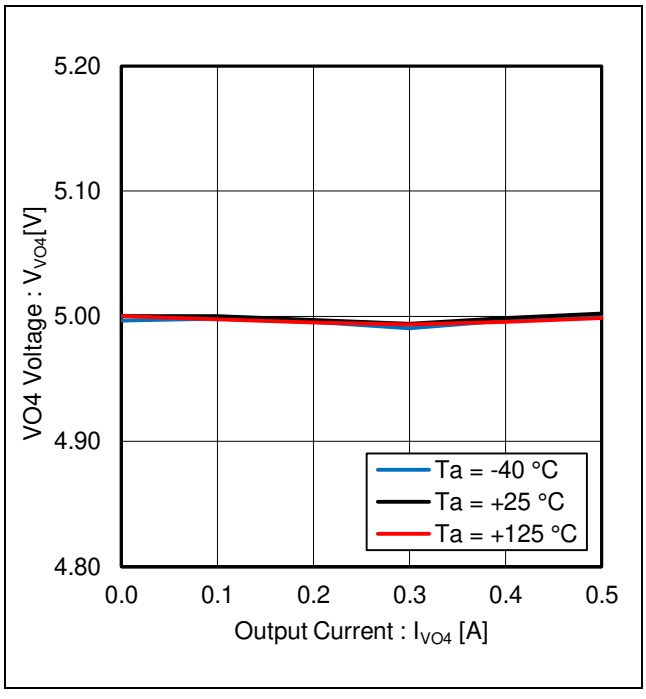


Figure 22. Output Voltage VO4 vs Output Current
("VO4 Load Regulation", V_{S4} = 3.3 V)

Typical Performance Curves - continued

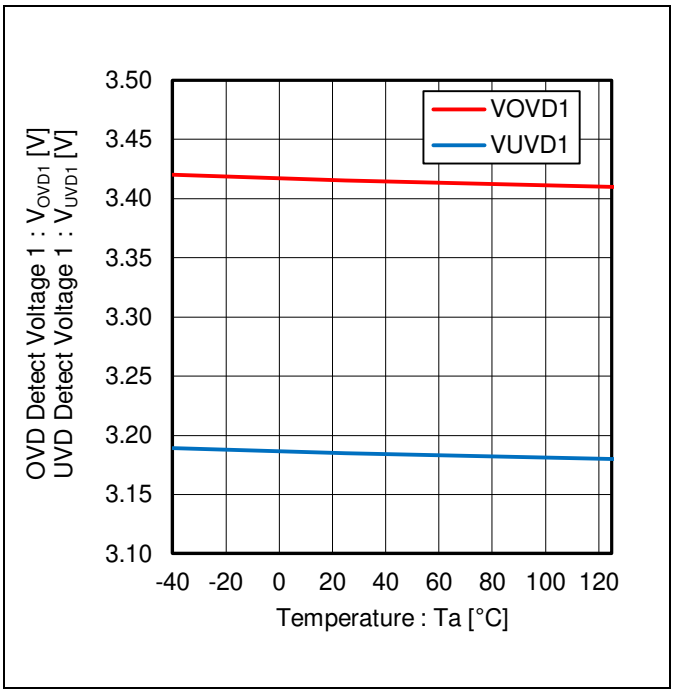


Figure 23. OVD1/UVD1 Detect Voltage vs Temperature
(V_{CC} = 12 V)

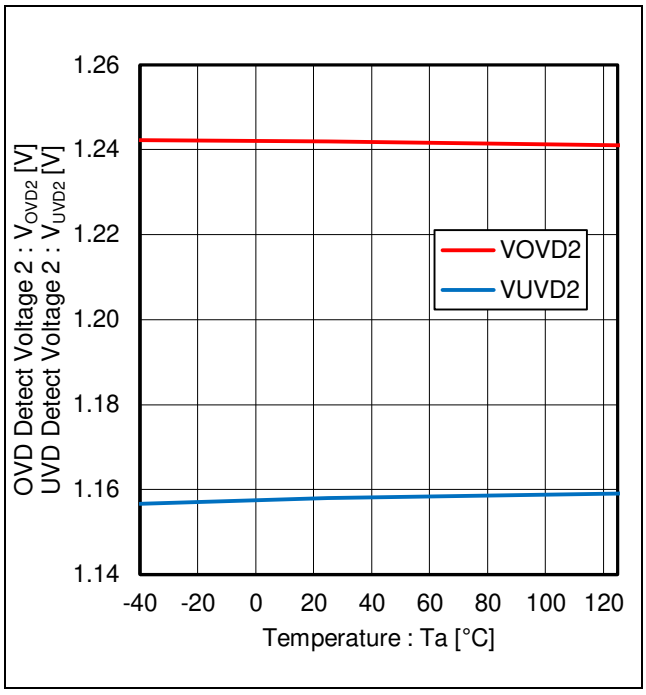


Figure 24. OVD2/UVD2 Detect Voltage vs Temperature
(V_{CC} = 12 V)

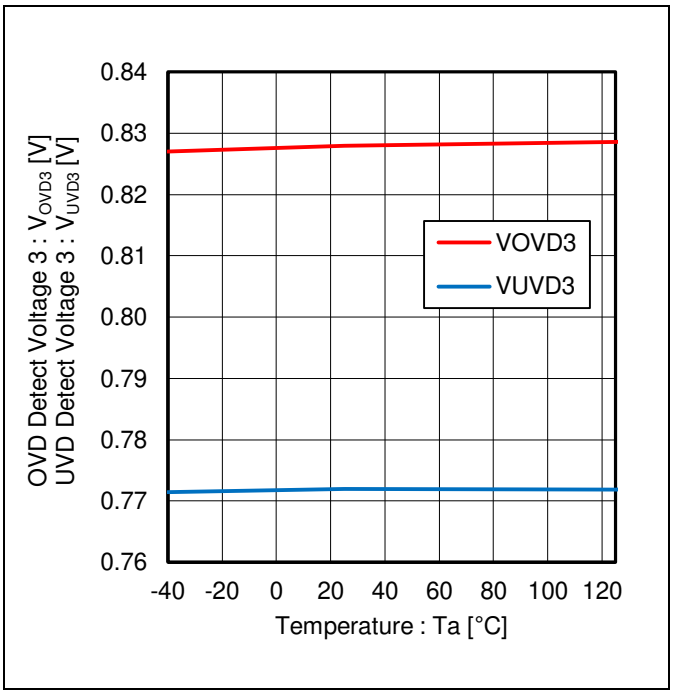


Figure 25. OVD3/UVD3 Detect Voltage vs Temperature
(V_{CC} = 12 V)

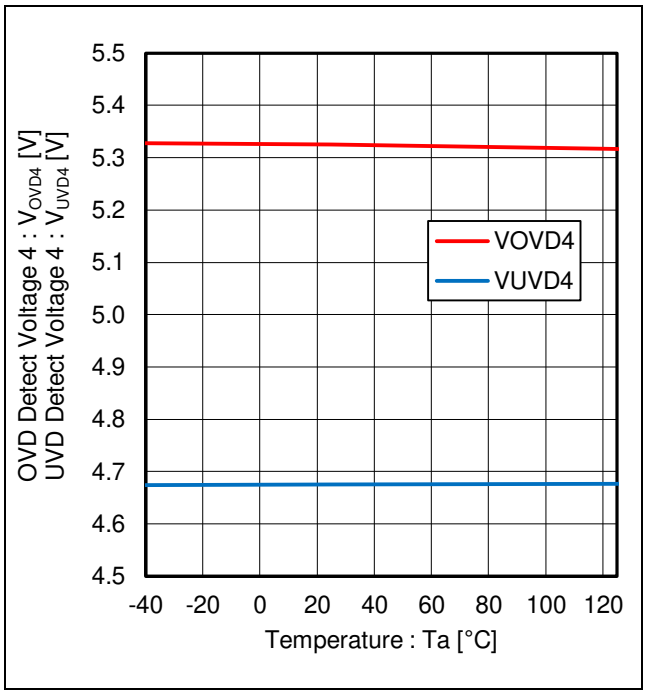


Figure 26. OVD4/UVD4 Detect Voltage vs Temperature
(V_{CC} = 12 V)

Typical Performance Curves - continued

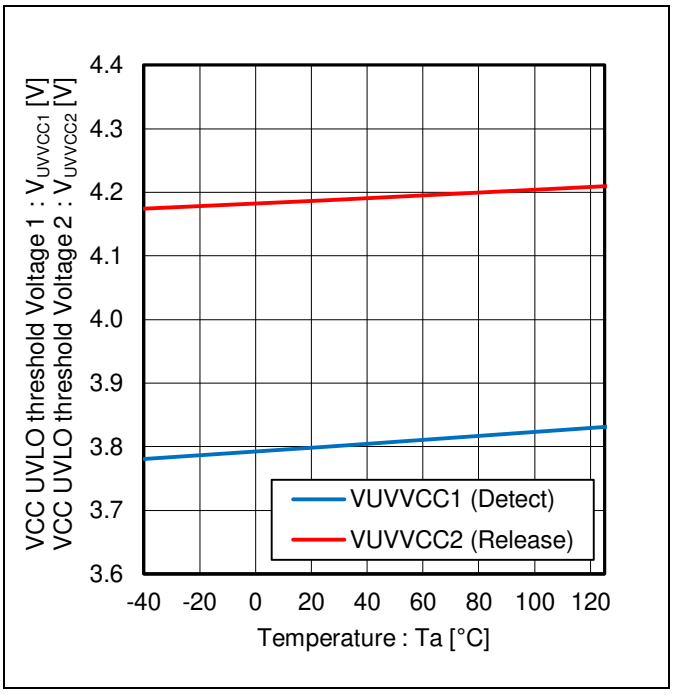


Figure 27. VCC UVLO Threshold Voltage vs Temperature
("VCC UVLO Threshold")

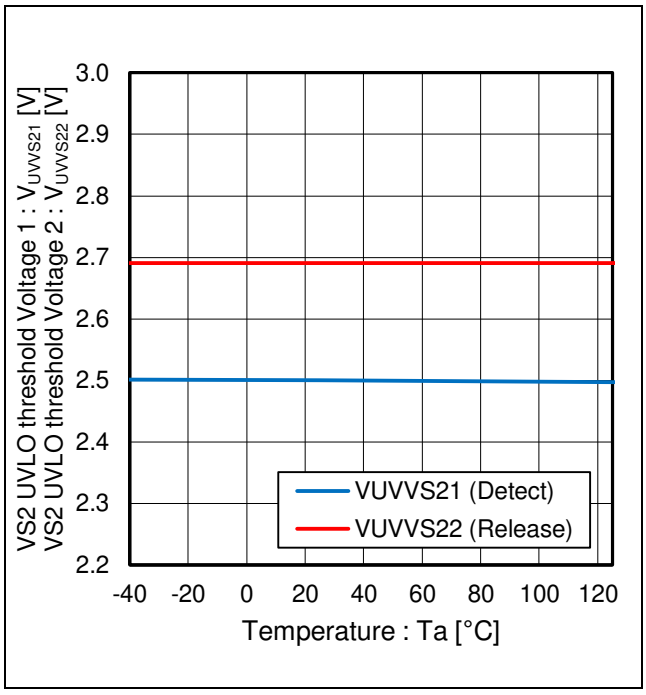


Figure 28. VS2 UVLO Threshold Voltage vs Temperature
("VS2 UVLO Threshold", V_{CC} = 12 V)

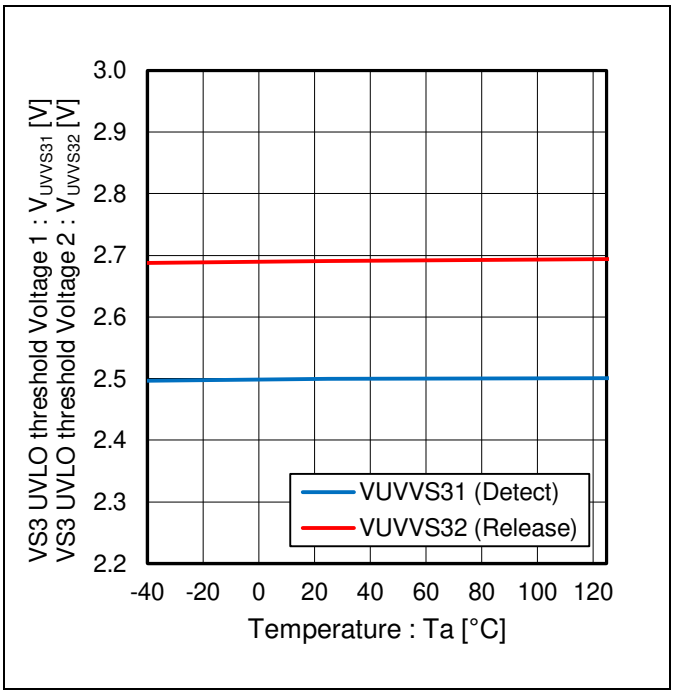


Figure 29. VS3 UVLO Threshold Voltage vs Temperature
("VS3 UVLO Threshold", V_{CC} = 12 V)

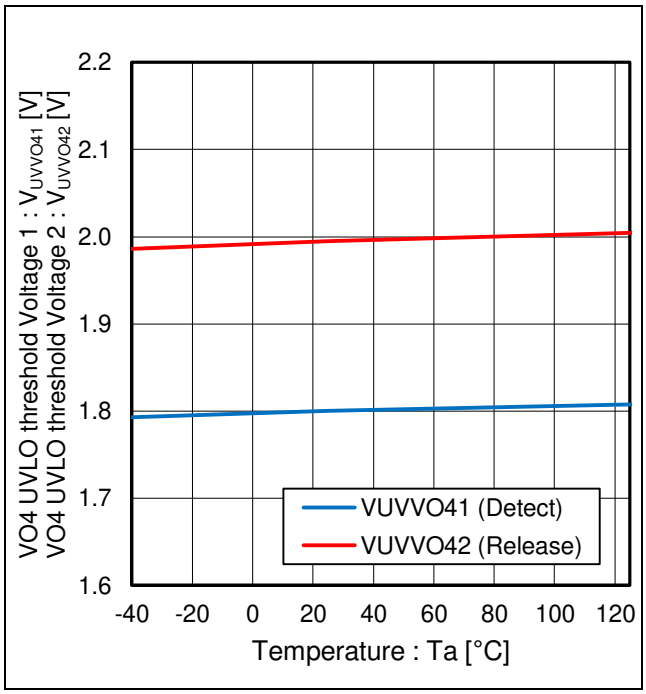


Figure 30. VO4 UVLO Threshold Voltage vs Temperature
("VO4 UVLO Threshold", V_{CC} = 12 V)

Typical Performance Curves - continued

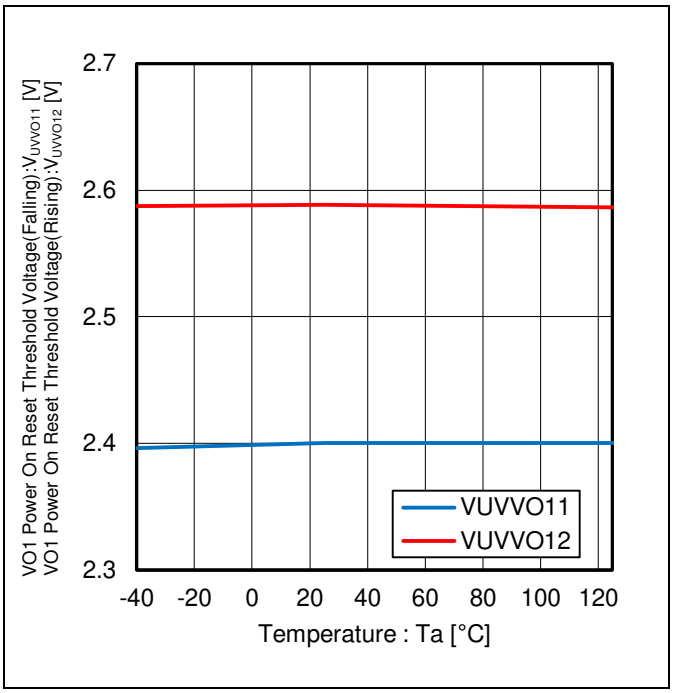


Figure 31. VO1 Power On Reset Threshold Voltage vs Temperature
("VO1RST Threshold", V_{CC} = 12 V)

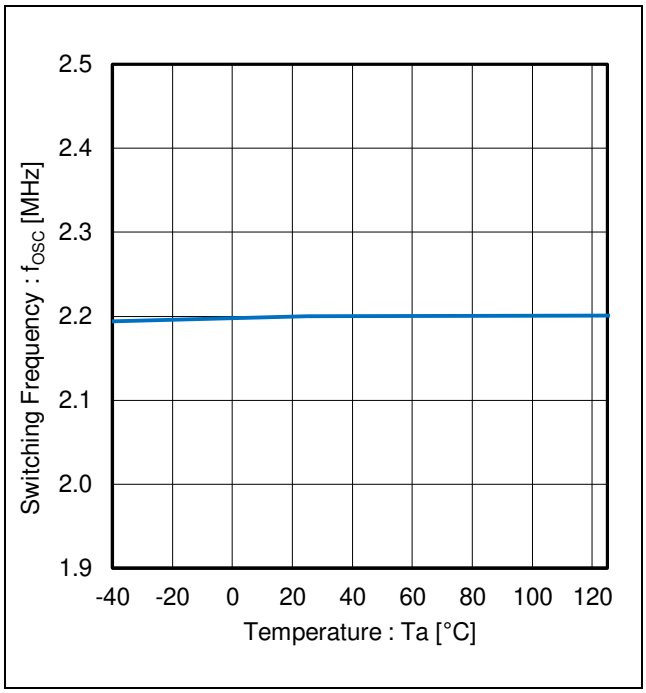


Figure 32. Switching Frequency vs Temperature
(the SSCGEN pin = 0 V)

Typical Performance Curves - continued

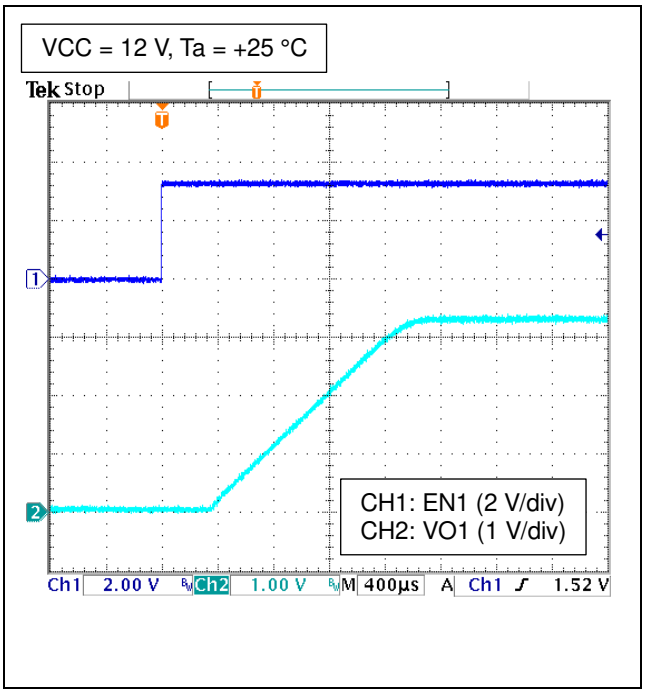


Figure 33. VO1 Power On Waveform
(V_{CC} = 12 V, Ta = +25 °C)

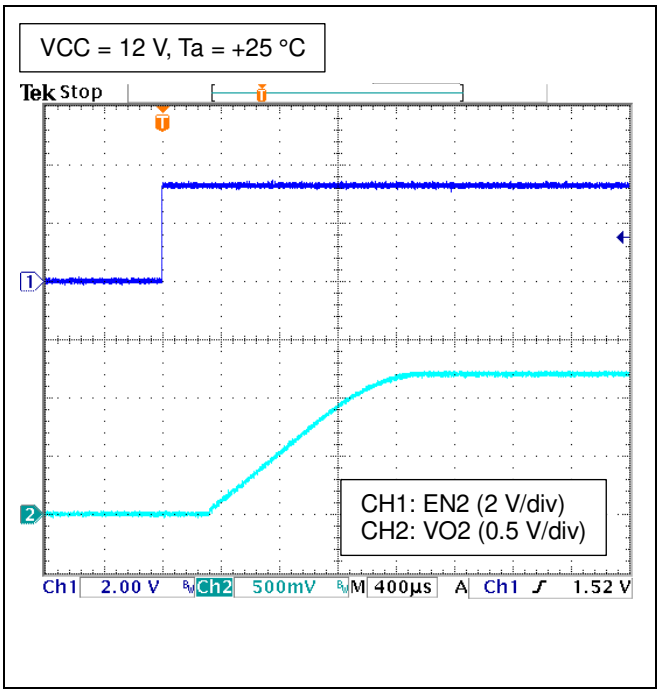


Figure 34. VO2 Power On Waveform
(V_{CC} = 12 V, V_{S2} = 3.3 V, Ta = +25 °C)

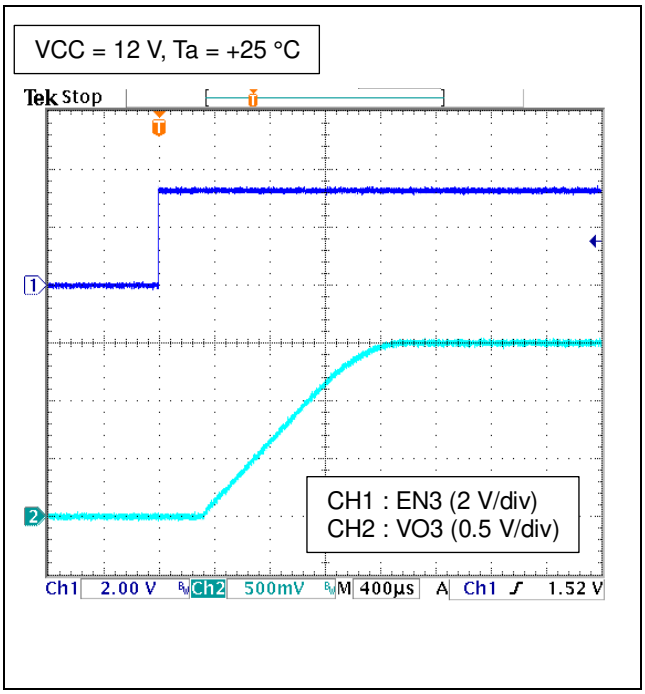


Figure 35. VO3 Power On Waveform
(V_{CC} = 12 V, V_{S3} = 3.3 V, Ta = +25 °C)

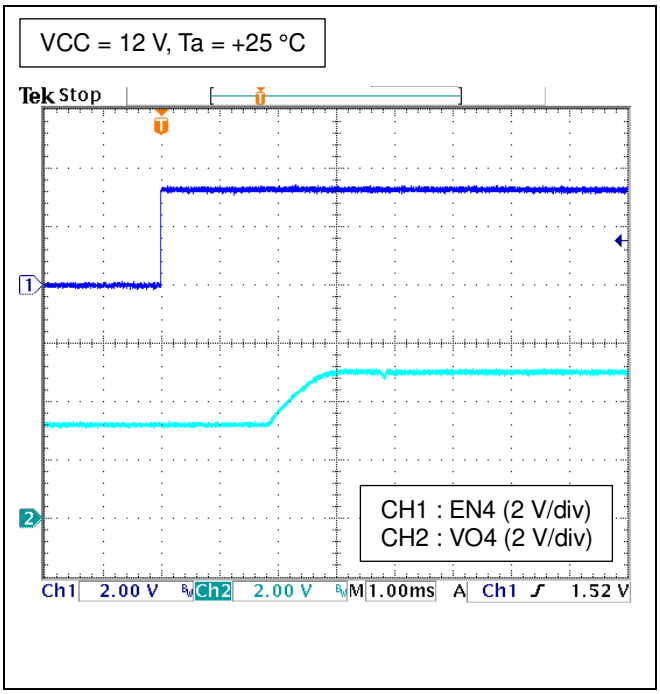
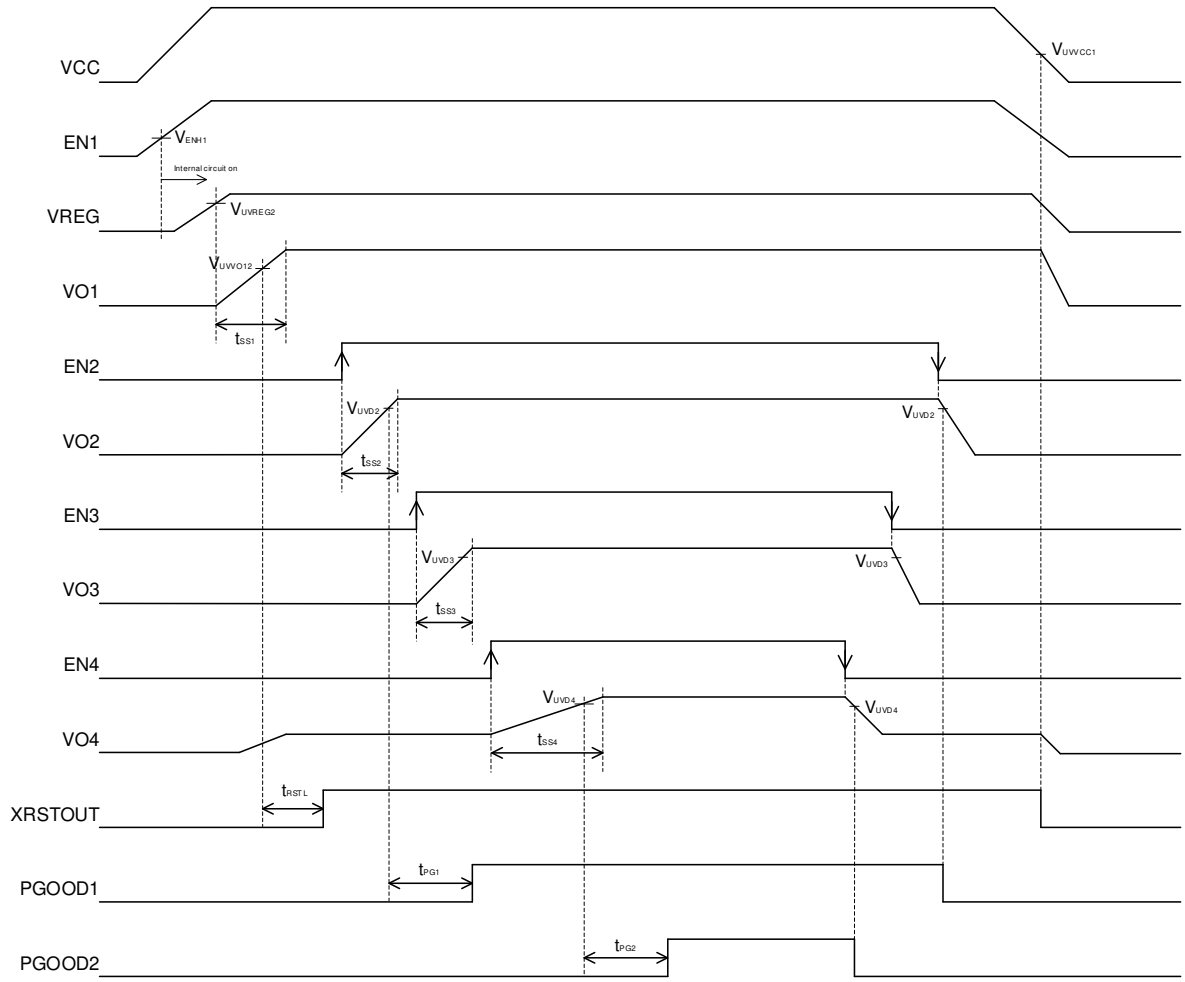


Figure 36. VO4 Power On Waveform
(V_{CC} = 12 V, Ta = +25 °C)

Timing Chart

An example of EN1 tied to VCC, and EN2, EN3, and EN4 controlled by microcomputer.



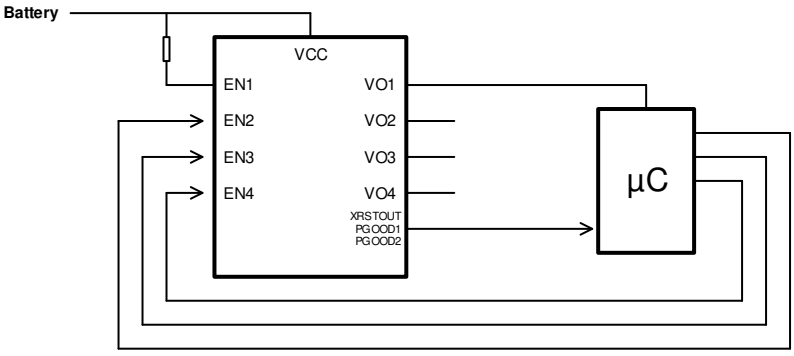
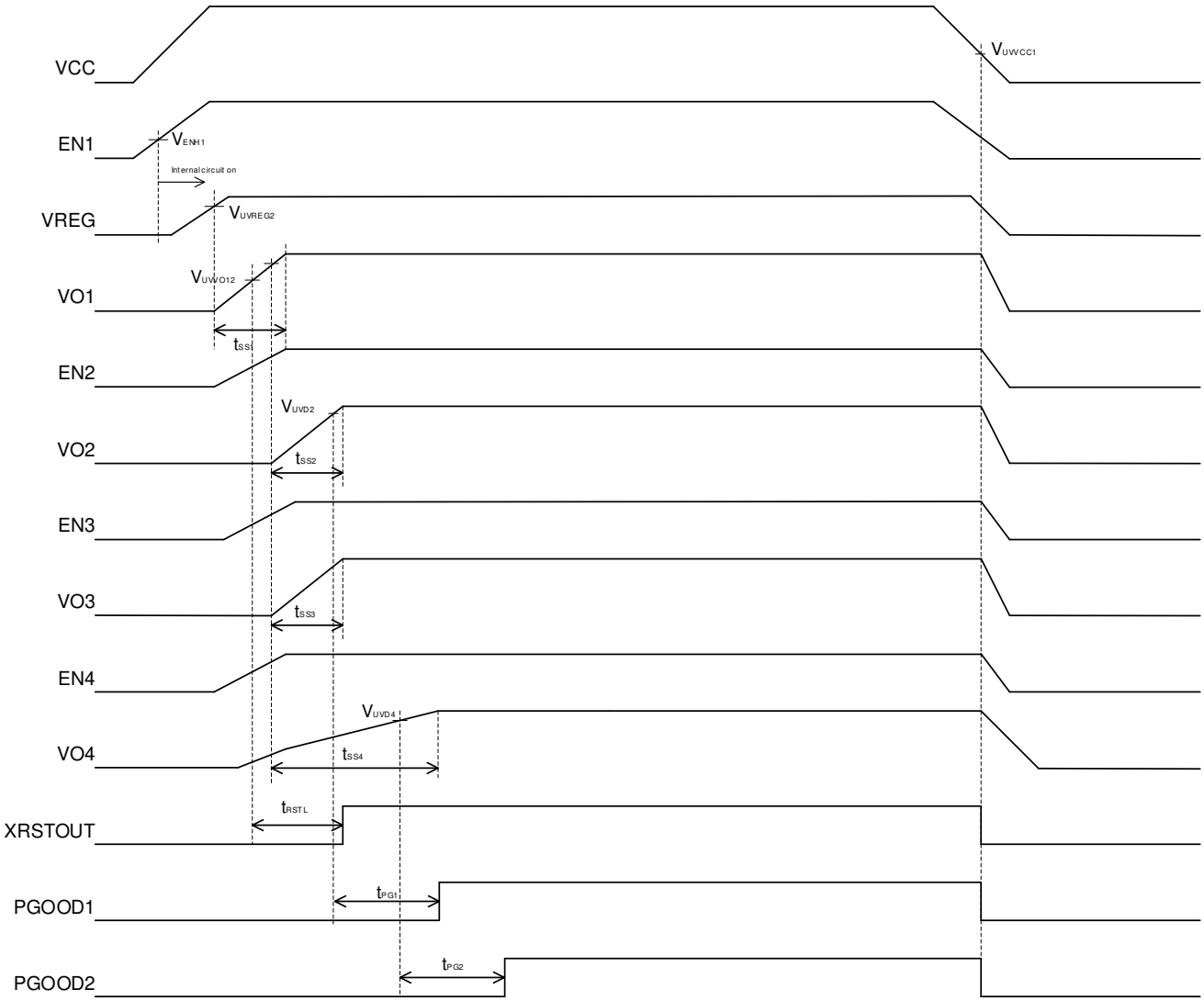


Figure 37. Timing Chart1

Timing Chart - continued

An example of EN1 tied to VCC, and EN2, EN3 and EN4 tied to VO1.



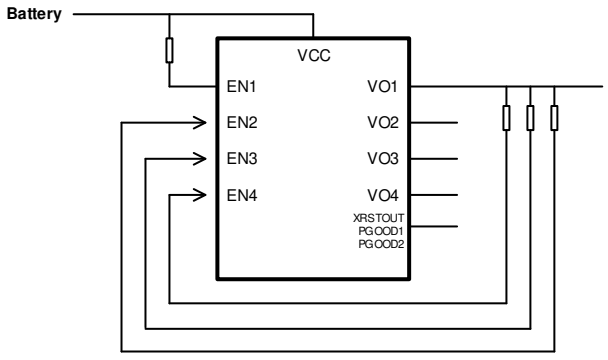


Figure 38. Timing Chart2

Timing Chart - continued

An example of enable signals sequentially controlled.

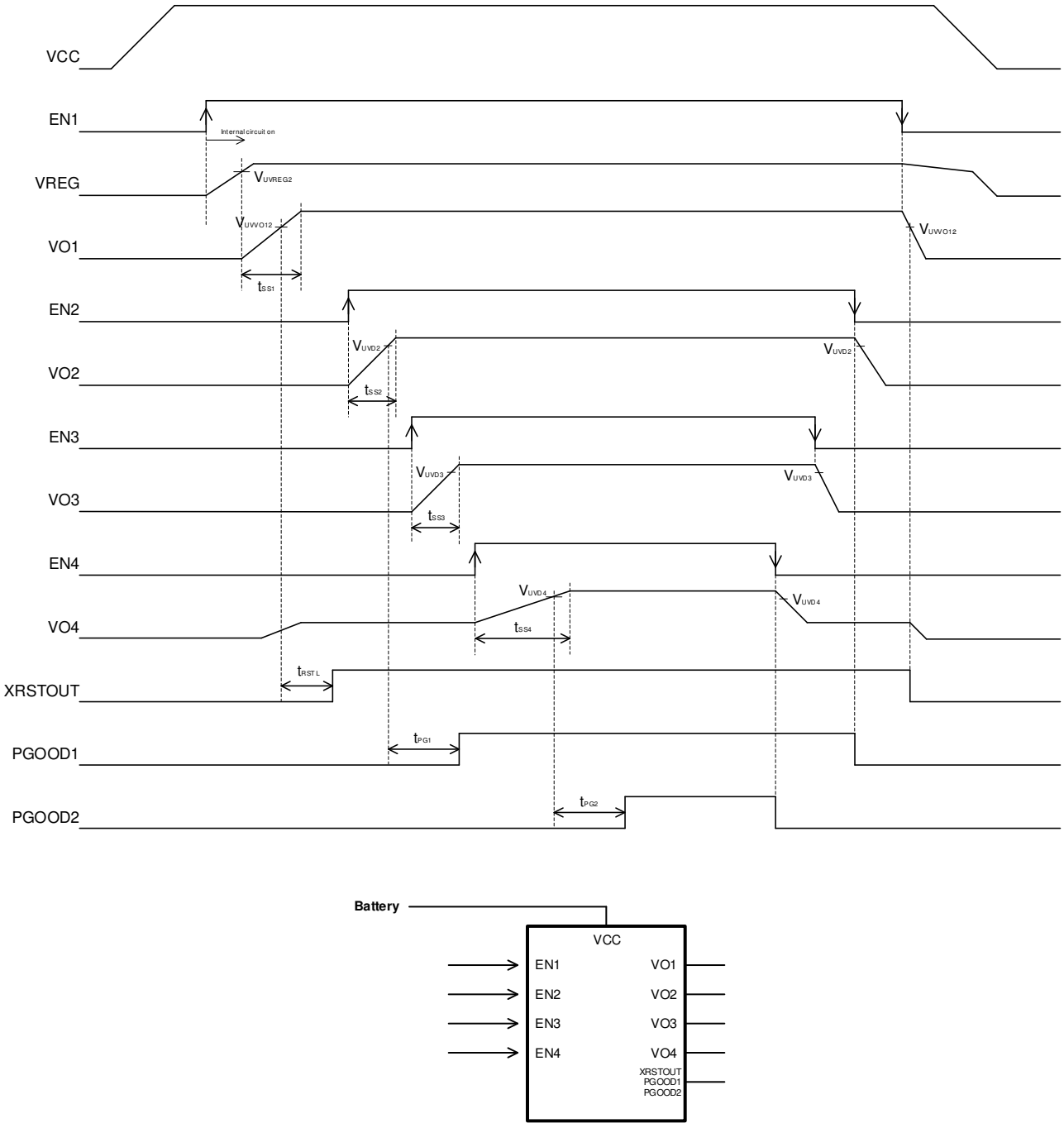


Figure 39. Timing Chart3

Timing Chart - continued

An example of WDEN controlled by external signal.

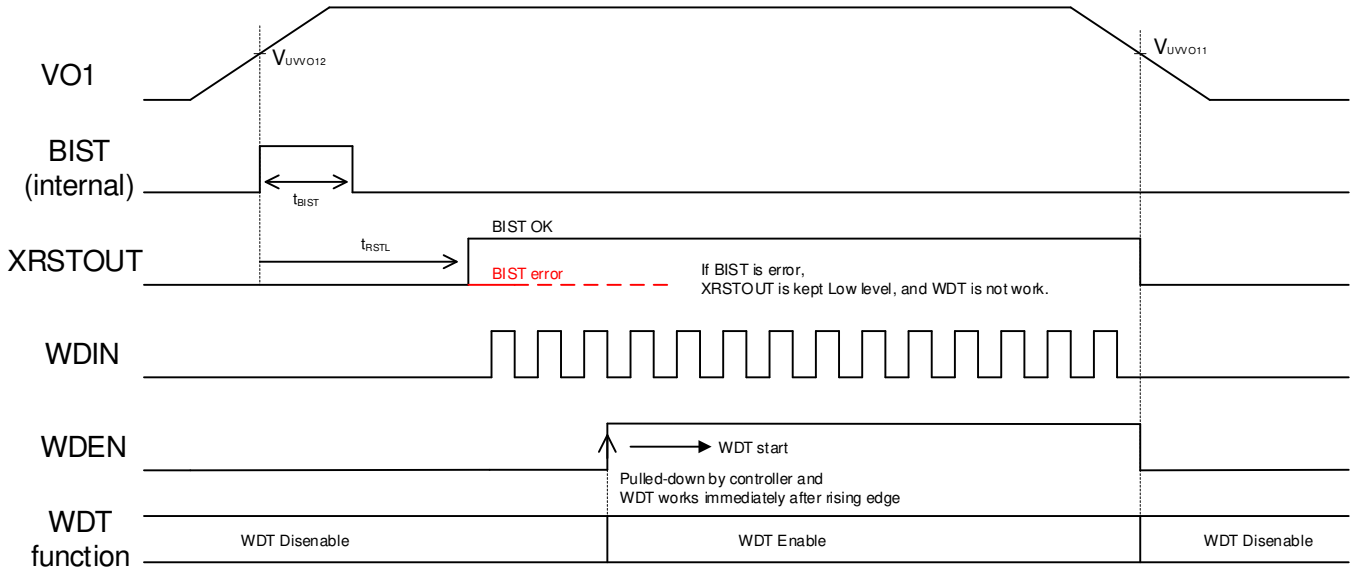


Figure 40. Timing Chart of WDEN controlled by External Signal

An example of WDEN tied to VO1

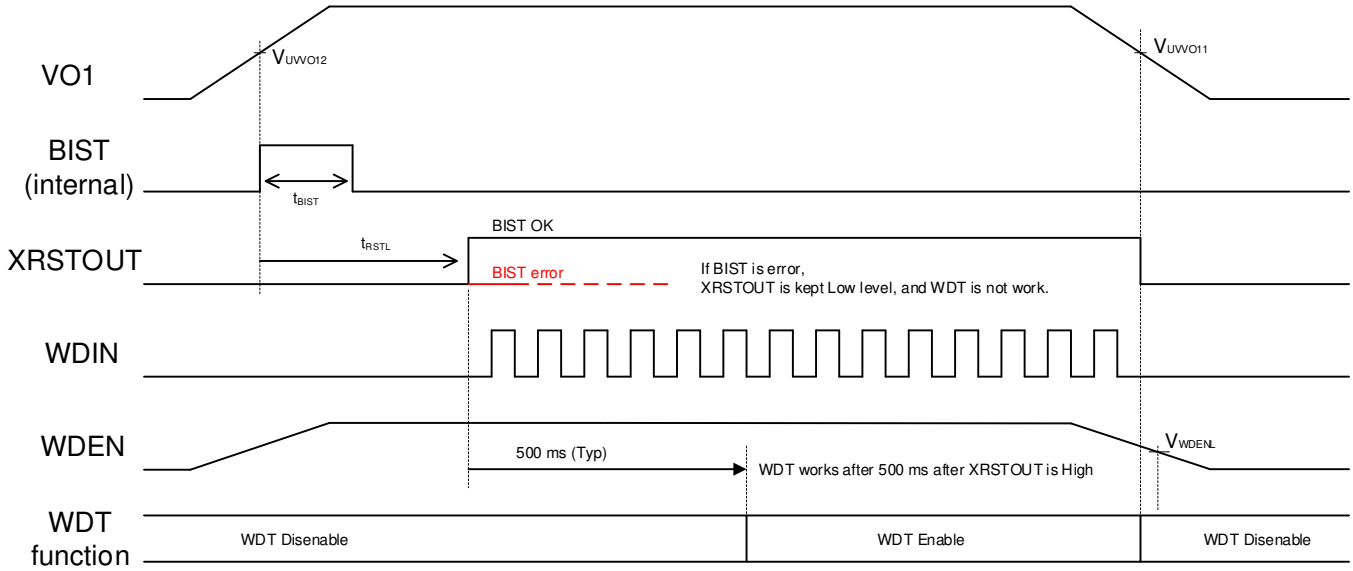
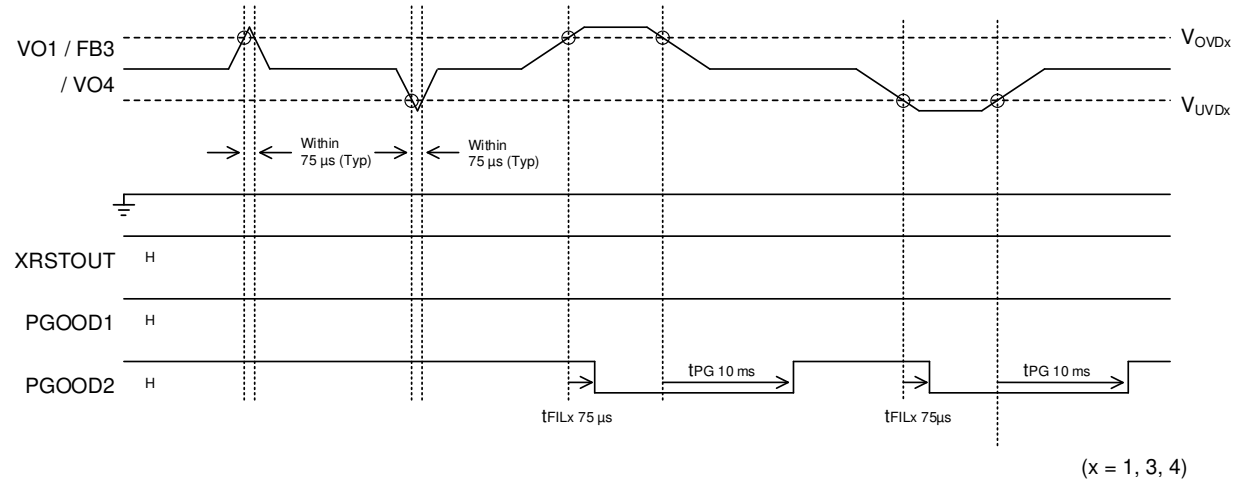


Figure 41. Timing Chart of WDEN tied to VO1

Timing Chart - continued

BUCK1/BUCK3/BOOST4 OVD and UVD



BUCK2 OVD and UVD

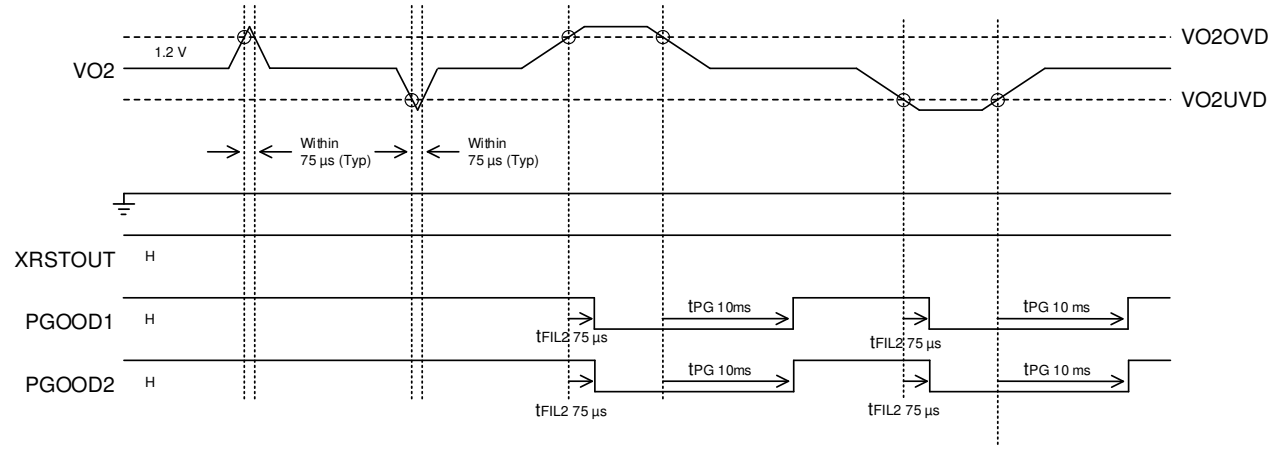
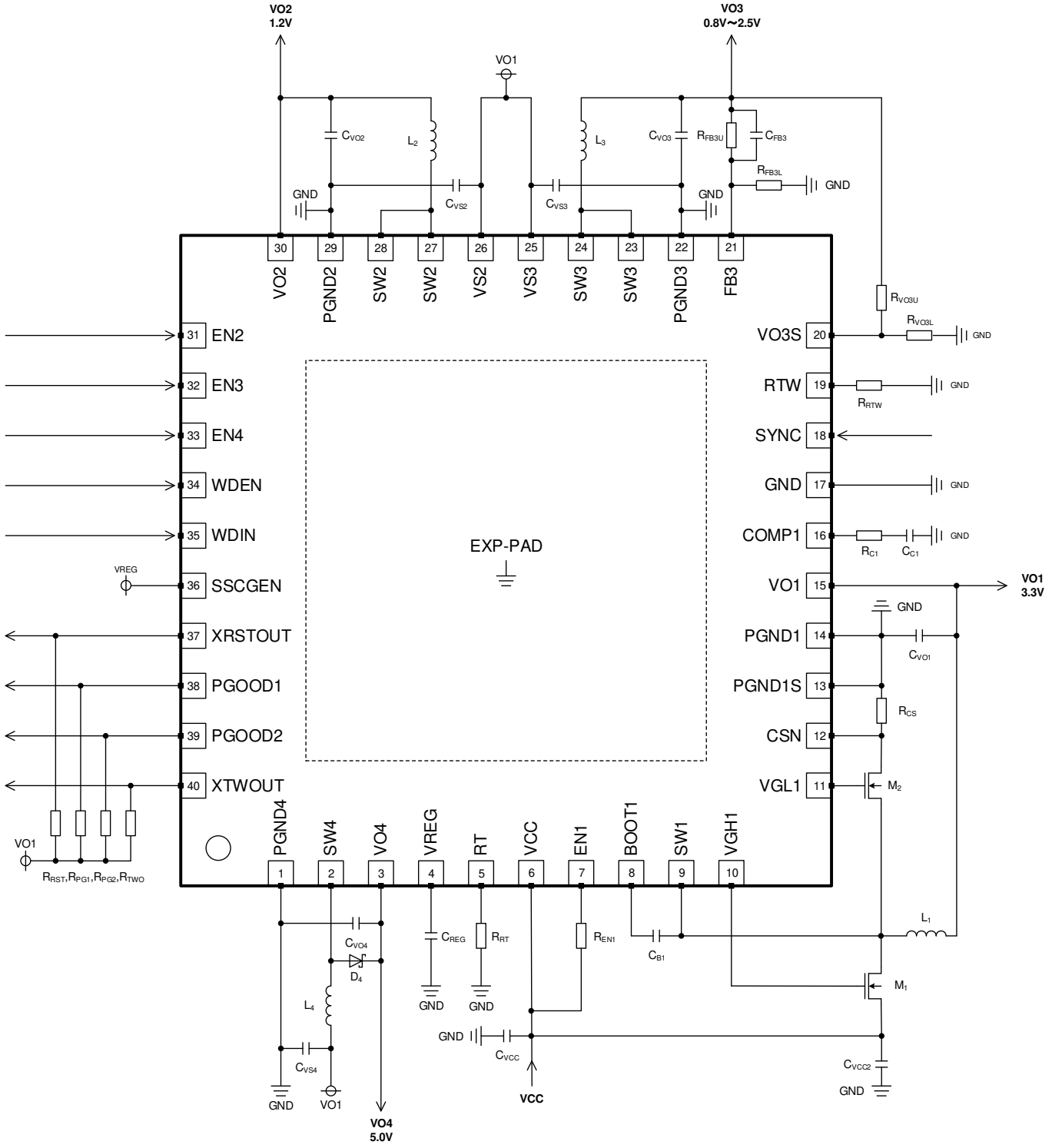


Figure 42. Timing Chart of OVD/UVD Detect

Application Example



Selection of Components Externally Connected

Item	Value			unit	Parts No.	Maker	Note
	Min (Note 1)	Typ	Max (Note 2)				
IC	-	-	-	-	BD39031MUF-C	ROHM	
R_{EN1}	9.7	10	100	kΩ	MCR01 series	ROHM	EN1 pull up resistor
R_{C1}	32	33	34	kΩ	MCR01 series	ROHM	VO1 compensation resistor
R_{CS}	8.7	9	15	mΩ	PMR18EZPJU9L0	ROHM	VO1 current sense resistor
R_{FB3U}	1	13	47	kΩ	MCR01 series	ROHM	VO3 feedback resistor (Upper side)
R_{FB3L}	1	15	47	kΩ	MCR01 series	ROHM	VO3 feedback resistor (Lower side)
R_{VO3U}	1	13	47	kΩ	MCR01 series	ROHM	VO3 sense resistor (Upper side)
R_{VO3L}	1	15	47	kΩ	MCR01 series	ROHM	VO3 sense resistor (Lower side)
R_{RT}	8.8	9.1	9.4	kΩ	MCR01 series	ROHM	Switching frequency setting resistor
R_{RTW}	9.7	27	48.5	kΩ	MCR01 series	ROHM	WDT detection time setting resistor
R_{RST}	0.97	10	48.5	kΩ	MCR01 series	ROHM	XRSTOUT pull up resistor
R_{PG1}	0.97	10	48.5	kΩ	MCR01 series	ROHM	PGOOD1 pull up resistor
R_{PG2}	0.97	10	48.5	kΩ	MCR01 series	ROHM	PGOOD2 pull up resistor
R_{TWO}	0.97	10	48.5	kΩ	MCR01 series	ROHM	XTWOUT pull up resistor
C_{VCC}	0.7	1	1.5	µF	GCM21BR71H105MA03	Murata	VCC input capacitor, Range: 50 V
C_{VCC2}	7	10	22	µF	GCM32EC71H106KA03	Murata	VCC input capacitor, Range: 50 V
C_{REG}	1.54	2.2	2.86	µF	GCM21BR71A225MA37	Murata	VREG5 output capacitor, Range: 10 V
C_{B1}	0.07	0.1	0.13	µF	GCM188R71C104MA37	Murata	VO1 boot strap capacitor, Range : 16 V
C_{C1}	840	1200	1560	pF	GCM155R71H122KA37	Murata	VO1 phase compensation capacitor
C_{VO1}	47 x3	47 x4	47 x8	µF	GCM32ER70J476ME19	Murata	VO1 output capacitor, Range: 6.3 V
C_{VS2}	1.5	2.2	4.3	µF	GCM188R70J225ME22	Murata	VO2 input capacitor, Range: 6.3 V
C_{VO2}	32.9	47	122	µF	GCM32ER70J476ME19	Murata	VO2 output capacitor, Range: 6.3 V
C_{VS3}	1.5	2.2	4.3	µF	GCM188R70J225ME22	Murata	VO3 input capacitor, Range: 6.3 V
C_{FB3}	154	220	286	pF	GCM155R71H221KA37	Murata	VO3 feedback capacitor
C_{VO3}	32.9	47	122	µF	GCM32ER70J476ME19	Murata	VO3 output capacitor: 6.3 V
C_{VS4}	1.5	2.2	4.3	µF	GCM188R70J225ME22	Murata	VO4 input capacitor: 6.3 V
C_{VO4}	15.4	22	43	µF	GCM31CR71A226KE02	Murata	VO4 output capacitor: 10 V
L_1	1.0	1.5	2.9	µH	CLF10060NIT-1R5N-D	TDK	VO1 output coil
L_2	1.5	2.2	4.3	µH	CLF5030NIT-2R2N-D	TDK	VO2 output coil
L_3	1.5	2.2	4.3	µH	CLF5030NIT-2R2N-D	TDK	VO3 output coil
L_4	1.5	2.2	4.3	µH	CLF5030NIT-2R2N-D	TDK	VO4 output coil
D_4	-	-	-	-	RBR2LAM30ATF	ROHM	VO4 SBD, Range: 30 V/2 A, VF = 0.49 V
M_1, M_2	-	-	-	-	FDMC9430L-F085 NVMFD5C466NL	ON Semicon-ductor	Dual Nch FET, 40 V / 12 A Dual Nch FET, 40 V / 52 A

(Note 1) Consider torerance, temperature characteristic and DC bias properties not to become less than the minimum.
(Note 2) Consider torerance and temperature characteristic not to become less than the maximum.

Selection of Components Externally Connected - continued

1. Selection of Inductor L Value (BUCK1, BUCK2, BUCK3, BOOST4)

When the switching regulator supplies current continuously to the load, the LC filter is necessary for the smoothness of the output voltage. The inductor value to use is selectable from the following.

BUCK1: L_1	1.5 µH, 2.2 µH
BUCK2: L_2	2.2 µH, 3.3 µH
BUCK3: L_3	2.2 µH, 3.3 µH
BOOST4: L_4	2.2 µH, 3.3 µH

It is necessary for the rating current of the inductor to choose enough margins for the peak current. The inductor peak current of Buck converter can be approximated by the following equation.

Peak current $I_{PEAKBUCK}$ of BUCK1, BUCK2, BUCK3

$$\Delta I_{LBUCK} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{\mathrm{L} \times f_{SW} \times V_{IN}} \quad [\mathrm{A}]$$

$$I_{PEAKBUCK} = I_{OUT} + \frac{1}{2} \times \Delta I_{LBUCK} \quad [\mathrm{A}]$$

Where:

ΔI_{LBUCK}	is inductor ripple current of buck converter.
V_{IN}	is input voltage.
V_{OUT}	is output voltage.
f_{SW}	is switching frequency.
L	is inductor value.

The inductor peak current of boost converter can be approximated by the following equation.

Peak current $I_{PEAKBOOST}$ of BOOST4

$$\Delta I_{LBOOST} = \frac{V_{IN}}{\mathrm{L} \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad [\mathrm{A}]$$

$$I_{LAVE} = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \eta} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad [\mathrm{A}]$$

$$I_{PEAKBOOST} = I_{LAVE} + \frac{1}{2} \times \Delta I_{LBOOST} \quad [\mathrm{A}]$$

Where:

ΔI_{LBOOST}	is inductor ripple current of boost converter.
I_{LAVE}	is average current of boost converter.
V_{IN}	is input voltage.
V_{OUT}	is output voltage.
I_{OUT}	is output current.
f_{SW}	is switching frequency.
L	is inductor value.
η	is efficiency.

Selection of Components Externally Connected – continued

2. Selection of Output Capacitor Value (C_{VO1}, C_{VO2}, C_{VO3}, C_{VO4})

The output capacitor is selected on the basis of ESR that is required from the ripple voltage can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. The ceramic capacitor contributes to the size reduction of the application for it has small ESR. Frequency characteristic of ESR should be confirmed from the datasheet of the manufacturer to choose low ESR value in the switching frequency being used. It is necessary to consider the ceramic capacitor because the DC biasing characteristic is remarkable. For the voltage rating of the ceramic capacitor, twice or more the maximum output voltage is usually required. By selecting these high voltages rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R or more is recommended. Because the voltage rating of a mass ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, it is recommended to connect ceramic capacitors in parallel, or to use hybrid electrolytic capacitor.

The value of output capacitor to use is selectable in the following.

BUCK1: C_{VO1}	47 µF x4 to 47 µF x6
BUCK2: C_{VO2}	47 µF to 94 µF
BUCK3: C_{VO3}	47 µF to 94 µF
BOOST4: C_{VO4}	22 µH to 33 µF

These capacitors are rated in ripple current.
The RMS values of the ripple current that can be obtained from the following equation must not exceed the ripple current ratings.

$$I_{COBUCK(RMS)} = \frac{\Delta I_{LBUCK}}{\sqrt{12}} \quad [A]$$

Where:

$I_{COBUCK(RMS)}$ is RMS value of the buck converter output ripple current.
ΔI_{LBUCK} is ripple current of buck converter.

$$D_{BOOST} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

$$I_{COBOOST(RMS)} = \sqrt{(1 - D_{BOOST}) \times \left(I_{OUT}^2 \times \frac{D_{BOOST}}{(1-D_{BOOST})^2} + \frac{\Delta I_{LBOOST}{}^2}{3}\right)} \quad [A]$$

Where:

$I_{COBOOST(RMS)}$ is RMS value of the boost converter output ripple current.
D_{BOOST} is duty cycle of boost converter.
V_{IN} is input voltage.
V_{OUT} is output Voltage.
I_{OUT} is output current.
ΔI_{LBOOST} is inductor ripple current of boost converter.

Selection of Components Externally Connected – continued

3. Selection of Input Capacitor (C_{VCC}, C_{VCC2}, C_{VS2}, C_{VS3}, C_{VS4})

The Input capacitor is required to stabilize ripple voltage of the supplied power supply and is necessary to supply current in the on time for FET. The ceramic capacitor with low ESR is necessary for input capacitor. The C_{VCC} has to be connected near the IC for the stabilization of the power supplied to the analog block of the IC.
The value of input capacitor to use is selectable from the following ranges.

VCC : C_{VCC}	1.0 µF
BUCK1 : C_{VCC2}	10 µF
BUCK2 : C_{VS2}	2.2 µF to 3.3µF
BUCK3 : C_{VS3}	2.2 µF to 3.3µF
BOOST4 : C_{VS4}	2.2 µF to 3.3µF

These capacitors are rated in ripple current.
The RMS values of the ripple current that can be obtained in the following equation must not exceed the ripple current ratings.
The RMS value of the input ripple electric current is obtained in the following equation.

$$I_{CCBUCK(RMS)} = I_{O1(MAX)} \times \sqrt{D_{BUCK} \times (1 - D_{BUCK})} \quad [A]$$

Where:

$I_{CCBUCK(RMS)}$ is RMS value of the VCC input current.
$I_{O1(MAX)}$ is max output current.
D_{BUCK} is duty cycle of buck converter.

The RMS value of the input ripple current is obtained in the following equation.

$$I_{CCBOOST(RMS)} = \frac{\Delta I_{LBOOST}}{\sqrt{12}} = \frac{1}{\sqrt{12}} \times \frac{V_{IN}}{L \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad [A]$$

Where:

$I_{CCBOOST(RMS)}$ is RMS value of the VCC input ripple electric current.
ΔI_{LBOOST} is ripple current of boost.
V_{IN} is input voltage.
V_{OUT} is output Voltage.
f_{SW} is switching frequency.

In addition, in automotive and other applications requiring high reliability, it is recommended by making it into two series + two parallel structures to decrease the risk of ceramic capacitor destruction due to short circuit conditions. “Two series + two parallel structure in 1 package” lineups are respectively carried out by each capacitor supplier, confirm to each supplier for details.

When impedance on the input side is high because of long wiring from the power supply to VCC etc., high capacitance is needed. It is necessary to verify IC operation in actual condition for problem such as output turning off or output overshooting causes by change in VCC at transient response may occur.

Selection of Components Externally Connected - continued

4. FET (M1, M2)

The selection of MOSFET affects the efficiency of BUCK1. This product recommends the following MOSFET.

Parts No.	Maker	Channel	Pole	V_{DS}	I_D
FDMC9430L-F085	ON Semiconductor	Dual	N-Channel	40 V	12 A
NVMFD5C466NL	ON Semiconductor	Dual	N-Channel	40 V	52 A

In the selection of MOSFET, please give enough consideration for following contents.
- Drain – Source Rating
- Gate – Source Rating
- Drain Current
- Power Dissipation

Drain – Source Rating
It is recommended to select MOSFET with enough margins to be used for power supply range (VCC).

Gate - Source Rating
It is recommended to use MOSFET with more than 10 V of gate source rating.

Drain Current
Choose FET with more than the setting of either $I_{PEAKBUCK}$ or OCP for drain current.

Power Dissipation
Power consumption is calculated on a true specifications condition, and prevents from exceeding maximum allowable power consumption. Synchronization can roughly estimate the loss of commutation type MOSFET by the factor shown below.

(1) Loss of MOSFET ON Resistance
(2) Loss of Switching
(3) Loss of Output Capacitor
(4) Loss of Dead Time
(5) Loss of Gate Charge

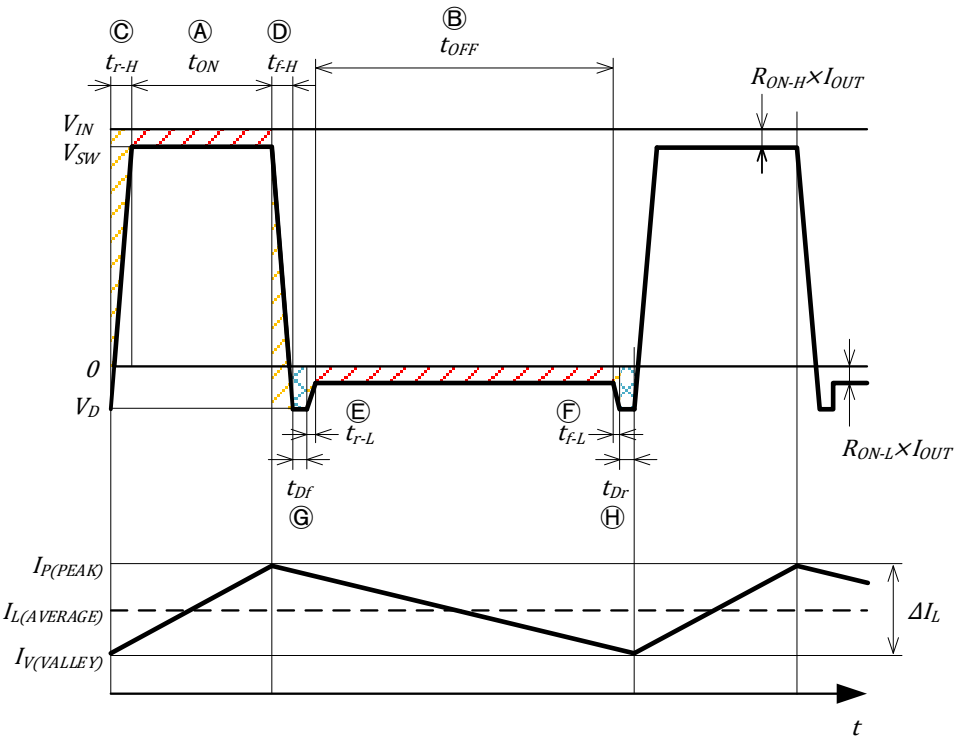


Figure 43. Relation between Switching Waveform and Loss

FET (M1, M2) - continued

(1) Loss of MOSFET ON Resistance

The conduction loss of the MOSFET is calculated in A section and B section of Figure 43.
High side MOSFET turns on the A section and turns off low side MOSFET, and it can be roughly estimated by output current, ON resistance, and on duty cycle.
High side MOSFET turns off the B section and low side MOSFET becomes ON, and it can be roughly estimated from output current, ON resistance and off duty cycle.
Power loss P_{ON-H} and P_{ON-L} are calculated by the following formula.

High side MOSFET

$$P_{ON-H} = \left[I_{OUT}^{2} + \frac{{\Delta I_L}^2}{12}\right] \times R_{ON-H} \times \frac{V_{OUT}}{V_{IN}} \quad [W]$$

Low Side MOSFET

$$P_{ON-L} = \left[I_{OUT}^{2} + \frac{{\Delta I_L}^2}{12}\right] \times R_{ON-L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad [W]$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \quad [A]$$

Where:

I_{OUT}	is output current.
R_{ON-H}	is on resistance of high side MOSFET.
R_{ON-L}	is on resistance of low side MOSFET.
V_{IN}	is input voltage.
V_{OUT}	is output voltage.
ΔI_L	is inductor ripple current of inductor.
f_{SW}	is switching frequency.
L	is Inductor value.

(2) Loss of Switching

The switching loss can be calculated by C, D, E, and F section of Figure 43.
When a high side and low side MOSFET switches ON/OFF in turn, a loss occurs during the transition to ON.
Because the formula for two triangular areas resembles a calculating formula of the power attenuation during a start and fall transition, this calculation can be approximated by a simple figure calculation.
Switching loss P_{SW-H} is demanded by following formula.

High side MOSFET

$$P_{SW-H} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times \left(t_{r-H} + t_{f-H}\right) \times f_{SW} \quad [W]$$

Where:

V_{IN}	is input voltage.
I_{OUT}	is output current.
t_{r-H}	is rise time of MOSFET.
t_{f-H}	is fall time of MOSFET.
f_{SW}	is switching frequency.

When low side MOSFET turns on by gate voltage which electricity runs through body diode and then turns off by gate voltage, drain voltage becomes equal to forward direction voltage of body diode and remains as low voltage, because load current flows in same direction through body diode. Therefore, switching loss P_{SW-L} is very few like in following formula.

loss of Switching - continued

Low side MOSFET

$$P_{SW-L} = \frac{1}{2} \times V_D \times I_{OUT} \times \left(t_{r-L} + t_{f-L}\right) \times f_{SW} \quad [W]$$

Where:

V_D	is forward voltage of body diode of low side MOSFET.
I_{OUT}	is output current.
t_{r-L}	is rise time of MOSFET.
t_{f-L}	is fall time of MOSFET.
f_{SW}	is switching frequency.

(3) Loss of Output Capacitor

A loss occurs when charging output capacitance C_{OSS} of high side and low side MOSFET in each switching cycle. This loss is demanded by following formula.

$$P_{COSS} = \frac{1}{2} \times (C_{OSS-L} + C_{OSS-H}) \times V_{IN}^2 \times f_{SW} \quad [W]$$

$$C_{OSS-L} = C_{DS-L} + C_{GD-L} \quad [F]$$

$$C_{OSS-H} = C_{DS-H} + C_{GD-H} \quad [F]$$

Where:

C_{OSS-L}	is output capacitance of low side MOSFET.
C_{DS-L}	is capacitance between drain and source of low side MOSFET.
C_{GD-L}	is capacitance between gate and drain of low side MOSFET.
C_{OSS-H}	is output capacitance of high side MOSFET.
C_{DS-H}	is capacitance between drain and source of high side MOSFET.
C_{GD-H}	is capacitance between gate and drain of high side MOSFET.
V_{IN}	is input voltage.
f_{SW}	is switching frequency.

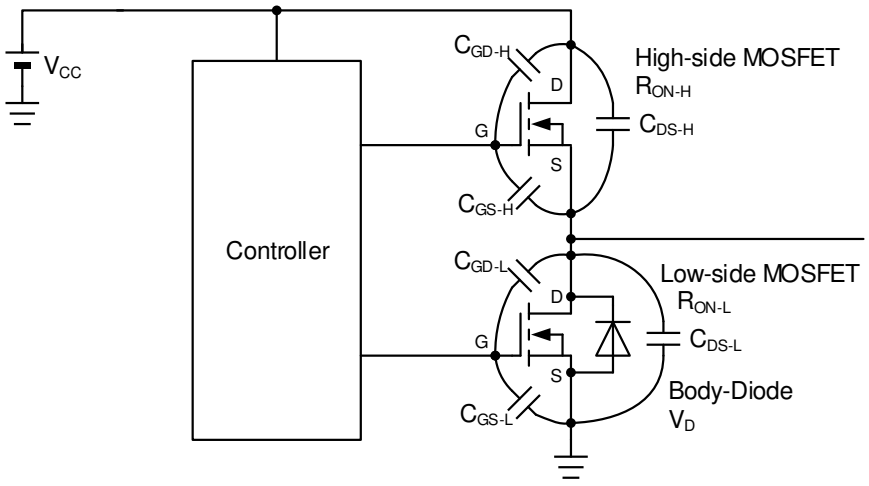


Figure 44. Synchronized Rectifier type DCDC Converter Circuit Diagram

FET (M1, M2) - continued

(4) Loss of Dead Time
When a high side and low side MOSFET are turned on at the same time, VIN-GND interval shorts circuit and a very big current spike will occur. The dead time which turns off both MOSFET is made to prevent this, but the inductor electric current flows continuously. This inductor electric current flows in a body diode of low side MOSFET during dead time. Dead time loss P_D is calculated in G section and H section of Figure 43 and is demanded by the following formula.

$$P_D = V_D \times I_{OUT} \times \left(t_{Dr} + t_{Df}\right) \times f_{SW} \quad [\mathrm{W}]$$

Where:

V_D	is forward voltage of body diode of low side MOSFET.
I_{OUT}	is output current.
t_{Dr}	is dead time at rise.
t_{Df}	is dead time at fall.
f_{SW}	is switching frequency.

(5) Loss of Gate Charge
A gate charge loss is power attenuation due to the charge of the gate of MOSFET. Depending on quantity of gate charge of a high side and the low side MOSFET (or gate capacitance), the gate charge loss is demanded by following formula.

$$P_G = \left(Q_{g-H} + Q_{g-L}\right) \times V_{gs} \times f_{SW} \ [\mathrm{W}]$$

or

$$P_G = (C_{GS-H} + C_{GS-L}) \times {V_{gs}}^2 \times f_{SW} \quad [\mathrm{W}]$$

Where:

Q_{g-H}	is gate charge of high side MOSFET.
Q_{g-L}	is gate charge of low side MOSFET.
C_{GS-H}	is capacitance between gate and source of high side MOSFET.
C_{GS-L}	is capacitance between gate and source of low side MOSFET.
V_{gs}	is gate drive voltage.
f_{SW}	is switching frequency.

All power loss of the MOSFET
Power loss P of the MOSFET is the value that added all these.

$$P = P_{ON-H} + P_{ON-L} + P_{SW-H} + P_{SW-L} + P_{COSS} + P_D + P_G \quad [\mathrm{W}]$$

Where:

P_{ON-H}	is high side MOSFET on resistance loss.
P_{ON-L}	is low side MOSFET on resistance loss.
P_{SW-H}	is high side MOSFET switching loss.
P_{SW-L}	is low side MOSFET switching loss.
P_{COSS}	is MOSFET output capacitance loss.
P_D	is dead time loss.
P_G	is gate charge loss.

5. BOOT1 Capacitor (C_{B1})
C_{B1} is a capacitor between BOOT1 and SW1. The voltage between BOOT1 and SW1 will be almost the same as voltage between VREG and GND. Ceramic capacitor with capacity of 0.1 µF is recommended for capacitor C_{B1}. Moreover, in order to maintain good temperature characteristics, capacitor with a characteristic of X7R or more is recommended.

6. VREG Capacitor (C_{REG})
C_{REG} is a capacitor between VREG and internal block. Ceramic capacitor with capacity of 2.2 µF is recommended for the VREG pin.

Selection of Components Externally Connected - continued

7. Switching Frequency Setting Resistor (R_{RT})
R_{RT} is a resistor to set switching frequency of BUCK1, BUCK2, BUCK3, and BOOST4. The resistor value is 9.1 kΩ.

8. WDT Timeout Setting Resistor (R_{RTW})
R_{RTW} is a resistor to set timeout of Watch Dog Timer.
The range of R_{RTW} is from 10 kΩ to 47 kΩ.
Details for setting R_{RTW} is describe in page 15.

9. Current Detection Resistor of BUCK1 (R_{CS})
The R_{CS} resistor sets the level of the over current protection of BUCK1. The level of the over current protection is decided in an expression below.

$$I_{OCP} = \frac{75mV(Typ)}{R_{CS}} \quad [A]$$

Because high current flows in R_{CS}, the resistor with enough margin must be selected for rating current and allowable power. It is recommended to use resistor of PMR series for current detection resistor.

10. Pull-up Resistor for Open Drain Output (R_{RST}, R_{PG1}, R_{PG2}, R_{TWO})
The XRSTOUT, PGOOD1, PGOOD2, and XTWOUT pins are the N-channel open drain output.
These pins are used to pull-up resistor to VO1 or to other power supplies. The range of resistor value is 1 kΩ to 47 kΩ.

11. Selection of Schottky Barrier Diode (SBD) (D_4)
It is necessary to use Schottky barrier diode to realize high efficiency.
Please select suitable Schottky barrier diode considering the following contents enough.

The maximum rating of reverse voltage must have enough margin against maximum output voltage of VO4.
In additional, current rating of SBD is necessary for peak forward current I_{DPEAK}.
Peak forward current I_{DPEAK} is defined by following expression.

$$I_{DPEAK} = \frac{I_{OUT}}{(1-D_{BOOST})} + \frac{\Delta I_{LBOOST}}{2} = \frac{I_{OUT}}{(1-D_{BOOST})} + \frac{1}{2} \times \left[\frac{V_{IN}}{\mathrm{L} \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)\right] \quad [A]$$

Where:

I_{OUT}	is output current.
D_{BOOST}	is duty cycle of boost converter.
ΔI_{LBOOST}	is inductor ripple current.
V_{IN}	is input voltage. (= VO1 voltage)
V_{OUT}	is output voltage.

The forward average rectify current is equal to output current I_{OUT}
The power loss of SBD can be approximated by the following equation.

$$P_{DIODE} = I_{OUT} \times V_F \times \frac{V_{IN}}{V_{OUT}} \quad [W]$$

Where:

P_{DIODE}	is power loss of SBD.
I_{OUT}	is output current.
V_F	is forward voltage of SBD.
V_{IN}	is input voltage. (= VO1 voltage)
V_{OUT}	is output voltage.

Selection of Components Externally Connected - continued

12. Phase Compensation (BUCK1)

High response characteristic can be achieved by setting total gain zero cross frequency f_C (Gain 0 dB frequency) high. However, give consideration that responsiveness and the stability are in relation of trade-off. Switching regulator application are sampled by switching frequency. In order to sustain gain at switching frequency, zero cross frequency should be set lower than 1/2 to 1/10 of the switching frequency. In general, the characteristics which application design must target are;

150˚ or less (phase margin 30˚ or more) phase delay at Gain 1 (0 dB)

Zero cross frequency to be lower than 1/2 to 1/10 of the switching frequency.

To increase the response characteristic, zero cross frequency must be higher.

BUCK1 phase compensation is set by capacitor and resistor between the COMP1 pin and Ground. (BUCK2, BUCK3, and BOOST4 have phase compensation network of built-in COMP pins. No need for adjustment.)

Following values are the recommend value of phase compensation of BUCK1.

R_{C1}	33 kΩ
C_{C1}	1200 pF

Actual behavior will vary by several factors such as PCB layout, wiring, components, and usage condition (temp). It is necessary to verify the stability and response characteristic on the actual application. For frequency characteristic confirmation, gain phase analyzer or FRA will be used. Measurement method shall be checked with measurement equipment manufacturer.

13. VO3 Output Voltage Setting (BUCK3)

Output of VO3 can be calculated by following equation.

$$V_{O3} = 0.8\,V(Typ) \times \frac{R_{FB3U}+R_{FB3U}}{R_{FB3L}} \quad [V]$$

Output of VO1, VO2 and VO4 are fixed voltage.

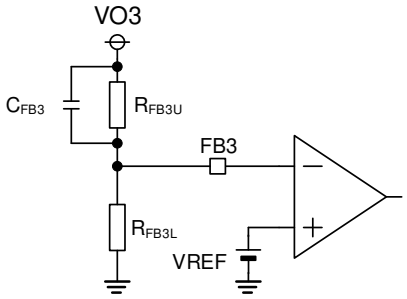


Figure 45. FB3 Feedback Circuit

Feedback resistor R_{FB3L} shall be set to 47 kΩ or less. Also low R_{FB3U}+ R_{FB3L} reduces efficiency, therefore set values that current through feedback resistor will be sufficiently lower than output current I_{OUT}.
The resistor recommended for output voltage setting must have high accuracy resistor of less than 1 %.
The resistor is connected near this IC, and is located so it is not affected by the noise of the SW1 pin.
Also, C_{FB3} is connected 220 pF to stabilize control system.

R_{VO3U} and R_{VO3L} resistor connected to the VO3S pin sets the overvoltage detection level of BUCK3. The reason of separating pin is to protect IC with overvoltage detection from an error which may occur when the FB3 pin shorts GND. The resistor value of R_{VO3U}, R_{VO3L} are the same as R_{FB3U}, R_{FB3L}.

Selection of Components Externally Connected - continued

14. Selection of EN1 Resistor

When an alien substance causes short between pins, the EN1 pin may short-circuit with the VCC pin. In this case, the external components may exceed rating. When a countermeasure is necessary for above mentioned cases, insert resistance in the EN pin as shown in the following figure. The resistance value is 400 kΩ or less.

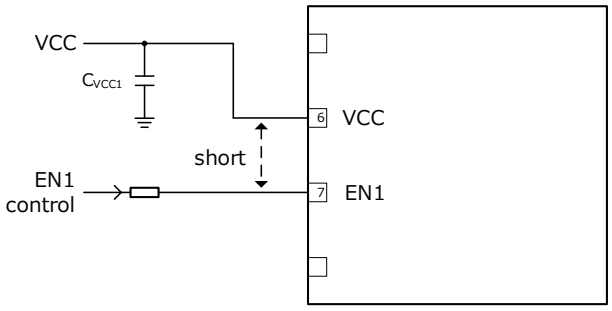


Figure 46. The EN1 Pin Resistor

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

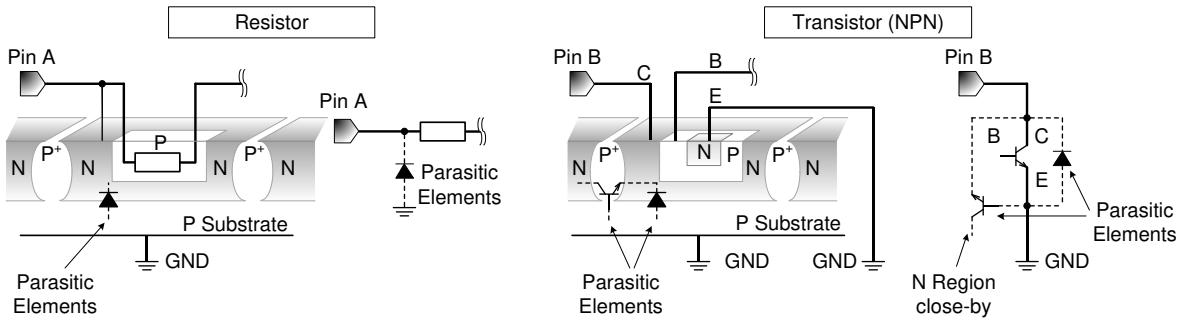


Figure 47. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

B	D	3	9	0	3	1	M	U	F	-	CE 2

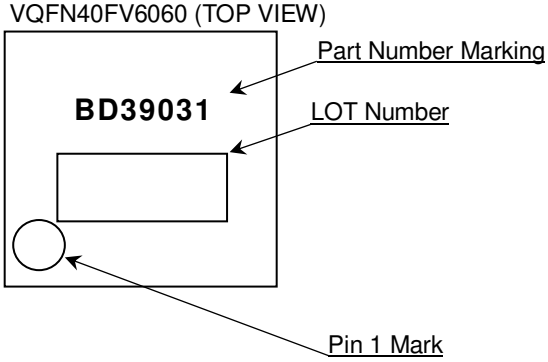
Part Number

Package
MUF: VQFN40FV6060

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

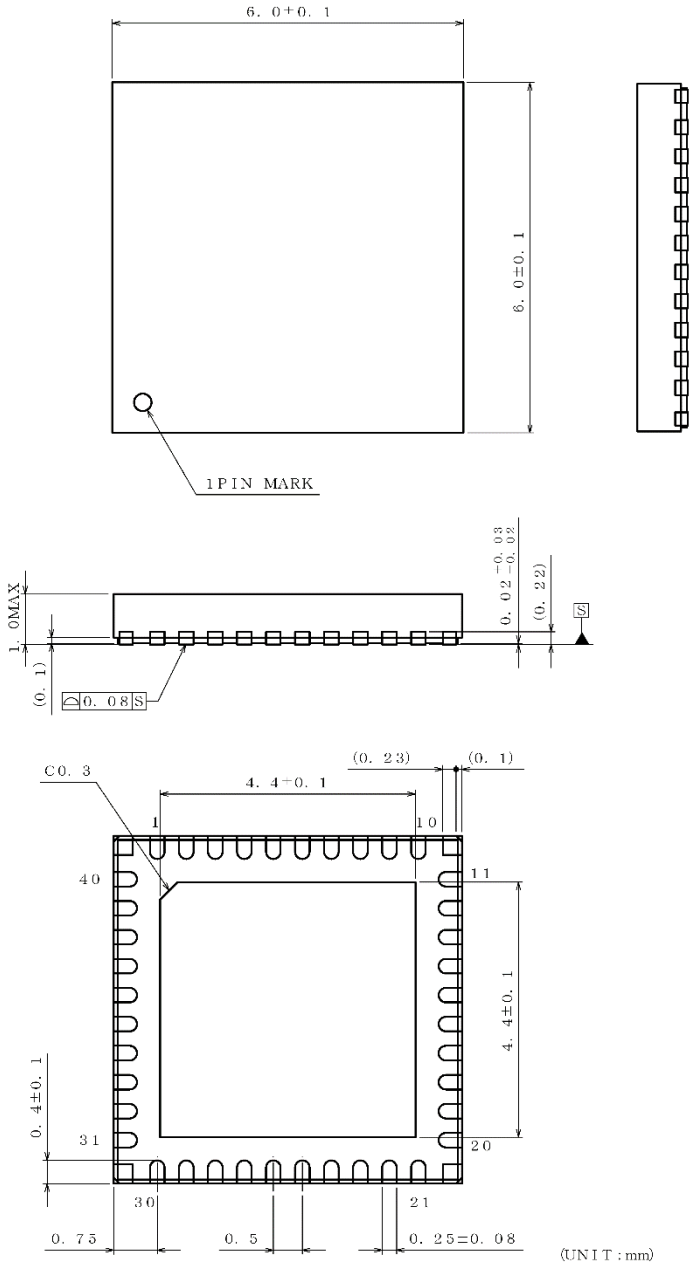
Marking Diagrams

VQFN40FV6060 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN40FV6060

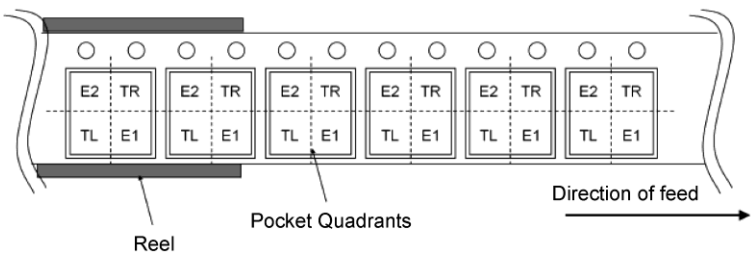


NOTE: Dimensions in ( ) for reference only.

PKG: VQFN40FV6060
Drawing No. EX406-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
05.Mar.2020	001	New Release

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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