FemtoClock® Crystal-to-3.3V, 2.5V CML Clock Generator

General Description

The 845254 is a 3.3V/2.5V CML clock generator designed for Ethernet applications. The device synthesizes either a 50MHz, 62.5MHz, 100MHz, 125MHz, 156.25MHz, 250MHz or 312.5MHz clock signal with excellent phase jitter performance. The clock signal is distributed to four low-skew differential CML outputs. The device is suitable for driving the reference clocks of Ethernet PHYs. The device supports 3.3V and 2.5V voltage supply and is packaged in a small, lead-free (RoHS 6) 32-lead VFQFN package. The extended temperature range supports telecommunication, wireless infrastructure and networking end equipment requirements.

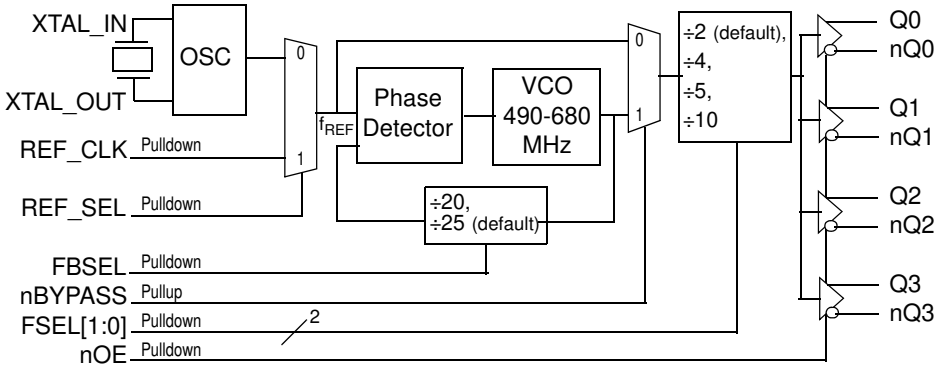
Features

- Clock generation of: 50MHz, 62.5MHz, 100MHz, 125MHz, 156.25MHz, 250MHz and 312.5MHz
- Four differential CML clock output pairs
- 25MHz reference clock (selectable internal crystal oscillator and external LVCMOS clock)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.405ps (typical)

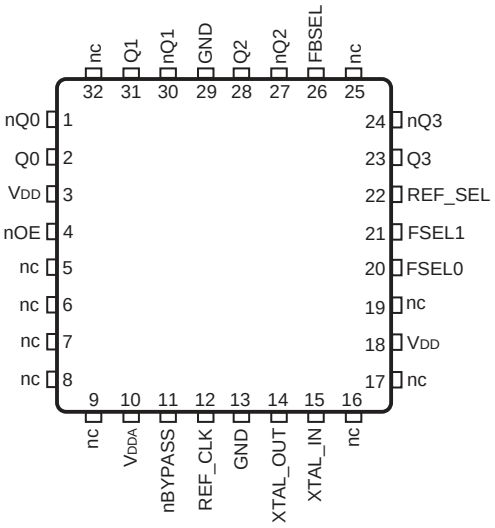
Offset	Noise Power
100Hz	-104.6 dBc/Hz
1kHz	-118.4 dBc/Hz
10kHz	-124.1 dBc/Hz
100kHz	-125.3 dBc/Hz

- LVCMOS interface levels for the control inputs
- Full 3.3V and 2.5V supply voltage
- Available in lead-free (RoHS 6) 32 VFQFN package
- -40°C to 85°C ambient operating temperature
- **Replacement part: 843002AYLF**

Block Diagram



Pin Assignment



845254
32 lead VFQFN
5.0mm x 5.0mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ0, Q0	Output		Differential clock output pair. CML interface levels.
3, 18	V_{DD}	Power		Core supply pins.
4	nOE	Input	Pulldown	Output enable pin. See Table 3E for function. LVCMOS/LVTTL interface levels.
5, 6, 7, 8, 9, 16, 17, 19, 25, 32	nc	Unused		Do not connect.
10	V_{DDA}	Power		Analog supply pin.
11	nBYPASS	Input	Pullup	PLL bypass pin. See Table 3D for function. LVCMOS/LVTTL interface levels.
12	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
13, 29	GND	Power		Power supply ground.
14, 15	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
20, 21	FSEL0, FSEL1	Input	Pulldown	Output frequency divider select enable pins. See Table 3C for function. LVCMOS/LVTTL interface levels.
22	REF_SEL	Input	Pulldown	PLL reference clock select pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
23, 24	Q3, nQ3	Output		Differential clock output pair. CML interface levels.
26	FBSEL	Input	Pulldown	PLL feedback divider select pin. See Table 3B for function. LVCMOS/LVTTL interface levels.
27, 28	nQ2, Q2	Output		Differential clock output pair. CML interface levels.
30, 31	nQ1, Q1	Output		Differential clock output pair. CML interface levels.

NOTE: *Pulldown* and *pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. PLL Reference Clock Select Function Table

Input	
REF_SEL	**Operation**
0 (default)	The crystal interface is the selected reference clock.
1	The REF_CLK input is the selected reference clock.

NOTE: REF_SEL is an asynchronous control.

Table 3B. PLL Feedback Select Function Table

Input	
FBSEL	**Operation**
0 (default)	$f_{VCO} = f_{REF} * 25$
1	$f_{VCO} = f_{REF} * 20$

NOTE: FBSEL is an asynchronous control.

Table 3C. Output Divider Select Function Table

Input			Output Frequency f_{OUT} with f_{REF} = 25MHz	
FSEL1	**FSEL0**	**Operation**	**FBSEL = 0**	**FBSEL = 1**
0 (default)	0 (default)	$f_{OUT} = f_{VCO} \div 2$	312.5MHz	250MHz
0	1	$f_{OUT} = f_{VCO} \div 4$	156.25MHz	125MHz
1	0	$f_{OUT} = f_{VCO} \div 5$	125MHz	100MHz
1	1	$f_{OUT} = f_{VCO} \div 10$	62.5MHz	50MHz

NOTE: FSEL[1:0] are asynchronous controls.

Table 3D. PLL nBYPASS Function Table

Input	
nBYPASS	**Operation**
0	PLL is bypassed. The reference frequency f_{REF} is divided by the selected output divider. AC specifications do not apply in PLL bypass mode.
1 (default)	PLL is enabled. The reference frequency f_{REF} is multiplied by the selected feedback divider and then divided by the selected output divider.

NOTE: nBYPASS is an asynchronous control.

Table 3E. Output Enable Function Table

Input	
nOE	**Operation**
0 (default)	Outputs enabled.
1	Outputs disabled (high-impedance).

NOTE: nOE is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	43.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
I_{DD}	Power Supply Current				88	mA
I_{DDA}	Analog Supply Current				12	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	2.5	V_{DD}	V
I_{DD}	Power Supply Current				84	mA
I_{DDA}	Analog Supply Current				11	mA

Table 4C. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	FBSEL, nOE, FSEL[1:0], REF_SEL, REF_CLK	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		nBYPASS	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	FBSEL, nOE, FSEL1:0, REF_SEL, REF_CLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nBYPASS	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 4D. CML DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage		V_{DD} - 0.025	V_{DD} - 0.01	V_{DD}	V
V_{OUT}	Output Voltage Swing		300	450	600	mV
V_{DIFF_OUT}	Differential Output Voltage Swing		600	900	1200	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

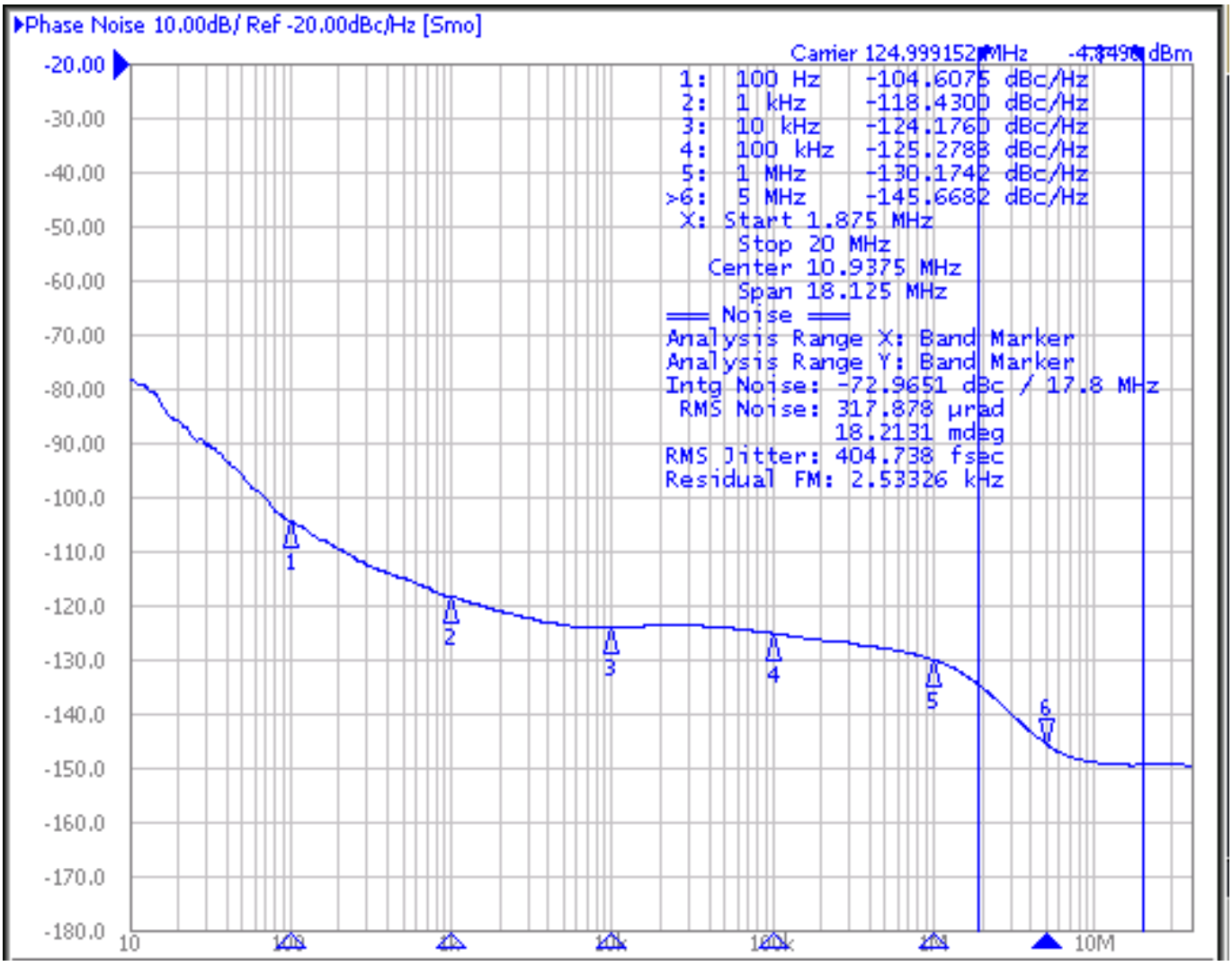
AC Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

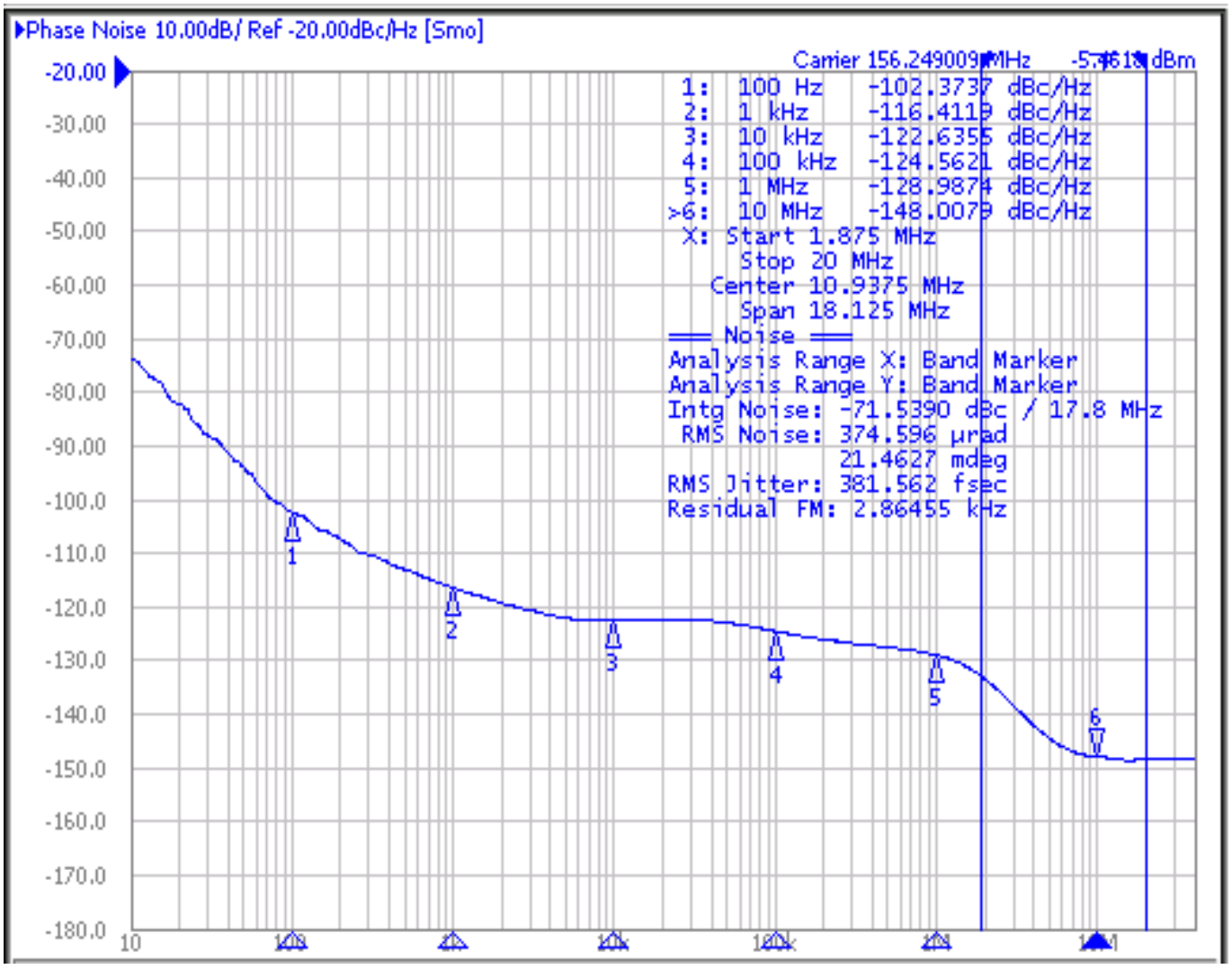
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency; NOTE 1	FBSEL = 0, FSEL[1:0] = 00		312.5		MHz
		FBSEL = 0, FSEL[1:0] = 01		156.25		MHz
		FBSEL = 0, FSEL[1:0] = 10		125		MHz
		FBSEL = 0, FSEL[1:0] = 11		62.5		MHz
		FBSEL = 1, FSEL[1:0] = 00		250		MHz
		FBSEL = 1, FSEL[1:0] = 01		125		MHz
		FBSEL = 1, FSEL[1:0] = 10		100		MHz
		FBSEL = 1, FSEL[1:0] = 11		50		MHz
tsk(o)	Output Skew; NOTE 1, 2, 3				65	ps
$t_{jit}(Ø)$	RMS Phase Jitter (Random); NOTE 4	3.3V, f_{OUT} = 125MHz, Integration Range: 1.875MHz – 20MHz		0.405		ps
		3.3V, f_{OUT} = 156.25MHz, Integration Range: 1.875MHz – 20MHz		0.381		ps
		2.5V, f_{OUT} = 125MHz, Integration Range: 1.875MHz – 20MHz		0.400		ps
		2.5V, f_{OUT} = 156.25MHz, Integration Range: 1.875MHz – 20MHz		0.401		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		800	ps
odc	Output Duty Cycle	FSEL[1:0] = 10	45		55	%
		FSEL[1:0] ≠ 10	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using an 18pF, 25MHz crystal.
NOTE 1: f_{REF} = 25MHz.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Please refer to the phase noise plots.

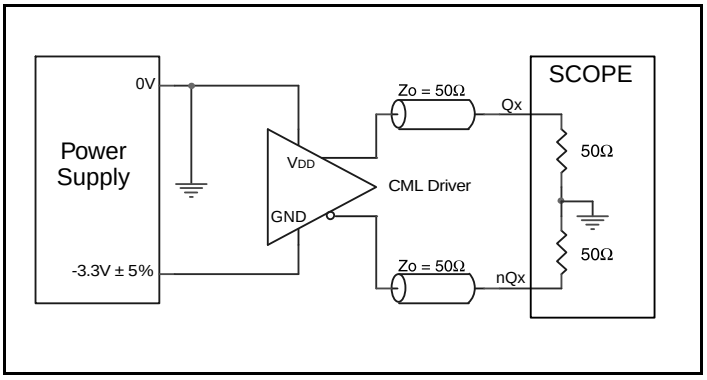
Typical Phase Noise at 125MHz (3.3V)



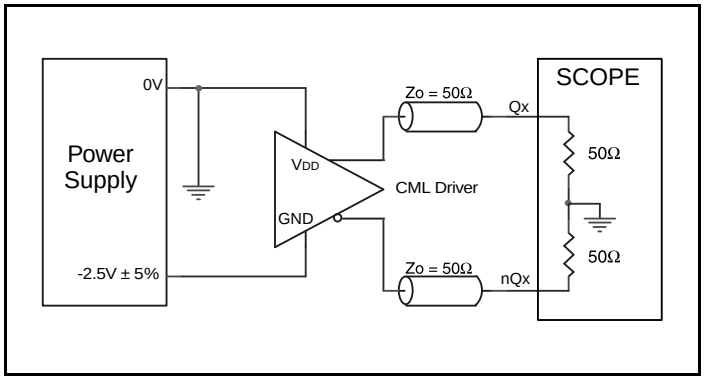
Typical Phase Noise at 156.25MHz (3.3V)



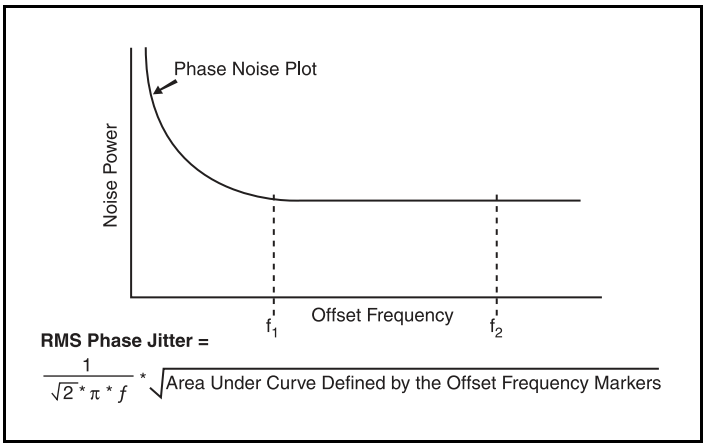
Parameter Measurement Information



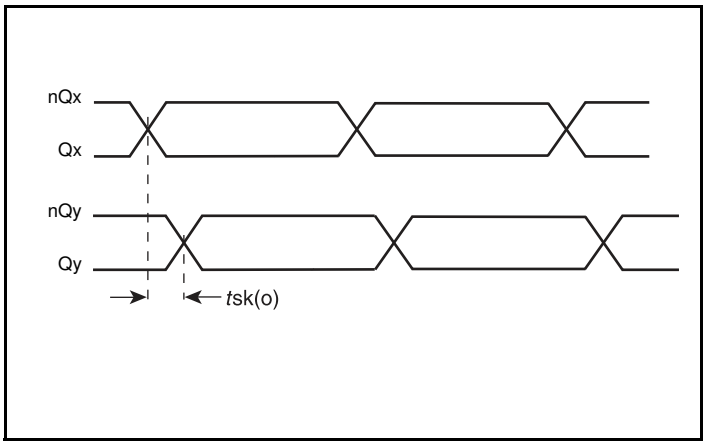
3.3V CML Output Load AC Test Circuit



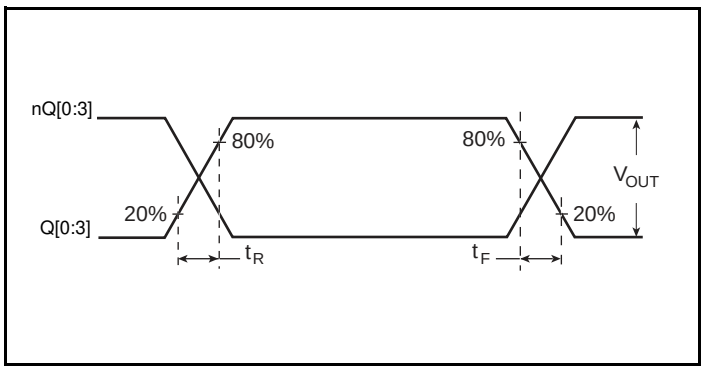
2.5V CML Output Load AC Test Circuit



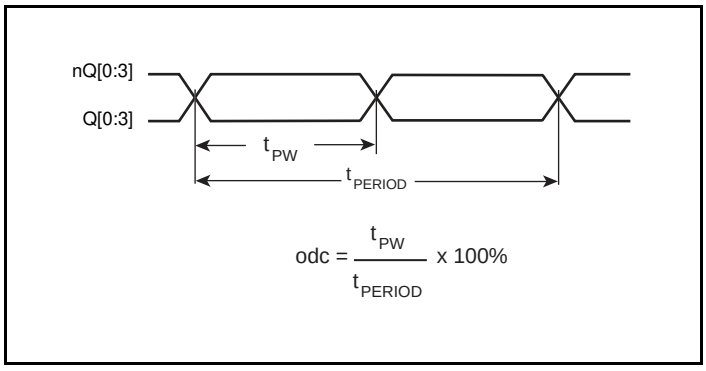
RMS Phase Jitter



Output Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 845254 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

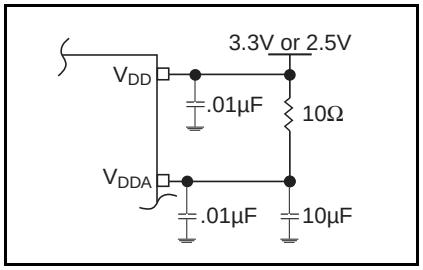


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Outputs:

CML Outputs

All unused CML outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 845254 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

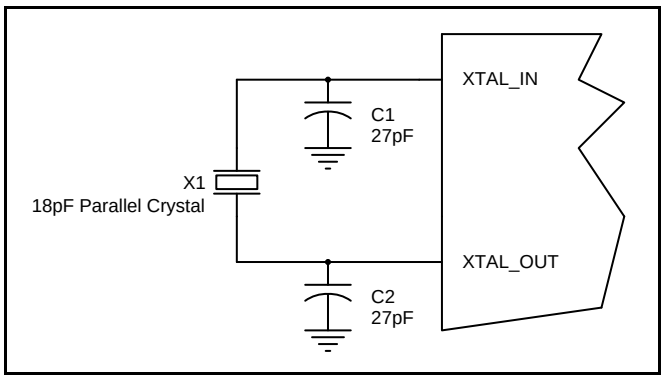


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

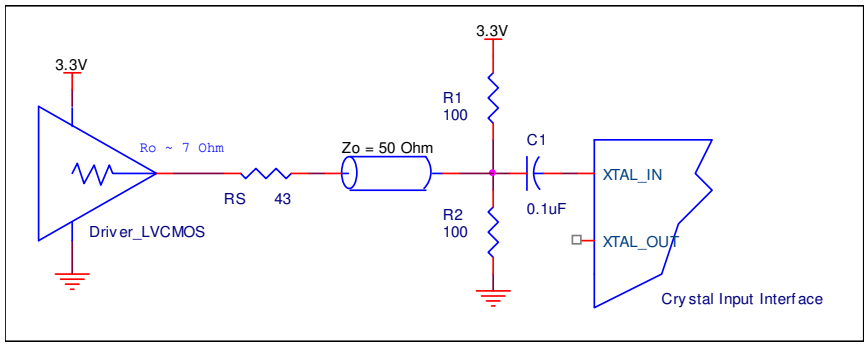


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

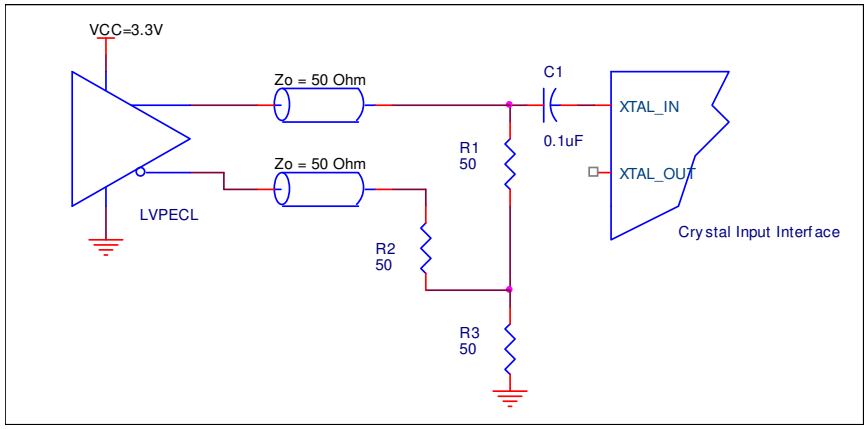


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

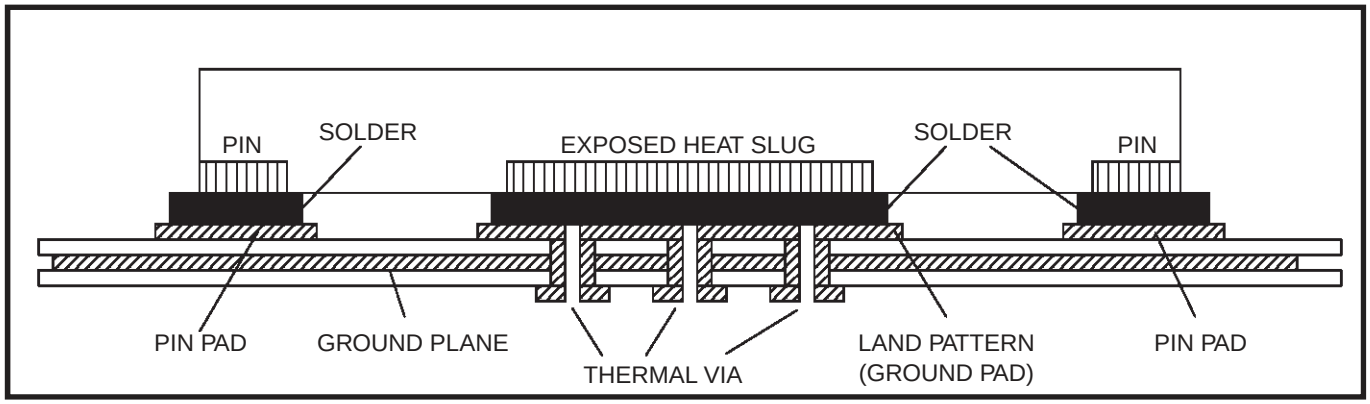


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 5 shows an example of ICS845254I application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of CML terminations are shown in this schematic.

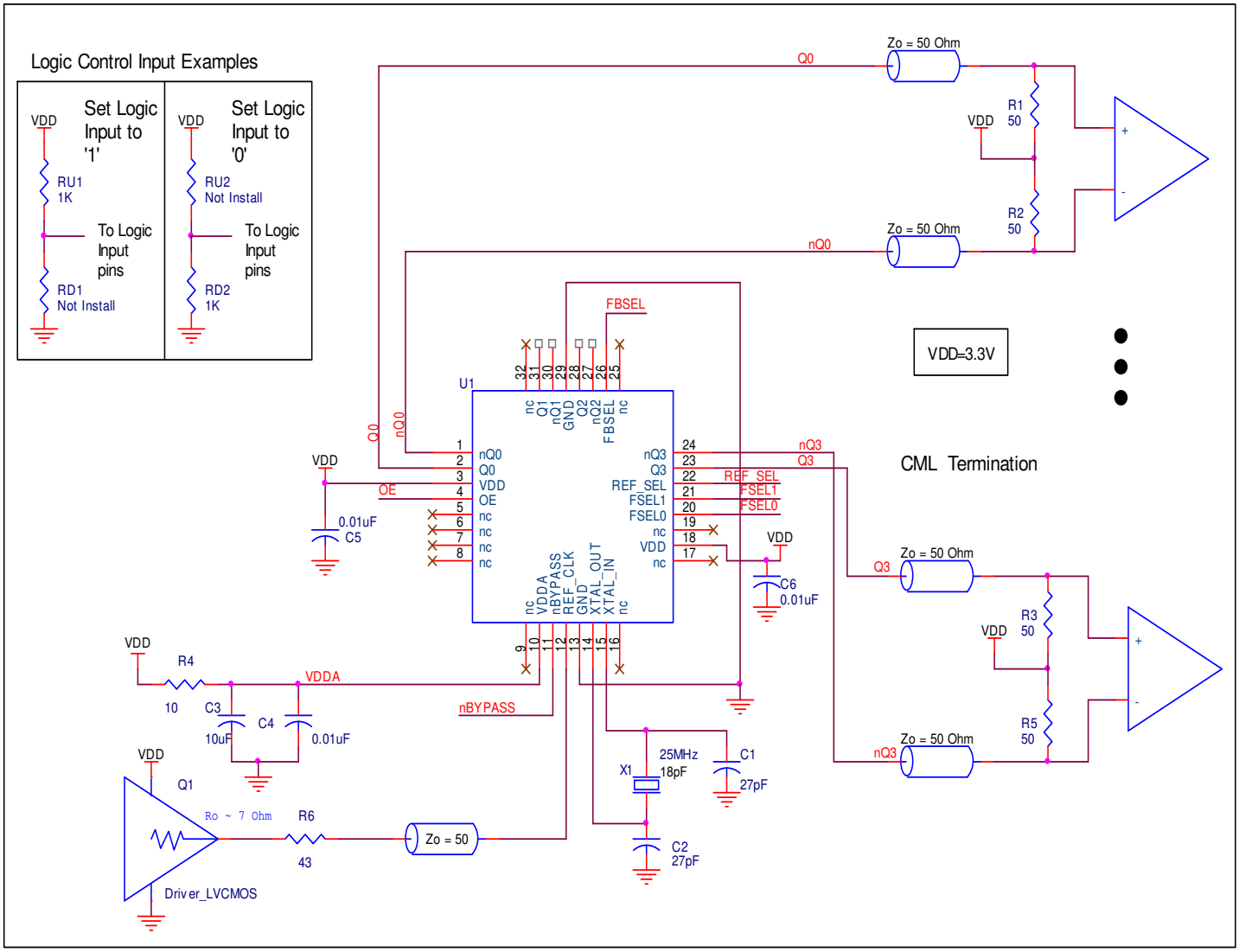


Figure 5. 845254 Schematic Layout Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 845254.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 845254 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA})$ = 3.465V * (88mA + 12mA) = **346.5mW**
- Power $(outputs)_{MAX}$ = **36.1mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 36.1mW = **144.4mW**

Total Power$_{MAX}$ (3.465V, with all outputs switching) = 346.5mW + 144.4mW = **490.99mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 43.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.491W * 43.4°C/W = 106°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the CML driver output pair. The CML output circuit and termination are shown in Figure 6.

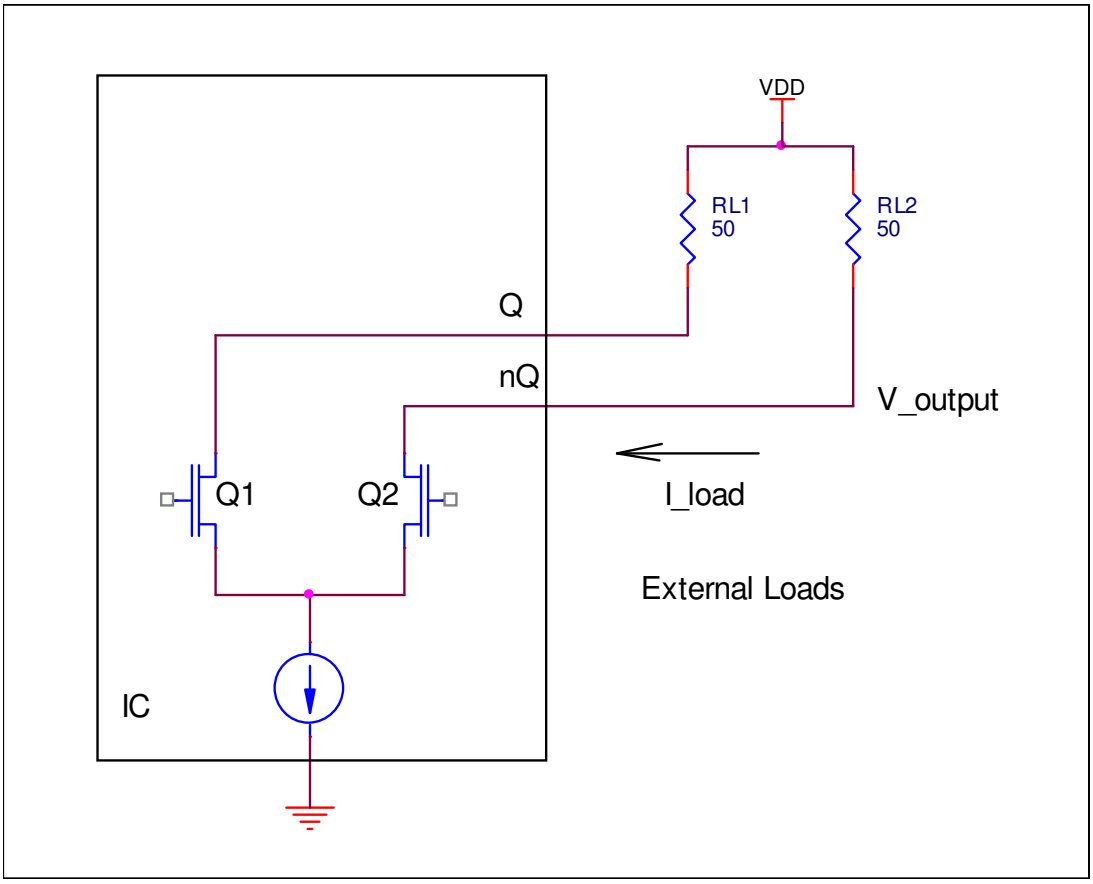


Figure 6. CML Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations:

Power dissipation when the output driver is logic LOW:

Pd_L = I_Load * V_Output

= $(V_{OUT\_MAX} / R_{L)} * (V_{DD\_MAX} - V_{OUT\_MAX})$

= (600mV/50Ω) * (3.465V – 600mV)

= 34.38mW

Power dissipation when the output driver is logic HIGH:

Pd_H = I_Load * V_Output

= (0.025V/50Ω) * (3.465V – 0.025V)

= 1.72mW

Total Power Dissipation per output pair = Pd_H + Pd_L = **36.1mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 lead VFQFN

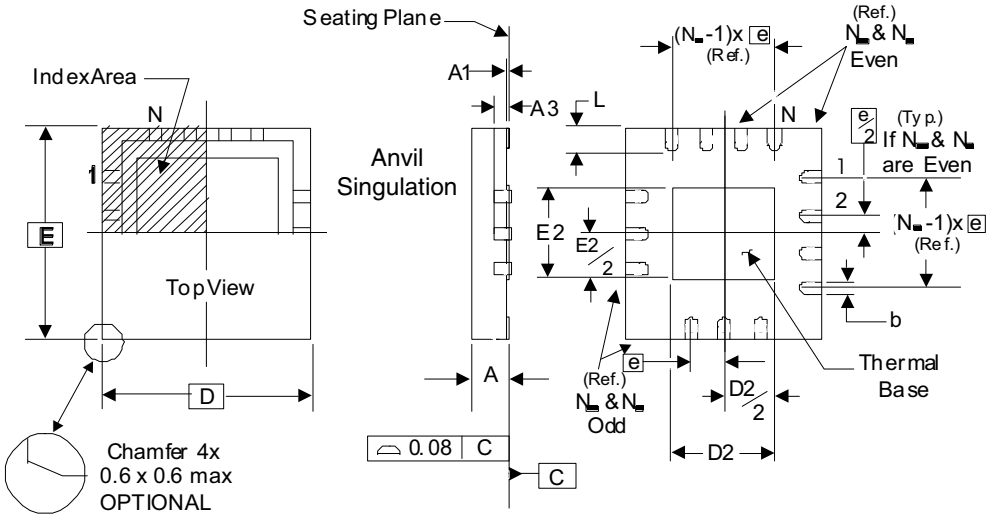
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

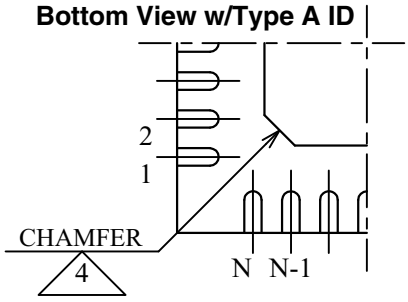
Transistor Count

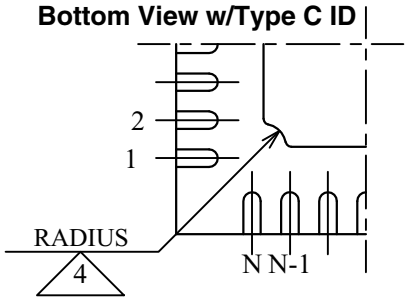
The transistor count for the 845254 is: 3064

Package Outline and Package Dimensions

Package Outline - K Suffix for VFQFN Packages







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
845254AKILF	ICS45254AIL	Lead-Free, 32 Lead VFQFN	Tray	-40°C to 85°C
845254AKILFT	ICS45254AIL	Lead-Free, 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	PDN #CQ-15-04 Product Discontinuance Notice – Last Time buy Expires on August 14, 2016.	08/25/15

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.