High Efficiency Single Synchronous Buck PWM Controller

General Description

The RT8241D PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The RT8241D supports on chip voltage programming function between 0.675V and 0.9V by controlling GX digital inputs.

The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8241D achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs and enter diode emulation mode at light load condition. The buck conversion allows this device to directly step down high voltage batteries at the highest possible efficiency. The RT8241D is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.675V.

The RT8241D is available in a WQFN-12L 2x2 package.

Ordering Information

RT8241D□□

- Package Type
  QW : WQFN-12L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

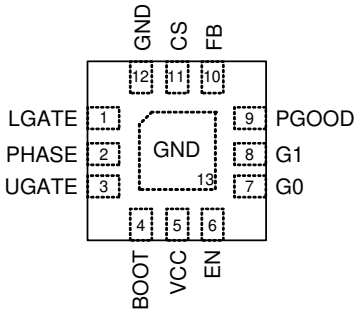
- **Meet Intel VCCSA Voltage Slew Rate**
- **Built-in 1% Reference Voltage**
- **2-Bit Programmable Output Voltage with Integrated Transition Support**
- **Quick Load-Step Response within 100ns**
- **4700ppm/°C Programmable Current Limit by Low Side $R_{DS(ON)}$ Sensing**
- **4.5V to 26V Battery Input Range**
- **Internal Ramp Current Limit Soft-Start Control**
- **Drives Large Synchronous Rectifier FETs**
- **Integrated Boost Switch**
- **Over/Under Voltage Protection**
- **Thermal Shutdown**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook Computers
- CPU/GPU Core Supply
- Chipset/RAM Supply
- Generic DC/DC Power Regulator

Pin Configurations

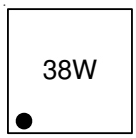
(TOP VIEW)



WQFN-12L 2x2

Marking Information

RT8241DGQW



38 : Product Code

W : Date Code

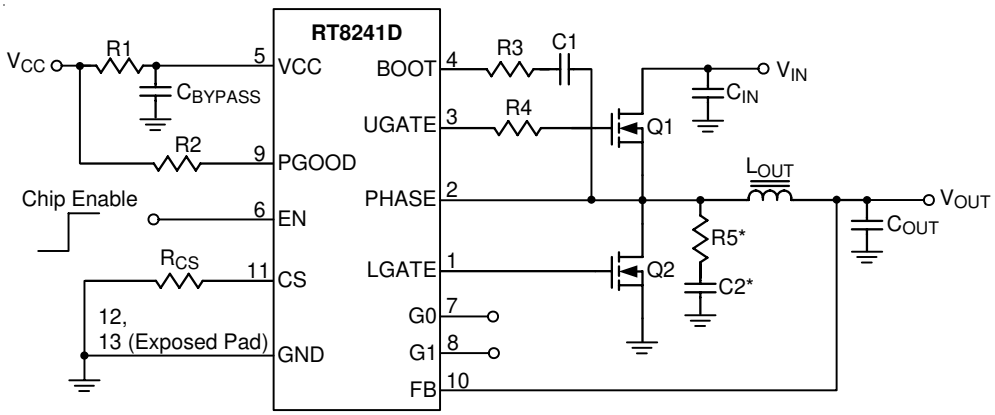
RT8241DZQW

38 : Product Code

W : Date Code

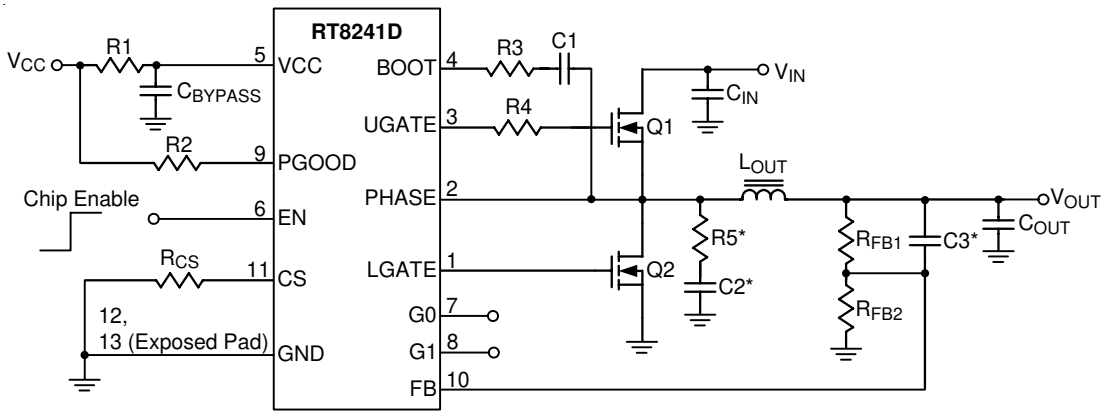
Typical Application Circuit

For Fixed Voltage Regulator :



* : Optional

For Adjustable Voltage Regulator :



* : Optional

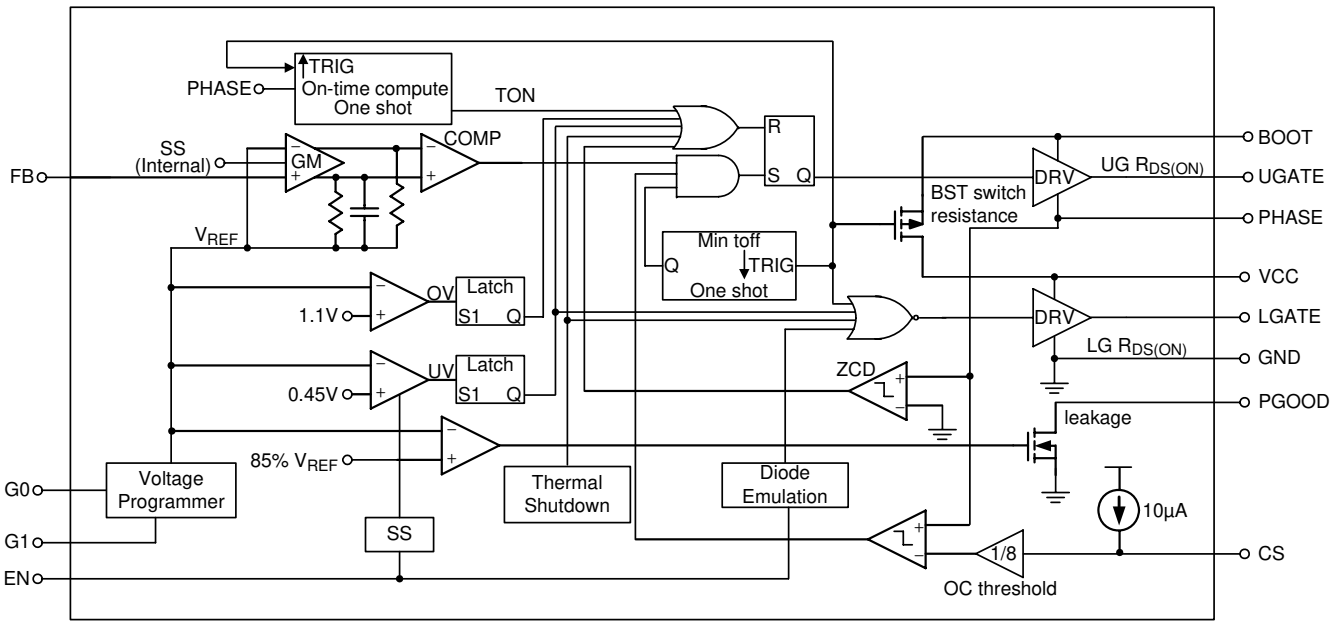
Table 1. VID Table

G0	G1	V_{FB}
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LGATE	Gate Drive Output for Low Side External MOSFET.
2	PHASE	External Inductor Connection Pin for PWM Converter. It behaves as the current sense comparator input for low side MOSFET $R_{DS(ON)}$ sensing and reference voltage for on time generation.
3	UGATE	Gate Drive Output for the High Side External MOSFET.
4	BOOT	Supply Input for High Side Driver. Connect a capacitor to the floating node (PHASE) pin.
5	VCC	Control Voltage Input. Provides the power for the buck controller, the low side driver and the bootstrap circuit for high side driver. Bypass to GND with a 4.7μF ceramic capacitor.
6	EN	Chip Enable (Active High).
7	G0	2-Bit Input Pin.
8	G1	2-Bit Input Pin.
9	PGOOD	Open Drain Power Good Indicator. High impedance indicates power is good.
10	FB	Output Voltage Feedback Input.
11	CS	Current Limit Threshold Setting Input. Connect a setting resistor to GND and the current limit threshold is equal to 1/8 of the voltage seen at this pin.
12, 13 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VCC, FB, PGOOD, EN, CS, G0, G1 to GND ---------- –0.3V to 6V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - <20ns ---------- –8V to 38V
- BOOT to PHASE ---------- –0.3V to 6V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-12L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  - WQFN-12L 2x2, θ_{JA} ---------- 165°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 4.5V to 26V
- Control Voltage, V_{CC} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, V_{IN} = 8V, V_{EN} = 5V, V_{CS} = 1V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
VCC Quiescent Supply Current	I_Q	FB forced above the regulation point, V_{EN} = 5V	--	500	1250	μA
VCC Shutdown Current	I_{SHDN}	V_{CC} current, V_{EN} = 0V	--	--	1	μA
CS Shutdown Current		CS pull to GND	--	--	1	μA
FB Error Comparator Threshold	V_{FB}	T_A = 25°C	–1	0	1	%
		T_A = –40°C to 85°C (Note 5)	–1.5	0	1.5	
V_{OUT} Voltage Range	V_{OUT}		0.675	--	3.3	V
On-Time, Pulse Width	t_{ON}	V_{FB} = 0.9V (f_{SW} = 300kHz)	--	400	--	ns
Minimum Off-Time	t_{OFF}		250	400	550	ns

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sensing							
CS Source Current				9	10	11	μA
CS Source Current Temperature Coefficient				--	4700	--	ppm/°C
Zero Crossing Threshold			PHASE – GND	–10	--	5	mV
Protection Function							
Current Limit Threshold Offset			GND – PHASE = VCS/8	–20	0	20	mV
Negative Current Limit Threshold Offset			PHASE – GND = VCS/8	--	3	--	mV
Under Voltage Protection			UVP Detect, Falling Edge	0.41	0.45	0.49	V
UVP Fault Delay			V_{FB} = 0.375V	--	3.5	--	μs
Over Voltage Protection			OVP Detect, Rising Edge	1.065	1.1	1.133	V
OVP Fault Delay			V_{FB} = 1.183V	--	5	--	μs
V_{CC} Under Voltage Lockout (UVLO) Threshold		V_{UVLO}	Falling edge, PWM disabled below this level	3.5	3.7	3.9	V
V_{CC} UVLO Hysteresis		ΔV_{UVLO}		--	100	--	mV
VOUT Soft-Start			From EN = High to V_{OUT} = 95%	--	0.8	--	ms
Dynamic VID Slew Rate		S_{GX}	G0/G1 Transition	1.75	--	10	mV/μs
UVP Blank Time			From EN signal going high	--	3	-	ms
Thermal Shutdown		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	10	--	
Driver On-Resistance							
UGATE Driver Source		$R_{UGATEsr}$	BOOT–PHASE forced to 5V, UGATE High State	--	1.8	3.6	Ω
UGATE Driver Sink		$R_{UGATEsk}$	BOOT–PHASE forced to 5V, UGATE Low State	--	1.2	2.4	Ω
LGATE Driver Source		$R_{LGATEsr}$	LGATE, High State	--	1.8	3.6	Ω
LGATE Driver Sink		$R_{LGATEsk}$	LGATE, Low State	--	0.8	1.34	Ω
Dead Time			LGATE Rising (V_{PHASE} = 1.5V)	--	30	--	ns
			UGATE Rising	--	30	--	
Internal Boost Charging Switch On-Resistance			VCC to BOOT, 10mA	--	--	80	Ω
EN Threshold							
EN Threshold Voltage	Logic-High	V_{IH}		1.8	--	--	V
	Logic-Low	V_{IL}		--	--	0.5	
Voltage Programming (G0, G1)							
G0, G1 Input Threshold Voltage	Logic-High			750	--	--	mV
	Logic-Low			--	--	300	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD (upper side threshold determined by OVP threshold)						
Trip Threshold		Falling edge, measured at FB, with respect to reference, no load.	–19	–15	–11	%
Trip Hysteresis			--	3	--	%
Fault Propagation Delay		Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		High State, forced to 5V	--	--	1	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

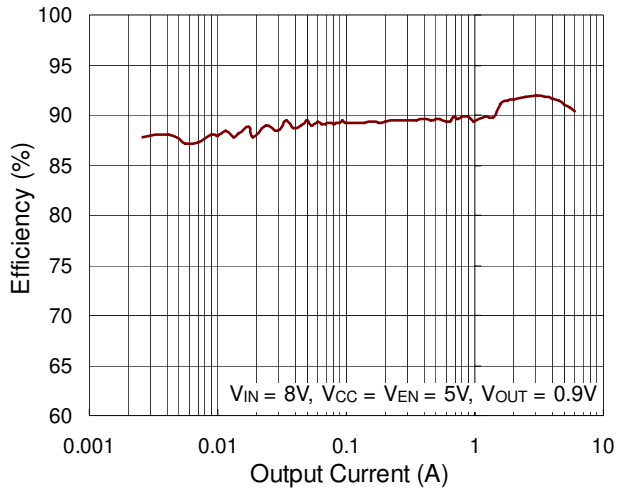
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

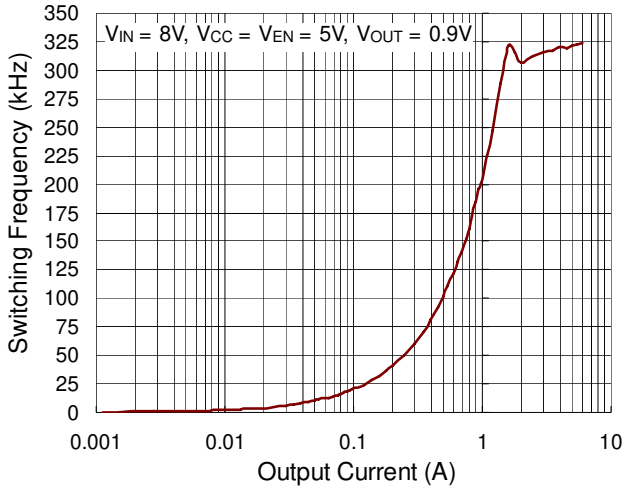
Note 5. Guaranteed by Design.

Typical Operating Characteristics

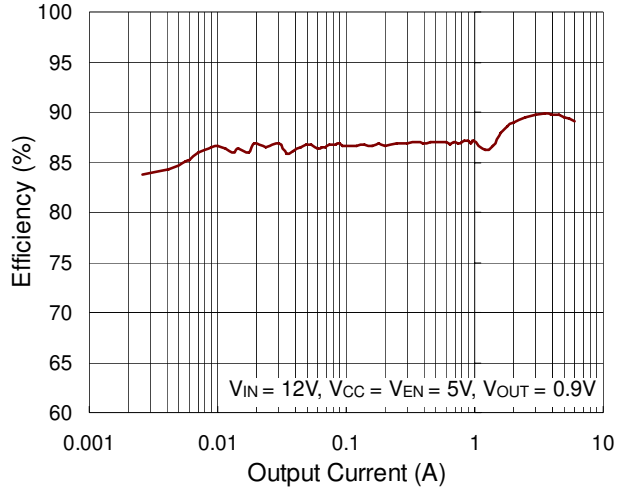
Efficiency vs. Output Current



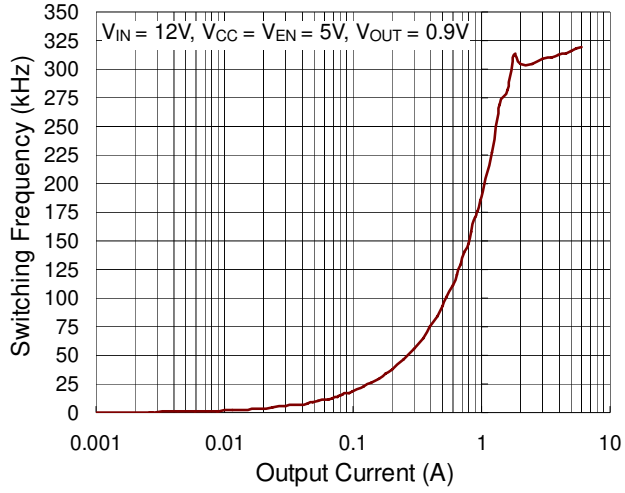
Switching Frequency vs. Output Current



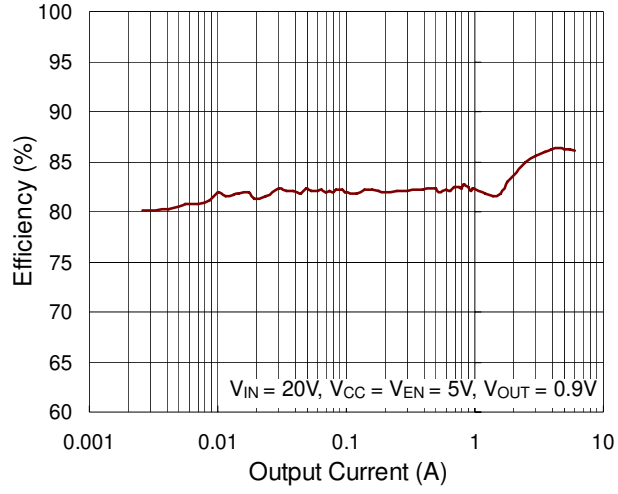
Efficiency vs. Output Current



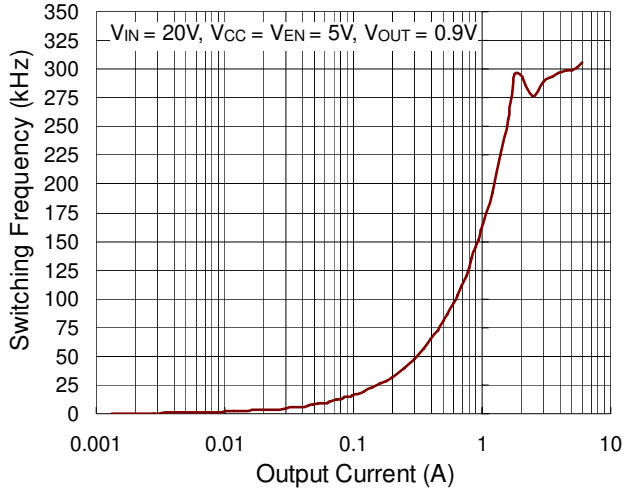
Switching Frequency vs. Output Current



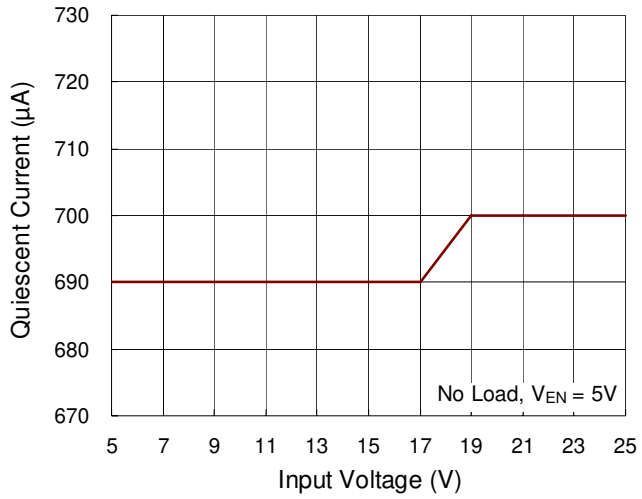
Efficiency vs. Output Current



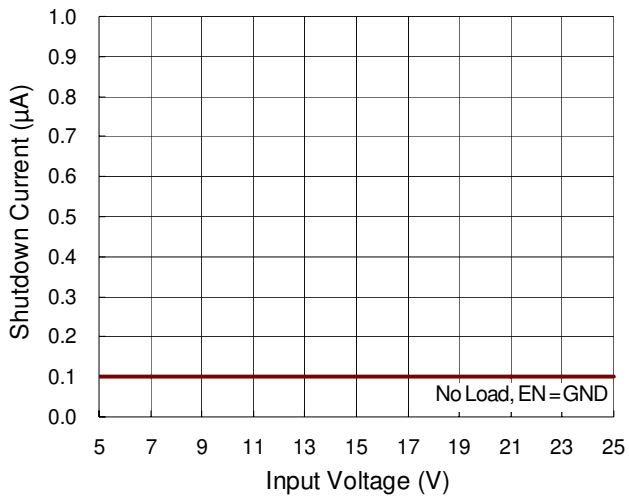
Switching Frequency vs. Output Current



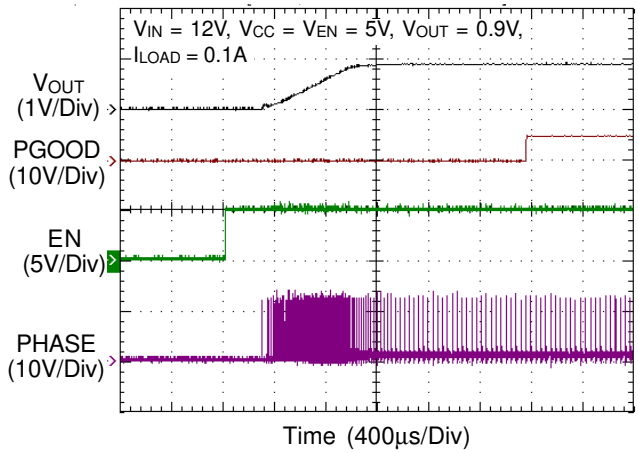
Quiescent Current vs. Input Voltage



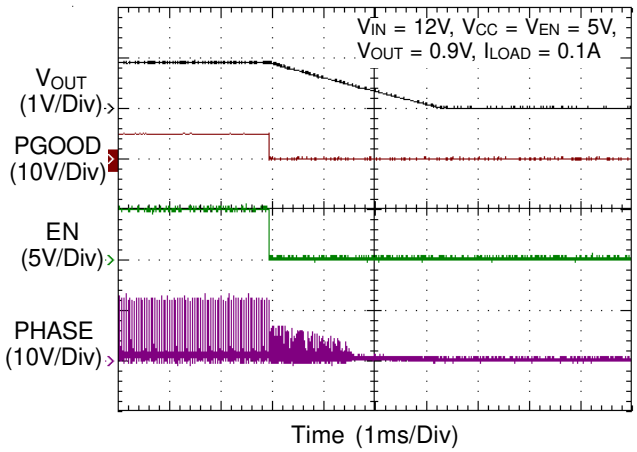
Shutdown Current vs. Input Voltage



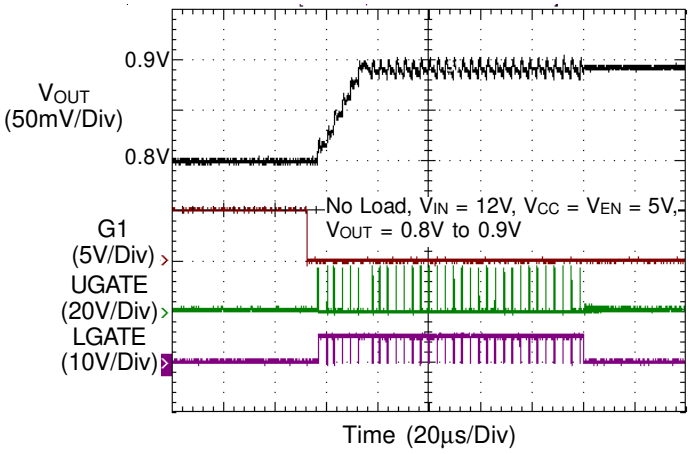
Power On from EN



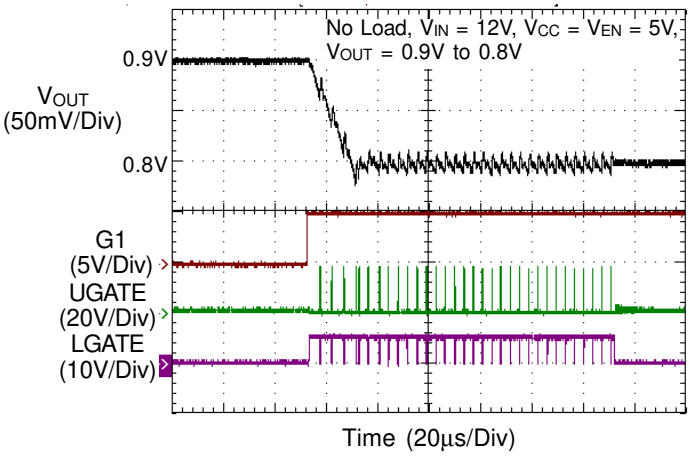
Power Off from V_{IN}



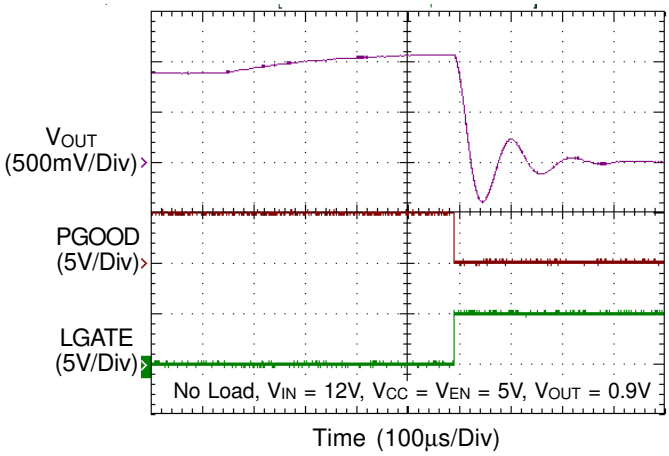
Dynamic VID Up



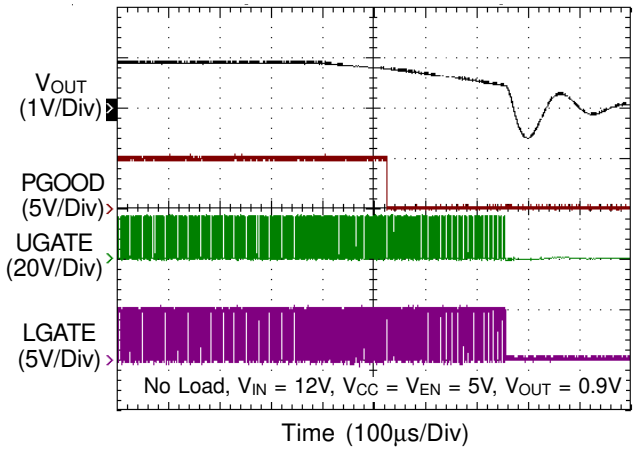
Dynamic VIN Down



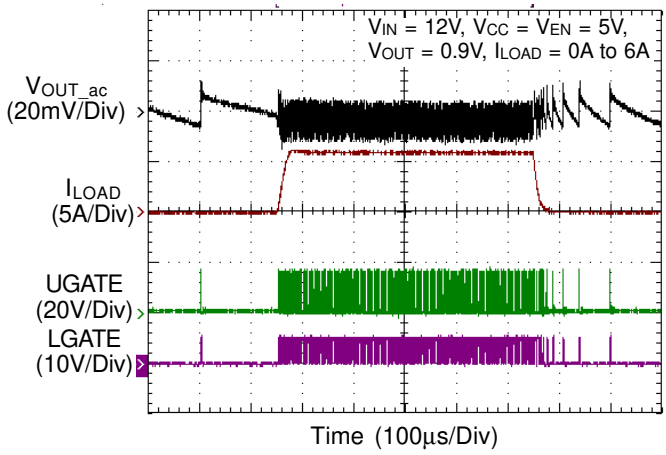
Over Voltage Protection



Under Voltage Protection



Load Transient Response



Application Information

The RT8241D is of a constant on-time PWM controller which provides four DC feedback voltages by controlling the G0 and G1 digital input. The constant on-time PWM control scheme handles wide input/output ratios with ease and provides 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs, while avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The Mach Response™, DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so the output ripple voltage provides the PWM ramp signal. Referring to the function diagrams of the RT8241D, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the high side MOSFET is turned off. The pulse width of this one shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control (TON)

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high side switch directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

Diode-Emulation Mode

RT8241D automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increasing V_{OUT} ripple or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current when the inductor freewheeling current becomes negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that is required for the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light-load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

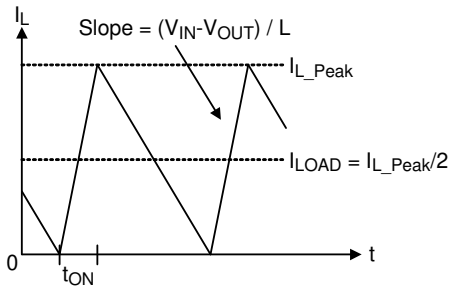


Figure 1. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance

remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Output Voltage Setting (FB)

As Figure 2 shows, the output voltage can be adjusted from 0.675V to 3.3V by setting the feedback resistors R_{FB1} and R_{FB2}. Choose R_{FB2} to be approximately 20kΩ, and solve for R_{FB1} using the equation :

$$V_{OUT} = V_{FB} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

where V_{FB} is as shown in Table 2.

Table 2. Feedback Voltage Selection

G0 State	G1 State	Feedback Voltage
0	0	V_{FB} = 0.9V
0	1	V_{FB} = 0.8V
1	0	V_{FB} = 0.725V
1	1	V_{FB} = 0.675V

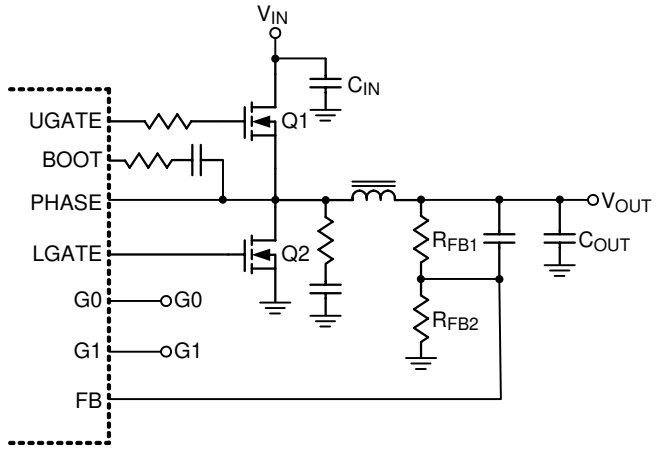


Figure 2. Setting V_{OUT} with a Resistor-Divider

Output Voltage Transition Operation

The digital input control pin Gx allows V_{OUT} to transition to both higher and lower values. For a downward transition, the rapid change of Gx from high to low will suddenly cause V_{FB} to drop to a new internal V_{REF}. At this time the LGATE will drive high to turn on the low side MOSFET and draw current from the output capacitor via the inductor. LGATE will remain on until V_{FB} falls to the new internal V_{REF}, at which point a normal UGATE switching cycle begins, as shown in Figure 3. For a down transition, the low side MOSFET remains on until V_{FB} reaches the new internal V_{REF}. Thus, the negative inductor current will be increased. If the negative current become large enough to trigger NOCP, the low side MOSFET will be turned off to prevent large negative current from damaging the component. Refer to the Negative Over Current Limit section for a full description.

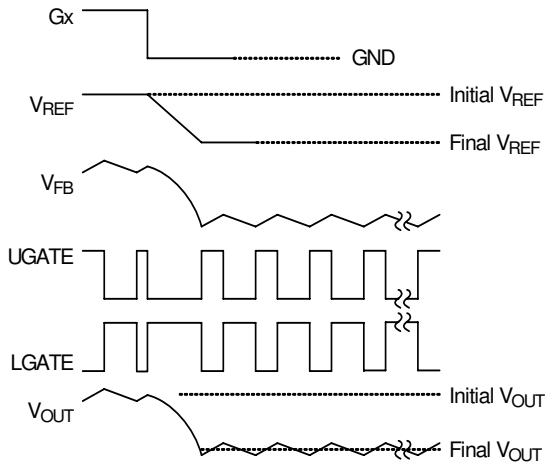


Figure 3. Output Voltage Down Transition

For an upward transition (from lower to higher V_{OUT}) as shown in Figure 4, Gx changes from low to high and causes V_{FB} to rise to a new internal V_{REF}. This quickly trips the V_{FB} comparator regardless of whether DEM is active or not, generating an UGATE on-time and causing a subsequent LGATE to be turned on. At the end of the minimum off-time (400ns), if V_{FB} is still below the new internal V_{REF}, another UGATE on-time will be started. This sequence continues until the FB pin exceeds the new internal V_{REF}.

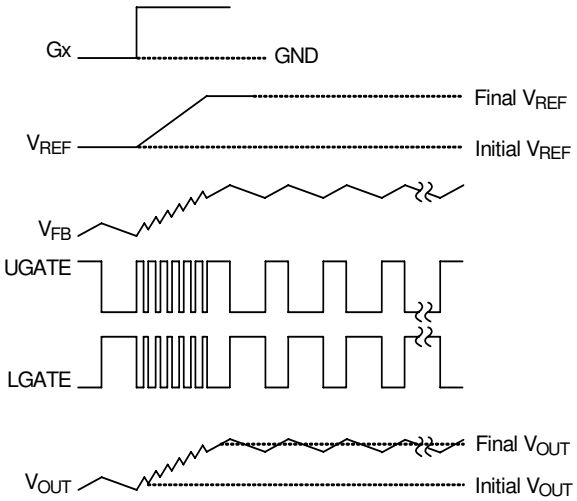


Figure 4. Output Voltage Up Transition

If the V_{OUT} change is significant, there can be several consecutive cycle of UGATE on-time followed by minimum LGATE time. This can cause a rapid increase in inductor current: typically it only takes a few switching cycles for inductor current to rise up to the current limit. At some point the V_{FB} will rise up to the new internal V_{REF} and the UGATE pulses will cease, but the inductor's LI^2 energy must then flow into the output capacitor. This can create a significant overshoot, as shown in Figure 5.

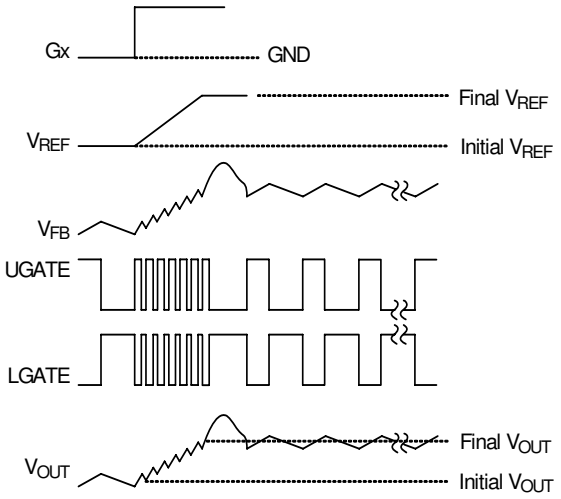


Figure 5. Output Voltage Up Transition with Overshooting

This overshoot can be approximated by the following equation, where I_{CL} is the current limit, V_{FINAL} is the desired set point for the final voltage, L is in µH and C_{OUT} is in µF.

$$V_{MAX} = \sqrt{\left(\frac{I_{CL}^2 \times L}{C_{OUT}}\right) + V_{FINAL}^2}$$

Current Limit Setting (OCP)

The RT8241D has a cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at the CS pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure. 6). In order to provide both good accuracy and a cost effective solution, the RT8241D supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The CS pin should be connected to GND through the trip voltage setting resistor, R_{CS}. The 10µA CS terminal source current , I_{CS}, and the trip voltage setting resistor, R_{CS}, set the CS trip voltage, V_{CS}, as in the following equation.

$$V_{CS}(mV) = R_{CS}(k\Omega) \times 10(\mu A)$$

The Inductor current can be monitored by the voltage between GND and the PHASE pin. Hence, the PHASE pin should be connected to the drain terminal of the low side MOSFET. I_{CS} has temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET.

While the comparison is being done during the OFF state, V_{CS} sets the valley level of the inductor current. Thus, the load current at over current threshold, I_{LOAD_OC}, can be calculated as follows :

$$I_{LOAD\_OC} = \frac{V_{CS}}{8 \times R_{DS(ON)}} + \frac{I_{ripple}}{2}$$

$$= \frac{V_{CS}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over current condition, the current to the load exceeds the current to the output capacitor, thus causing the output voltage to fall. Eventually the voltage crosses the under voltage protection threshold and the device shuts down.

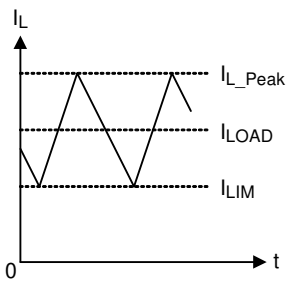


Figure 6. "Valley" Current Limit

Negative Over Current Limit (PWM Only Mode)

The RT8241D supports cycle-by-cycle negative over current limiting in CCM Mode only. The over current limit is set to be negative but is the same absolute value as the positive over current limit. If output voltage continues to rise, the low side MOSEFT remains on. Thus, the inductor current is reduced and reverses direction after it reaches zero. When there is too much negative current in the inductor, the low side MOSFET is turned off and the current flows towards V_{IN} through the body diode of the high side MOSFET. Because this protection limits the discharge current of the output capacitor, the output voltage

tends to rise, eventually hitting the over voltage protection threshold and shutting down the device. If the device hits the negative over current threshold again before output voltage is discharged to the target level, the low side MOSFET is turned off and the process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current threshold is reached, the low side MOSFET is turned off, the high side MOSFET is then turned on, and the device resumes normal operation.

MOSFET Gate Driver (UGATE, LGATE)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the V_{CC} supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on. The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull-down transistor that drives LGATE low is robust, with a 0.8Ω typical on resistance. A 5V bias voltage is delivered from the V_{CC} supply. The instantaneous drive current is supplied by the flying capacitor between VCC and GND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate drain coupling, which can lead to efficiency killing, EMI-producing shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high side MOSFET without degrading the turn-off time, as shown in Figure 7.

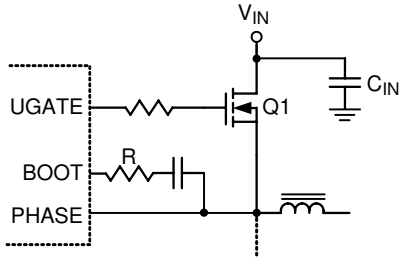


Figure 7. Reducing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the feedback voltage is above 1.1V or below 0.45V, PGOOD will be pulled low. PGOOD is allowed to be high until soft-start ends and the output reaches 89% of its set voltage. There is a 2.5µs delay built into PGOOD circuitry to prevent false transition.

When Gx changes, PGOOD remains in its present state for 32 clock cycles. Meanwhile, V_{OUT} or V_{FB} regulates to the new level.

POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VCC rises above 3.7V (typ.). After POR is triggered, the RT8241D will reset the fault latch and prepare the PWM for operation. Below 3.6V (typ.), the VCC Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from the power supply input after EN is enabled. It clamps the ramping of the internal reference voltage which is compared with the FB signal. The typical soft-start duration is 0.8ms.

Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When V_{FB} exceeds 1.1V, over voltage protection is triggered and the low side MOSFET is latched on. This activates the low side MOSFET to discharge the output capacitor. The RT8241D is latched once OVP is triggered and can only be released by VCC or EN power on reset. There is a 5µs delay built into the over voltage protection circuit to prevent false transitions.

Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When V_{FB} is less than 0.45V, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. In order to remove the residual charge on the output capacitor during the under voltage period, if PHASE is greater than 1V, the LGATE is forced high until PHASE is lower than 1V. There is a 3.5µs delay built into the under voltage protection circuit to prevent false transitions. During soft-start, the UVP blanking time is 3ms.

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of peak-to-peak ripple current to the maximum average inductor current. Select a low pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without tripping the OVP circuit. For CPU core voltage converters and other applications where the output is subject to violent load transient, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain at an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic and unstable operation. However, it is easy to add sufficient series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting FB divider close to the inductor. There are two related but distinct ways including double pulsing and feedback loop instability to identify the unstable operation. Double pulsing occurs due to noise on the output or because the ESR is too low such that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillation at the output after line or load perturbations that can trip the over voltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for stability checking is to apply a very zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC probe. Do not allow more than one ringing cycle after the initial step-response under- or overshoot.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8241D, the maximum junction temperature is 125°C

and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-12L 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for WQFN-12L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8241D package, the derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

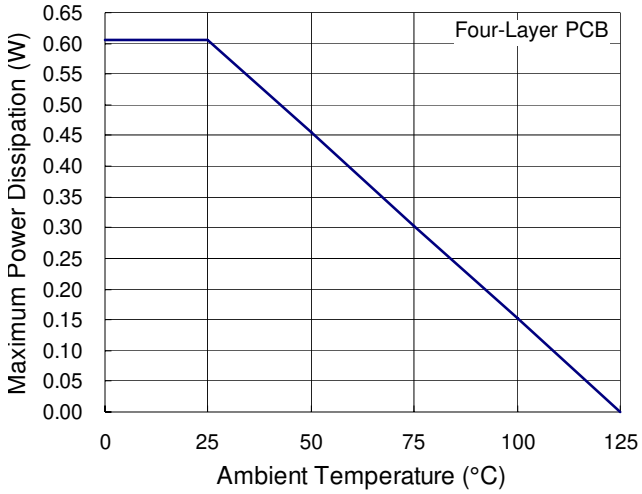


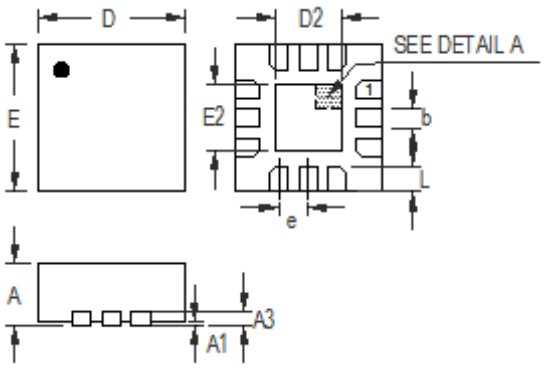
Figure 8. Derating Curves for the RT8241D Package

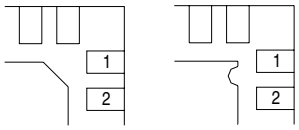
Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to converter instability. For best performance of the RT8241D, the following guidelines should be strictly followed.

- Connect an RC low-pass filter from VCC, (1μF and 10Ω are recommended). Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should be kept away from high voltage switching nodes to prevent it from coupling.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components pertaining to V_{OUT}, FB, GND, EN, PGOOD, CS and VCC should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to prevent it from coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
e	0.400		0.016	
D2	0.850	0.950	0.033	0.037
E2	0.850	0.950	0.033	0.037
L	0.250	0.350	0.010	0.014

W-Type 12L QFN 2x2 Package

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