

Evaluating the ADuM4195-1 Isolated Amplifier with Fixed Gain and Single-Ended Output

FEATURES

- ▶ ADuM4195-1 isolated amplifier in a SOIC-8 package
- ▶ ADuM6028-5BRIZ isolated on-board power supply
- ▶ Isolated 5 V DC accessible through extra terminals
- ▶ Two separate input options:
 - ▶ Maximum 1,000 V DC pre-configured
 - ▶ User-configurable maximum 200 V DC
- ▶ Input reverse-polarity protection

EQUIPMENT NEEDED

- ▶ Power supply, 5 V DC $\pm 10\%$, 50 mA
- ▶ Adjustable DC voltage source, 0 to 1 kV
- ▶ 2 \times DMM, 5 and one-half digit

GENERAL DESCRIPTION

The EVAL-ADuM4195-1EBZ is a compact isolated DC voltage monitoring board with an isolated on-board power supply to facilitate the setup and testing of the performance characteristics of the ADuM4195-1.

On the input side of the board, two separate inputs are available: The P1000 input is pre-configured to accept up to 1 kV DC, while the P200 input can be user-configured for voltages up to 200 V DC. Additional connectors provide access to the isolated 5 V DC supply and the shutdown (SD) input of the ADuM4195-1.

On the output side of the board, the output of the ADuM4195-1 is directly accessible (pre-configured) or may be first-order low-pass filtered by adding a resistor and a capacitor. A single 5 V DC supply is sufficient to power both the input and output side of the board, while the optional power disable (PDIS) pin can be used to disable the on-board supply in applications where low-power consumption is at premium.

Full specifications for the ADuM4195-1 are available in the ADuM4195-1 data sheet, which must be consulted in conjunction with this user guide when working with the EVAL-ADuM4195-1EBZ.

EVALUATION BOARD PHOTOGRAPH



Figure 1. EVAL-ADuM4195-1EBZ

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REVISION HISTORY**1/2023—Revision 0: Initial Version**

CONNECTORS

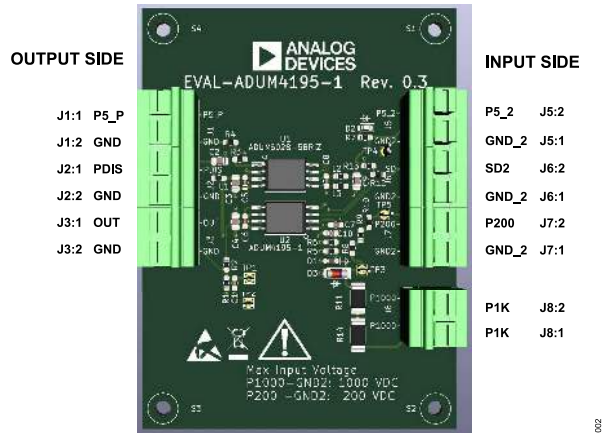


Figure 2. Location of Connectors

PIN DESCRIPTION

Table 1. Pin List

Pin	Parameter	Description
J1:1	P5_P	Input. Power supply +5 V DC.
J1:2	GND	Power supply GND (low-side ground).
J2:1	PDIS	Input. Disables the isolated power supply ($R_{IN} = 1\text{ k}\Omega$). Enable: Leave open. Disable: Connect to P5_P.
J2:2	GND	Power supply GND (low-side ground).
J3:1	OUT	Isolated amplifier output.
J3:2	GND	Output GND (low-side ground).
J5:1	GND_2	Isolated power supply output ground (high-side ground).
J5:2	P5_2	Output. Isolated power supply, +5 V DC (maximum 5 mA), high-side.

Table 1. Pin List (Continued)

Pin	Parameter	Description
J6:1	GND_2	Power supply GND (high-side ground).
J6:2	SD2	Input. Shuts down isolated amplifier ($R_{IN} = 4.8\text{ k}\Omega$). Operate: Leave open. Shutdown: Connect to P5_2.
J7:1	GND_2	Input. Reference ground for P200 input and P1K input.
J7:2	P200	Input. Positive input of user-configurable voltage-divider (maximum 200 V DC).
J8:1	P1K (P1000)	Positive input of high-voltage divider. Input impedance $Z_{IN} = 2\text{ M}\Omega 1.5\text{ pF}$. Maximum voltage $V_{MAX} = 1\text{ kV DC}$ at $T_A = 30^\circ\text{C}$.
J8:2	P1K (P1000)	Same as J8:1.

DIAGNOSTIC LED

When power is supplied to J1:1 (P5_P) and J1:2 (GND), the on-board isolated power supply delivers +5 V DC to the isolated amplifier and to Pin J5:2 (P5_2). This is indicated by LED D2.

TEST POINTS

Test points are provided for oscilloscope probes.

Table 2. Test Points

Pin	Parameter	Description
TP1	OUT	Output of isolated amplifier, through R2.
TP2	U2:5 (GND ₁)	GND ₁ of isolated amplifier. Connected to GND.
TP3	U2:2 (V _{IN})	Input of isolated amplifier.
TP4	U2:4 (GND ₂)	GND ₂ of isolated amplifier. Connected to GND_2.
TP5	P200	Positive input of user-configurable voltage-divider.

TEST SETUP

The EVAL-ADuM4195-1EBZ default configuration is capable of handling input voltages of up to 1,000 V DC continuously. For such voltage levels, it is indispensable to secure the board on a dry, clean, and isolated surface, preferably using 15 mm nylon stand-offs for extra clearance. The input side of the board refers to the input of the isolation amplifier, whereas the output side refers to the output of the isolation amplifier. The input and output side are fully isolated from each other but may be connected to the same GND to facilitate testing. Use the following sequence to set up the board for evaluations up to 1,000 V DC:

1. Secure the board on the workbench.
2. Connect a well-regulated low-noise 5 V DC power supply (current rating approximately 50 mA) to J1:1 (+5 V DC) and J1:2 (GND). Note that the power supply must not exceed the absolute maximum voltage ratings of the [ADuM4195-1](#) during power cycling.
3. To measure the output voltage of the evaluation board, connect a digital multimeter (DMM) between J3:1 (VOOUT) and J3:2 (GND).
4. If the user also wants to monitor the isolation amplifier's input voltage directly at its V_{IN} pin, connect another DMM to TP3 (U2:2) and J6:1 (GND_2). Note that the DMM's input resistance poses an additional load on the evaluation board's input divider network and hence affects the accuracy of the divider ratio. Make sure that the DMM is set to high-impedance ($R_{IN} > 10\text{ M}\Omega$). Although this is a low-voltage measurement, it is referenced to the high-side GND_2 potential. It is therefore recommended to use the appropriate high-voltage cabling for this measurement.
5. Switch on the 5 V DC power supply. The LED D2 indicates that the isolated supply of the board's input side is now on. The output current on the power supply must read $I_{OUT} < 35\text{ mA}$.
6. Connect a low-noise precision high-voltage DC source (DC voltage calibrator) with its positive terminal to J8:1 (P1000) and its negative terminal to J7:1 (GND_2). The voltage source must have a sufficient current rating of $I_{OUT} > 3\text{ mA}$. Use the appropriate high-voltage cabling for this connection. Set the output voltage to 0 V DC and turn the supply on to allow for a sufficient warmup time before starting to test the evaluation board.
7. The user can now analyze the performance of the ADuM4195-1 by varying the voltage at the high-side input and record the voltage low-side output J3:1.

INPUT DIVIDERS

CONFIGURATION

In its default configuration, the EVAL-ADuM4195-1EBZ is set up for a maximum input voltage of 1,000 V DC. This is accomplished by the high-voltage divider R5, R6, R11, and R14. The high-voltage divider's ratio can be calculated as:

$$V(VIN)/V(P1000) = (R5||R6)/((R5||R6) + R11 + R14) \quad (1)$$

An input low-voltage divider configuration can be established on the EVAL-ADuM4195-1EBZ by keeping R5 and R6, and adding R8, R9, and R10 to form a second input divider that can be used separately, with its input at J7:2 (P200). The low-voltage divider's ratio can be calculated as:

$$V(VIN)/V(P200) = (R5||R6)/((R5||R6) + R8 + R9 + R10) \quad (2)$$

To use the low-voltage divider, it is not required to remove the high-voltage resistors R11 and R14. R5 and R6 have been chosen so that the input on the low-voltage divider can be configured for the maximum input voltages down to the approximate 5 V DC to give the maximum flexibility on the EVAL-ADuM4195-1EBZ input range.

MODIFYING THE HIGH-VOLTAGE DIVIDER

Modifications to the high-voltage divider should leave the high-voltage input resistors R11 and R14 unchanged to avoid the printed circuit board (PCB) area around them to be unnecessarily contaminated with flux residues. Then, the resistor R5 and resistor R6 can be altered to adopt for input voltages of up to 500 V DC, rather than 1 kV DC.

Choose resistor values where U2:VIN (at TP3) never exceeds your system's (VDD2 minimum – 0.6 V) under all operating conditions.

Examples, assuming VDD2 minimum = 5 V DC:

Maximum 1,000 V DC input at Pin J8:1 (default setup)

R5 = 9.100 kΩ

R6 = 200.0 kΩ

(nominal divider error: –1.52%, full-scale input voltage: 1015 V)

Maximum 750 V DC input at Pin J8:1

R5 = 12.00 kΩ

R6 = 200.0 kΩ

(nominal divider error: –4.06%, full-scale input voltage: 780 V)

Maximum 500 V DC input at Pin J8:1

R5 = 18.00 kΩ

R6 = 200.0 kΩ

(nominal divider error: –6.94%, full-scale input voltage: 534 V)

MODIFYING THE LOW-VOLTAGE DIVIDER

In default configuration, the input resistor string of R8, R9, and R10 on the low-voltage divider is not populated, and can be configured as follows:

With the following parameters,

VD = maximum voltage at divider input, // maximum allowable voltage: 200 V DC

VIN = maximum voltage at U2:VIN, // 4.4 V = VDD2 min – 0.6V,

the low-voltage divider ratio is DR = VIN/VD.

The total value of the string RLV = R8 + R9 + R10 can then be calculated:

$$RLV = (R5||R6) \times (1/DR - 1) \quad (3)$$

For example, using the maximum allowable input range on the low-voltage divider:

VD = 200 V DC

VIN = 4.4 V

R5 = 9.100 kΩ (default setup)

R6 = 200.0 kΩ (default setup)

R5||R6 = 8.704 kΩ

DR = 4.4/200 = 0.022

$$RLV = 8.704 \text{ k}\Omega \times (1/0.022 - 1) = 386.93 \text{ k}\Omega \quad (4)$$

With R8, R9, and R10 = 137 kΩ

Nominal divider error: –5.74%

Full-scale input voltage: 211 V

GENERAL REMARKS

USEFUL INPUT RANGE

Configure the input divider so that the maximum $U2:V_{IN}$ always stays approximately 0 to 5 % below ($V_{DD2} - 0.6V$), even if this requires dividing $U2:V_{OUT}$ to adopt for the input range of a downstream analog-to-digital converter (ADC). This ensures the excellent input range of the [ADuM4195-1](#) to be fully used.

DIVIDER RESISTORS

Additional adjustment of the resistor R6 can reduce the nominal divider error further, if needed. However, in a voltage monitoring system, a downstream ADC, or processor takes care of the final calibration and adjustment of the gain and offset, thus eliminating the need for lower divider errors. However, divider resistors must be chosen for the lowest possible temperature coefficients to ensure stable divider accuracy over the full required temperature range.

Note also that in worst-case, the voltage-divider exhibits twice the error contribution of its individual resistors, thus making the total divider error approximately 0.2% when choosing 0.1% resistors.

REVERSE INPUT PROTECTION

In applications where accidental reverse input voltages are expected, a reverse input protection diode can be used. This is accomplished by diode D1. The leakage current through the diode D1 can impair divider accuracy and linearity. Therefore, Resistors R5||R6 have a relatively low value, while D1 is selected for low reverse leakage current to minimize impact on linearity. If maximum current into the input-voltage divider is limited to less than 1 mA, it is recommended to remove D1 to achieve optimum linearity of the EVAL-ADuM4195-1EBZ.

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

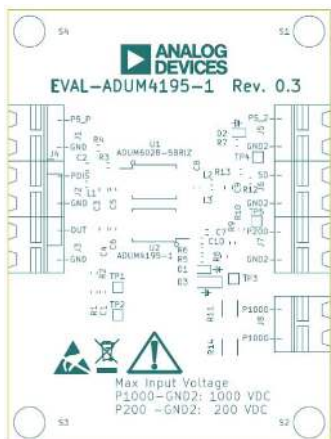


Figure 3. Top Silkscreen

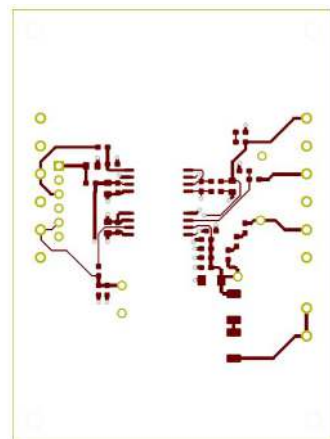


Figure 5. Top Layer

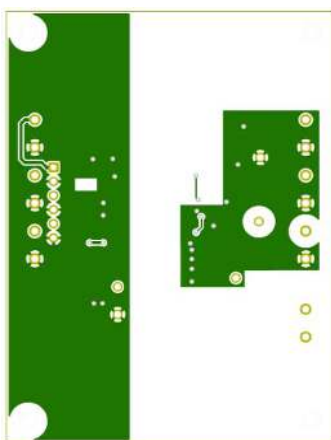


Figure 4. Bottom Layer

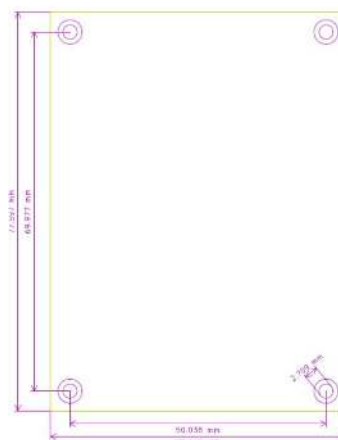


Figure 6. Dimensions

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

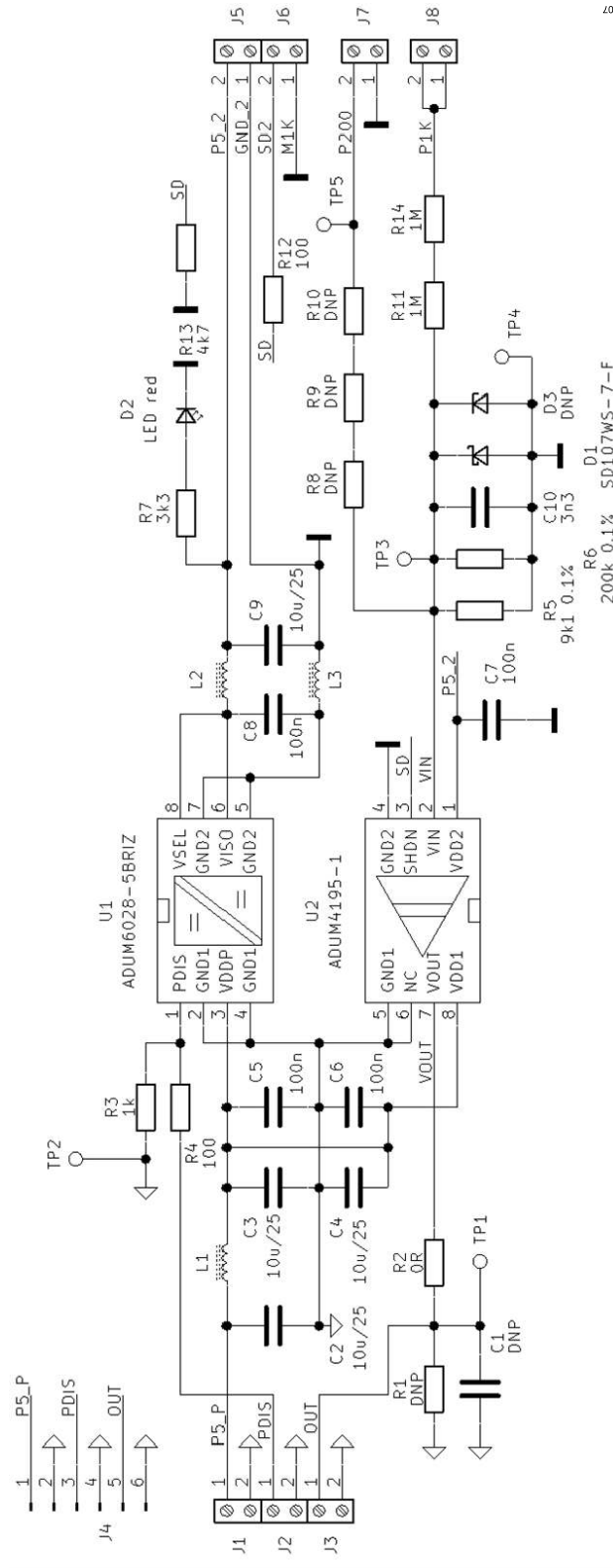


Figure 7. Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Reference	Quantity	Component	Value	Manufacture	Part No.
C1	1	C	DNP	Tayo Yuden	TMK212BBJ106MGHT
C2, C3, C4, C9	4	C	10 μ /25	Tayo Yuden	TMK212BBJ106MGHT
C5, C6, C7, C8	4	C	100n/25	TDK	CGA3E2X7R1E104K080AA
C10	1	C	3n3/25	KEMET	C0603C332J3GACAUTO
D1	1	D_Schottky	SD107WS-7-F	Diodes	SD107WS-7-F
D2	1	LED	LED red	Vishay	TLMS1000-GS08
D3	1	D_Zener	DNP		
J1, J2, J3, J5, J6, J7, J8	7	Terminal	1792863	Phoenix Contact	1792863
J4	1	Conn_01x06	DNP		
L1, L2, L3	3	L_Filter	280/10	TDK	MHF1608BAC252ATD25
R1, R8, R9, R10	4	R	DNP		
R2	1	R	0R	Stackpole	HCJ0603ZT0R00
R3	1	R	1K	Vishay	RCC06031K00FKEA
R4, R12	2	R	100R	Vishay	RCC06031K00FKEA
R5	1	R	9k1/0.1%	Panasonic	ERA-3ARB912V
R6	1	R	200k/0.1%	Panasonic	ERA-3AEB204V
R7	1	R	3k3	Vishay	RCC06033K30FKEA
R11, R14	2	R	1M	Stackpole	HVCB2010FKC1M00
R13	1	R	4k7	Vishay	RCC06034K70FKEA
TP1, TP2, TP3, TP4, TP5	5	TestPoint	KS1035	Keystone	1035
U1	1	ADuM6028-5	ADuM6028-5	Analog Devices	ADuM6028-5BRIZ
U2	1	ADuM4195-1W	ADuM4195-1W	Analog Devices	ADuM4195-1WBRIZ

ORDERING INFORMATION**NOTES****ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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