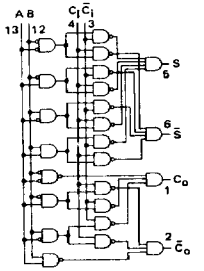
MC1019
MC1219

Provides the SUM, $\overline{SUM}$, CARRY, and $\overline{CARRY}$ functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN and $\overline{CARRY\ IN}$.

POSITIVE LOGIC



$S = ABC_l + A\overline{B}\overline{C}_l + \overline{A}B\overline{C}_l + \overline{A}\overline{B}C_l$

$\overline{S} = \overline{A}\overline{B}\overline{C}_l + \overline{A}BC_l + A\overline{B}C_l + AB\overline{C}_l$

$C_o = ABC_l + AB\overline{C}_l + A\overline{B}C_l + \overline{A}BC_l$

$\overline{C}_o = \overline{A}\overline{B}\overline{C}_l + A\overline{B}\overline{C}_l + \overline{A}B\overline{C}_l + \overline{A}\overline{B}C_l$

DC Input Loading Factor: A, B = 1
C_l, $\overline{C}_l$ = 2

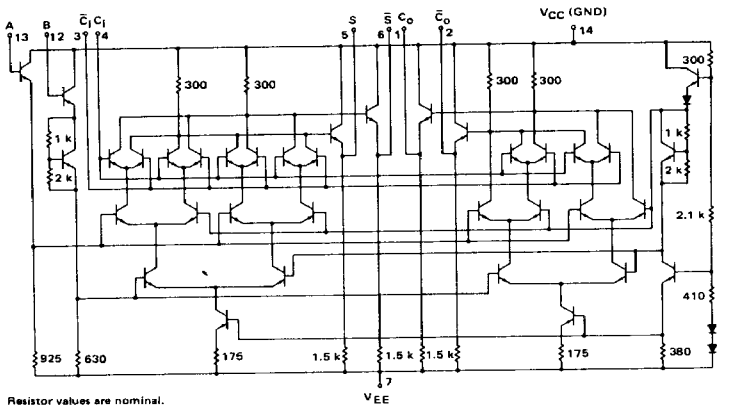
DC Output Loading Factor = 25

Power Dissipation = 145 mW typical

TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
A	B	C_l	$\overline{C}_l$	S	$\overline{S}$	C_o	$\overline{C}_o$
0	0	0	1	0	1	0	1
0	0	1	0	1	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	1	0	1	0

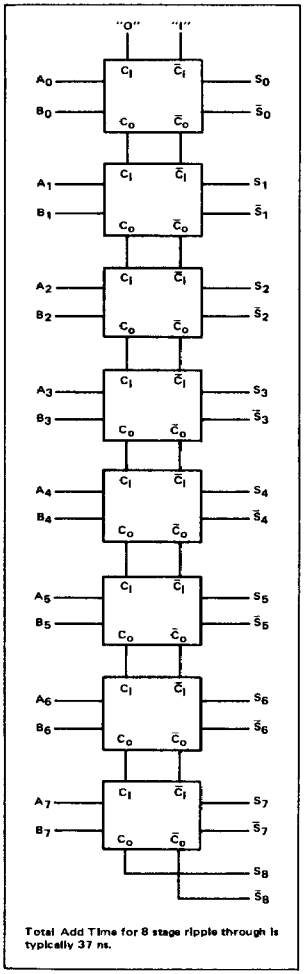
CIRCUIT SCHEMATIC



Resistor values are nominal.

171

FIGURE 1 - 8 BIT RIPPLE-THROUGH ADDER



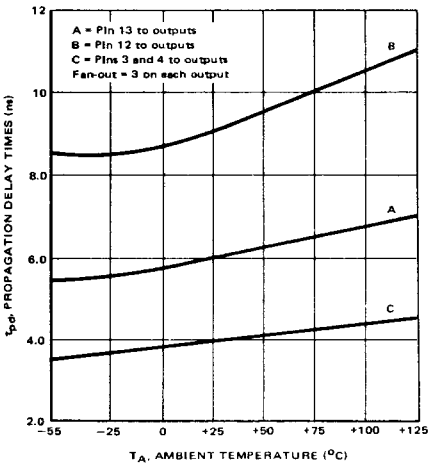
Total Add Time for 8 stage ripple through is typically 37 ns.

APPLICATIONS INFORMATION

The MC1019/MC1219 full adder exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Carry. This device permits practical ripple-through adders as shown in Figure 1, as well as ripple-through multipliers.

The schematic of the full adder illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The B input is translated negative two levels, to switch current between either the left or right branch of the tree. The A input is translated negative one level to switch current at the second level of branching. The Carry inputs switch current through the third level of branching. Depending upon the eight possible combinations of inputs, one specific branch in the Sum generating tree will be carrying current. Thus the proper output state is determined. The Carry generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown in Figure 2.

FIGURE 2 - TYPICAL PROPAGATION DELAY TIMES



172

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1219 Test Limits							MC1019 Test Limits						
			−55°C		+25°C		+125°C		Unit	0°C		+25°C		+75°C		Unit
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	7	-	-	-	35	-	-	mAdc	-	-	-	35	-	-	mAdc
Input Current	$2\ I_{in}$	3	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
	$2\ I_{in}$	4	-	-	-	200	-	-		-	-	-	200	-	-	
	$1.5\ I_{in}$	12	-	-	-	150	-	-		-	-	-	150	-	-	
	$1.5\ I_{in}$	13	-	-	-	150	-	-		-	-	-	150	-	-	
Input Leakage Current	I_R	12	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		13	-	-	-	0.2	-	1.0		-	-	-	0.2	-	1.0	
		3	-	-	-	1.0	-	5.0		-	-	-	1.0	-	5.0	
		4	-	-	-	1.0	-	5.0		-	-	-	1.0	-	5.0	
"SUM" Logic "1" Output Voltage‡	V_{OH}‡*	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"SUM" Logic "0" Output Voltage	V_{OL}*	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"CARRY" Logic "1" Output Voltage‡	V_{OH}‡*	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"CARRY" Logic "0" Output Voltage	V_{OL}*	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Addend Input Propagation Delay	t_{12-5+}	5	8.0	13.0	8.0	13.0	8.0	13.0	ns	8.0	13.0	8.0	13.0	8.0	13.0	ns
	t_{12+5-}	5	7.0	11.5		12.0	10.0	16.0			12.0		12.0	9.0	14.0	
	t_{12+1+}	1	8.0	12.0		12.0	11.0	17.0			12.0		12.0		14.0	
	t_{12-1-}	1	9.0	14.5	9.0	14.5	10.0	15.0		9.0	14.5	9.0	14.5		14.5	
Rise Time	t_{5+}	5	8.0	13.0	9.0	14.0	9.0	14.0		9.0	14.0	9.0	14.0		14.0	
	t_{1+}	1	5.0	8.5	5.0	8.5	8.0	12.0		5.0	8.5	5.0	8.5	7.0	10.0	
Fall Time	t_{5-}	5		8.0		8.5	7.0	11.5			8.5		8.5	6.0	9.5	
	t_{1-}	1		8.0		8.0	7.0	10.0			8.0		8.0	6.0	9.0	
Augend Input Propagation Delay	t_{13+5-}	5	6.0	8.5	6.0	8.5	7.0	10.5	ns	6.0	8.5	6.0	8.5	6.0	9.5	ns
	t_{13-5+}		5.0	8.5	5.0	8.5		11.0		5.0	8.5	5.0	8.5		9.0	
Rise Time	t_{5+}				6.0	9.0		11.0		6.0	9.0	6.0	9.0		9.5	
Fall Time	t_{5-}				5.0	8.5		11.0		5.0	8.5	5.0	8.5		9.5	
Carry Input Propagation Delay	t_{4-5+}	5	3.0	5.0	3.0	5.0	3.0	5.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns
	t_{4+5-}		4.0	7.5	4.0	7.5	8.0	10.0		4.0	7.5	4.0	7.5	5.0	8.5	
Rise Time	t_{5+}		5.0	8.0	6.0	8.5	7.0	10.5		6.0	8.5	6.0	8.5	6.0	9.5	
Fall Time	t_{5-}		5.0	8.0	5.0	8.5	7.0	11.0		5.0	8.5	5.0	8.5	6.0	9.5	

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)

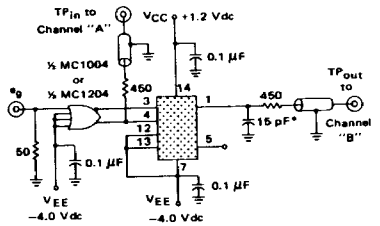
* V_{OH} and V_{OL} limits apply only if not more than one input (pin 3, 4, 12 or 13) is at a Threshold Voltage ($V_{IL\ max}$ or $V_{IH\ min}$). Conduct tests with one input at a Threshold Voltage and apply appropriate $V_{OL\ max}$ or $V_{OH\ min}$ voltages to all other inputs.

173

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{OL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{OH\,min}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1219	−55°C	-5.2 to -1.405	-1.580	-1.165 to -0.825	-0.990		-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-1.380	-0.875 to -0.530	-0.700	-	-5.2	-2.5
MC1019	0°C	-5.2 to -1.350	-1.525	-1.020 to -0.740	-0.875	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-1.435	-0.950 to -0.615	-0.775		-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	3	4	-	7,12,13	-	14
Input Current	$2\,I_{in}$	3	4, 13	-	3, 12	7	-	14
	$2\,I_{in}$	4	3, 12	-	4, 13		-	
	$1.5\,I_{in}$	12	3, 13	-	4, 12		-	
	$1.5\,I_{in}$	13	3, 12	-	4, 13		-	
Input Leakage Current	I_R	12	4	3	-	7,12,13	-	14
		13	4	3	-	7,12,13	-	
		3	-	4	-	3,7,12,13	-	
		4	-	3	-	4,7,12,13	-	
"SUM" Logic "1" Output Voltage‡	V_{OH}‡*	5	3, 12, 13*	4*	-	7	5	14
			4, 13*	3, 12	-			
			4, 12*	3, 13*	-			
			3*	4, 12, 13*	-			
"SUM" Logic "0" Output Voltage	V_{OL}*	5	4, 12, 13*	3*	-	7	-	14
			3, 13*	4, 12*	-		-	
			3, 12*	4, 13*	-		-	
			4*	3, 12, 13*	-		-	
"CARRY" Logic "1" Output Voltage‡	V_{OH}‡*	1	3, 13*	4, 12*	-	7	1	14
			3, 12*	4, 13*	-			
			4*	3, 12, 13*	-			
			3*	4, 12, 13*	-			
"CARRY" Logic "0" Output Voltage	V_{OL}*	1	4, 12, 13*	3*	-	7	-	14
			3, 12, 13*	4*	-		-	
			4, 13*	3, 12*	-		-	
			4, 12*	3, 13*	-		-	
Switching Times (Fan-out = 3)			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Addend Input Propagation Delay	t_{12-5+}	5	12	5	-	7	-	14
	t_{12+5-}	5		5	-		-	
	t_{12+1+}	1		1	-		-	
	t_{12-1-}	1		1	-		-	
Rise Time	t_{5+}	5		5	-		-	
	t_{1+}	1		1	-		-	
Fall Time	t_{5-}	5		5	-		-	
	t_{1-}	1		1	-		-	
Augend Input Propagation Delay	t_{13+5-}	5	13	5	-	7	-	14
	t_{13-5+}				-		-	
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}				-		-	
Carry Input Propagation Delay	t_{4-5+}	5	4	5	-	7	-	14
	t_{4+5-}				-		-	
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}				-		-	

SWITCHING TIME TEST CIRCUIT @ 25°C

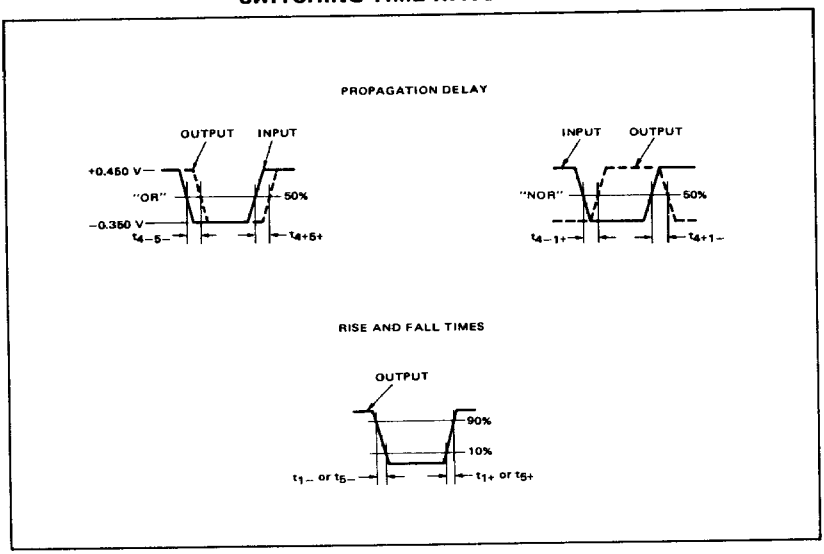


*Load corresponds to fan-out = 3.

Switching test circuit is shown for pulse in on pin 4 and pulse out on pin 1, however all other input–output combinations specified may be tested similarly according to the full subtractor truth table.

Input pulse t_r and t_f = 5.0 ± 0.5 ns

SWITCHING TIME WAVEFORMS



175