# ISL3034E

6-Channel High Speed, Auto-Direction Sensing Logic Level Translator

FN6492
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The ISL3034E is a 6-channel bidirectional, auto-direction sensing, level translator that provides the required level shifting in multi-voltage systems at data transfer rates up to 100Mbps. The auto-direction sensing feature makes the ISL3034E ideally suited for generic six channel level translation especially if bit-by-bit direction control is desired. The $V_{CC}$ and $V_L$ supply voltages set the logic levels on either side of the device. Logic signals on the IC's $V_L$ side appear as higher voltage logic signals on the IC's $V_{CC}$ side. Logic signals on the IC's $V_{CC}$ side appear as higher voltage logic signals on the IC's $V_L$ side.

The ISL3034E operates at full speed with external input drivers that source as little as 4mA output current. Each I/O channel is pulled up to $V_{CC}$ or $V_L$ by an internal 30µA current source, allowing the ISL3034E to be driven by either push-pull or open-drain drivers.

Drive the ISL3034E's enable (EN) input low to place the IC into a low-power shutdown mode with all I/O lines tri-stated. The device features an automatic shutdown mode that places the part in the same shutdown state when $V_{CC}$ is less than $V_L$.

The ISL3034E operates with $V_{CC}$ voltages from +2.2V to +3.6V and $V_L$ voltages from +1.35V to +3.2V, making it ideal for data transfer between low-voltage microcontrollers or ASICs and higher voltage components.

## Related Literature

For a full list of related documents, visit our website:

- ISL3034E device page

## Features

- Best-In-Class ESD protection: ±15kV IEC61000-4-2 ESD protection on all input, output, and I/O lines
- 100Mbps ensured data rate
- Six bidirectional channels
- Auto-direction sensing eliminates direction control logic pins
- Enable input for logic control of low power SHDN Mode
- Compatible with 4mA input drivers or larger
- +1.35V ≤ $V_L$ ≤ +3.2V and +2.2V ≤ $V_{CC}$ ≤ +3.6V supply voltage range
- Pb-Free (RoHS compliant)
- 16Ld µTQFN (2.6mmx1.8mm) and 16 Ld TQFN (3mmx3mm) packages

## Applications

- Simplifies the interface between two logic ICs operating at different supply voltages

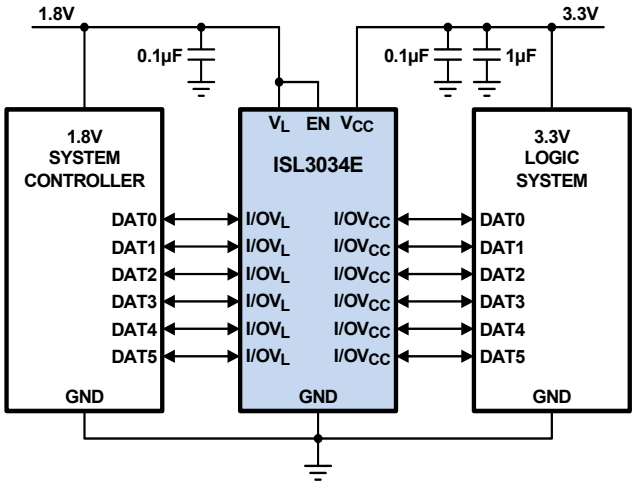



FIGURE 1. TYPICAL OPERATING CIRCUIT

TABLE 1. SUMMARY OF FEATURES

| PART NUMBER | DATA RATE (Mbps) | NUMBER OF CHANNELS | EN PIN? | $I/OV_L$ SHDN STATE | $I/OV_{CC}$ SHDN STATE |
|---|---|---|---|---|---|
| ISL3034E | 100 | 6 | YES | 16.5k to $V_L$ | 16.5kΩ to $V_{CC}$ |

# Ordering Information

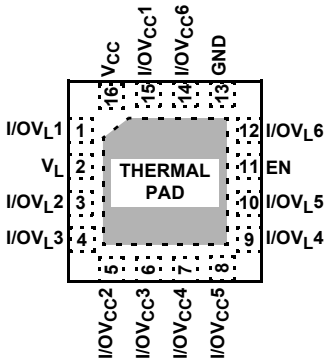
| PART NUMBER (Note 4) | PART MARKING | TEMP. RANGE (°C) | TAPE AND REEL (UNITS) (Note 3) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|---|
| ISL3034EIRTZ (Note 1) | 34TZ | -40 to +85 | - | 16 Ld TQFN | L16.3x3A |
| ISL3034EIRTZ-T (Note 1) | 34TZ | -40 to +85 | 6k | 16 Ld TQFN | L16.3x3A |
| ISL3034EIRUZ-T (Note 2) | GAE | -40 to +85 | 3k | 16 Ld UTQFN | L16.2.6x1.8A |

NOTES:

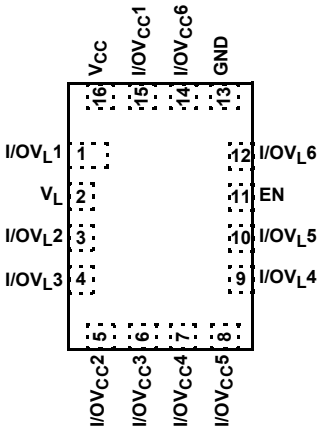
1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Refer to TB347 for details about reel specifications.
4. For Moisture Sensitivity Level (MSL), see the ISL3034E product information page. For more information about MSL, see TB363.

# Pin Configuration

(16 LD TQFN)
TOP VIEW




(16 LD UTQFN)
TOP VIEW




# Pin Descriptions

| NAME | FUNCTION |
|---|---|
| $V_{CC}$ | $V_{CC}$ power supply, +2.2V to +3.6V. Decouple $V_{CC}$ to ground with a 0.1µF capacitor. |
| $V_L$ | $V_L$ logic supply, +1.35V to +3.2V. Decouple $V_L$ to ground with a 0.1µF capacitor. |
| GND | Ground Pin |
| EN | ±15kV IEC61000 ESD Protected Enable Input. Logic “0” puts the device in shutdown. Logic “1” enables the device. |
| $I/OV_{CC}x$ | ±15kV IEC61000 ESD Protected Input/Output channel referenced to $V_{CC}$. |
| $I/OV_Lx$ | ±15kV IEC61000 ESD Protected Input/Output channel referenced to $V_L$. |

## Absolute Maximum Ratings

(All voltages referenced to GND.)

$V_{CC}$, $V_L$ . . . . . -0.3V to +4V
$I/OV_{CC\_}$ . . . . . -0.3V to ($V_{CC}$ + 0.3V)
$I/OV_{L\_}$ . . . . . -0.3V to ($V_L$ + 0.3V)
EN . . . . . -0.3V to +4V
Short-Circuit Duration $I/OV_{L\_}$, $I/OV_{CC\_}$ to GND . . . . . Continuous

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 16 Ld TQFN Package (Notes 5, 6) . . . . . | 74 | 10 |
| 16 Ld UTQFN Package (Notes 5, 6) . . . . . | 93 | 44 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Operating Conditions

Operating Temperature Range . . . . . -40°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. $\theta_{JA}$ is measured with the component mounted on a high-effective thermal conductivity test board in free air, and with "direct attach" features for the QFN and TQFN. See TB379 for details.
6. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

$V_{CC}$ = +2.2V to +3.6V, $V_L$ = +1.35V to +3.2V, EN = $V_L$, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_L$ = +1.8V and $T_A$ = +25°C. (Note 7).

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN (Note 9) | TYP | MAX (Note 9) | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | | |
| $V_L$ Supply Range | $V_L$ | (Note 7) | Full | 1.35 | - | 3.2 | V |
| $V_{CC}$ Supply Range | $V_{CC}$ | (Note 7) | Full | 2.2 | - | 3.6 | V |
| $V_{CC}$ Quiescent Supply Current | $I_{CC}$ | $I/OV_{CC}$ = $V_{CC}$, $I/OV_L$ = $V_L$ | Full | - | 18 | 30 | µA |
| $V_L$ Quiescent Supply Current | $I_{VL}$ | $I/OV_{CC}$ = $V_{CC}$, $I/OV_L$ = $V_L$ | Full | - | 12 | 18 | µA |
| $V_{CC}$ Shutdown Supply Current | $I_{CCSD}$ | EN = GND or $V_L$ > $V_{CC}$ + 0.7V | Full | - | - | 2.5 | µA |
| $V_L$ Shutdown Supply Current | $I_{LSD}$ | EN = GND or $V_L$ > $V_{CC}$ + 0.7V | Full | - | - | 4 | µA |
| EN Input Current | $I_{IN\_EN}$ | | Full | - | | 1 | µA |
| $V_L$ - $V_{CC}$ Shutdown Threshold High | $V_{TH\_H}$ | $V_{CC}$ rising | Full | -0.2 | 0.05$V_L$ | 0.7 | V |
| $V_L$ - $V_{CC}$ Shutdown Threshold Low | $V_{TH\_L}$ | $V_{CC}$ falling | Full | -0.2 | 0.1$V_L$ | 0.7 | V |
| $I/OV_{CC}$, $I/OV_L$ Pull-Up Resistance During Shutdown | $R_{PU\_SD1}$ | EN = GND | Full | 10 | 16.5 | 23 | kΩ |
| $I/OV_{L\_}$ Pull-Up Current | $I_{VL\_PU}$ | EN = $V_L$, $I/OV_L$ = GND | Full | 20 | - | 75 | µA |
| $I/OV_{CC\_}$ Pull-Up Current | $I_{VCC\_PU}$ | EN = $V_L$, $I/OV_{CC}$ = GND | Full | 20 | - | 75 | µA |
| $I/OV_L$ to $I/OV_{CC}$ DC Resistance | $R_{ON}$ | | Full | - | 3 | - | kΩ |
| **ESD PROTECTION** | | | | | | | |
| All Input and I/O Pins From Pin to GND | | IEC61000-4-2 Air-Gap Discharge | 25 | - | ±15 | - | kV |
| | | IEC61000-4-2 Contact Discharge | 25 | - | >±9 | - | kV |
| | | Human Body Model | 25 | - | ±15 | - | kV |
| All Pins | | HBM, per JEDEC | 25 | - | >±12 | - | kV |
| | | Machine Model, per JEDEC | 25 | - | ±1300 | - | V |

**Electrical Specifications** $V_{CC}$ = +2.2V to +3.6V, $V_L$ = +1.35V to +3.2V, EN = $V_L$, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_L$ = +1.8V and $T_A$ = +25°C. (Note 7). **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | | TEMP (°C) | MIN (Note 9) | TYP | MAX (Note 9) | UNITS |
|---|---|---|---|---|---|---|---|---|
| **LOGIC-LEVEL THRESHOLDS** | | | | | | | | |
| I/$OV_L$ Input Voltage High Threshold | $V_{IHL}$ | (Note 8) | | Full | - | - | $V_L$ - 0.2 | V |
| I/$OV_L$ Input Voltage Low Threshold | $V_{ILL}$ | (Note 8) | | Full | 0.15 | - | - | V |
| I/$OV_{CC}$ Input Voltage High Threshold | $V_{IHC}$ | (Note 8) | | Full | - | - | $V_{CC}$ - 0.4 | V |
| I/$OV_{CC}$ Input Voltage Low Threshold | $V_{ILC}$ | (Note 8) | | Full | 0.2 | - | - | V |
| EN Input Voltage High Threshold | $V_{IH}$ | | | Full | - | - | $V_L$ - 0.4 | V |
| EN Input Voltage Low Threshold | $V_{IL}$ | | | Full | 0.4 | - | - | V |
| I/$OV_L$ Output Voltage High | $V_{OHL}$ | $I_{OH}$ = 20µA, I/$OV_{CC}$ ≥ $V_{CC}$ - 0.4V | | Full | 2/3 $V_L$ | - | - | V |
| I/$OV_L$ Output Voltage Low | $V_{OLL}$ | $I_{OL}$ = 20µA, I/$OV_{CC}$ ≤ 0.2V | | Full | - | - | 1/3 $V_L$ | V |
| I/$OV_{CC}$ Output Voltage High | $V_{OHC}$ | $I_{OH}$ = 20µA, I/$OV_L$ ≥ $V_L$ - 0.2V | | Full | 2/3 $V_{CC}$ | - | - | V |
| I/$OV_{CC}$ Output Voltage Low | $V_{OLC}$ | $I_{OL}$ = 20µA, I/$OV_L$ ≤ 0.15V | | Full | - | - | 1/3 $V_{CC}$ | V |
| **RISE/FALL TIME ACCELERATOR STAGE** | | | | | | | | |
| Accelerator Pulse Duration | | On falling edge | | 25 | - | 3 | - | ns |
| | | On rising edge | | 25 | - | 3 | - | ns |
| I/$OV_L$ Output Accelerator Source Impedance | | $V_L$ = 1.62V | | 25 | - | 11 | - | Ω |
| | | $V_L$ = 3.2V | | 25 | - | 6 | - | Ω |
| I/$OV_{CC}$ Output Accelerator Source Impedance | | $V_{CC}$ = 2.2V | | 25 | - | 9 | - | Ω |
| | | $V_{CC}$ = 3.6V | | 25 | - | 8 | - | Ω |
| I/$OV_L$ Output Accelerator Sink Impedance | | $V_L$ = 1.62V | | 25 | - | 9 | - | Ω |
| | | $V_L$ = 3.2V | | 25 | - | 8 | - | Ω |
| I/$OV_{CC}$ Output Accelerator Sink Impedance | | $V_{CC}$ = 2.2V | | 25 | - | 10 | - | Ω |
| | | $V_{CC}$ = 3.6V | | 25 | - | 9 | - | Ω |
| **TIMING CHARACTERISTICS** ($R_{SOURCE}$ = 150Ω, Input rise/fall time ≤ 1ns) | | | | | | | | |
| I/$OV_{CC}$ Rise Time | $t_{RVCC}$ | $R_S$ = 150Ω, $C_{I/OVCC}$ = 10pF, push-pull drivers | | Full | - | - | 3.2 | ns |
| I/$OV_{CC}$ Fall Time | $t_{FVCC}$ | $R_S$ = 150Ω, $C_{I/OVCC}$ = 10pF | | Full | - | - | 3.2 | ns |
| I/$OV_L$ Rise Time | $t_{RVL}$ | $R_S$ = 150Ω, $C_{I/OVL}$ = 15pF, push-pull drivers | $V_L$ ≥ 1.35V | Full | - | - | 4 | ns |
| | | | $V_L$ ≥ 1.62V | Full | - | - | 3.5 | ns |
| I/$OV_L$ Fall Time | $t_{FVL}$ | $R_S$ = 150Ω, $C_{I/OVL}$ = 15pF | $V_L$ ≥ 1.35V | Full | - | - | 4 | ns |
| | | | $V_L$ ≥ 1.62V | Full | - | - | 3.5 | ns |
| I/$OV_{CC}$ Propagation Delay (Driving I/$OV_L$) | $t_{PDVCC}$ | $R_S$ = 150Ω, $C_{I/OVCC}$ = 10pF, push-pull drivers | $V_L$ ≥ 1.35V | Full | - | - | 7.5 | ns |
| | | | $V_L$ ≥ 1.62V | Full | - | - | 6.5 | ns |
| $t_{PDVCC}$ Channel-to-Channel Skew (Note 10) | $t_{SKEWC}$ | | $V_L$ ≥ 1.35V | Full | - | - | 1.3 | ns |
| | | | $V_L$ ≥ 1.62V | Full | - | - | 1 | ns |
| I/$OV_L$ Propagation Delay (Driving I/$OV_{CC}$) | $t_{PDVL}$ | $R_S$ = 150Ω, $C_{I/OVL}$ = 15pF, push-pull drivers | | Full | - | - | 6.5 | ns |
| $t_{PDVL}$ Channel-to-Channel Skew (Note 10) | $t_{SKEWL}$ | | $V_L$ ≥ 1.35V | Full | - | - | 1.3 | ns |
| | | | $V_L$ ≥ 1.62V | Full | - | - | 0.8 | ns |

**Electrical Specifications** $V_{CC}$ = +2.2V to +3.6V, $V_L$ = +1.35V to +3.2V, EN = $V_L$, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $V_L$ = +1.8V and $T_A$ = +25°C. (Note 7). **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | | TEMP (°C) | MIN (Note 9) | TYP | MAX (Note 9) | UNITS |
|---|---|---|---|---|---|---|---|---|
| Delay from EN High to I/$OV_{CC}$ Active | $t_{EN-VCC}$ | $R_{LOAD}$ = 1MΩ, $C_{I/OVCC}$ = 10pF | | 25 | - | 1.5 | - | µs |
| Delay from EN High to I/$OV_L$ Active | $t_{EN-VL}$ | $R_{LOAD}$ = 1MΩ, $C_{I/OVL}$ = 15pF | | 25 | - | 1.5 | - | µs |
| Maximum Data Rate | $D.R._{1.35}$ | Push-pull operation, $R_{SOURCE}$ = 150Ω, $C_{I/OVCC}$ = 10pF, $C_{I/OVL}$ = 15pF, | $V_L \geq 1.35V$ | Full | 85 | - | - | Mbps |
| | $D.R._{1.6}$ | | $V_L \geq 1.62V$ | Full | 100 | - | - | Mbps |

NOTES:

7. $V_L$ must be less than or equal to $V_{CC}$ - 0.2V during normal operation. However, $V_L$ can be greater than $V_{CC}$ during start-up and shutdown conditions and the part will not latch-up nor be damaged.
8. Input thresholds are referenced to the boost circuit.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Delta between all I/$OV_L$ channel prop delays, or delta between all I/$OV_{CC}$ channel prop delays, all channels tested at the same test conditions.

# Test Circuits and Waveforms

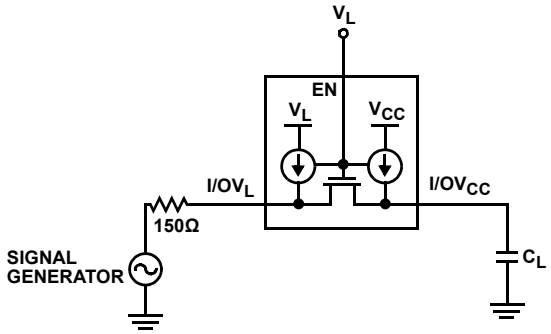



FIGURE 2A. TEST CIRCUIT

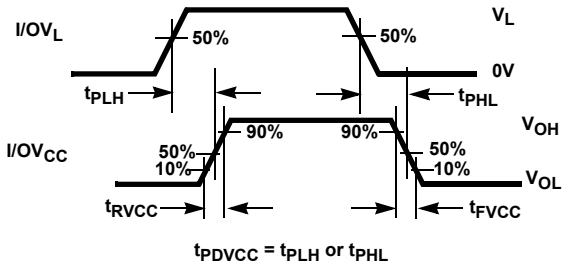



FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. I/$OV_{CC}$ OUTPUT PROPAGATION DELAY AND TRANSITION TIMES (PUSH - PULL)

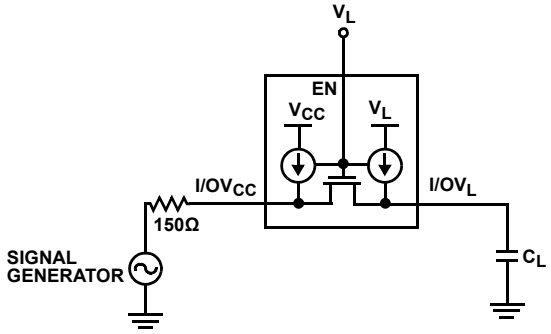



FIGURE 3A. TEST CIRCUIT

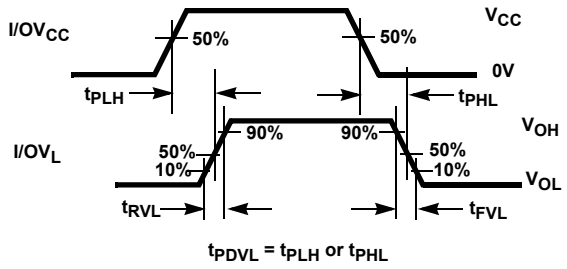
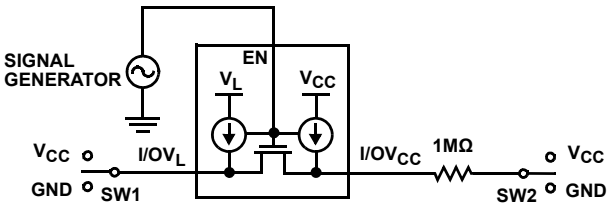



FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. I/$OV_L$ OUTPUT PROPAGATION DELAY AND TRANSITION TIMES (PUSH - PULL)

## Test Circuits and Waveforms (Continued)




| PARAMETER | SW1 | SW2 |
|---|---|---|
| $t_{ENL}$ | GND | $V_{CC}$ |
| $t_{ENH}$ | $V_{CC}$ | GND |

FIGURE 4A. TEST CIRCUIT

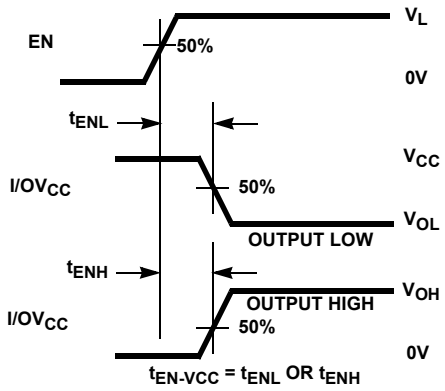
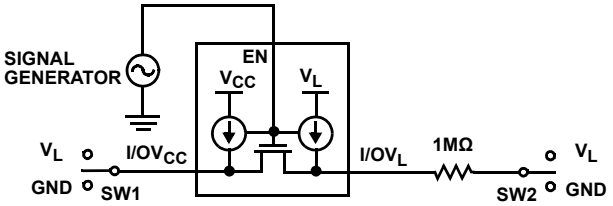



FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. $I/OV_{CC}$ OUTPUT ENABLE TIMES




| PARAMETER | SW1 | SW2 |
|---|---|---|
| $t_{ENL}$ | GND | $V_L$ |
| $t_{ENH}$ | $V_L$ | GND |

FIGURE 5A. TEST CIRCUIT

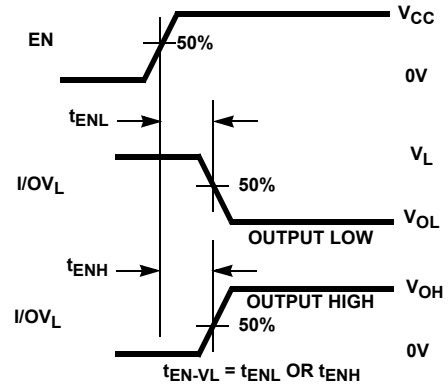



FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. $I/OV_L$ OUTPUT ENABLE TIMES

# Application Information

## Overview

The ISL3034E is a 100Mbps, bidirectional voltage level translating IC for multi-supply voltage systems. The device shifts lower voltage levels on one interface side (supplied by $V_L$) to a higher voltage level on the other interface side (supplied by $V_{CC}$), or vice versa. $V_{OH}$ of the $I/OV_L$ pins tracks the $V_L$ supply, while $V_{OH}$ of the $I/OV_{CC}$ pins tracks the $V_{CC}$ supply.

The ISL3034E features bit-by-bit auto-direction sensing to increase flexibility and eliminate the need for direction control pins. On-chip pull-up current sources in the active mode and pull-up resistors in SHDN mode eliminate the need for most external bus resistors. Open-drain or push-pull type drivers can interface with this level translator, and the device can also be used for unidirectional level shifting.

The ISL3034E is a general purpose 6-Channel level translator. Power supply ranges allow level shifting between 1.5V, 1.8V, and 2.5V powered devices on the $V_L$ side to 2.5V and 3.3V devices on the $V_{CC}$ side.

## Principles of Operation

When enabled, the level shifter detects transitions on an I/O pin and drives the appropriate logic level on the corresponding I/O pin on the other “side”. If the transition was low-to-high, the channel shifts the voltage up to $V_{CC}$ (for transitions on an $I/OV_L$ pin) or down to $V_L$ (for transitions on an $I/OV_{CC}$ pin), and then drives the shifted level on the other side. The ISL3034E enables when EN = 1 AND $V_{CC} > V_L + 200mV$.

Upon detecting a transition on either I/O pin, that channel’s accelerator circuitry actively drives the opposite side’s (output) pin to GND or the output’s supply rail, then turns off. Weak hold circuitry then maintains the logic state until the input is tri-stated, or until another active transition occurs on either I/O pin for that channel. Figure 6 on page 7 shows the simplified block diagram of one level shifting channel.

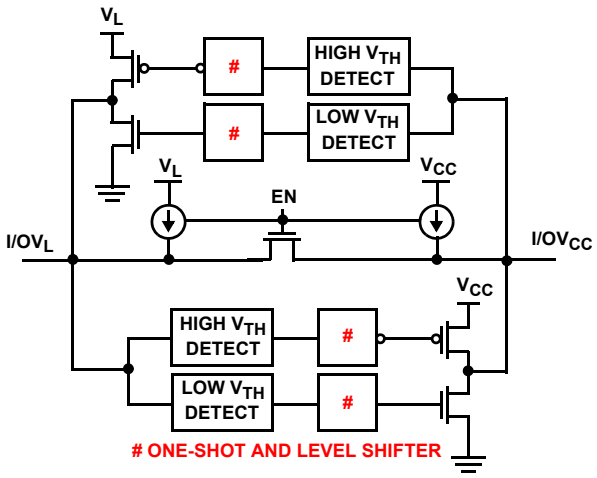



FIGURE 6. ONE CHANNEL SIMPLIFIED SCHEMATIC

The accelerator circuitry comprises high and low threshold detectors, one-shots with level shifters, and large output drivers. A transition on one of the $I/OV_L$ or $I/OV_{CC}$ pins momentarily defines that pin as an input. When the high or low threshold is crossed, a one-shot fires either the PMOS or NMOS driver, respectively, on the opposite side (effectively the output). These drivers are large enough to quickly drive the output node to its respective supply or to GND. Note that this transition on the “output” trips the transition detector on that pin, firing its accelerator, which feeds back to the “input” to help reinforce slow transitions, such as those from an open-drain type driver. When the one-shot (and thus the accelerator) times out (approximately 3ns to 4ns), the large output drivers tri-state and the pins are weakly held in the last state by the small NMOS transistor between $I/OV_L$ and $I/OV_{CC}$ (for a low) or by the small current sources (for a high). In this static state, the I/O pins are easily overdriven by the next transition from an external driver. Having large pull-up and pull-down devices in the accelerator (vs just an active pull-up) nearly eliminates the concern about the external driver’s output impedance, and that impedance’s effect on $V_{OL}$, fall times, and data rate.

The weak pull-up current sources on each I/O pin and the NMOS pass transistors remain ON whenever the IC is enabled. If a channel’s external driver tri-states, the weak pull-up currents either keep the I/O pins high, or the current sources pull the I/O pins high if the last state was a low. In the latter case, each channel’s accelerators once again fire when either the $I/OV_L$ or the $I/OV_{CC}$ voltage crosses the accelerator’s high threshold level.

## Auto Direction Sensing

Each level translator channel independently and automatically determines the direction of data transfer without any external control signals. As described in “Principles of Operation” on page 7, a transition on either of the channel’s I/O pins momentarily defines that pin as an input, which then translates and drives that input signal to the channel’s corresponding pin on the other port (now the output). After a brief period of active driving, both I/O pins return to their weak “hold” mode, in which the next transition on either I/O pin determines the direction for the next transfer.

Auto sensing saves valuable processor GPIO pins and simplifies the software associated with the peripheral interface.

## Using Open Drain Drivers

The level translators’ accelerator based architecture works equally well when driven by push-pull or open drain type drivers. The low static pull-up current is easily overdriven by an active pull-down, and the feedback nature of the accelerators (that is, the accelerator firing in one direction also triggers the accelerator in the opposite direction) aids the passive pull-up when the input signal passes the accelerator’s high threshold. The pull-up current and load capacitance set the input signal rise time, and thus the maximum data rate. For slow data rates the internal pull-up current may suffice, but higher data rates or more heavily loaded signal lines may require an external pull-up resistor.

## Using External Bus Resistors

As mentioned in "Overview" on page 7, the ISL3034E incorporates I/O pin pull-up current sources when enabled, and I/O pin pull-up resistors in SHDN mode. Therefore, external pull-up or pull-down resistors are not necessary, and are not recommended, unless using high-speed open drain signaling.

## Power Supplies

### WIDE SUPPLY RANGE

The device operates across a wide range of supply voltages. $V_L$ is designed to connect to the supply of 1.5V, 1.8V, and 2.5V powered devices, while $V_{CC}$ is targeted for 2.5V and 3.3V components. Note that $V_{CC}$ must be greater than $V_L$ for proper operation.

### POWER SUPPLY SEQUENCING

Either $V_{CC}$ or $V_L$ can be powered up first, but the IC remains in SHDN until $V_{CC}$ exceeds $V_L$ by as much as 200mV. $V_L$ may exceed $V_{CC}$ by as much as 4V without causing any damage.

### I/O PIN INPUT THRESHOLDS VS SUPPLY VOLTAGE

Although the "Electrical Specifications" table on page 4 shows the I/O pin input thresholds ($V_{IH}$, $V_{IL}$) with a fixed delta from the supplies or GND, the thresholds are better represented as a percentage of the supplies. The typical I/O$V_{CC}$ $V_{IH}$ runs about 55% to 60% of $V_{CC}$, while the corresponding $V_{IL}$ runs about 33% of $V_{CC}$. The typical I/O$V_L$ $V_{IH}$ runs about 60% to 70% of $V_L$, while the corresponding $V_{IL}$ runs about 25% to 35% of $V_L$.

## Low Power SHDN Mode

The ISL3034E features a low power SHDN mode that tri-states all the I/O and output pins, considerably reduces current consumption, and enables any pull-up resistors on a port's I/O pins (see Table 1 on page 1). The device enters SHDN mode when the EN input switches low, or automatically when the $V_{CC}$ voltage drops below the $V_L$ voltage. The $V_L$ supply powers the EN circuitry.

## Unidirectional Level Translator with Heavy Loading

In applications where the ISL3034E is used as an unidirectional level translator, care must be taken to provide sufficient current drive if the output is heavily loaded. Figure 7 depicts a circuit where the output is loaded by some 500Ω. In this case, no matter how well $V_{CC}$ is buffered, the output oscillates, and the device might even turn into a latch-up condition. The internal feedback structure of the ISL3034E also causes this oscillation to appear at the input side (Figure 8).

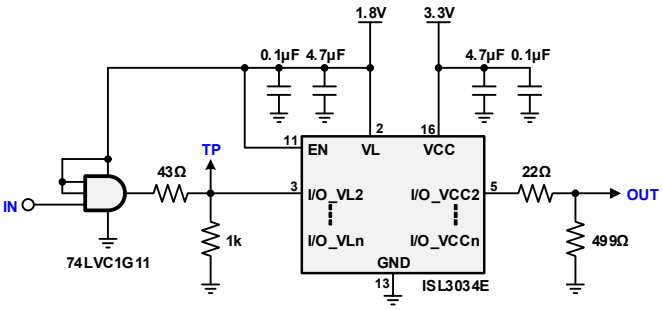



FIGURE 7. LOAD UNIDIRECTIONAL LEVEL TRANSLATOR WITH HEAVY LOADING OF THE UNBUFFERED OUTPUT

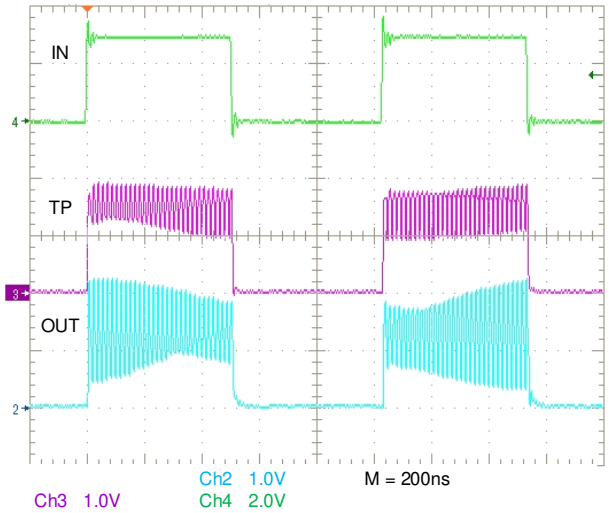



FIGURE 8. SIGNAL WAVEFORMS AT THE VARIOUS TEST POINTS OF THE CIRCUIT IN Figure 7

Figure 9 and Figure 10 show that to prevent the output from oscillations and latch-up conditions, a logic gate driver with enough current drive is inserted between the IC output and the low-impedance load.

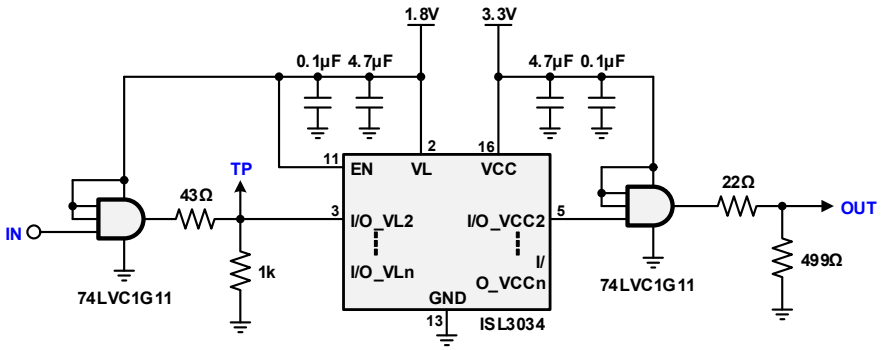



FIGURE 9. LOAD UNIDIRECTIONAL LEVEL TRANSLATOR WITH HEAVY LOADING OF A BUFFERED OUTPUT

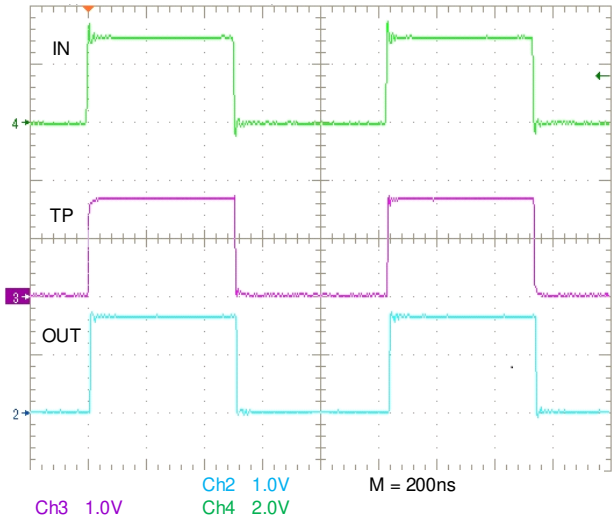



FIGURE 10. SIGNAL WAVEFORMS AT THE VARIOUS TEST POINTS OF THE CIRCUIT IN Figure 9

## Best-in-Class ESD Protection

All pins on the ISL3034E include class 3 (>12kV) Human Body Model (HBM) ESD protection structures, but the input and I/O pins incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM and ±15kV to IEC61000-4-2. The I/O$V_{CC}$ pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins or connecting a memory card can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up and without degrading the level shifting performance. This built-in ESD protection eliminates the need for board level protection structures (for example, transient suppression diodes) and the associated undesirable capacitive load they present. To ensure the full benefit of the built-in ESD protection, connect the IC's GND pin directly to a low impedance GND plane.

## IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (typically I/O$V_{CC}$ pins in memory card applications) but the ISL3034E features IEC61000 ESD protection on all logic and I/O pins (both I/O$V_L$ and I/O$V_{CC}$, as well as CLK pins). Unlike HBM and MM methods which only test each pin-to-pin combination without applying power, IEC61000 testing is also performed with the IC in its typical application configuration (power applied). The IEC61000 standard's lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into the device's pins allows the design of equipment meeting Level 4 criteria without the need for additional board level protection.

### AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. All the EN, and I/O pins withstand ±15kV air-gap discharges, relative to GND.

### CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The ISL3034E survives ±9kV contact discharges (relative to the GND pin) on the EN, CLK, and I/O pins.

## Layout and Decoupling Considerations

This level translator's high data rate and fast signal transitions require that the accelerators have high transient currents. Use short, low inductance supply traces and decouple within $1/8^{th}$ inch of the IC with very low impedance GND return paths.

## Typical Performance Curves

$V_{CC}$ = 3.3V, $V_L$ = 1.8V, $C_L$ = 15pF, $R_{SOURCE}$ = 150Ω, data rate = 100Mbps, push-pull driver, $T_A$ = +25°C; unless otherwise specified.

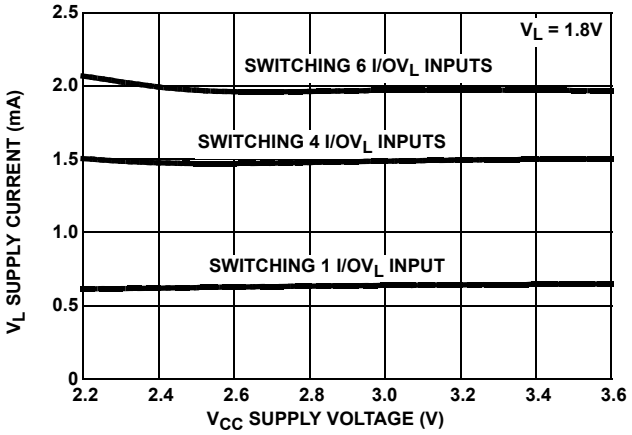



FIGURE 11. $V_L$ SUPPLY CURRENT vs $V_{CC}$ SUPPLY VOLTAGE

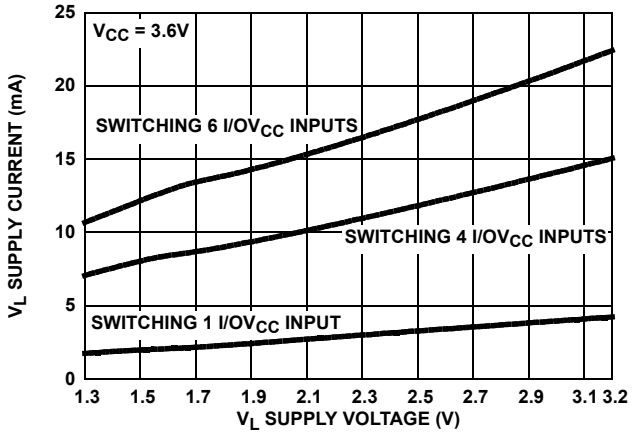



FIGURE 12. $V_L$ SUPPLY CURRENT vs $V_L$ SUPPLY VOLTAGE

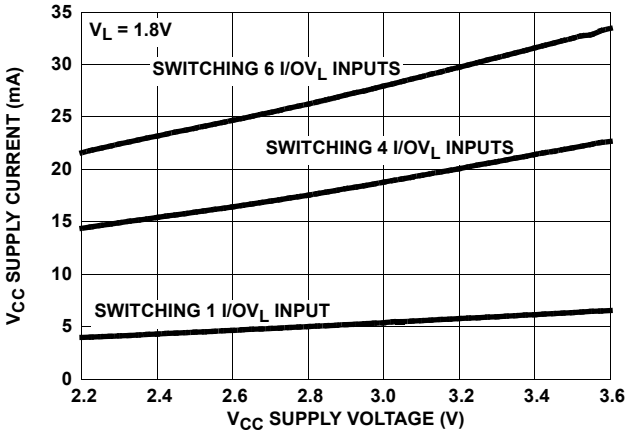



FIGURE 13. $V_{CC}$ SUPPLY CURRENT vs $V_{CC}$ SUPPLY VOLTAGE

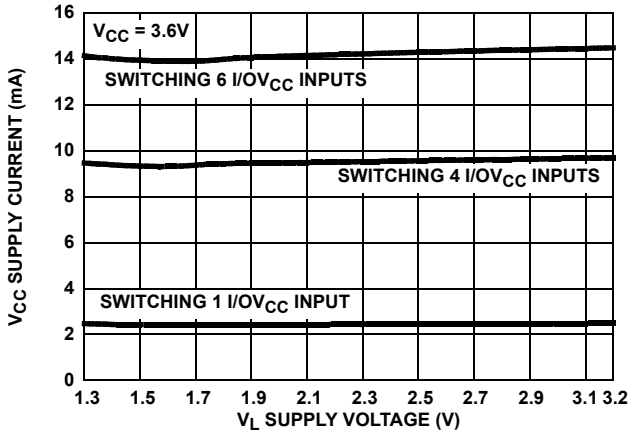



FIGURE 14. $V_{CC}$ SUPPLY CURRENT vs $V_L$ SUPPLY VOLTAGE

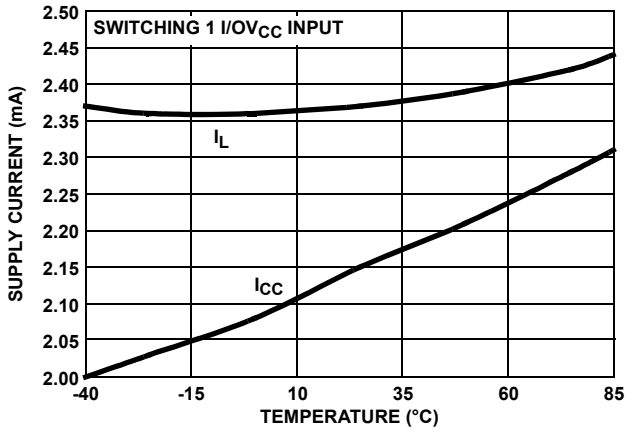



FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

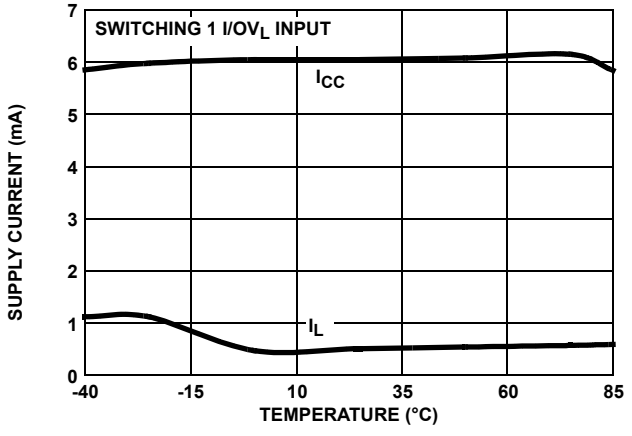



FIGURE 16. SUPPLY CURRENT vs TEMPERATURE

## Typical Performance Curves

$V_{CC}$ = 3.3V, $V_L$ = 1.8V, $C_L$ = 15pF, $R_{SOURCE}$ = 150Ω, data rate = 100Mbps, push-pull driver, $T_A$ = +25°C; unless otherwise specified. **(Continued)**

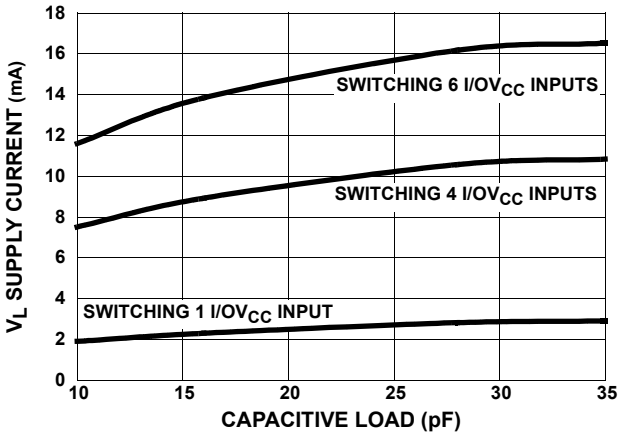



FIGURE 17. $V_L$ SUPPLY CURRENT vs I/O$V_L$ CAPACITIVE LOAD

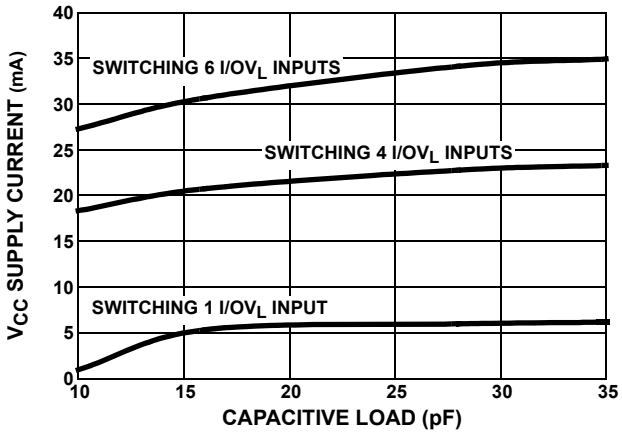



FIGURE 18. $V_{CC}$ SUPPLY CURRENT vs I/O$V_{CC}$ CAPACITIVE LOAD

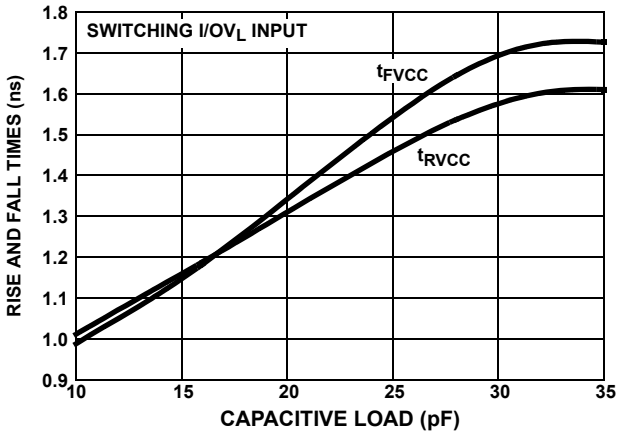



FIGURE 19. RISE/FALL TIME vs I/O$V_{CC}$ CAPACITIVE LOAD

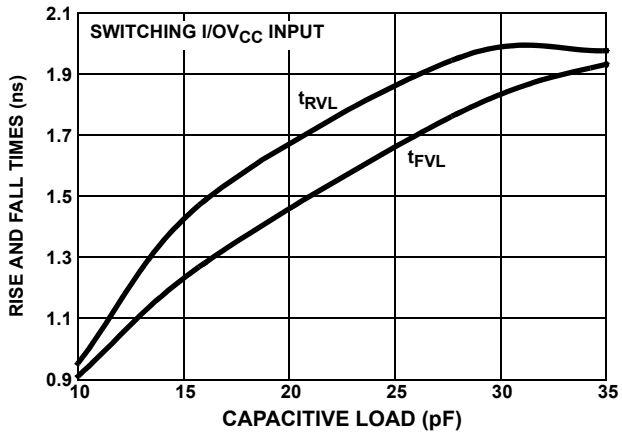



FIGURE 20. RISE/FALL TIME vs I/O$V_L$ CAPACITIVE LOAD

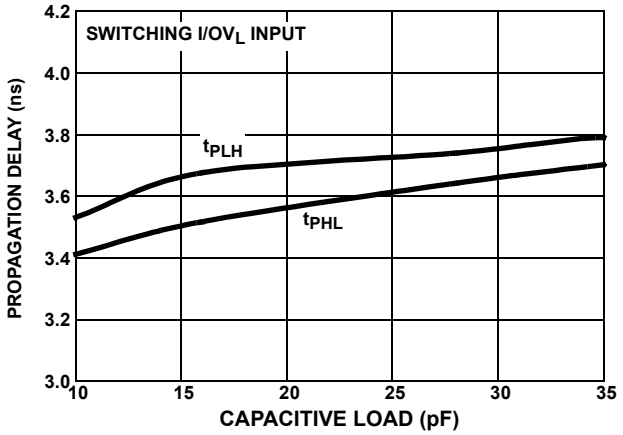



FIGURE 21. PROPAGATION DELAY vs I/O$V_{CC}$ CAPACITIVE LOAD

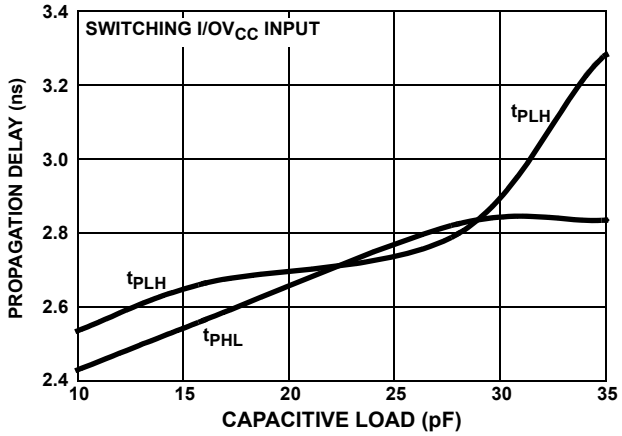



FIGURE 22. PROPAGATION DELAY vs I/O$V_L$ CAPACITIVE LOAD

## Typical Performance Curves

$V_{CC}$ = 3.3V, $V_L$ = 1.8V, $C_L$ = 15pF, $R_{SOURCE}$ = 150Ω, data rate = 100Mbps, push-pull driver, $T_A$ = +25°C; unless otherwise specified. **(Continued)**

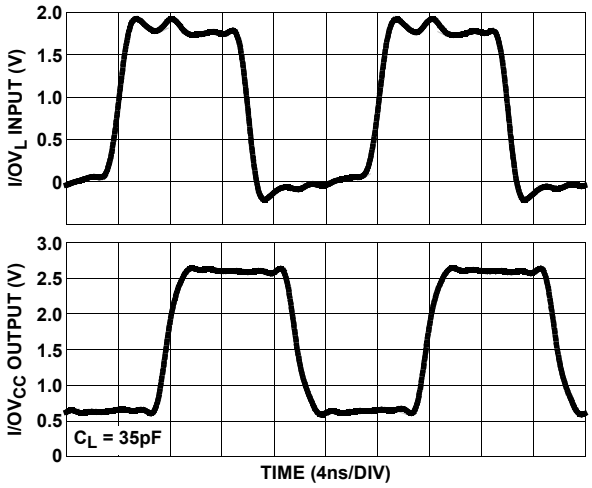



FIGURE 23. $I/OV_{CC}$ OUTPUT WAVEFORMS (100Mbps)

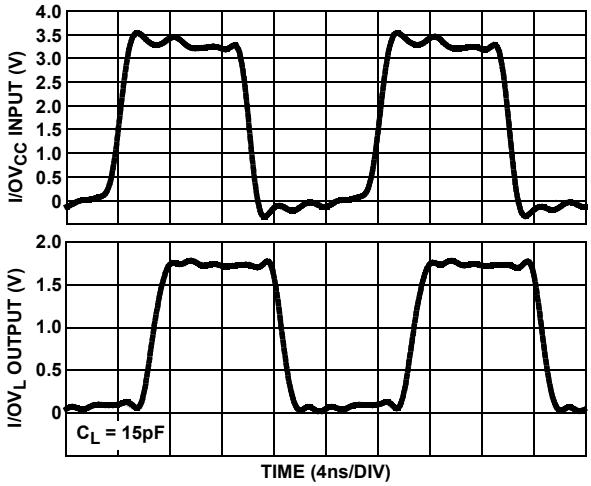



FIGURE 24. $I/OV_L$ OUTPUT WAVEFORMS (100Mbps)

## Die Characteristics

### Substrate and QFN Thermal Pad Potential (Powered Up):

GND

### Transistor Count:

2600

### Process:

Si Gate BiCMOS

# Revision History

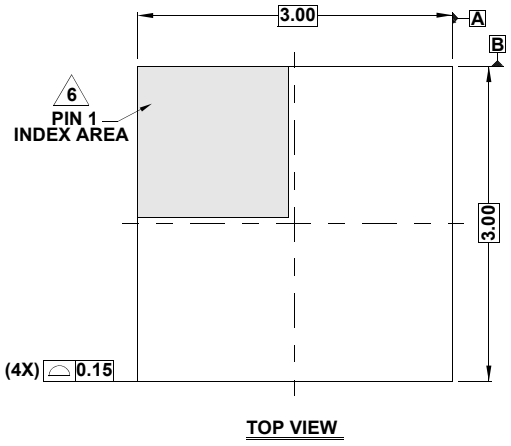
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| Nov 7, 2019 | FN6492.2 | Updated links throughout.<br>Added “Unidirectional Level Translator with Heavy Loading” section.<br>Updated disclaimer |
| May 3, 2018 | FN6492.1 | Removed information about obsolete ISL3035E and ISL3036E devices.<br>Updated datasheet title.<br>Added Related Literature section on page 1.<br>Updated Figure 1.<br>Added Note 4 and tape and reel quantity column to Ordering Information table on page 2.<br>Updated Package Outline Drawing L16.3x3A on page 12 to latest revision. Changes from previous version are as follows:<br>Updated to new format (removed dimensions table), added land pattern<br>Updated Package Outline Drawing L16.2.6x1.8A on page 13 to latest revision. Changes from previous version are as follows:<br>Changed value in Note 5 from 0.30mm to 0.25mm.<br>Removed Package Outline Drawing L14.3.5x3.5.<br>Added Revision History.<br>Applied new header/footer and added new Renesas disclaimer. |
| Mar 31, 2009 | FN6492.0 | Initial release. |

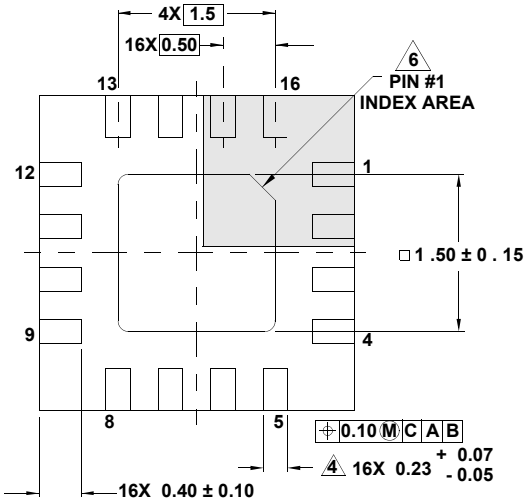
# Package Outline Drawings

For the most recent package outline drawing, see L16.3x3A.

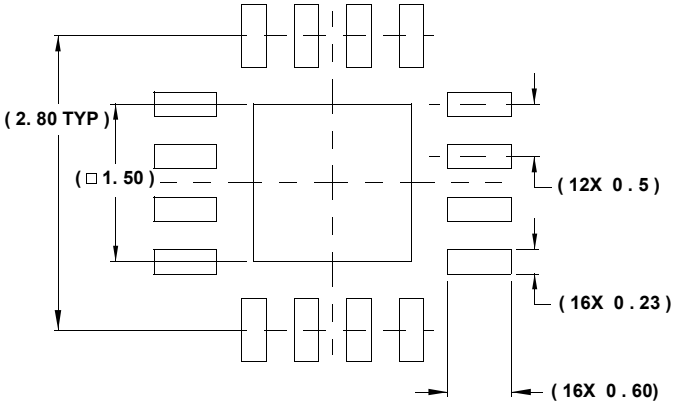
L16.3x3A
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 7/11



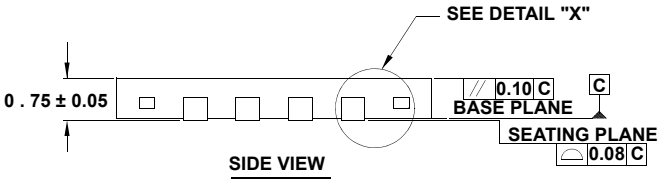

TOP VIEW



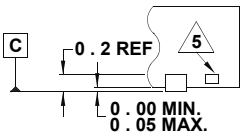

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN



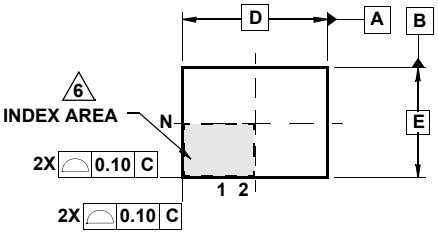

SIDE VIEW



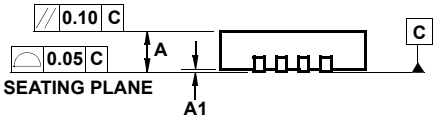

DETAIL "X"

**NOTES:**

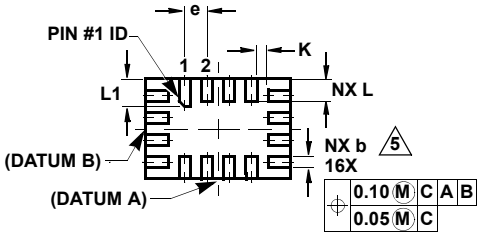
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



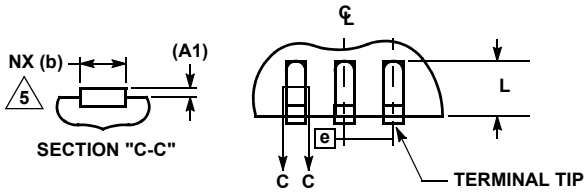

TOP VIEW

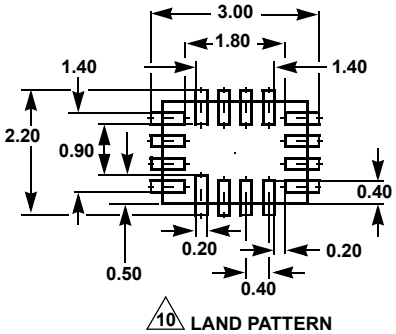



SIDE VIEW




BOTTOM VIEW




**L16.2.6x1.8A**
**16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.45 | 0.50 | 0.55 | - |
| A1 | - | - | 0.05 | - |
| A3 | | 0.127 REF | | - |
| b | 0.15 | 0.20 | 0.25 | 5 |
| D | 2.55 | 2.60 | 2.65 | - |
| E | 1.75 | 1.80 | 1.85 | - |
| e | | 0.40 BSC | | - |
| K | 0.15 | - | - | - |
| L | 0.35 | 0.40 | 0.45 | - |
| L1 | 0.45 | 0.50 | 0.55 | - |
| N | | 16 | | 2 |
| Nd | | 4 | | 3 |
| Ne | | 4 | | 3 |
| θ | 0 | - | 12 | 4 |

Rev. 6 1/14

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Technical Brief TB389.

**For the most recent package outline drawing, see L16.2.6x1.8A.**

## Notice

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## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

## Contact Information

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