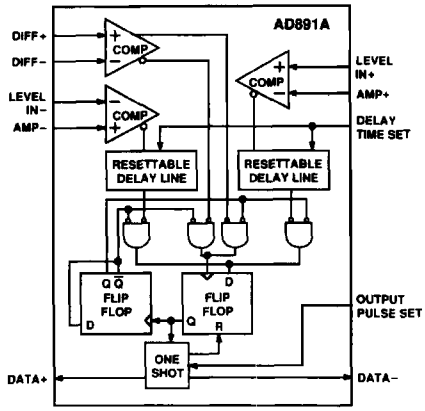
50 Mb/s Rigid Disk Data Qualifier

AD891A

FEATURES

- **Three Matched, Offset-Trimmed Comparators**
- **ECL Logic Permits 50 Mb/s Transfer Rates**
- **Three Levels of Data Qualification**
  - **Amplitude**
  - **Time Above Threshold**
  - **Polarity of Data**
- **100 ps Typical Additional Pulse Pairing**
- **Temperature Compensated Operation**
- **Compatible with 10KH ECL Logic**
- **One-Shot Period Set Using External Resistor**
- **Time Above Threshold Qualification Set Using an External Resistor**

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD891A disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891A provides three levels of data qualification. Level qualification is performed on alternating half-cycles of the data waveform using a user-defined threshold level which is applied to each of two comparators. The outputs of each comparator drive a user-programmable "resettable" delay-line. The "resettable" delay-line function allows the user to define the minimum time a data pulse must exceed the amplitude qualification level before a zero-crossing can be detected. The resettable delay-lines drive NAND gated flip-flops. A third zero-crossing comparator is employed to clock the NAND gated flip-flop. The NAND-gated flip-flop in turn drives the second flip-flop. The second flip-flop feeds back to the input of the NAND-gated flip-flop. The toggle action of the second flip-flop, therefore, provides alternate polarity data qualification. To ensure symmetric operation and low pulse pairing, all three comparators have trimmed offsets.

An external RLC passive delay-line/differentiator should be used with the AD891A; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

Each valid data pulse causes a one-shot to generate a pulse with a user-defined width. During the one-shot period the NAND-gated flip-flop is disabled, preventing detection of additional zero-crossing events. The one-shot also drives the ECL "Data Output" driver. The one-shot requires a single metal-film resistor to set its pulse width. Temperature stability is maintained by the use of an internal bandgap reference.

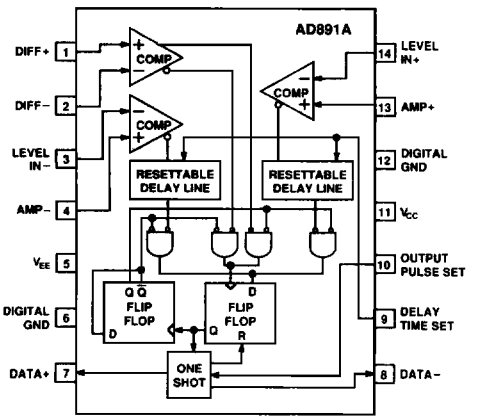
The AD891A's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10KH ECL logic levels. The AD891A can drive a properly terminated 75 Ω transmission line.

The AD891A is specified to operate over the commercial (0 to +70°C) temperature range. It is available in a 20-pin PLCC package (samples are available in a 14-pin side braze package).

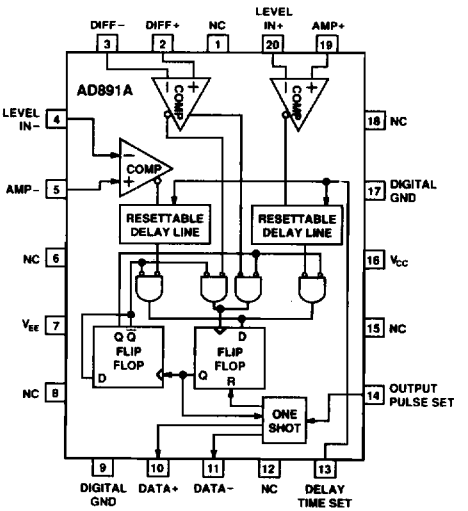
This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN CONFIGURATIONS

14-Pin Side Brazed Package (D)



20-Pin PLCC Package (P)



ORDERING GUIDE

Model	Package Description	Package Option*
AD891AJP	20-Pin PLCC	P-20A
AD891AJD	14-Pin Side Brazed Ceramic DIP (Samples Only)	D-14

*For outline information see Package Outline section.