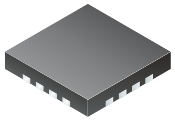


Wide Input Voltage, Eco-mode™, Single Synchronous Step-Down Controller

Check for Samples: TPS53219

FEATURES

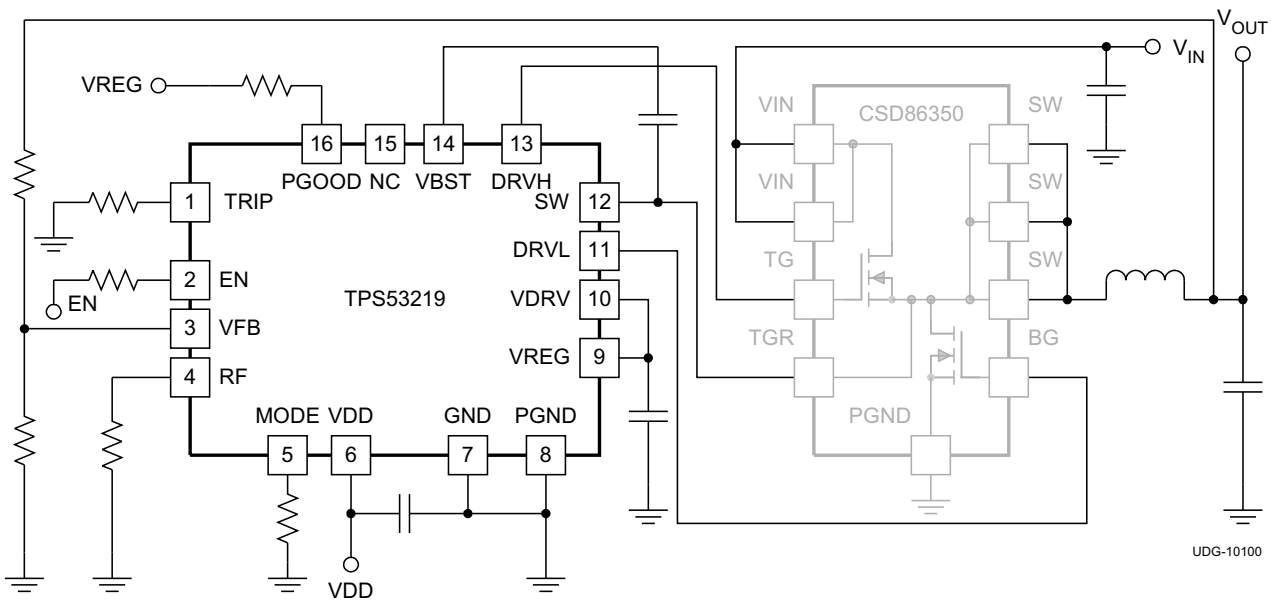
- **Wide Input Voltage Range: 4.5 V to 28 V**
- **Output Voltage Range: 0.6 V to 5.5 V**
- **Wide Output Load Range: 0 A to > 20 A**
- **Built-In 0.6-V Reference**
- **Built-In LDO Linear Voltage Regulator**
- **Auto-Skip Eco-mode™ for Light-Load Efficiency**
- **D-CAP™ Mode with 100-ns Load-Step Response**
- **Adaptive On-Time Control Architecture with 8 Selectable Frequency Settings**
- **4700ppm/°C $R_{DS(on)}$ Current Sensing**
- **0.7-ms, 1.4-ms, 2.8-ms and 5.6-ms Selectable Internal Voltage Servo Soft-Start**
- **Pre-Charged Start-up Capability**
- **Built-In Output Discharge**
- **Power Good Output**
- **Integrated Boost Switch**
- **Built-in OVP/UVP/OCP**
- **Thermal Shutdown (Non-latch)**
- **3 mm × 3mm QFN, 16-Pin (RGT) Package**

APPLICATIONS

- **Point-of-Load Systems**
  - **Storage Computer**
  - **Server Computer**
  - **Multi-Function Printer**
  - **Embedded Computing**

DESCRIPTION

The TPS53219 is small-sized single buck controller with adaptive on-time D-CAP™ mode control. The device is suitable for low output voltage, high current, PC system power rail and similar point-of-load (POL) power supplies in digital consumer products. The small package and minimal pin-count save space on the PCB, while the dedicated EN pin and pre-set frequency selections simplify the power supply design. The skip-mode at light load conditions, strong gate drivers and low-side FET $R_{DS(on)}$ current sensing supports low-loss and high efficiency, over a broad load range. The conversion input voltage (high-side FET drain voltage) range is between 3 V and 28 V, and the output voltage range is between 0.6 V and 5.5 V. The TPS53219 is available in a 16-pin, QFN package specified from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Eco-mode, D-CAP are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

TA	PACKAGE	ORDERING DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
–40°C to 85°C	Plastic QFN (RGT)	TPS53219RGTR	16	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS53219RGTT	16	Mini-reel	250	

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
Input voltage range	VBST		–0.3 to 37	V
	VBST(2)		–0.3 to 7	
	VDD		–0.3 to 28	
	SW	DC	–2.0 to 30	
		Pulse <20ns, E = 5 µJ	–7	
	VDRV, EN, TRIP, VFB, RF, MODE		–0.3 to 7	
Output voltage range	DRVH		–2.0 to 37	V
	DRVH(2)		–0.3 to 7	
	DRVL, VREG		–0.5 to 7	
	PGOOD		–0.3 to 7	
T_J	Junction temperature range		150	°C
T_{STG}	Storage temperature range		–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to the SW terminal

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53219 16-PIN RGT	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	51.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	85.4	
θ_{JB}	Junction-to-board thermal resistance	20.1	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	19.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage range	VBST	–0.1		34.5	V
	VDD	4.5		25	
	SW	–1.0		28	
	VBST(1)	–0.1		6.5	
	EN, TRIP, VFB, RF, VDRV, MODE	–0.1		6.5	
Output voltage range	DRVH	–1.0		34.5	V
	DRVH(1)	–0.1		6.5	
	DRVL, VREG	–0.3		6.5	
	PGOOD	–0.1		6.5	
T_A	Operating free-air temperature	–40		85	°C

(1) Voltage values are with respect to the SW terminal.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, VDD = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VDD}	VDD supply current	VDD current, T_A = 25°C, No Load, V_{EN} = 5 V, V_{VFB} = 0.630 V		420	590	µA
I_{VDDSDN}	VDD shutdown current	VDD current, T_A=25°C, No Load, V_{EN}=0 V			10	µA
INTERNAL REFERENCE VOLTAGE						
V_{VFB}	VFB regulation voltage	VFB voltage, CCM condition(1)		600		mV
V_{VFB}	VFB regulation voltage	T_A = 25°C	597	600	603	mV
		0°C ≤ T_A≤ 85°C	595.2	600.0	604.8	
		-40°C ≤ T_A≤ 85°C	594	600	606	
I_{VFB}	VFB input current	V_{VFB} = 0.630V, T_A = 25°C		0.002	0.200	µA
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50 mA		1.5	3	Ω
		Sink, I_{DRVH} = 50 mA		0.7	1.8	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50 mA		1.0	2.2	Ω
		Sink, I_{DRVL} = 50 mA		0.5	1.2	
t_{DEAD}	Dead time	DRVH-off to DRVL-on	7	17	30	ns
		DRVL-off to DRVH-on	10	22	35	
LDO OUTPUT						
V_{VREG}	LDO output voltage	0 mA ≤ I_{VREG} ≤ 50 mA	5.76	6.20	6.67	V
I_{VREG}	LDO output current(1)	Maximum current allowed from LDO			50	mA
V_{DO}	LDO drop out voltage	V_{VDD} = 4.5 V, I_{VREG} = 50 mA			364	mV
BOOT STRAP SWITCH						
V_{FBST}	Forward voltage	$V_{VREG-VBST}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{VBSTLK}	VBST leakagecurrent	V_{VBST} = 23 V, V_{SW} = 17 V, T_A = 25°C		0.01	1.5	µA
DUTY AND FREQUENCY CONTROL						
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	150	260	400	ns
$t_{ON(min)}$	Minimum on-time	V_{IN} = 17 V, V_{OUT} = 0.6 V, R_{RF} = 0 Ω to VREG, T_A = 25°C(1)		35		ns
SOFTSTART						
t_{SS}	Internal soft-start time	0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 39 kΩ		0.7		ms
		0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 100kΩ		1.4		
		0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 200 kΩ		2.8		
		0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 470 kΩ		5.6		
POWERGOOD						
V_{THPG}	PG threshold	PG in from lower	92.5%	96.0%	98.5%	
		PG in from higher	108%	111%	114%	
		PG hysteresis	2.5%	5.0%	7.8%	
R_{PG}	PG transistor on-resistance		15	30	50	Ω
$t_{PG(del)}$	PG delay after soft-start		0.8	1	1.2	ms

(1) Ensured by design. Not production tested.

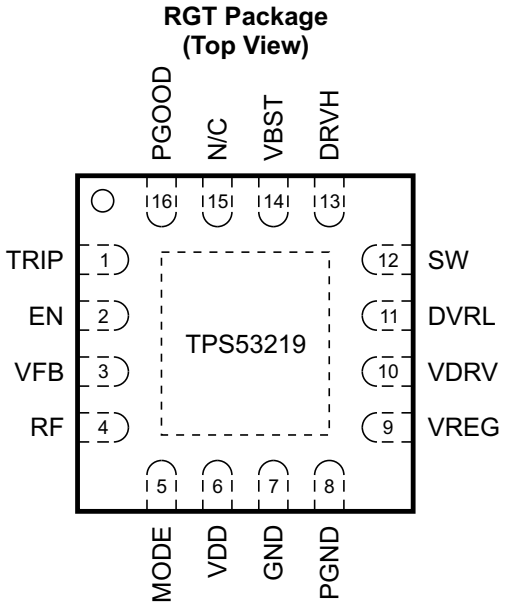
ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, VDD = 12 V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD AND SETTING CONDITIONS						
V_{EN}	EN voltage threshold	Enable	1.8			V
		Disable			0.5	
I_{EN}	EN input current	V_{EN} = 5 V			1.0	µA
f_{SW}	Switching frequency	R_{RF} = 0 Ω to GND, T_A = 25°C (1)	200	250	300	kHz
		R_{RF} = 187 kΩ to GND, T_A = 25°C (1)	250	300	350	
		R_{RF} = 619 kΩ to GND, T_A = 25°C (1)	350	400	450	
		R_{RF} = Open, T_A = 25°C (1)	450	500	550	
		R_{RF} = 866 kΩ to V_{REG}, T_A = 25°C (1)	580	650	720	
		R_{RF} = 309 kΩ to V_{REG}, T_A = 25°C (1)	670	750	820	
		R_{RF} = 124 kΩ to V_{REG}, T_A = 25°C (1)	770	850	930	
		R_{RF} = 0 Ω to V_{REG}, T_A = 25°C (1)	880	970	1070	
VO DISCHARGE						
I_{Dischg}	VO discharge current	V_{EN} = 0 V, V_{SW} = 0.5 V	5	13		mA
PROTECTION: CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIP} = 1 V, T_A = 25°C	9	10	11	µA
TC_{ITRIP}	TRIP current temp. coef.	T_A = 25°C (2)		4700		ppm/°C
V_{TRIP}	Current limit threshold setting range	$V_{TRIP-GND}$ voltage	0.2		3	V
V_{OCL}	Current limit threshold	V_{TRIP} = 3.0 V	355	375	395	mV
		V_{TRIP} = 1.6 V	185	200	215	
		V_{TRIP} = 0.2 V	17	25	33	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3.0 V	–406	–375	–355	mV
		V_{TRIP} = 1.6 V	–215	–200	–185	
		V_{TRIP} = 0.2 V	–33	–25	–17	
$V_{AZC(adj)}$	Auto zero cross adjustable range	Positive	3	15		mV
		Negative		–15	–3	
PROTECTION: UVP AND OVP						
V_{OVP}	OVP trip threshold voltage	OVP detect	115%	120%	125%	
$t_{OVP(del)}$	OVP propagation delay time	VFB delay with 50-mV overdrive		1		µs
V_{UVP}	Output UVP trip threshold voltage	UVP detect	65%	70%	75%	
$t_{UVP(del)}$	Output UVP propagation delay time		0.8	1	1.2	ms
$t_{UVP(en)}$	Output UVP enable delay time	from EN to UVP workable, R_{MODE} = 39 kΩ	2.00	2.55	3.00	ms
UVLO						
V_{UVVREG}	VREG UVLO threshold	Wake up	4.00	4.18	4.50	V
		Hysteresis		0.25		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (2)		145		°C
		Hysteresis (2)		10		

(1) Not production tested. Test conditions are V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} =10 A and using the application circuit shown in Figure 17 and Figure 18.
(2) Ensured by design. Not production tested

PIN DESCRIPTION

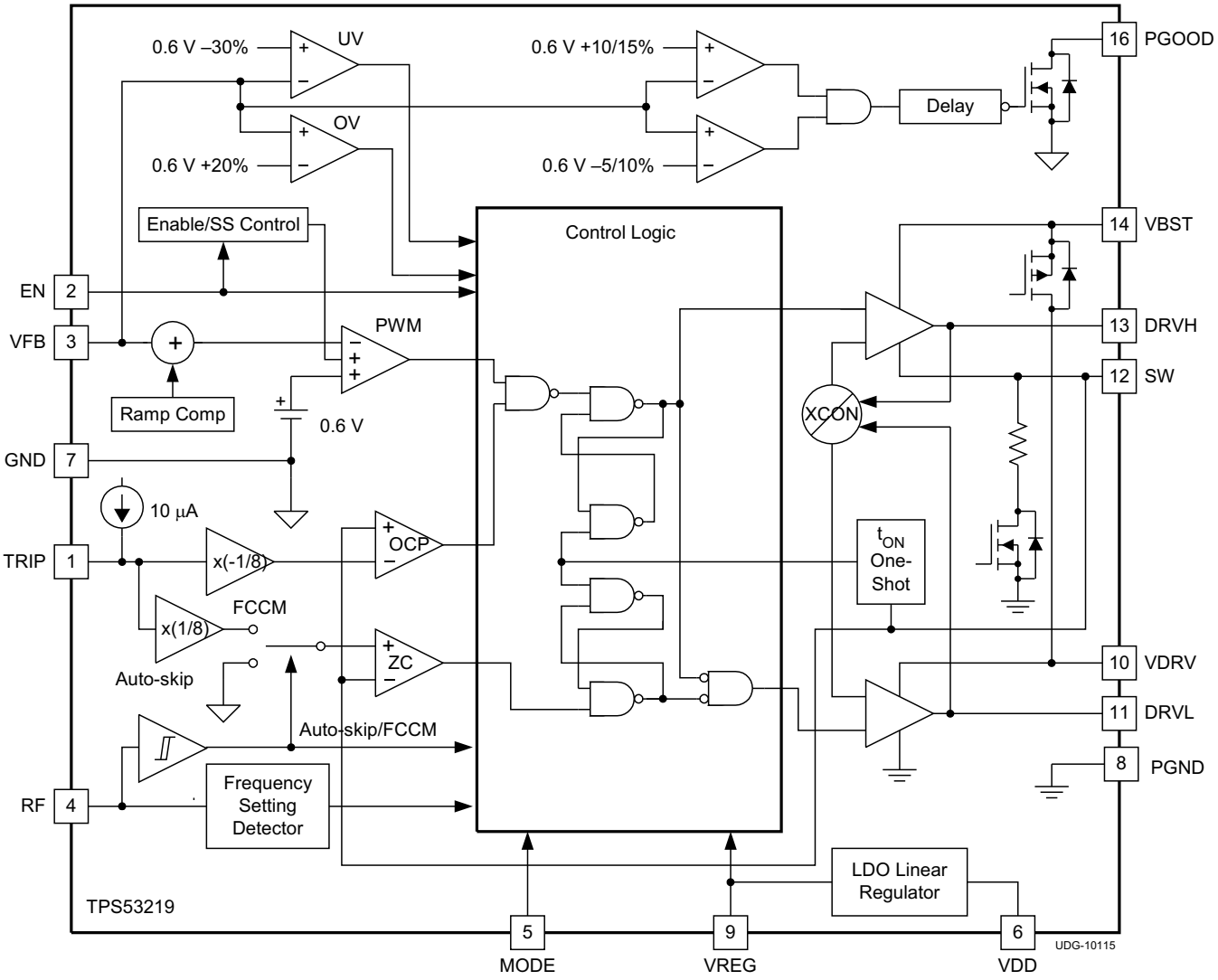


PIN FUNCTIONS

PIN NAME	PIN NO.	I/O/P(1)	DESCRIPTION
DRVH	13	O	High-side MOSFET driver output. The SW node referenced floating driver. The gate drive voltage is defined by the voltage across VBST to SW node bootstrap flying capacitor.
DRVL	11	O	Synchronous MOSFET driver output. The PGND referenced driver. The gate drive voltage is defined by VDRV voltage.
EN	2	I	Enable pin
GND	7	–	Ground pin
MODE	5	I	Soft-start and Skip/CCM selection. Connect a resistor to select soft-start time using Table 1 . The soft-start time is detected and stored into internal register during start-up.
NC	15	–	No connection.
PGOOD	16	O	Open drain power good flag. Provides 1-ms start up delay after the VFB pin voltage falls within specified limits. When VFB goes out specified limits PGOOD goes low within 10 µs.
PGND	8	G	Power ground.
RF	4	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using Table 2. The switching frequency is detected and stored during the startup.
SW	12	P	Output of converted power. Connect this pin to the output inductor.
TRIP	1	I	OCL detection threshold setting pin. 10 µA at room temp, 4700ppm/°C current is sourced and set the OCL trip voltage as follows. $V_{OCL}=V_{TRIP}/8$ ($V_{TRIP} \le 3$ V, $V_{OCL} \le 375$ mV)
VBST	14	P	Supply input for high-side FET gate driver (boost terminal). Connect a capacitor from this pin to SW-node. Internally connected to VREG via bootstrap MOSFET switch.
VDD	6	P	Controller power supply input.
VDRV	10	I	Gate drive supply voltage input. Connect to VREG if using LDO output as gate drive supply.
VFB	3	I	Output feedback input. Connect this pin to V_{OUT} through a resistor divider.
VREG	9	O	6.2-V LDO output

(1) I=Input, O=Output, P=Power

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

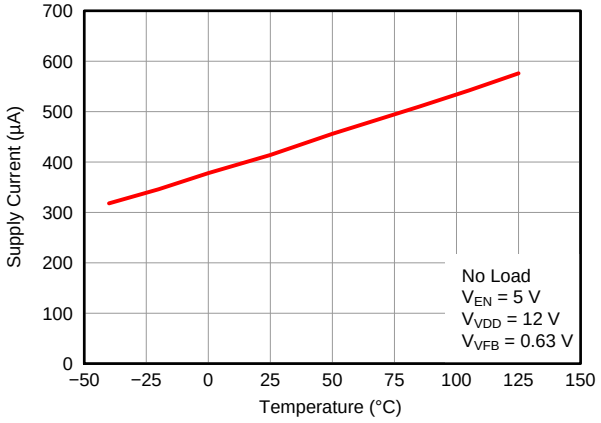


Figure 1. VDD Supply Current vs Temperature

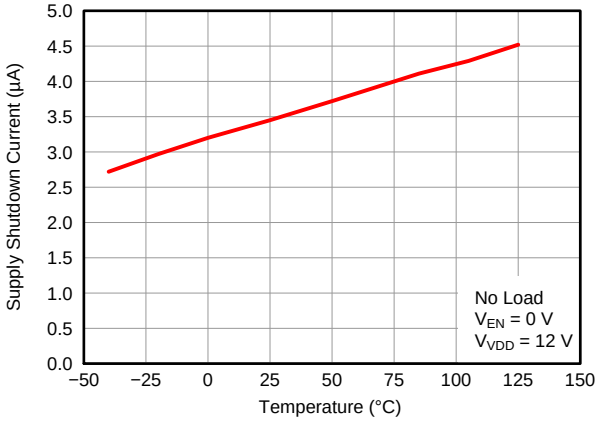


Figure 2. VDD Shutdown Current vs Temperature

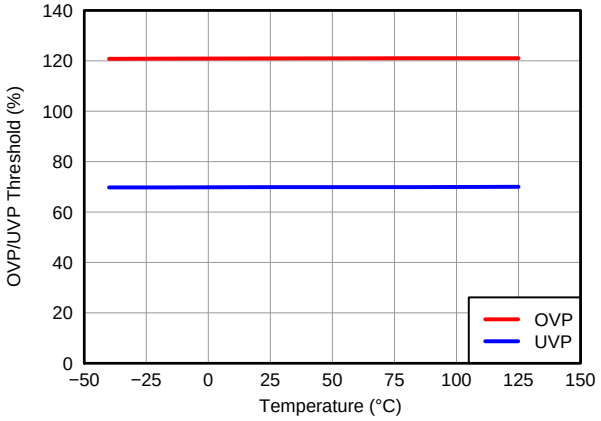


Figure 3. OVP/UVP Threshold vs Temperature

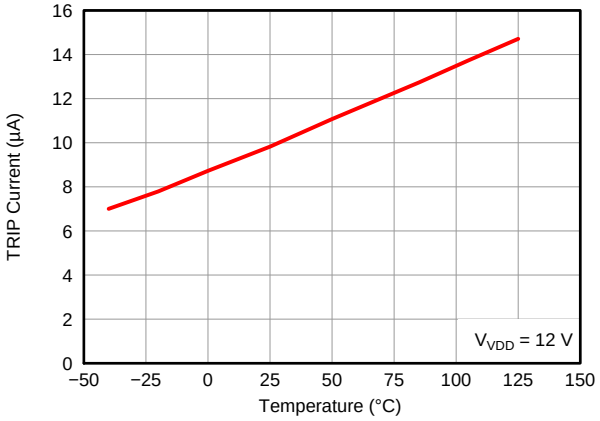


Figure 4. TRIP Pin Current vs Temperature

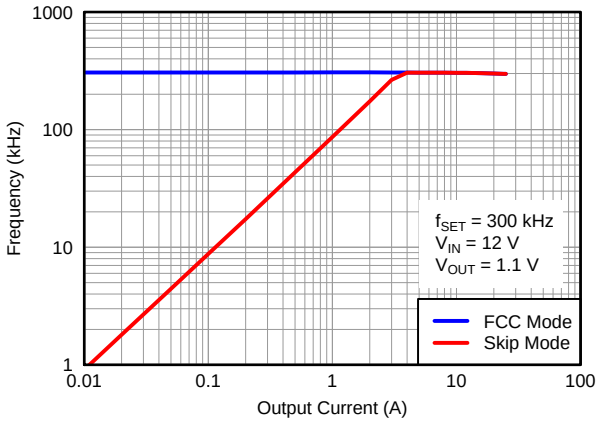


Figure 5. Switching Frequency vs Output Current

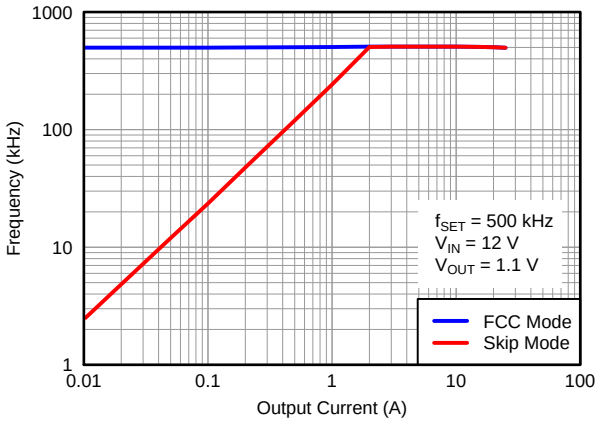


Figure 6. Switching Frequency vs Output Current

TYPICAL CHARACTERISTICS (continued)

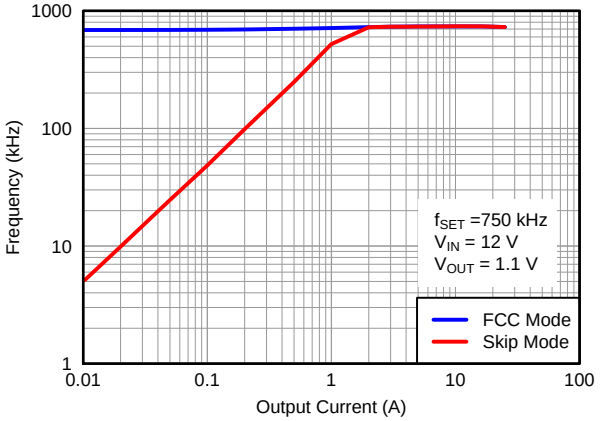


Figure 7. Switching Frequency vs Output Current

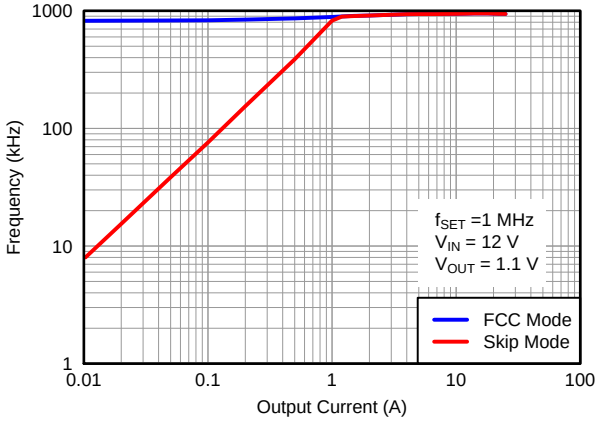


Figure 8. Switching Frequency vs Output Current

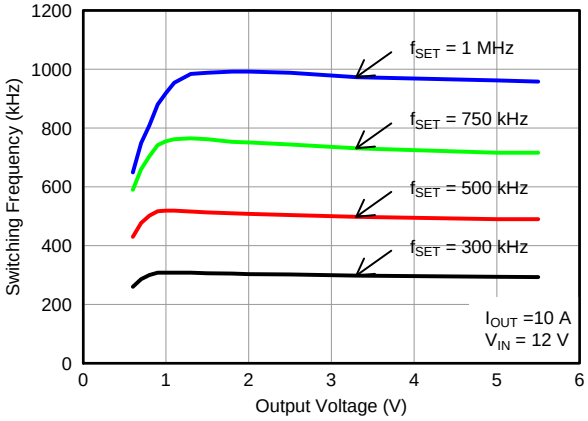


Figure 9. Switching Frequency vs Output Voltage

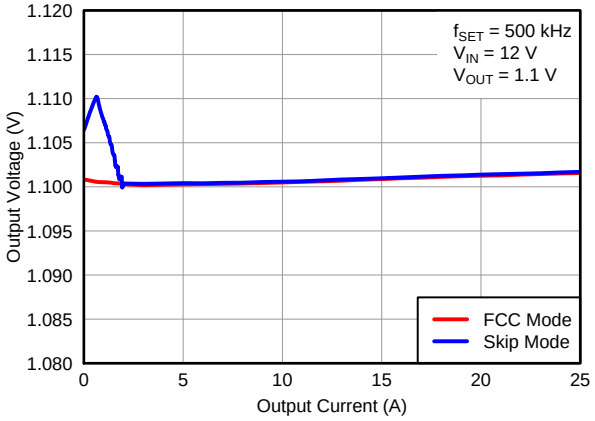


Figure 10. Output Voltage vs Output Current

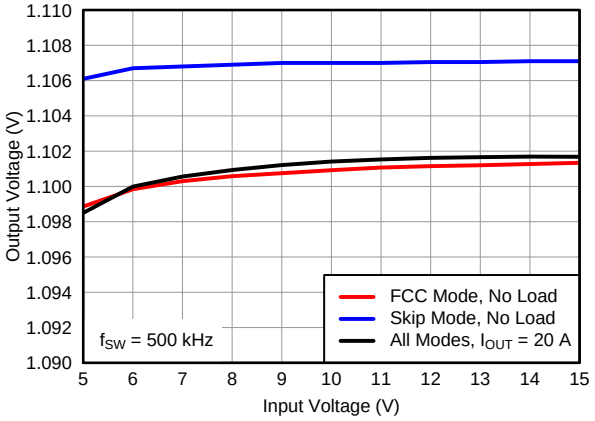


Figure 11. Output Voltage vs Input Voltage

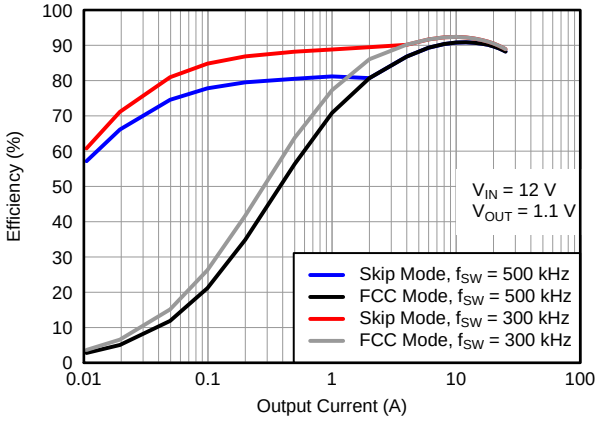


Figure 12. Efficiency vs Output Current

TYPICAL CHARACTERISTICS (continued)

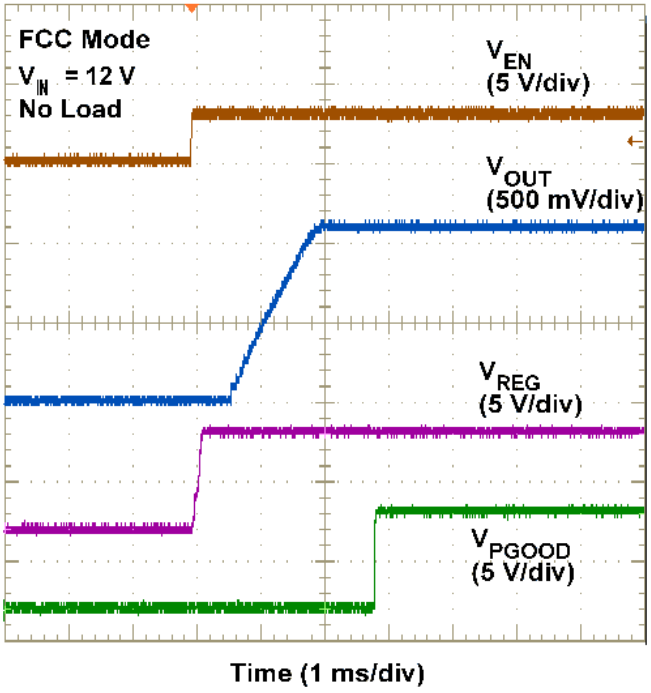


Figure 13. Start up Waveform)

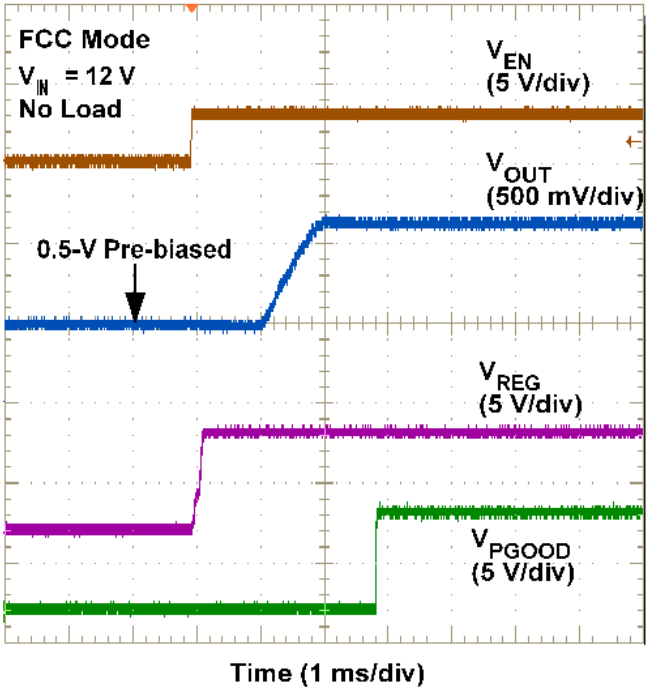


Figure 14. Pre-bias Start up Waveform)

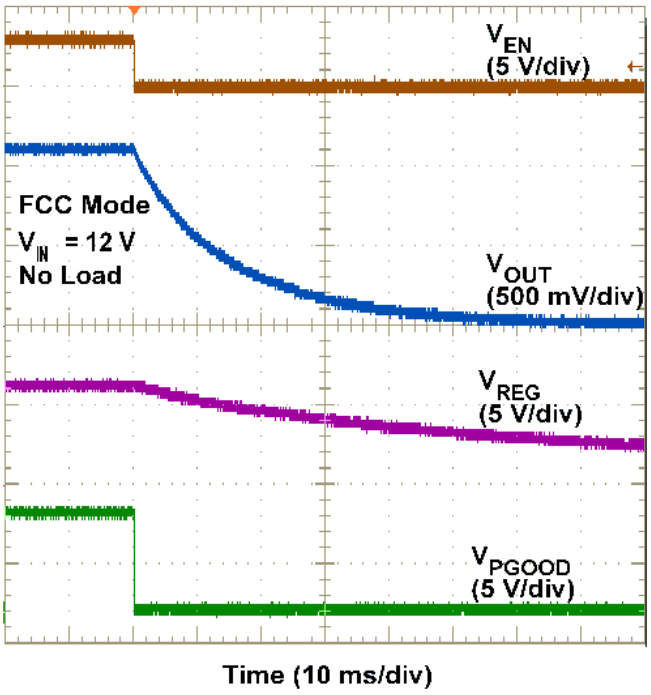


Figure 15. Turn Off Waveform

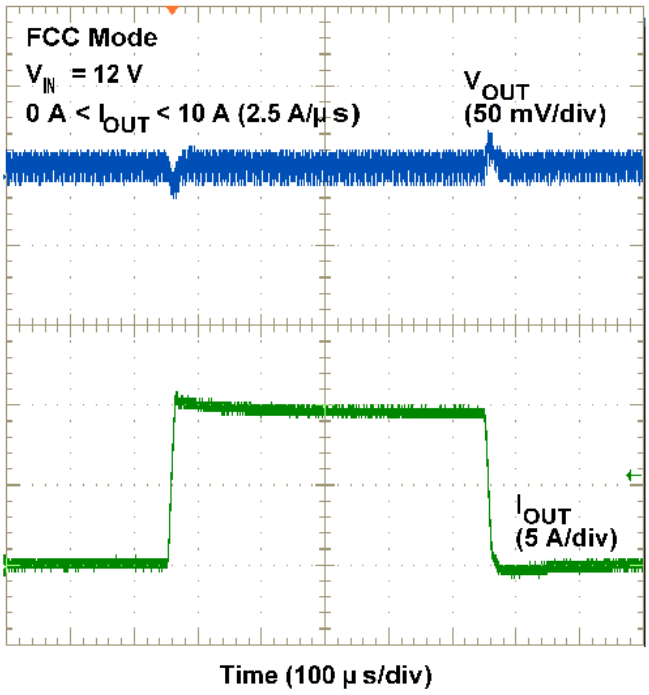


Figure 16. Load Transient Response

APPLICATION CIRCUIT DIAGRAM

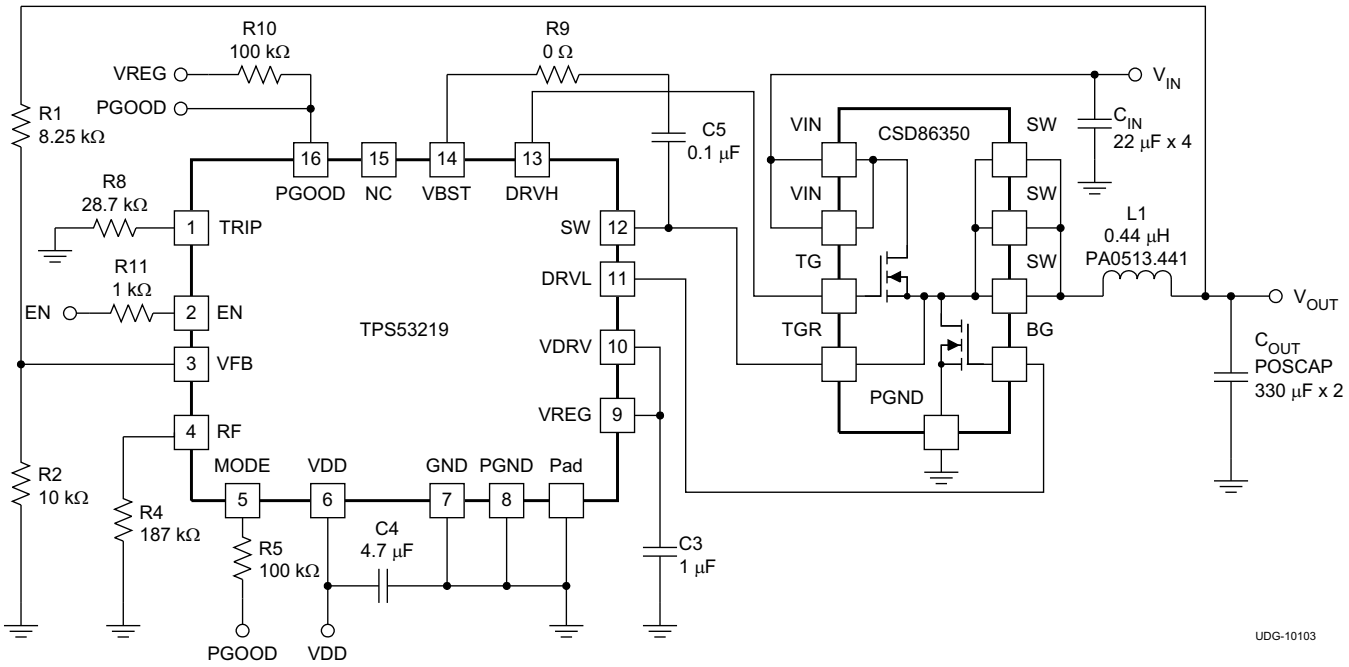


Figure 17. Typical Application Circuit Diagram with Power Block

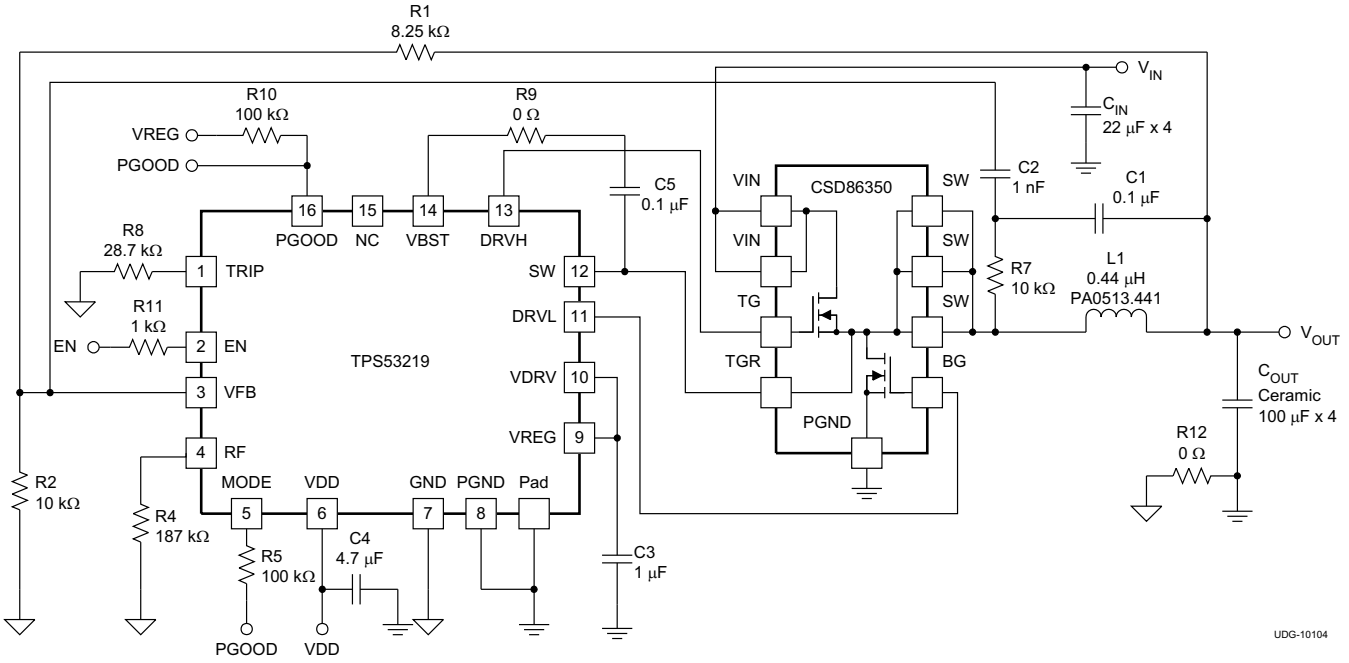


Figure 18. Typical Application Circuit Diagram with Ceramic Output Capacitors

General Description

The TPS53219 is a high-efficiency, single channel, synchronous buck regulator controller suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 3 V up to 28V. The D-CAP™ mode uses the ESR of the output capacitor(s) to sense the device current . One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The TPS53219 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms. The strong gate drivers allow low $R_{DS(on)}$ FETs for high-current applications.

Enable and Soft-Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.4 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 6.2 V at the VREG pin. The controller then uses the first 250 µs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. However, switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

Table 1. Soft-Start and MODE

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM (1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device goes into Forced CCM after PGOOD becomes high.

Adaptive On-Time D-CAP™ Control

The TPS53219 does not have a dedicated oscillator that determines switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT}/V_{IN}$).

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in Table 2. (Leaving the resistance open sets the switching frequency to 500 kHz.)

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS	SWITCHING FREQUENCY (kHz)
0 Ω to GND	250
187 kΩ to GND	300
619 kΩ to GND	400
Open	500
866 kΩ to VREG	650
309 kΩ to VREG	750
124 kΩ to VREG	850
0 Ω to VREG	970

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a *set* signal to terminate the off time (turn off the low-side MOSFET and turn on high-side MOSFET). The *set* signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 19.

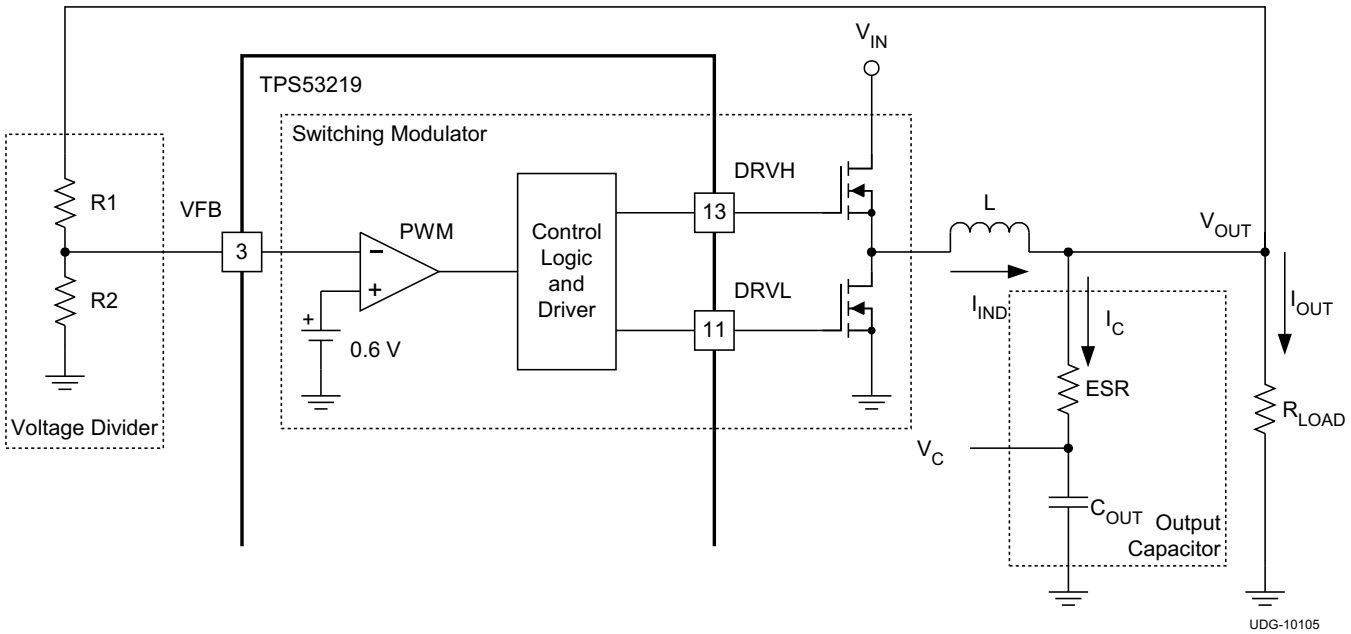


Figure 19. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}} \quad (1)$$

For the loop stability, the 0 dB frequency, f_0, defined below must be lower than ¼ of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \quad (2)$$

According to the equation above, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance on the order of several 100 µF and ESR in range of 10 mΩ. These yields an f_0 on the order of 100 kHz or less and a more stable loop. However, ceramic capacitors have an f_0 at more than 700 kHz, and require special care when used with this modulator. An application circuit for ceramic capacitor is described in section External Parts Selection with All Ceramic Output Capacitors.

Ramp Signal

The TPS53219 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the S/N ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

Light Load Condition in Auto-Skip Operation

While the MODE pin is pulled low via R_{MODE}, TPS53219 automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{O(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the $IO_{(LL)}$ given in Equation 3. For example, it is 60 kHz at $IO_{(LL)}$/5 if the frequency setting is 300 kHz.

Adaptive Zero Crossing

The TPS53219 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

Output Discharge Control

When EN becomes low, the TPS53219 discharges output capacitor using internal MOSFET connected between the SW pin and the PGND pin while the high-side and low-side MOSFETs are maintained in the *OFF* state. The typical discharge resistance is 40 Ω. The soft discharge occurs only as EN becomes low. After VREG becomes low, the internal MOSFET turns off and the discharge function becomes inactive.

Low-Side Driver

The low-side driver is designed to drive high-current low-$R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 1.0 Ω for VDRV to DRVL and 0.5 Ω for DRVL to GND. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. The bias voltage VDRV can be delivered from 6.2 V VREG supply or from external power source. The instantaneous drive current is supplied by an input capacitor connected between the VDRV and PGND pins.

The average low-side gate drive current is calculated in Equation 4.

$$I_{GL} = C_{GL} \times V_{VDRV} \times f_{SW} \quad (4)$$

High-Side Driver

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, the bias voltage is delivered from the VDRV pin supply. The average drive current is calculated using Equation 5.

$$I_{GH} = C_{GH} \times V_{VDRV} \times f_{SW} \quad (5)$$

The instantaneous drive current is supplied by the flying capacitor between VBST and SW pins. The drive capability is represented by internal resistance, which is 1.5 Ω for VBST to DRVH and 0.7 Ω for DRVH to SW.

The driving power which needs to be dissipated from TPS53219 package.

$$P_{DRV} = (I_{GL} + I_{GH}) \times V_{VDRV} \quad (6)$$

Power Good

The TPS53219 has power-good output that indicates *high* when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% or –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-µs) internal delay. The power-good output is an open drain output and must be pulled up externally.

Current Sense and Overcurrent Protection

TPS53219 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53219 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 7. Note that the V_{TRIP} is limited up to approximately 3 V internally.

$$V_{TRIP}\left(mV\right) = R_{TRIP}\left(k\Omega\right) \times I_{TRIP}\left(\mu A\right) \tag{7}$$

The inductor current is monitored by the voltage between GND pin and SW pin so that SW pin should be connected to the drain terminal of the low-side MOSFET properly. I_{TRIP} has 4700 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. The GND pin is used as the positive current sensing node. The GND pin should be connected to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

As the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in Equation 8.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{8}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7 ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

During the CCM, the negative current limit (NCL) protects the external FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity. Note that the threshold still represents the valley value of the inductor current.

Overvoltage and Undervoltage Protection

TPS53219 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53219 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7 ms soft-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches UV threshold, then both high-side MOSFET and low-side MOSFET driver will be OFF and the device restarts after an hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

UVLO Protection

The TPS53219 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than the UVLO threshold voltage, the switch mode power supply shuts off. This is non-latch protection.

Thermal Shutdown

The TPS53219 uses temperature monitoring. If the temperature exceeds the threshold value (typically 145°C), the device is shut off. This is non-latch protection.

External Components Selection

Selecting external components is a simple process using D-CAP™ Mode.

1. CHOOSE THE INDUCTOR

The inductance should be determined to give the ripple current of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves the signal-to-noise ratio and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (9)$$

The inductor also requires a low DCR to achieve good efficiency. It also requires enough room above the peak inductor current before saturation. The peak inductor current can be estimated in Equation 10.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (10)$$

2. CHOOSE THE OUTPUT CAPACITOR(S)

When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy Equation 2. For jitter performance, Equation 11 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10\,mV \times (1 - D)}{0.6\,V \times I_{IND(ripple)}} = \frac{10\,mV \times L \times f_{SW}}{0.6\,V} = \frac{L \times f_{SW}}{60} \ (\Omega) \quad (11)$$

where

- D is the duty factor
- the required output ripple slope is approximately 20 mV per t_{SW} (switching period) in terms of VFB terminal voltage

3. DETERMINE THE VALUE OF R1 AND R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 19. R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is between 10 kΩ and 20 kΩ. Determine R1 using Equation 12.

$$R1 = \frac{V_{OUT} - \left(\frac{I_{IND(ripple)} \times ESR}{2}\right) - 0.6}{0.6} \times R2 \quad (12)$$

External Parts Selection with All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in Equation 2 cannot be satisfied. The ripple injection approach as shown in Figure 18 is implemented to increase the ripple on the VFB pin and make the system stable. C2 can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

The increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from V_{OUT} and they can be calculated using Equation 13 and Equation 14.

$$V_{INJ(SW)} = \frac{(V_{IN} - V_{OUT})}{R7 \times C1} \times \frac{D}{f_{SW}} \quad (13)$$

$$V_{INJ(OUT)} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (14)$$

The DC value of VFB can be calculated by Equation 15.

$$V_{FB} = 0.6 + \frac{\left(V_{INJ(SW)} + V_{INJ(OUT)}\right)}{2} \quad (15)$$

And the resistor divider value can be determined by Equation 16.

$$R1 = \frac{(V_{OUT} - V_{FB})}{V_{FB}} \times R2 \quad (16)$$

LAYOUT CONSIDERATIONS:

Certain points must be considered before starting a layout work using the TPS53219.

- Inductor, V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - The most important loop to minimize the area of is the path from the V_{IN} capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible.
  - The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of VOUT capacitor(s) at ground as close as possible.
  - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from VDRV capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND of the device, and back to source of the low-side MOSFET through ground. Connect negative node of VDRV capacitor, source of the low-side MOSFET and PGND of the device at ground as close as possible.
- Because the TPS53219 controls output voltage referring to voltage across V_{OUT} capacitor, the top-side resistor of the voltage divider should be connected to the positive node of V_{OUT} capacitor. In a same manner both bottom side resistor and GND of the device should be connected to the negative node of V_{OUT} capacitor. The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid via(s) between these resistors and the device.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the frequency setting resistor from RF pin to ground, or to the PGOOD pin, and make the connections as close as possible to the device. The trace from the RF pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as switch node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in Figure 18) from the terminal of ceramic output capacitor. The AC coupling capacitor (C7 in Figure 18) can be placed near the device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53219RGTR	NRND	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53219	
TPS53219RGTT	NRND	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53219	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

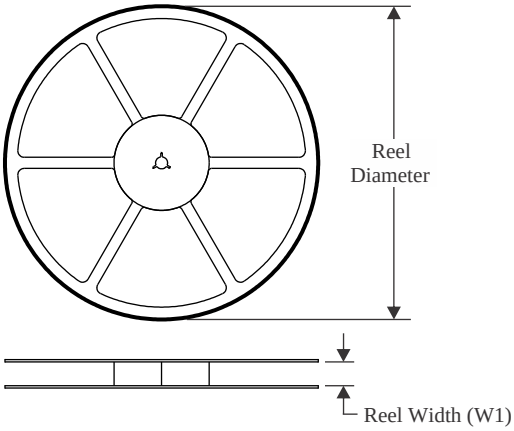
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

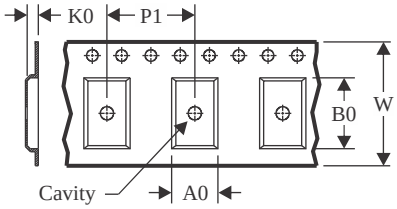
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

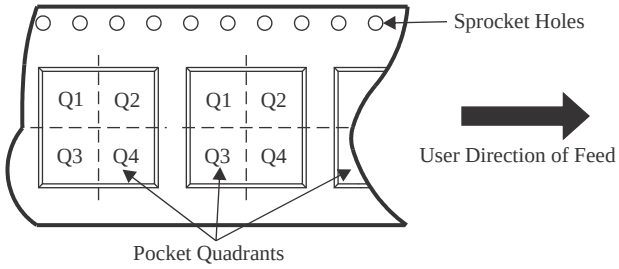


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

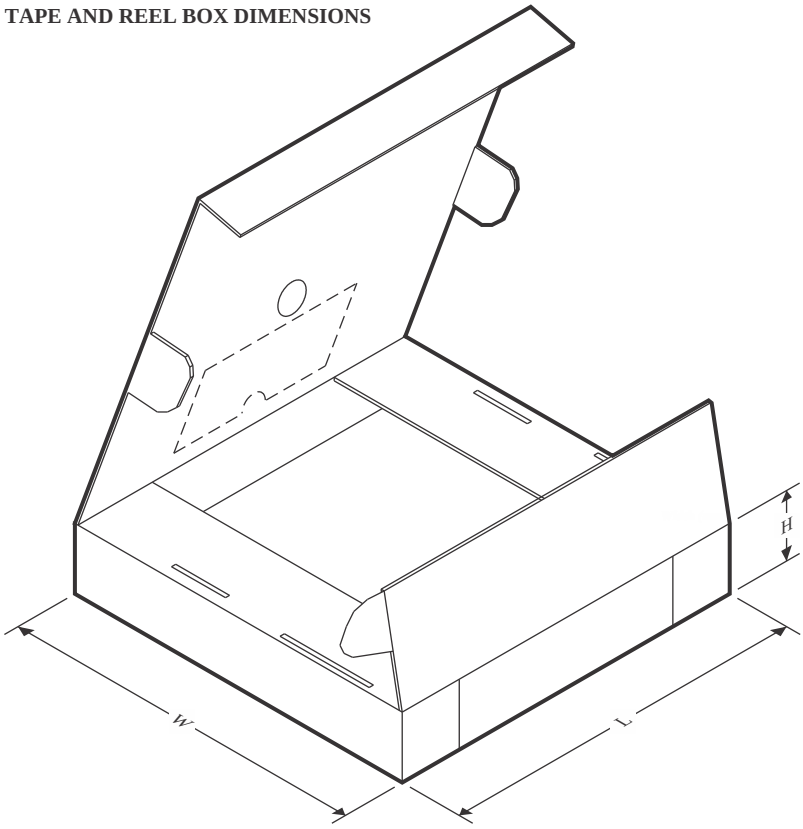
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53219RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53219RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

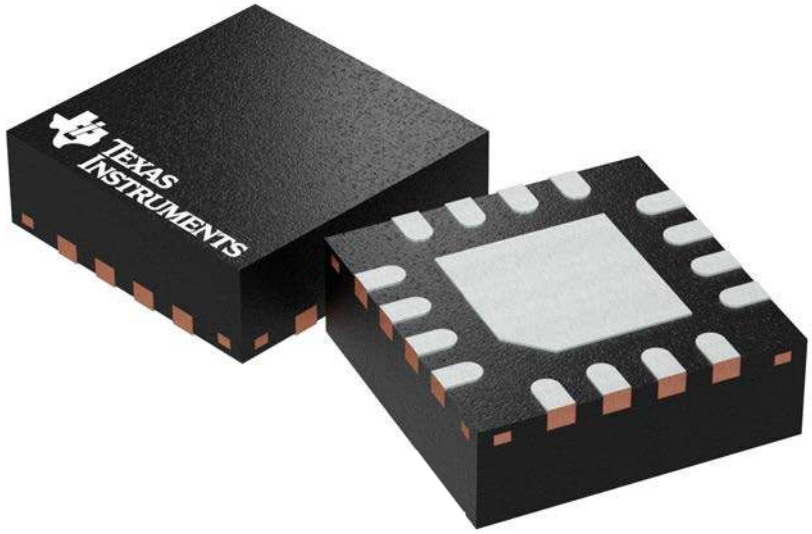


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53219RGTR	VQFN	RGT	16	3000	335.0	335.0	25.0
TPS53219RGTT	VQFN	RGT	16	250	182.0	182.0	20.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



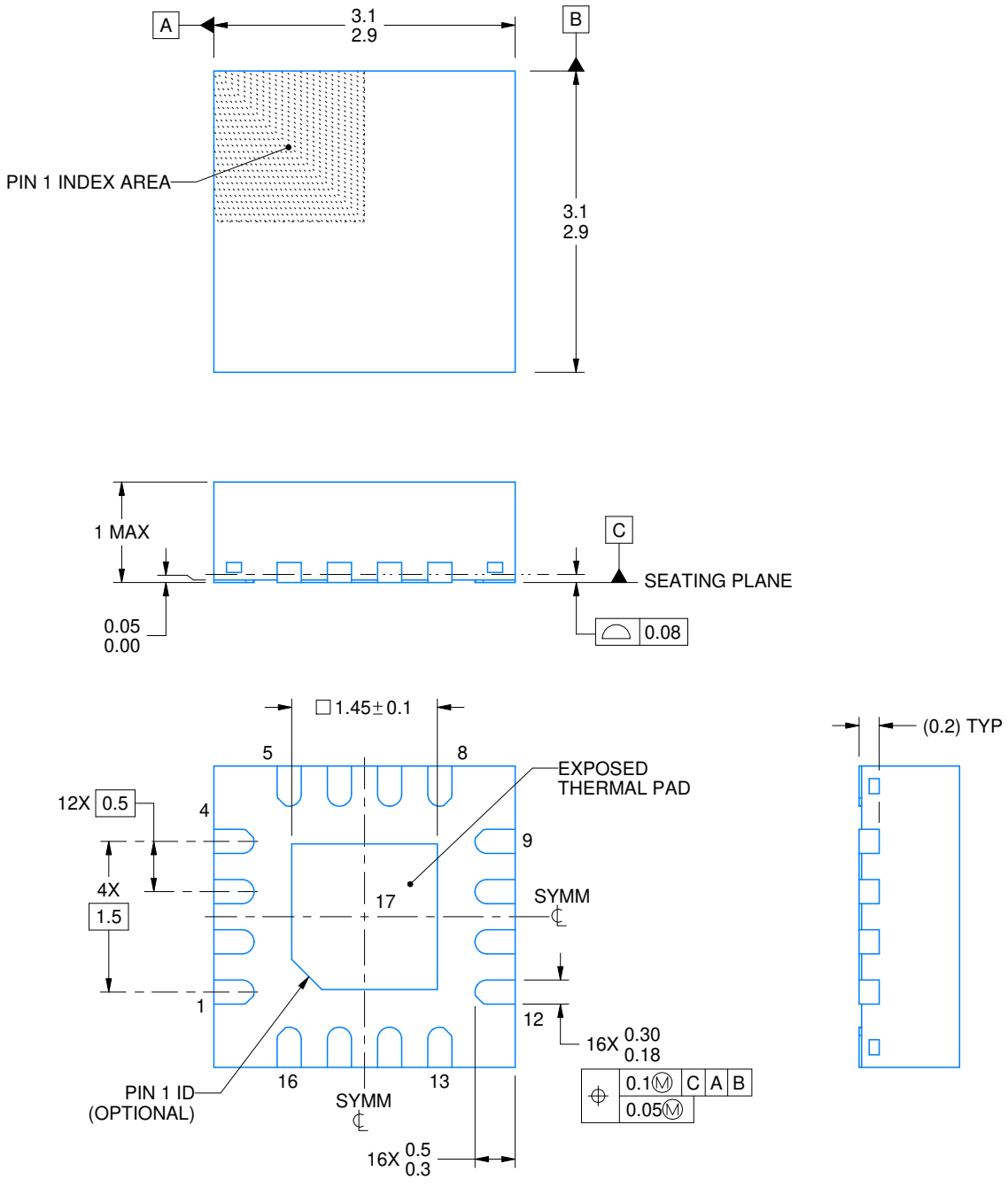
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

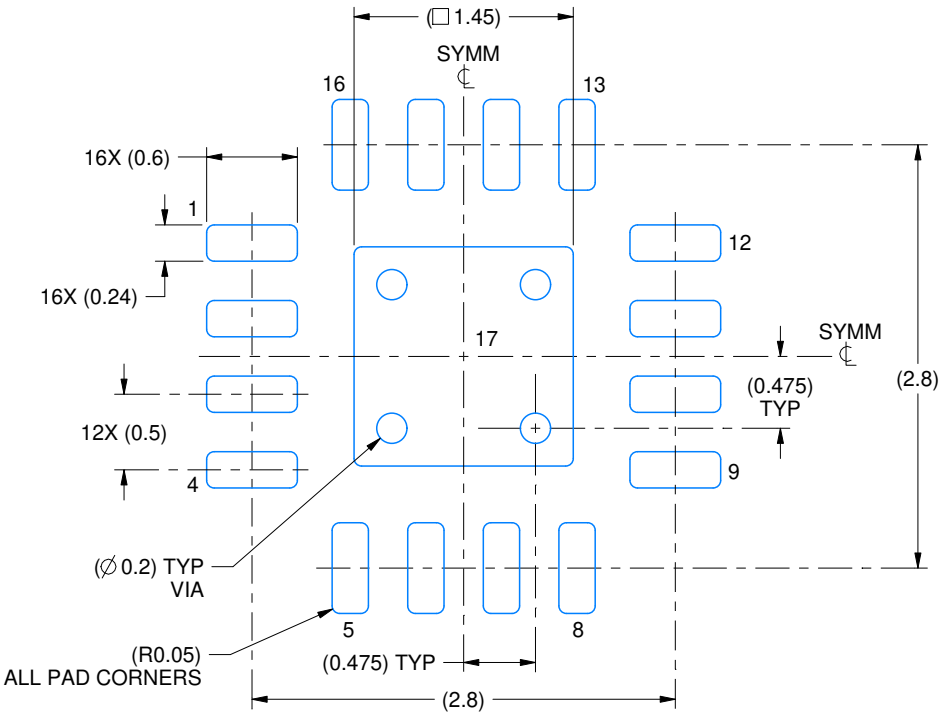
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

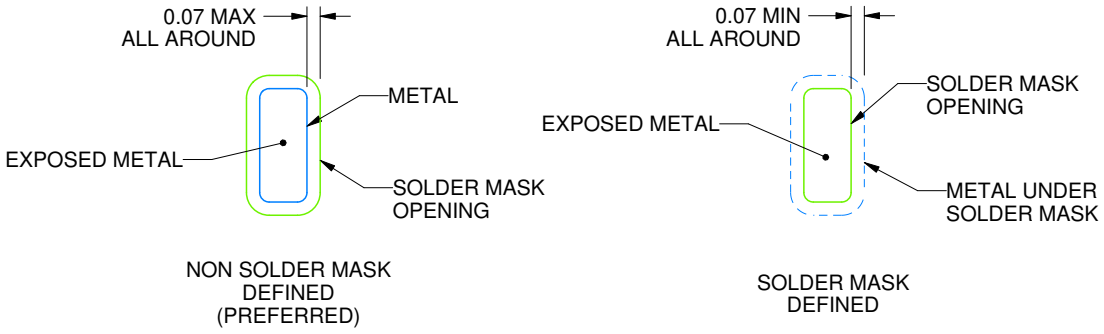


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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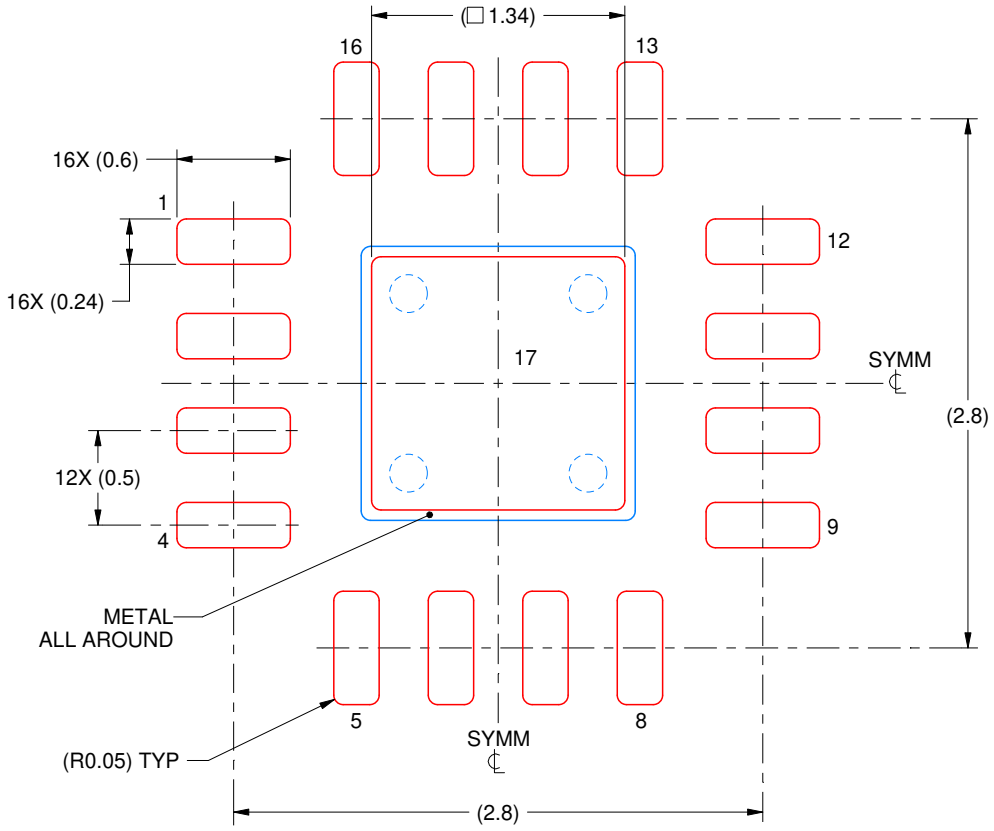
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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