TELEDYNE LECROY
Everywhereyoulook™

QualiPHY™
Compliance Test Software

QPHY-DDR2

DDR2 Serial Data Compliance Software

Instruction Manual

Revision B – November, 2017

Relating to:

XStreamDSO™ Version 8.5.x.x and later

QualiPHY Software Version 8.5.x.x and later

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About This Manual

This manual assumes that you are familiar with using an oscilloscope–in particular the Teledyne LeCroy oscilloscope that will be used with QualiPHY–and that you have purchased the QPHY-DDR2 software option. Some of the images in this manual may show QualiPHY products other than QPHY-DDR2, or were captured using different model oscilloscopes, as they are meant to illustrate general concepts only. Rest assured that while the user interface may look different from yours, the functionality is identical.

Introduction

About QualiPHY

QualiPHY is highly automated compliance test software meant to help you develop and validate the PHY (physical-electrical) layer of a device, in accordance with the official documents published by the applicable standards organizations and special interest groups (SIGs). You can additionally set custom variables and limits to test compliance to internal standards.

QualiPHY is composed of a “framework” application that enables the configuration and control of separate tests for each standard through a common user interface. Features include:

- **Multiple Data Source Capability**
- **User-Defined Test Limits**: Tighten limits to ensure devices are well within the passing region, even if subsequently measured with different equipment.
- **Flexible Test Results Reporting** that includes XML Test Record Generation. Understand device performance distribution, or obtain process related information from the devices under test.

About QPHY-DDR2

QPHY-DDR2 is an automated test package performing all of the real time oscilloscope tests for Double Data Rate in accordance with JEDEC Standard No. 79-2E.

The software can be run on any Teledyne LeCroy oscilloscope with at least 2.5 GHz bandwidth, 20 GS/s sampling rate, and 12 MB free space on the D: drive.

Required Equipment

- Teledyne LeCroy real-time oscilloscope, ≥2.5 GHz BW, installed with:
  - XStreamDSO v.5.9.x.x minimum* with an activated QPHY-DDR2 option key
  - QualiPHY software v.5.9.x.x minimum with an activated QPHY-DDR2 component

  ***Note**: The versions of XStreamDSO and QualiPHY software must match, so upgrade your version of QualilPHY if you have upgraded your oscilloscope firmware. The versions listed above are the minimum versions required for this product. The QualiPHY software may be installed on a remote PC, but all other software must be run on the oscilloscope.
- Three or more ≥ 4 GHz bandwidth probes (voltage swing must be at least ± 2.5 Vp-p.)

  Note: Minimum 6 GHz bandwidth probes recommended.
- PCF200 Probe Deskew and Calibration Fixture (included with WaveLink probe systems)

Remote Host Computer System Requirements

Usually, the oscilloscope is the host computer for the QualiPHY software, and all models that meet the acquisition requirements will also meet the host system requirements. However, if you wish to run the QualiPHY software from a remote computer, these minimum requirements apply:

- Operating System:
  - Windows 7 Professional
  - Windows 10 Professional
- 1 GHz or faster processor
- 1 GB (32-bit) or 2 GB (64-bit) of RAM
- Ethernet (LAN) network capability
- Hard Drive:
  - At least 100 MB free to install the framework application
  - Up to 2 GB per standard installed to store the log database (each database grows from a few MB to a maximum of 2 GB)

See Set Up Remote Control for configuration instructions.

QPHY-DDR2 Basic Functionality

Signals Measured

The compliance test probes the following signals (# is the negative polarity of the differential signal):

CK, CK# Input

Differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output (read) data is referenced to the crossings of CK and CK# (both directions of crossing).

DQ Input/Output

Bi-directional data bus input/output.

DQS, DQS# Input/Output

Data strobe output with read data, input with write data. This signal is in phase with read data and 90 degrees out of phase with write data. The data strobes DQS may be used in single ended mode or paired with optional complementary signal DQS# to provide differential pair signaling to the system during both reads and writes.

ADD/CTRL

Address and control signals can be measured in addition to the clock, data and strobe. Bank Address (BA0 – BA2), Chip Select (CS), Command Inputs (RAS, CAS and WE), Clock Enable (CKE) and On Die Termination (ODT) can all be specified as the signal under test.

Burst Access

The functionality is extracted from JEDEC Standard No. 79-2E section 3.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command.

Prior to normal operation, the DDR2 SDRAM must be initialized.

Burst Read

The Burst Read command is initiated by having CS# and CAS# LOW while holding RAS# and WE# HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

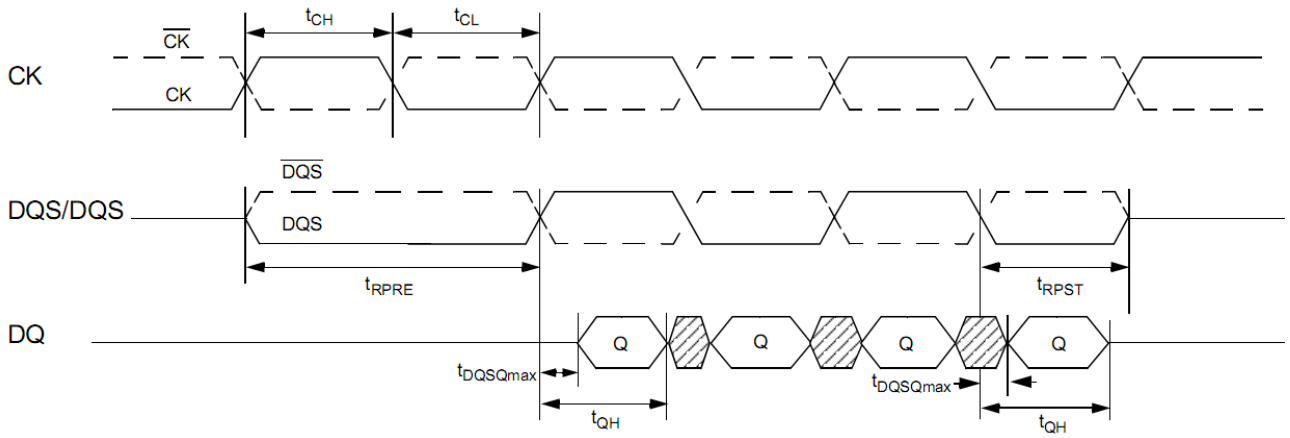


Figure 1. Data output (read) timing [JESD79-2E figure 32]

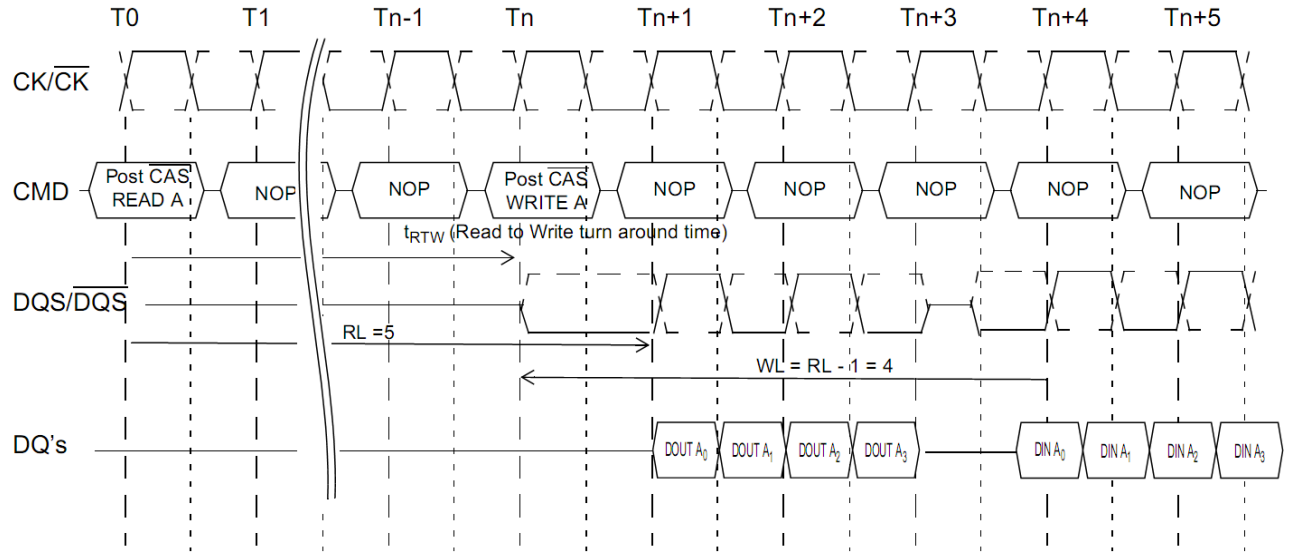


Figure 2. Burst read followed by burst write [JESD79-2E figure 35]

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Burst Write

The Burst Write command is initiated by having CS#, CAS# and WE# LOW while holding RAS# HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the [first rising edge]. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst.

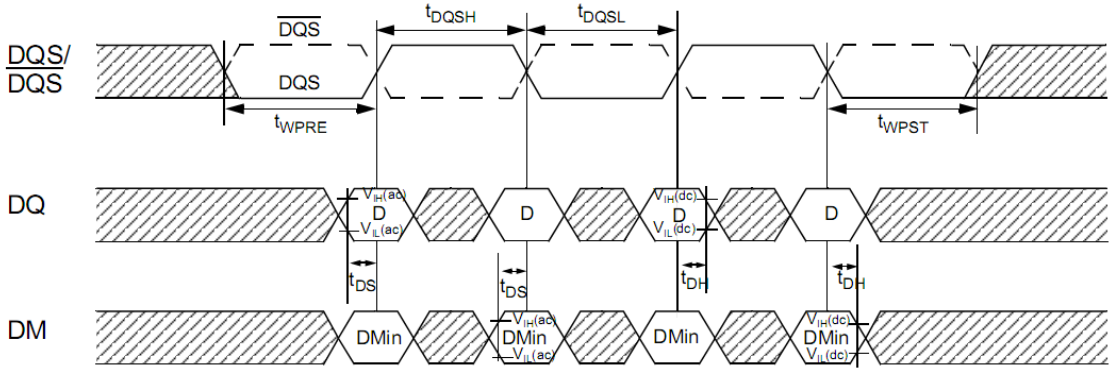


Figure 3. Data input (write) timing [JESD79-2E figure 38]

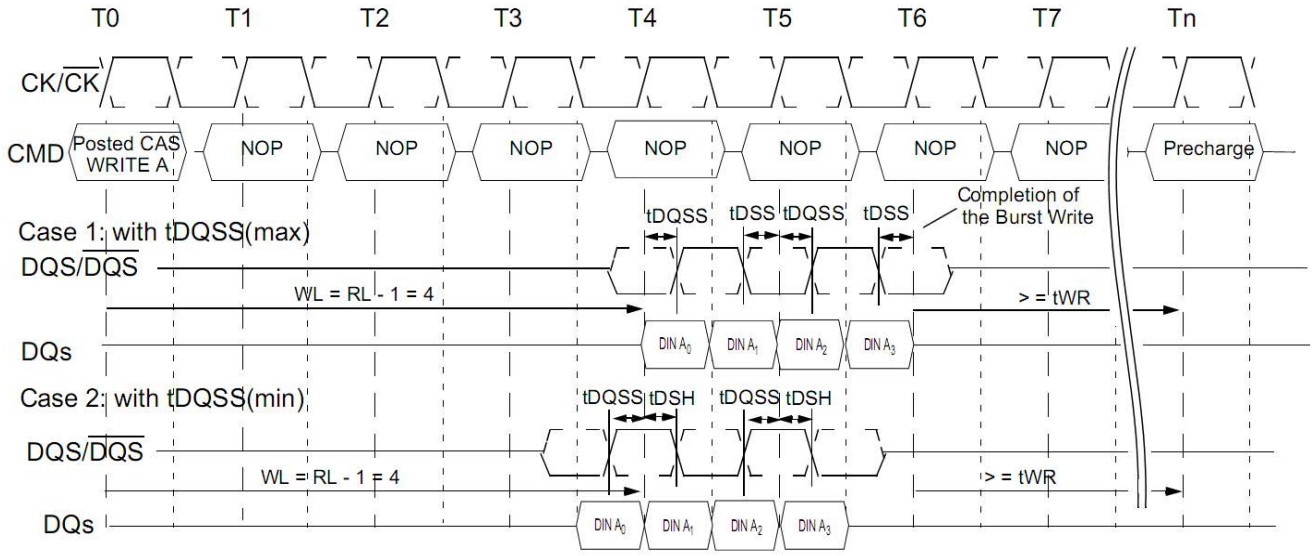
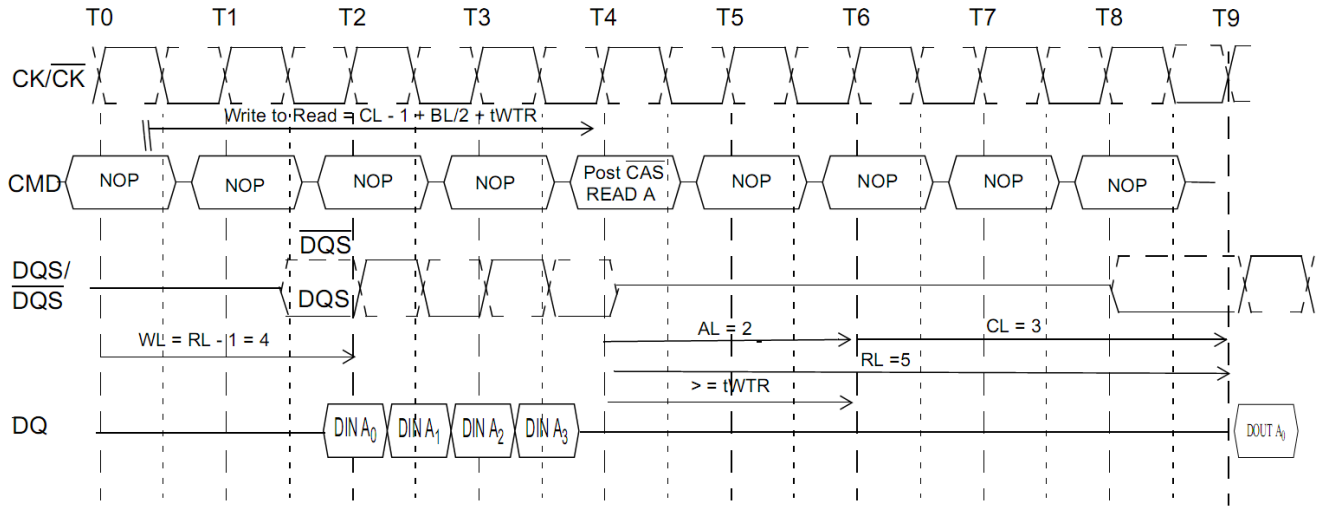


Figure 4. Burst write operation [JESD79-2E figure 39]



NOTE The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in the timing parameter table of this standard.

Figure 5. Burst write followed by burst read [JESD79-2E figure 41]

Installation and Setup

QualiPHY is a Windows-based application that can be configured with one or more serial data compliance components. Each compliance component is purchased as a software option.

Install Base Application

Download the latest version of the QualiPHY software from:

teledynelecroy.com/support/softwaredownload under Oscilloscope Downloads > Software Utilities.

If the oscilloscope is not connected to the Internet, copy the installer onto a USB memory stick then transfer it to the oscilloscope desktop or a folder on a D:\ drive to execute it.

Run **QualiPHYInstaller.exe** and follow the installer prompts. Choose all the components you plan to activate. If you omit any components now, you will need to update the installation to activate them later.

By default, the oscilloscope appears as local host when QualiPHY is executed on the oscilloscope. Follow the steps under Add Connection to QualiPHY to check that the IP address is **127.0.0.1**.

Activate Components

The serial data compliance components are factory installed as part of the main application in your oscilloscope and are individually activated through the use of an alphanumeric code uniquely matched to the oscilloscope's serial number. This option key code is what is delivered when purchasing a software option.

To activate a component on the oscilloscope:

1. From the menu bar, choose **Utilities > Utilities Setup**.
2. On the Options tab, click **Add Key**.
3. Use the Virtual Keyboard to **Enter Option Key**, then click **OK**.

   If activation is successful, the key code now appears in the list of Installed Option Keys.
4. Restart the oscilloscope application by choosing **File > Exit**, then double-clicking the **Start DSO** icon on the desktop.

Set Up Dual Monitor Display

Teledyne LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability. This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

See the oscilloscope Operator's Manual or Getting Started Manual for instructions on setting up dual monitor display.

Set Up Remote Control

QualiPHY software can be executed from a remote host computer, controlling the oscilloscope through a LAN Connection. To set up remote control:

- The oscilloscope must be connected to a LAN and assigned an IP address (fixed or dynamic).
- The host computer must be on the same LAN as the oscilloscope.

Configure Oscilloscope for Remote Control

1. From the menu bar, choose **Utilities → Utilities Setup...**
2. Open the **Remote** tab and set Remote Control to **TCP/IP**.
3. Verify that the oscilloscope shows an IP address.

Add Connection to QualiPHY

1. On the host PC, download and run **QualiPHYInstaller.exe**.
2. Start QualiPHY and click the **General Setup** button.
3. On the **Connection** tab, click **Scope Selector**.
4. Click **Add** and choose the connection type. Enter the oscilloscope IP address from Step 3 above. Click **OK**.
5. When the oscilloscope is properly detected, it appears on the Scope Selector dialog. Select the connection, and click **OK**.

   QualiPHY is now ready to control the oscilloscope.

Select Connection

Multiple oscilloscopes may be accessible to a single remote host. In that case, go to General Setup and use the Scope Selector at the start of the QPHY session to choose the correct connection.

QualiPHY tests the oscilloscope connection when starting a test. The system warns you if there is a connection problem.

Using QualiPHY

This section provides an overview of the QualiPHY user interface and general procedures. For detailed information about the QPHY-DDR2 software option, see QPHY-DDR2 Testing.

Accessing the Software

Once QualiPHY is installed and activated, it can be accessed from the oscilloscope menu bar by choosing **Analysis > QualiPHY**, or by double-clicking the **QualiPHY desktop icon** on a remote computer.

The QualiPHY framework dialog illustrates the overall software flow, from general set up through running individual compliance tests. Work from left to right, making all desired settings on each sub-dialog.

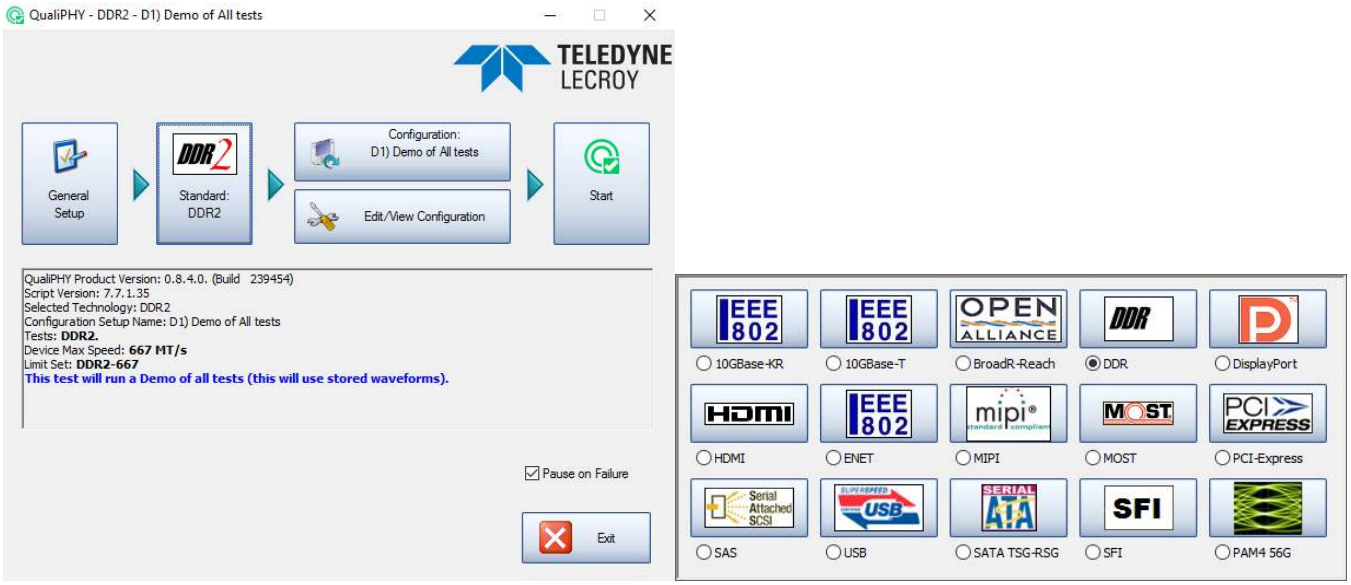


Figure 6. QualiPHY framework dialog and Standard selection menu

The sub-dialogs are organized into tabs each containing configuration controls related to that part of the process. These are described in more detail in the following sections.

If **Pause on Failure** is checked, QauliPHY prompts to retry a measure whenever a test fails.

Report Generator launches the manual report generator dialog.

The **Exit** button at the bottom of the framework dialog closes the QualiPHY application.

General Setup

The first sub-dialog contains general system settings. These remain in effect for each session, regardless of Standard, until changed.

Connection tab

Shows **IP Address** of the test oscilloscope (local host 127.0.0.1 if QualiPHY is run from the oscilloscope). The **Scope Selector** allows you to choose the oscilloscope used for testing when several are connected to the QualiPHY installation. See Set Up Remote Control for details.

Session Info tab

Optional information about the test session that may be added to reports, such as: **Operator Name**, **Device Under Test** (DUT), **Temperature** (in °C) of the test location, and any additional **Comments**. There is also an option to **Append Results** or **Replace Results** when continuing a previous session.

To optimize report generation, enter at least a DUT name at the beginning of each session.

Report tab

Settings related to automatic report generation. Choose:

- **Reporting behavior** of:
  - "Ask to generate a report after tests," where you'll be prompted to create a new file for each set of test results.
  - "Never generate a report after tests," where you'll need to manually execute the Report Generator to create a report.
  - "Always generate a report after tests," to autogenerate a report of the latest test results.
- **Default** report output type of XML, HTML, or PDF.
- A generic **Output file name**, including the full path to the report output folder.

Optionally, check **Allow style sheet selection in Report Generator** to enable the use of a custom .xslt when generating reports (XML and HTML output only). The path to the .xslt is entered on the Report Generator dialog.

Report Generator launches the Report Generator dialog, which contains the same settings as the Report tab, only applied to individual reports.

Advanced tab

This tab launches the **X-Replay Mode** dialog. See X-Replay Mode.

About tab

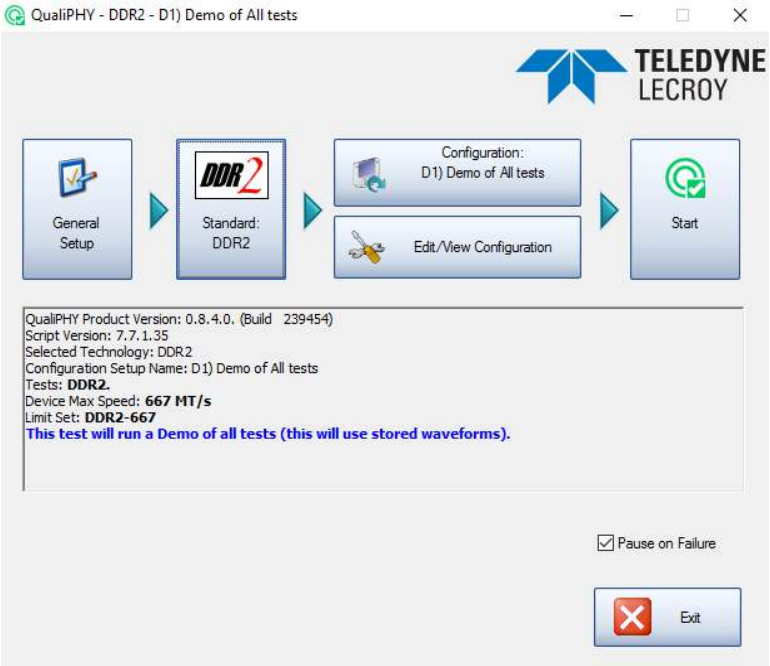
Information about your QualiPHY installation.

QualiPHY Test Process

Once general system settings are in place, these are the steps for running test sessions.

Set Up Test Session

1. Connect the oscilloscope to the DUT. See QPHY-DDR2 Testing Physical Setup.
2. Access the QualiPHY software to display the framework dialog.



3. If running QualiPHY remotely, click **General Setup** and open the **Scope Selector** to select the correct oscilloscope connection.
4. If you have more than one component activated, click **Standard** and select the desired standard to test against. Otherwise, your one activated component will appear as the default selection.

   Note: Although all the QualiPHY components appear on this dialog, only those selected when installing QualiPHY are enabled for selection.

5. Click the **Configuration** button and select the test configuration to run. These pre-loaded configurations are set up to run all the tests required for compliance and provide a quick, easy way to begin compliance testing. See QPHY-DDR2 Test Configurations for a description of your configurations.

   You can also create custom configurations for internal compliance tests by copying and modifying the pre-loaded configurations. See Customizing QualiPHY for details.

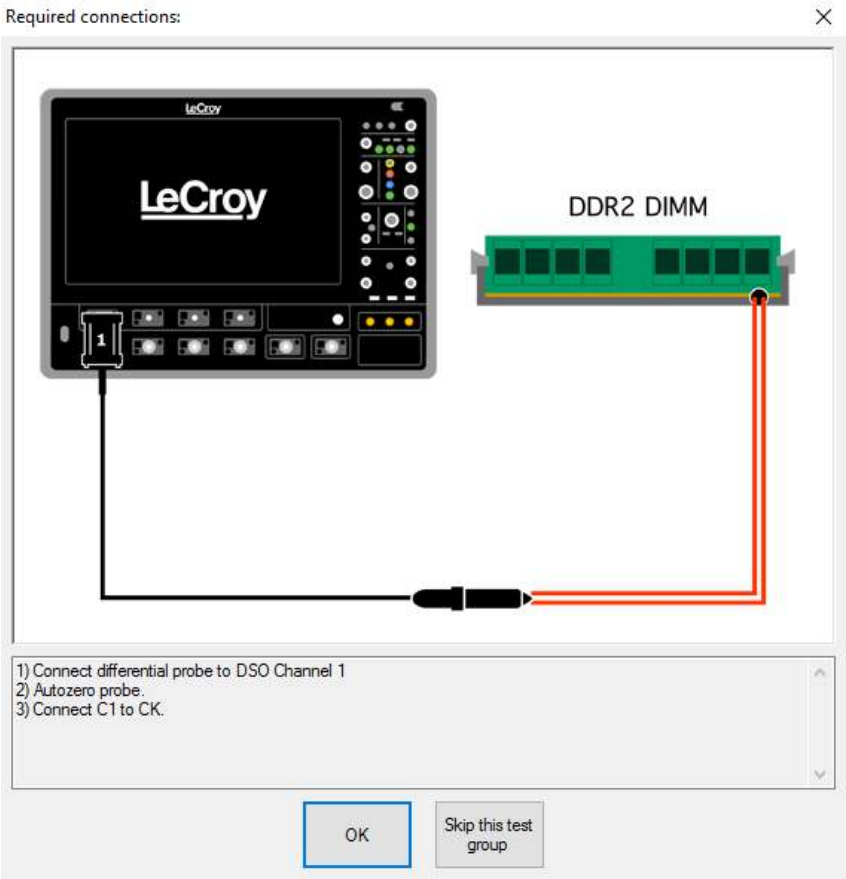
6. **Close** the Edit/View Configuration dialog to return to the framework dialog.

Run Tests

1. On the framework dialog, click **Start** to begin testing.

   When tests are in progress, this button changes to **Stop**. Click it at any time to stop the test in process. You'll be able to resume from the point of termination or from the beginning of the test.

2. Follow the pop-up window prompts. QualiPHY guides you step-by-step through each of the tests described in the standard specification, including diagrams of the connection to the DUT for each required test mode.



3. When all tests are successfully completed, both progress bars on the framework dialog are completely green and the message "All tests completed successfully" appears. If problems are encountered, you'll be offered options to:

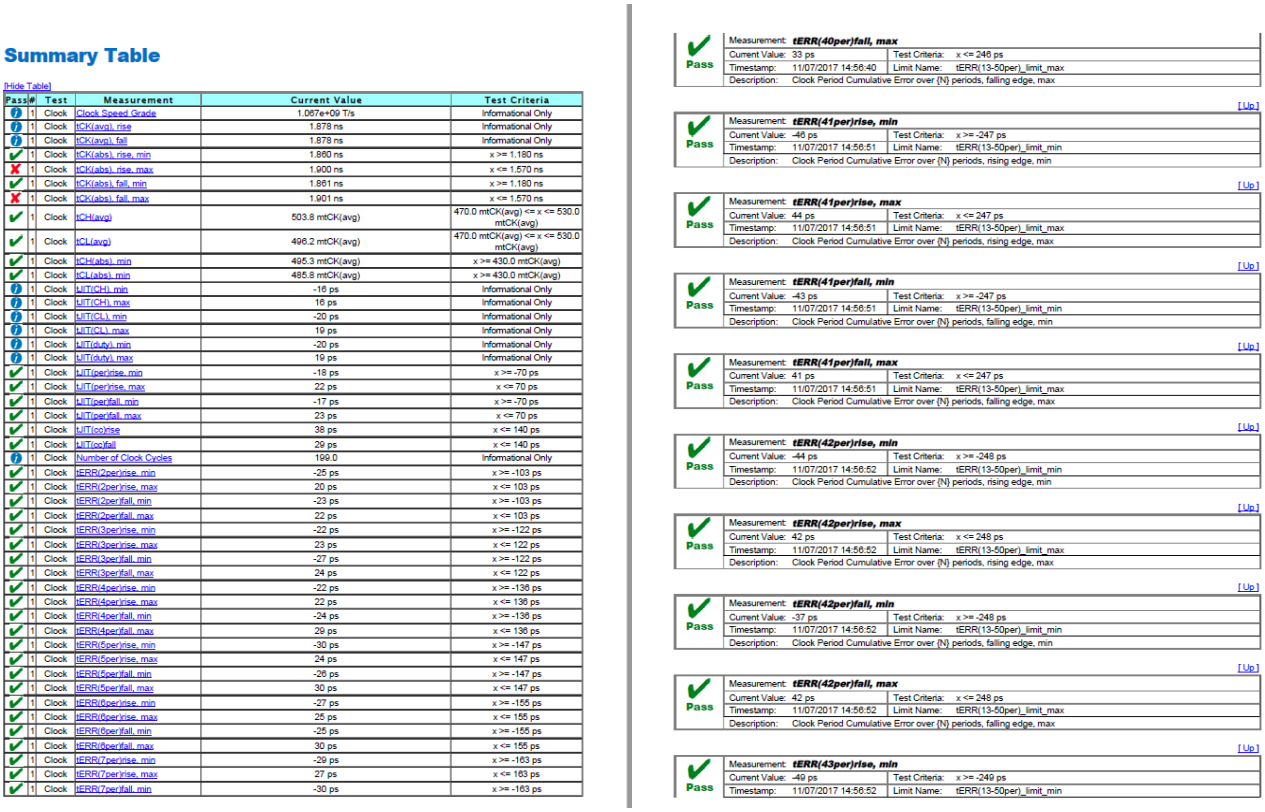
   - **Retry** the test from the latest established point defined in the script
   - **Ignore and Continue** with the next test
   - **Abort Session**

Generate Reports

The QualiPHY software automates report generation. On the framework dialog, go to **General Setup > Report** to pre-configure reporting behavior. You can also manually launch the **Report Generator** from the framework dialog once a test is run.

The Report Generator offers the same selections as the Report tab, only applied to each report individually, rather than as a system setting. This enables you to save reports for each test session, rather than overwrite the generic report file. There are also options to link a custom style sheet (.xslt) to the report, or to Exclude Informative Results.

The Test Report includes a summary table with links to the detailed test result pages.



Summary Table

[Hide Table]

Pass	#	Test	Measurement	Current Value	Test Criteria
ⓘ	1	Clock	Clock Speed Grade	1.067e+09 T/s	Informational Only
ⓘ	1	Clock	tCK(avg), rise	1.878 ns	Informational Only
ⓘ	1	Clock	tCK(avg), fall	1.878 ns	Informational Only
✔	1	Clock	tCK(abs), rise, min	1.860 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), rise, max	1.900 ns	x <= 1.570 ns
✔	1	Clock	tCK(abs), fall, min	1.861 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), fall, max	1.901 ns	x <= 1.570 ns
✔	1	Clock	tCH(avg)	503.8 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCL(avg)	496.2 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCH(abs), min	495.3 mtCK(avg)	x >= 430.0 mtCK(avg)
✔	1	Clock	tCL(abs), min	485.8 mtCK(avg)	x >= 430.0 mtCK(avg)
ⓘ	1	Clock	tJIT(CH), min	-16 ps	Informational Only
ⓘ	1	Clock	tJIT(CH), max	16 ps	Informational Only
ⓘ	1	Clock	tJIT(CL), min	-20 ps	Informational Only
ⓘ	1	Clock	tJIT(CL), max	19 ps	Informational Only
ⓘ	1	Clock	tJIT(duty), min	-20 ps	Informational Only
ⓘ	1	Clock	tJIT(duty), max	19 ps	Informational Only
✔	1	Clock	tJIT(per)rise, min	-18 ps	x >= -70 ps
✔	1	Clock	tJIT(per)rise, max	22 ps	x <= 70 ps
✔	1	Clock	tJIT(per)fall, min	-17 ps	x >= -70 ps
✔	1	Clock	tJIT(per)fall, max	23 ps	x <= 70 ps
✔	1	Clock	tJIT(cc)rise	38 ps	x <= 140 ps
✔	1	Clock	tJIT(cc)fall	29 ps	x <= 140 ps
ⓘ	1	Clock	Number of Clock Cycles	199.0	Informational Only
✔	1	Clock	tERR(2per)rise, min	-25 ps	x >= -103 ps
✔	1	Clock	tERR(2per)rise, max	20 ps	x <= 103 ps
✔	1	Clock	tERR(2per)fall, min	-23 ps	x >= -103 ps
✔	1	Clock	tERR(2per)fall, max	22 ps	x <= 103 ps
✔	1	Clock	tERR(3per)rise, min	-22 ps	x >= -122 ps
✔	1	Clock	tERR(3per)rise, max	23 ps	x <= 122 ps
✔	1	Clock	tERR(3per)fall, min	-27 ps	x >= -122 ps
✔	1	Clock	tERR(3per)fall, max	24 ps	x <= 122 ps
✔	1	Clock	tERR(4per)rise, min	-22 ps	x >= -136 ps
✔	1	Clock	tERR(4per)rise, max	22 ps	x <= 136 ps
✔	1	Clock	tERR(4per)fall, min	-24 ps	x >= -136 ps
✔	1	Clock	tERR(4per)fall, max	29 ps	x <= 136 ps
✔	1	Clock	tERR(5per)rise, min	-30 ps	x >= -147 ps
✔	1	Clock	tERR(5per)rise, max	24 ps	x <= 147 ps
✔	1	Clock	tERR(5per)fall, min	-26 ps	x >= -147 ps
✔	1	Clock	tERR(5per)fall, max	30 ps	x <= 147 ps
✔	1	Clock	tERR(6per)rise, min	-27 ps	x >= -155 ps
✔	1	Clock	tERR(6per)rise, max	25 ps	x <= 155 ps
✔	1	Clock	tERR(6per)fall, min	-25 ps	x >= -155 ps
✔	1	Clock	tERR(6per)fall, max	30 ps	x <= 155 ps
✔	1	Clock	tERR(7per)rise, min	-29 ps	x >= -163 ps
✔	1	Clock	tERR(7per)rise, max	27 ps	x <= 163 ps
✔	1	Clock	tERR(7per)fall, min	-30 ps	x >= -163 ps

Pass — Measurement: **tERR(40per)fall, max** — Current Value: 33 ps — Test Criteria: x <= 246 ps — Timestamp: 11/07/2017 14:56:40 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(41per)rise, min** — Current Value: -46 ps — Test Criteria: x >= -247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, rising edge, min

[Up]

Pass — Measurement: **tERR(41per)rise, max** — Current Value: 44 ps — Test Criteria: x <= 247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, rising edge, max

[Up]

Pass — Measurement: **tERR(41per)fall, min** — Current Value: -43 ps — Test Criteria: x >= -247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, falling edge, min

[Up]

Pass — Measurement: **tERR(41per)fall, max** — Current Value: 41 ps — Test Criteria: x <= 247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(42per)rise, min** — Current Value: -44 ps — Test Criteria: x >= -248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, rising edge, min

[Up]

Pass — Measurement: **tERR(42per)rise, max** — Current Value: 42 ps — Test Criteria: x <= 248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, rising edge, max

[Up]

Pass — Measurement: **tERR(42per)fall, min** — Current Value: -37 ps — Test Criteria: x >= -248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, falling edge, min

[Up]

Pass — Measurement: **tERR(42per)fall, max** — Current Value: 42 ps — Test Criteria: x <= 248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(43per)rise, min** — Current Value: -49 ps — Test Criteria: x >= -249 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min

Figure 7. Test Report Summary Table and Details pages (DDR3 shown)

Reports are output to the folder D:\QPHY\Reports, or C:\LeCroy\QPHY\Reports if QualiPHY is installed on a remote PC.

You can add your own logo to the report by replacing the file *\QPHY\StyleSheets\CustomerLogo.jpg.

The recommended maximum size is 250x100 pixels at 72 ppi, 16.7 million colors, 24 bits. Use the same file name and format.

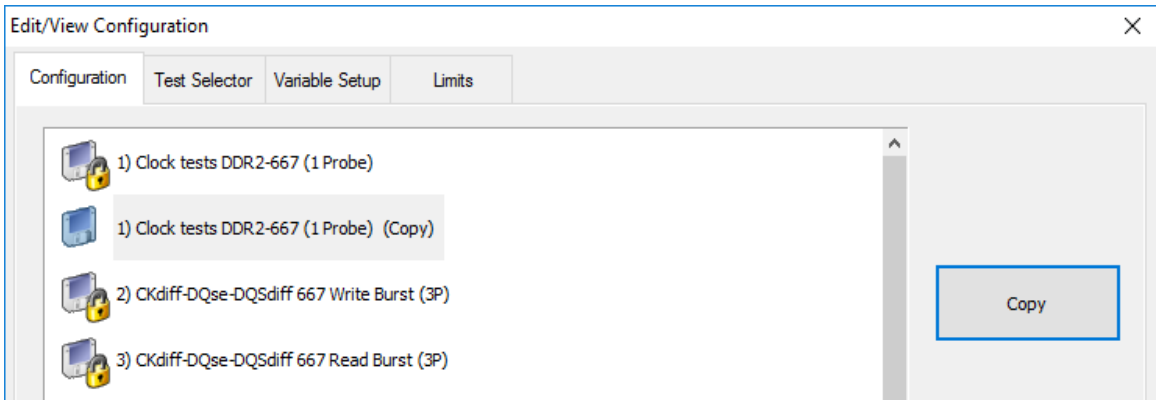
Customizing QualiPHY

Create custom test configurations by copying one of the standard configurations and modifying it. The pre-loaded configurations cannot be modified.

Copy Configuration

1. Access the QualiPHY framework dialog and select a **Standard**.
2. Click **Edit/View Configuration** and select the configuration upon which to base the new configuration. This can be a pre-loaded configuration or another copy.
3. Click **Copy** and enter a name and description. Once a custom configuration is defined, it appears on the Configuration tab with the defined name.

   Note: Until you enter a new name, the new configuration is shown followed by “(Copy)”.



4. Select the new, custom configuration and follow the procedures below to continue making changes.

   Note: If any part of a configuration is changed, the Save As button becomes active on the bottom of the dialog. If a custom configuration is changed, the Save button will also become active to apply the changes to the existing configuration, rather than make another copy

Select Tests

On the **Test Selector** tab, check the tests that make up the configuration. Each test is defined by the DDR2 standard. A description of each test is displayed when it is selected.

To loop an individual test or group of tests, select it from the list, then choose to **Loop selected test** until stopped or enter the number of repetitions. When defining a number of repetitions, enter the number of repetitions before selecting the checkbox.

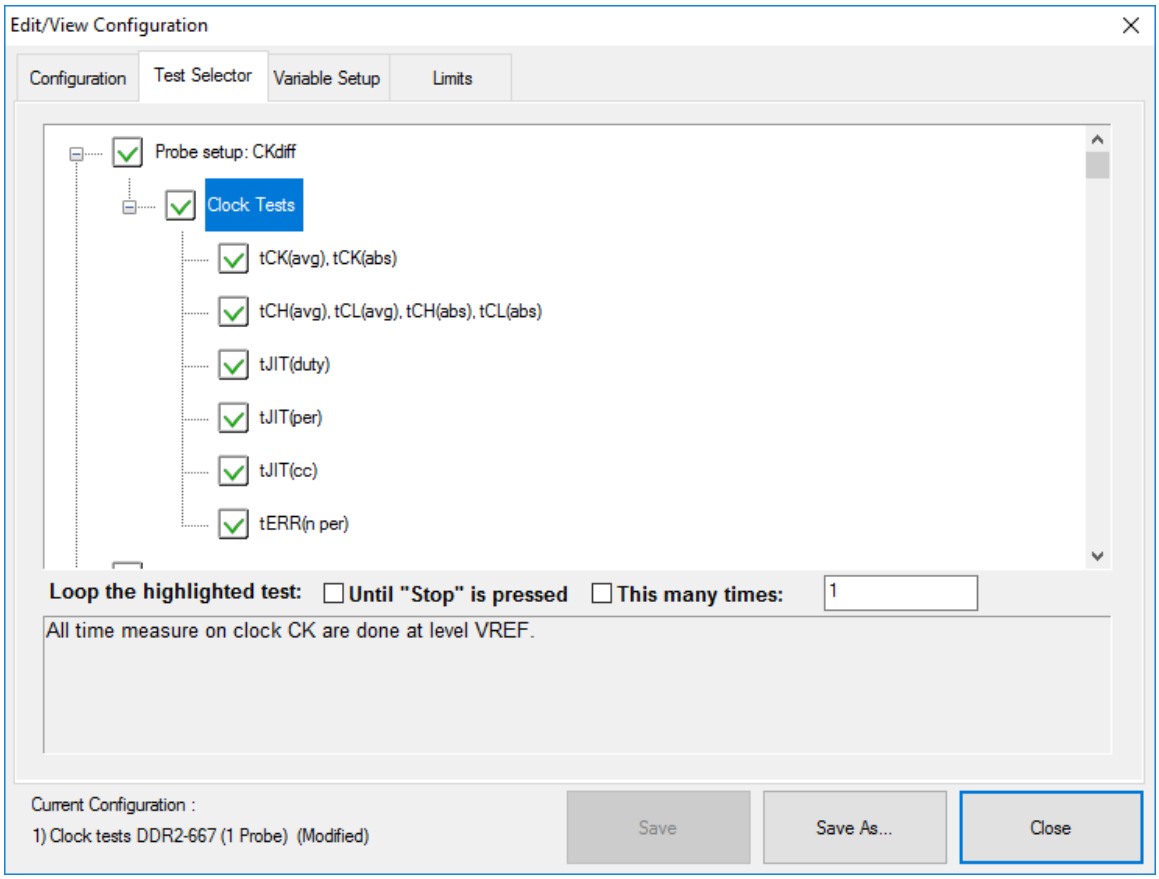


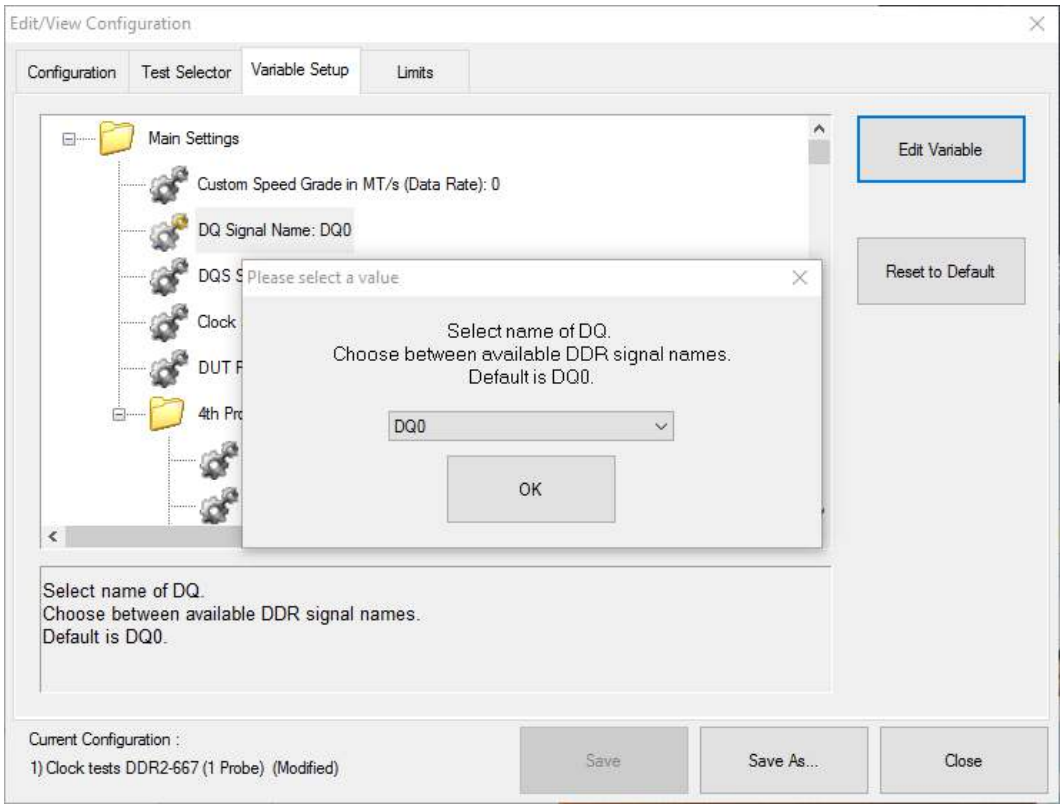
Figure 8. Configuration Test Selector Tab

Edit Variables

The Variable Setup tab contains a list of test variables. See QPHY-DDR2 Variables for a description of each.

To modify a variable:

1. Select the variable on the Variable Setup tab, then click **Edit Variable**. (You can also choose to Reset to Default at any time.)
2. The conditions of this variable appear on a pop-up. Choose the new condition to apply.



Edit Test Limits

The Limits tab shows the Limit Set currently associated with the configuration. Any limit set can be associated with a custom configuration by selecting it in this field.

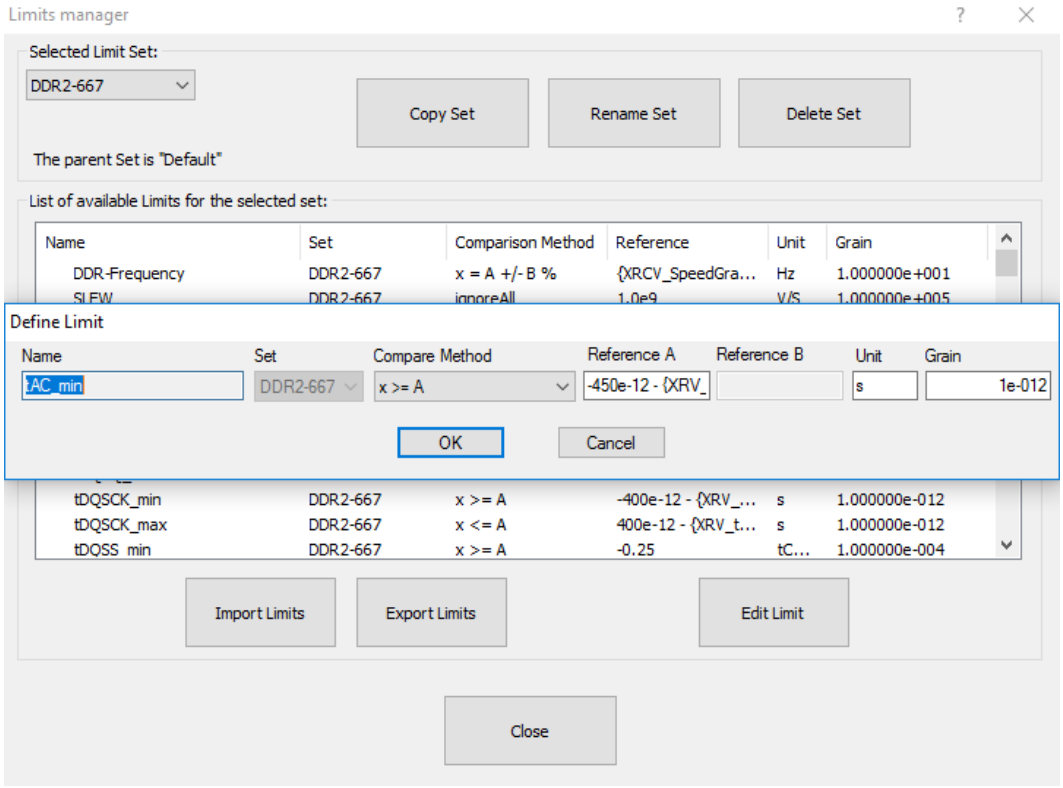
The Limits Manager shows the settings for every test limit in a limit set. Those in the default set are the limits defined by the standard.

To create a custom limit set:

1. On the Limits tab, click **Limits Manager**.
2. With the default set selected, click **Copy Set** and enter a name.

   Note: You can also choose to copy and/or modify another custom set that has been associated with this configuration.

3. Double click the limit to be modified, and in the pop-up enter the new values.



You can also **Import Limits** from a .csv file. Navigate to the file location after clicking the button.

Tip: Likewise, Export Limits creates a .csv file from the current limit set. You may wish to do this and copy it to format the input .csv file.

X-Replay Mode

The X-Replay mode window is an advanced (“developer”) view of QualiPHY. The tree in the upper-left frame enables you to navigate to processes in the DDR2 test script, in case you need to review the code, which appears in the upper-right frame.

Two other particularly useful features are:

- A **list of recent test sessions** in the lower-left frame. While you can only generate a report of the current test session in the QualiPHY wizard, in X-Replay Mode you can generate a report for any of these recent sessions. Select the session and choose **Report > Create Report** from the menu bar.
- The **QualiPHY log** in the bottom-right frame. The frame can be split by dragging up the lower edge. The bottom half of this split frame now shows the **raw Python output**, which can be useful if ever the script needs debugging.

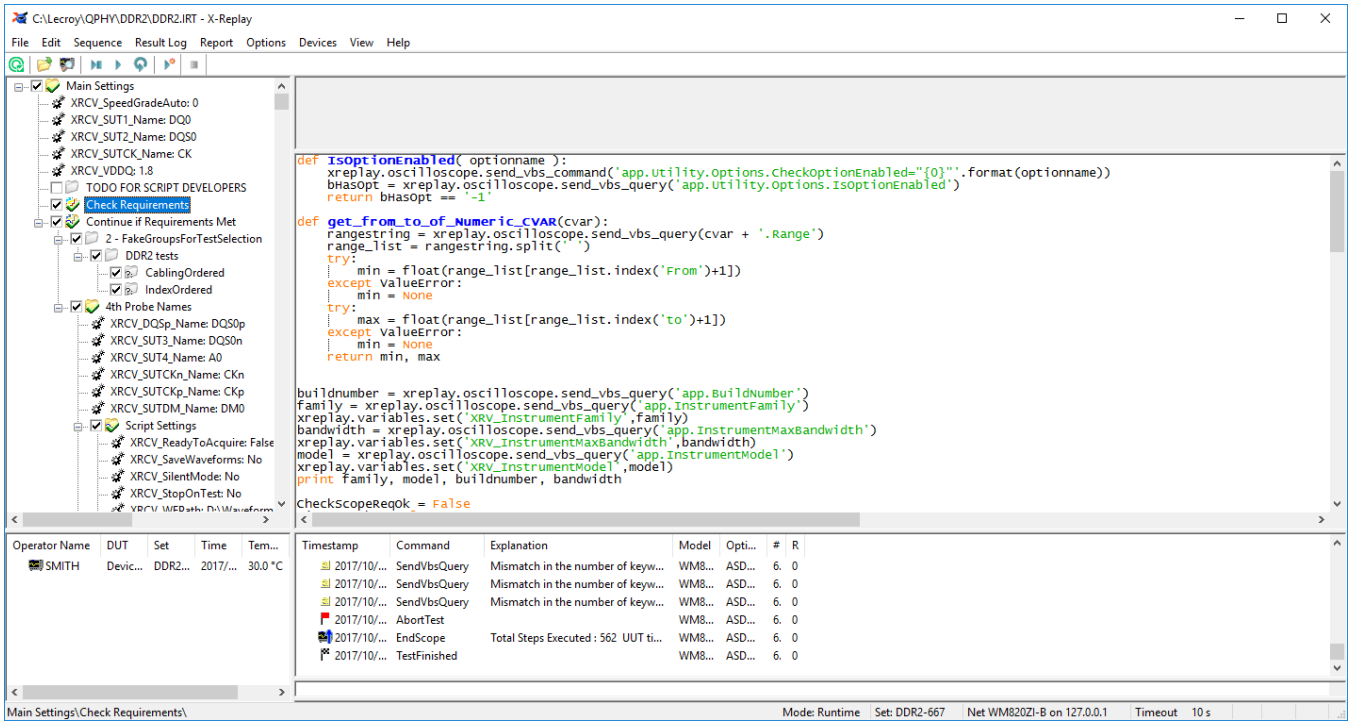


Figure 9. X-Replay Mode window

QPHY-DDR2 Testing

Test Preparation

Before beginning any test or data acquisition, the oscilloscope should be warmed for at least 20 minutes.

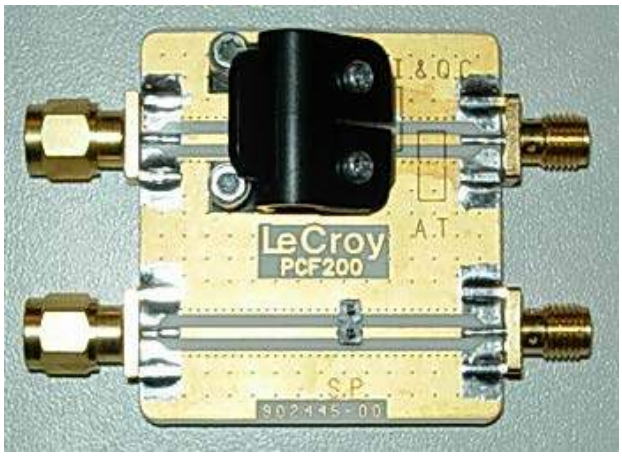
Calibration is automatically performed by the oscilloscope software; no manual calibration is required. The calibration procedure will be run again if the temperature of the oscilloscope changes by more than a few degrees.

Deskewing the Probes

For DDR measurements, it is crucial to make sure that probes are properly deskewed before running QPHY-DDR2 to ensure proper signal timing. Ideally, the same settings should be used when deskewing as when acquiring signals for analysis. This will ensure that the channels are deskewed using the same setup as when running conformance tests. Deskew values are saved and stored by QualiPHY at the beginning of each run.

Required Equipment

- PCF200 (included with "-PS" probe systems)



- Square-Pin (SP) tip (included with D4x0-PS, D6x0-PS, and Dxx30-PS)
- 50 Ω terminator

  Note: Alternatively an LPA-K-A adapter and a SMA cable could be used

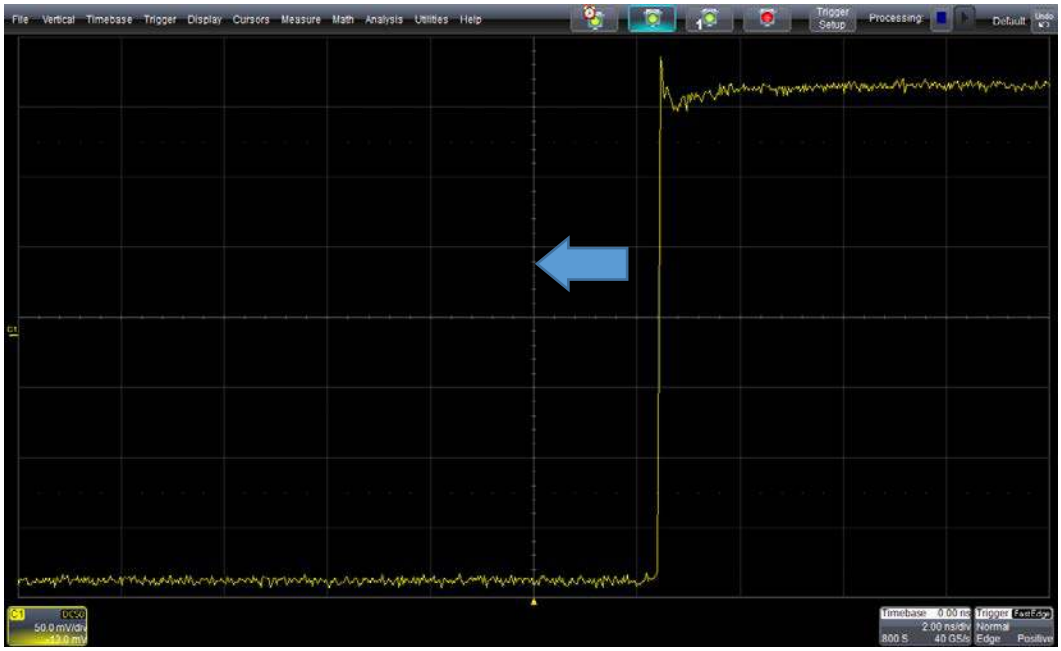
Methodology

Before beginning the procedure, be sure to warm the oscilloscope for at least 20 minutes.

1. Connect the PCF200 to the oscilloscope's fast edge output. The PCF200 fixture has two different signal paths that can be used, depending on the type of probe tip being used for the measurement:
   - The upper signal path is for deskewing Solder-In (SI), Quick-Connect (QC) and Adjustable Tip (AT) probe tips.
   - The lower circuit is for Square-Pin (SP) probe tips.

   Depending upon which probe tip is being used, connect the appropriate signal path to the fast edge output. For ease of connectivity it is recommended that SP tip is used. As long as the same tip is used to deskew each probe it does not matter which style of probe tip is used.
2. Connect probes electrically in a single-ended arrangement using their designated area on the fixture:
   - Connect the positive side of the probe to the signal trace (in between the two white strips). The positive polarity is indicated on the tip of the probe by a plus sign.
   - Connect the negative side to the ground plane (outside of the white strips).
   - In order to minimize reflections, apply a 50 Ω terminator to the end of the signal path in use. If a 50 Ω terminator is not available, an SMA cable can be used to terminate the PCF200 to one of the oscilloscope's outputs.
3. Set the oscilloscope **Trigger Source** to **Fast Edge**, **Trigger Type** to **Edge**.
4. Set a **Timebase** of approximately **10 ns/div** and **Timebase Delay** of **0.**

   Once everything is properly set up the oscilloscope display should look similar to the figure below. If there is no propagation delay due to the probe, and no internal oscilloscope channel propagation delay, the 50% trigger level will be at the center line of the oscilloscope grid.



5. From the channel setup dialog (C*n*):
   - Enable **Sinx/x** interpolation and set the **Averaging** to **50** sweeps.

- Touch the **Deskew** field once to highlight it, then adjust the deskew value to move the rising edge of the trace to the center of the display.

6. Now, decrease the **Timebase** to around **20 ps/div** and once again adjust the **Deskew** value so that the 50% rising edge point is centered in time.

Repeat this procedure for each probe using the same probe tip.

Note: Before moving on to the next probe, reset Averaging to 1 sweep and turn off Sinx/x interpolation.

When QualiPHY is started the deskew values from each channel dialog are saved and stored by QPHY at the beginning of each run. However, at the end of the testing these values will be erased. By saving a panel setup it is possible to refer to the deskew values after testing has completed.

Connecting the Probes

Determining Signals to Access

The required signals to probe depend up on which tests are being run in QPHY-DDR2. The tests are broken up into different “Probe Setups” to allow the user to easily see which signals are required for a particular test. You can view each of the probe setups in the Test Selector tab.

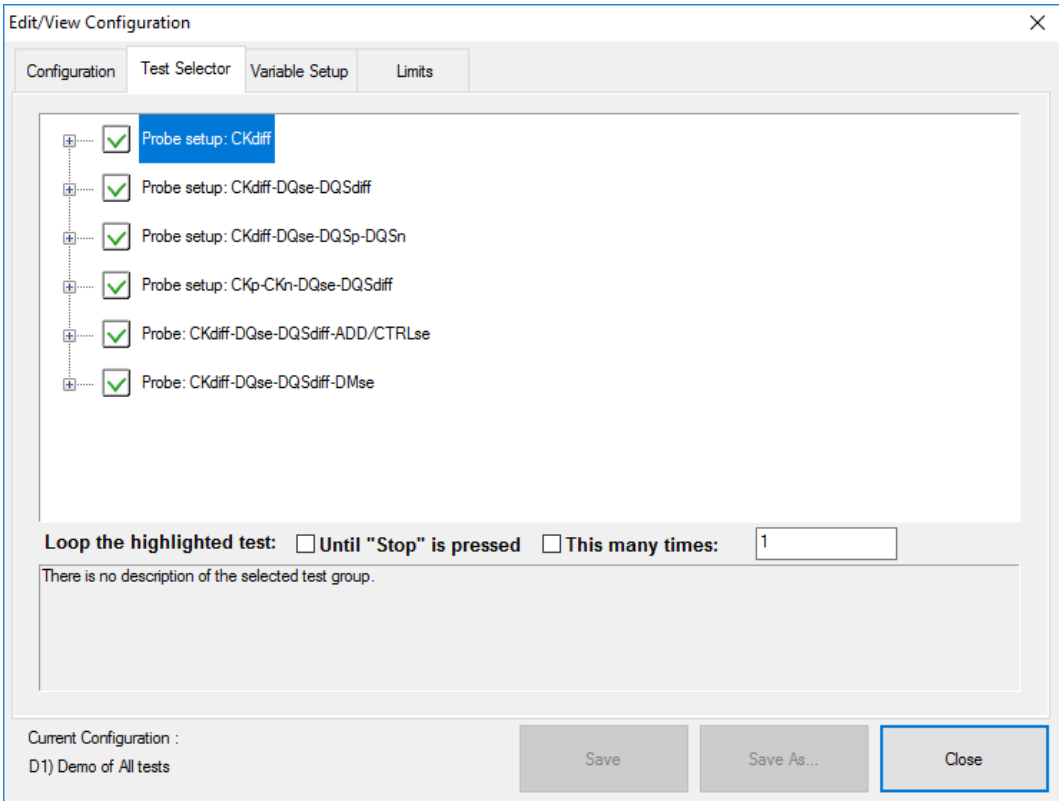


Figure 10. QPHY-DDR2 Probe Setups

Best Places to Probe

The DDR specification is defined at the balls of the DRAM so the probes should be placed as close to the DRAM as possible in order to closely follow the specification. This is important to minimize reflections on the signals. However, in some situations it can make sense to place the probes as close to the controller as possible. For example, if the user is a controller designer and is only interested in verifying the performance of the controller. It should be noted that some of the limits may not be applicable in this scenario.

One of the most desirable locations for probing is at the back side of the vias. This will generally result in good signal integrity; however, these may not always be accessible. Another alternative is to use an interposer such as the ones available from Nexus Technologies. No matter where the probes are placed it is essential to ensure that the probing points are equidistant from the DRAM. This will ensure that there is no additional skew introduced for timing measurements.

Read (R) and Write (W) Burst Requirements

R/W Burst Detection

QPHY-DDR2 separates R and W burst depending upon the skew between the data (DQ) and strobe (DQS) signals. For a W burst, QPHY expects to see that the DQ and DQS signals are approximately a quarter cycle out of phase. For an R burst, QPHY expects that the DQ and DQS signals are in phase.

R/W Burst Generation

It is recommended to capture a minimum of 10 R and 10 W bursts during each acquisition, but for greater statistical significance, it is encouraged to capture more. Programs which can communicate with the DRAM and controller are widely available online. One example is Memtest86+, which is available for download from memtest.org. When using Memtest, it is recommended to use test mode 7, which will randomly generate both R and W bursts. Additionally, a custom program can be used to stimulate the DUT.

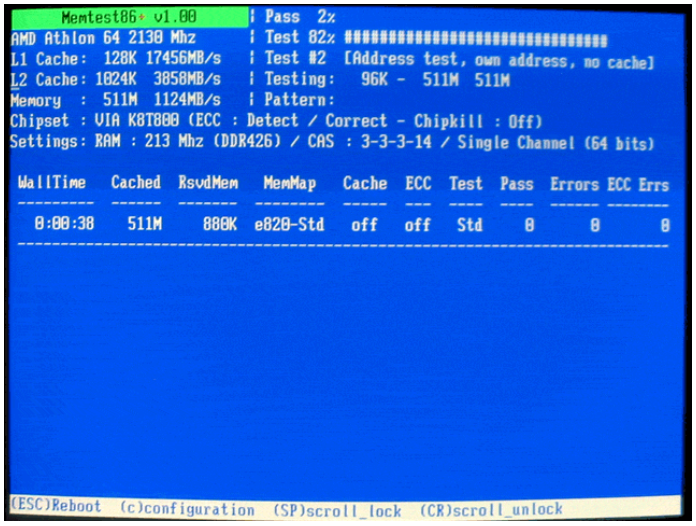


Figure 11. Memtest86+

Initial Signal Checking

Before running QPHY-DDR2, check the signals to verify that they make sense. This section covers some of the basic things which should be verified by the operator before running QPHY-DDR2.

Expected Channels

By default, QPHY-DDR2 expects to see the Clock (CK) on CH1, Strobe (DQS) on CH2 and Data (DQ) on CH3. This is what is shown in the connection diagram. The Input Channel variable can always be used to modify any of these channel assignments

Signal Amplitude

For best results, it is recommended that the signals take up 80% of the vertical grid.

Clock Frequency

By applying the Frequency measurement parameter to the CK signal, the user can verify that the DDR system is running at the expected transfer rate (Transfer Rate =Frequency * 2). This will also help in the limit selection. Do a quick visual inspection to ensure that the signal does not have any non-monotonic edges due to reflections.

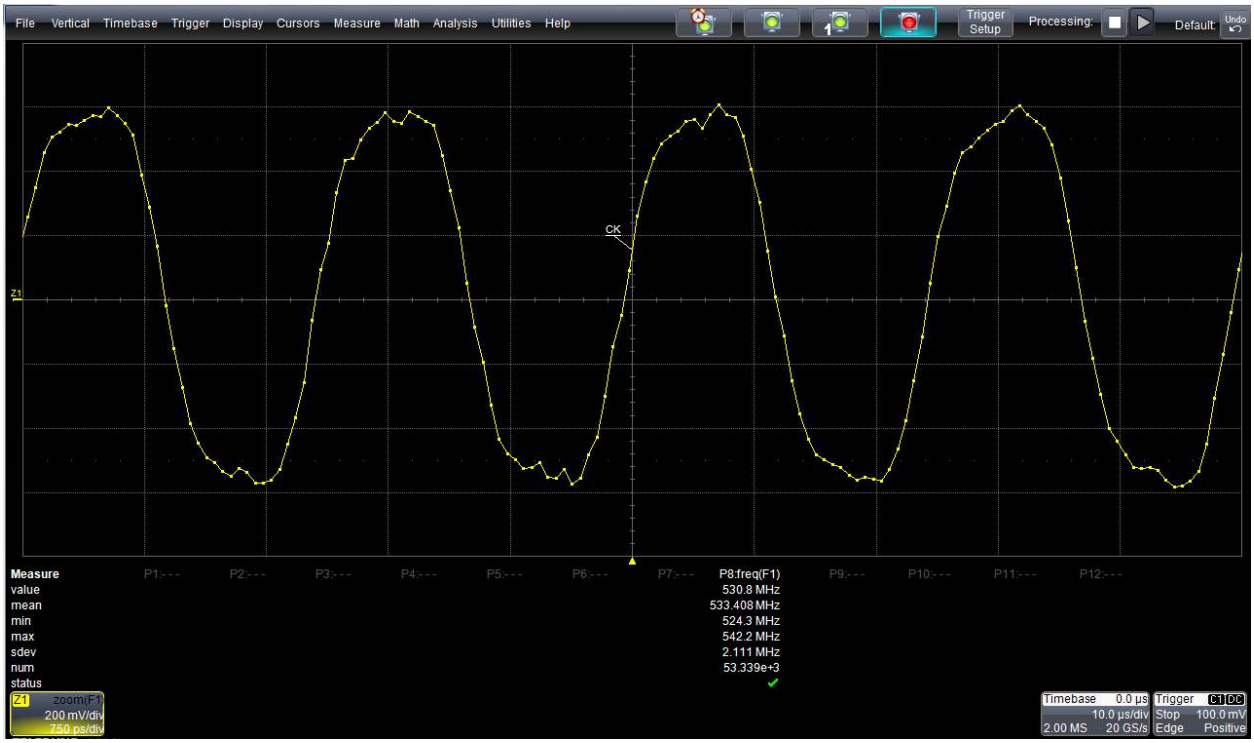


Figure 12. Verification of CK signal

Presence of R/W Burst

The operator should do a quick check to make sure their device is outputting the expected bursts. As a general rule of thumb, during a R burst DQ and DQS should be in phase and during a W burst DQ and DQS should be a quarter cycle out of phase. Additionally, the signal amplitude can be used to determine the presence of R and W bursts. If probing at the memory, R bursts will have a larger amplitude than W bursts.

Check Idle Levels

Before running QPHY-DDR2, validate the signal idle levels. Signal idle levels that are off will have an impact on the R/W burst detection, electrical, and timing measurements. DQS should have an idle level of ~ 0 mV. DQ should have an idle level of ~ VDD/2 (900 mV for DDR2).

QPHY-DDR2 Test Configurations

Test configurations include variable settings, limit sets, and test selections. See QPHY-DDR2 Variables for a description of each variable and its default value.

Clock tests DDR2-667 (1 Probe)

This configuration runs all of the clock tests using a single differential probe setup. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- tCK(avg), tCK(abs)
- tCH(avg), tCL(avg), tCH(abs), tCL(abs)
- tJIT(duty)
- tJIT(per)
- tJIT(CC)
- tERR(n per)

CKdiff-DQse-DQSdiff 667 Write Burst (3 Probes)

This configuration runs all of the tests that are run on write bursts of the DDR2 signals in which three probes are required (probe setup CKdiff-DQse-DQSdiff). All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram Tests
  - Write Bursts (Inputs)
- Electrical Tests
  - Write Bursts (Inputs)
    - Slew
      - Slew R
      - Slew F
    - Logic Levels
      - VIH(ac)
      - VIH(dc)
      - VIL(ac)
      - VIL(dc)
      - VSWING
    - AC Over/Undershoot
      - AC Overshoot Peak Amplitude
      - AC Overshoot Area above VDDQ
      - AC Undershoot Peak Amplitude
      - AC Undershoot Area below VSSQ
    - AC Over/Undershoot_DQS_CK
      - AC Overshoot Peak Amplitude
      - AC Overshoot Area above VDDQ
      - AC Undershoot Peak Amplitude
      - AC Undershoot Area below VSSQ
  - Timing Tests

- Write Bursts (Inputs)
  - Tests on bits (not using interpolation)
    - tDQSS
    - tDQSH
    - tDQSL
    - tDSS
    - tDSH
    - tDS (base+derated)
    - tDH (base+derated)

CKdiff-DQse-DQSdiff 667 Read Burst (3 Probes)

This configuration runs all of the tests that are run on read bursts of the DDR2 signals in which three probes are required (probe setup CKdiff-DQse-DQSdiff). All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram
  - Read Bursts (Outputs)
- Electrical Tests
  - Read Bursts (Outputs)
    - Sout (output slewrate)
      - SoutR
      - SoutF
      - tSLMR
- Timing Tests
  - Read Bursts (Outputs)
    - Tests on bits (no interpolation)
      - tDQSQ
      - tHP, tQHS, tQH
      - Measure tQHS
      - Measure tQH
      - tDQSCK
      - tAC

Eye Diagram (3 Probes Debug)

This configuration runs the Eye Diagram tests on both the read bursts and the write bursts using the probe setup CKdiff-DQse-DQSdiff. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram – Write Bursts (Inputs)
- Eye Diagram – Read Bursts (Outputs)

All Tests that Require 4 Probes

This configuration runs all of the tests that require four probes. These are the tests where the DQS is probed single ended, the CK is probed single ended, or the signal under test is an Address, Control or Data Mask line. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Probe setup CKdiff-DQse-DQSp-DQSn
  - Electrical Tests
    - Write Bursts (Inputs)
      - Slew
        - Slew R
        - Slew F
      - Logic Levels
        - VIH(ac)
        - VIH(dc)
        - VIL(ac)
        - VIL(dc)
        - VSWING
      - AC Over/Undershoot
        - AC Overshoot Peak Amplitude
        - AC Overshoot Area above VDDQ
        - AC Undershoot Peak Amplitude
        - AC Undershoot Area below VSSQ
      - AC Over/Undershoot_DQS_CK
        - AC Overshoot Peak Amplitude
        - AC Overshoot Area above VDDQ
        - AC Undershoot Peak Amplitude
        - AC Undershoot Area below VSSQ
    - Read Bursts (Outputs)
      - Sout (output slewrate)
        - SoutR
        - SoutF
        - tSLMR
  - Timing Tests
    - Write Bursts (Inputs)
      - tDS1(base)
      - tDH1(base)
- Probe setup CKp-CKn-DQse-DQSdiff
  - Electrical Tests
    - Write Bursts (Inputs)
      - VID(ac)
      - VIX(ac)
- Probe setup CKdiff-DQse-DQSdiff-ADD/CTRLse

- Electrical Tests
  - Write Bursts (Inputs)
    - Slew
      - Slew R
      - Slew F
    - Logic Levels
      - VIH(ac)
      - VIH(dc)
      - VIL(ac)
      - VIL(dc)
      - VSWING
    - AC Over/Undershoot
      - AC Overshoot Peak Amplitude
      - AC Overshoot Area above VDDQ
      - AC Undershoot Peak Amplitude
      - AC Undershoot Area below VSSQ
- Timing Tests
  - Write Bursts (Inputs)
    - tIS(base+derated)
    - tIH(base+derated)

- Probe setup CKdiff-DQse-DQSdiff-DMse
  - Electrical Tests
    - Write Bursts (Inputs)
      - Slew
        - Slew R
        - Slew F
      - Logic Levels
        - VIH(ac)
        - VIH(dc)
        - VIL(ac)
        - VIL(dc)
        - VSWING
      - AC Over/Undershoot
        - AC Overshoot Peak Amplitude
        - AC Overshoot Area above VDDQ
        - AC Undershoot Peak Amplitude
        - AC Undershoot Area below VSSQ
  - Timing Tests
    - Write Bursts (Inputs)
      - tDS(base+derated)
      - tDH(base+derated)

PrePostAmble Tests (3 Probes)

This configuration will run all DDR2 timing tests available on Preambles and Postambles when signals CKdiff-DQse-DQSdiff are connected. Use fixed value for Gain and Offset adapted to DDR2 levels.

The results of these measurements depend on the manner in which the signal returns to idle and in some cases will not give the intended results. In addition, the method for measurement is not completely defined by the DDR2 specification (see JESD79-2E, figure 97). For these reasons, if you choose to run these tests, do with care.

The tests run are:

- Timing Tests
    - Read Bursts (Outputs)
        - PrePostable tests using interpolation
            - tHZ(DQ)
            - tLZ(DQ)
            - tLZ(DQS)
            - tRPRE
            - tRPST
    - Write Bursts (Inputs)
        - Tests on PrePostamble using interpolation
            - tWPRE
            - tWPST

Demo of All Tests

This configuration uses saved waveforms in oscilloscope D:\Waveforms\DDR2 to run all of the DDR2 tests listed above. All variables are set to their defaults, except Use Stored Waveforms is set to Yes and Use Stored Trace for Speed Grade is set to Yes. The limit set in use is DDR2-667.

QPHY-DDR2 Test Descriptions

These are the standard DDR2 compliance tests.

Clock Tests

All time measure on clock CK are done at level VREF.

tCK(avg), Average Clock Period

tCK(avg) is defined as the average clock period over any 200 consecutive clock periods.

tCK(avg) = SUM(tCKi) / 200 where i=1 to 200

Measured on both the rising and the falling edge.

tCK(abs), Absolute Clock Period

tCK(abs) is defined as the absolute clock period of each of 200 consecutive clock periods.

Measured on both the rising and the falling edge.

tCH(avg), Average High Pulse Width

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

tCH(avg) = SUM(tCHi) / (200 x tCK(avg)) where I = 1 to 200

See Figure 13 as follows.

tCL(avg), Average Low Pulse Width

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

tCL(avg) = SUM(tCLi) / (200 x tCK(avg)) where i=1 to 200

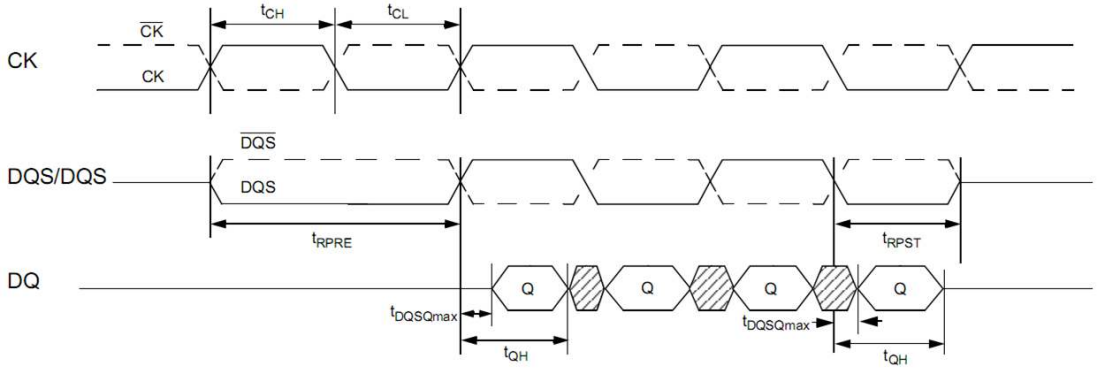


Figure 13. Data output (read) timing [JESD79-2E figure 32]

tCH(abs), Absolute High Pulse Width

tCH(abs) is defined as the absolute high pulse width, of each of 200 consecutive high pulses.

tCL(abs), Absolute Low Pulse Width

tCL(abs) is defined as the absolute low pulse width of each of 200 consecutive low pulses.

tJIT(duty), Half Period Jitter

Applicable only to 667 and 800 MHz device only.

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter over 200 consecutive cycles.

tCH jitter is the largest deviation of any single tCH from tCH(avg).

tCL jitter is the largest deviation of any single tCL from tCL(avg).

tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}

where,

tJIT(CH) = {tCHi - tCH(avg) where i=1 to 200}

tJIT(CL) = {tCLi - tCL(avg) where i=1 to 200}

tJIT(per), Clock Period Jitter

Applicable only to 667 and 800 MHz device only.

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). This test compares the average clock period (over 200 cycles) with each period inside the window. The smallest and largest values must be within limits.

tJIT(per) = Min/max of {tCKi - tCK(avg)} where i=1 to 200

Measured on both the rising and the falling edge.

There are different limits depending on whether the DLL is already locked or not:

- tJIT(per) defines the single period jitter when the DLL is already locked.
- tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

A configuration variable allows to define which limit to use.

tJIT(cc), Cycle to Cycle Period Jitter

Applicable only to 667 and 800 MHz device only.

tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles. This test compares the smallest and largest values of the difference between any two consecutive clock cycles inside a 200 cycles window.

tJIT(cc) = Min/max of {tCKi+1 – tCKi} where i = 1 to 199

Measured on both the rising and the falling edge.

There are different limit depending on whether the DLL is already locked or not:

- tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
- tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

A configuration variable allows to define which limit to use.

tERR(n per), Cumulative Error

Applicable only to 667 and 800 MHz device only.

tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg). This test compares the average clock period (over 200 cycles) with each n-bit period inside the window. The smallest and largest values must be within limits.

There are 6 different tests:
tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)

tERR(nper) = Min/max of {SUM(tCKi) - n x tCK(avg)}

where i=1 to n and:

n = 2 for tERR(2per)

n = 3 for tERR(3per)

n = 4 for tERR(4per)

n = 5 for tERR(5per)

6 ≤ n ≤ 10 for tERR(6-10per)

11 ≤ n ≤ 50 for tERR(11-50per)

Measured on both the rising and the falling edge.

Eye Diagram Tests

Write Burst (Inputs)

This is an informational only test that creates the eye diagram of all the write bursts found in the acquisition.

Read Burst (Outputs)

This is an informational only test that creates the eye diagram of all the read bursts found in the acquisition.

Electrical Tests on Write Bursts (Inputs)

Slew (input slew rate): SlewR and SlewF

Applies to all input signals. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(ac) min for rising edges (SlewR) and the range from VREF to VIL(ac) max for falling edges (SlewF) of single-ended signal.

For differential signals (e.g. CK - CK#) slew rate for rising edges is measured from CK - CK# = - 250 mV to CK - CK# = + 500 mV (+ 250 mV to - 500 mV for falling edges).

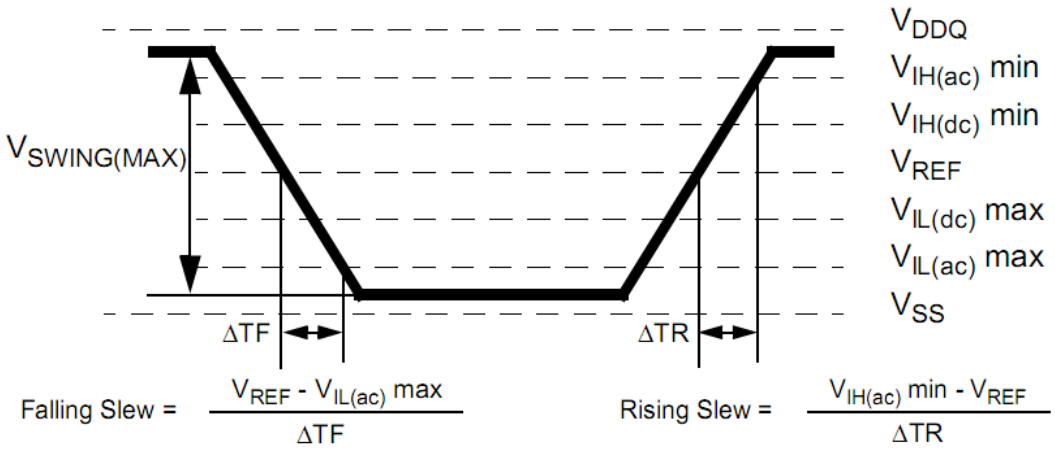


Figure 14. AC input test signal waveform [JESD79-2E figure 73]

Logic Levels

VIH(ac), maximum AC input logic high

Measures the local maximum value from VREF to VREF of the high pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

The lowest number must be greater than or equal to the minimum limit and the highest number must be less than or equal to the maximum limit.

VIH(dc), minimum DC input logic high

Measures the local minimum and maximum values from the first VIH(ac)min crossing point to the time corresponding to VIH(dc)min crossing a 1V/ns slewrate slope to VREF. If multiple pulses are measured, take the lowest, respectively the highest, number as the worst case.

The local minimum must be greater than or equal to the minimum limit. The local maximum must be less than or equal to the maximum limit.

VIL(ac), maximum AC input logic low

Measures the local minimum value from VREF to VREF of the low pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

The lowest number must be greater than or equal to the minimum limit and the highest number must be less than or equal to the maximum limit.

VIL(dc), minimum DC input logic low

Measures the local minimum and maximum values from the first VIL(ac)max crossing point to the time corresponding to VIL(dc)max crossing a 1V/ns slewrate slope to VREF. If multiple pulses are measured, take the lowest, respectively the highest, number as the worst case. The local minimum must be greater than or equal to the minimum limit. The local maximum must be less than or equal to the maximum limit.

VSWING(MAX), input signal maximum peak to peak swing

Measures the peak-to-peak value of the signal in a given Write frame. If multiple frames are measured, take, the highest number as the worst case. The measure must be less than or equal to the limit.

VID(ac), AC Differential Input Voltage

VID(ac) specifies the input differential voltage | VTR - VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as CK, DQS, LDQS or UDQS). The minimum value is equal to VIH(ac) - VIL(ac). This test requires probing each half of a differential signal. This test is only available in the configurations using 4 probes.

VIX(ac), AC Differential Input Cross Point Voltage

The typical value of VIX(ac) is expected to be about 0.5 x VDDQ of the transmitting device and VIX(ac) is expected to track variations in VDDQ. VIX(ac) indicates the voltage at which differential input signals must cross. This test requires probing each half of a differential signal. This test is only available in the configurations using 4 probes.

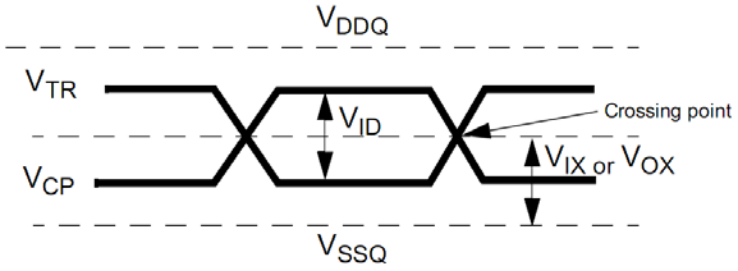


Figure 15. Differential signal levels [JESD79-2E figure 74]

AC Over/Undershoot

AC Overshoot Peak Amplitude

Measures maximum peak amplitude allowed for overshoot area.

AC Overshoot Area above VDDQ

Measures maximum overshoot area above VDDQ. AC Overshoot Peak Amplitude is prerequisite to compute area.

AC Undershoot Peak Amplitude

Measures maximum peak amplitude allowed for undershoot area.

AC Undershoot Area Below VDDQ

Measures Maximum undershoot area below VSSQ. AC Undershoot Peak Amplitude is prerequisite to compute area.

AC Over/Undershoot_DQS_CK

Same four tests as above group, only performed on the Data Strobe and Clock signals.

Note: The maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Register vendor data sheets specify the maximum over/undershoot induced in specific RDIMM applications. DRAM vendor data sheets also specify the maximum overshoot/undershoot that their DRAM can tolerate. This allows the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register induces in the specific RDIMM application. A variable allows this limit to be changed.

Electrical Tests on Read Bursts (Outputs)

Sout (Output Slew Rate)

Rise and Fall

Applies to all output signals (DQn data signals), but only for 400, 533 and 667 MHz device, not for 800 MHz device. The output slew rate is measured from VIL(ac) to VIH(ac) for the rising edge and from VIH(ac) to VIL(ac) for the falling edge. DRAM output slew rate specification applies to 400, 533 & 667 MHz speed devices.

Note: Absolute value of the slew rate as measured from (dc) to (dc) >= Slew rate as measured from (ac) to (ac).This is guaranteed by design and characterization. Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - DQS#) output slew rate is measured between DQS - DQS# = - 500 mV and DQS - DQS# = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

tSLMR

This is the ratio of the rising edge slewrate to the falling edge slewrate. This is a test recommended by Intel but not reported in the Jedec JESD79-2E standard. Therefore it is not selected in the standard configurations, but only in the All Tests configuration.

VOX(ac)

Measures AC Differential Output Cross Point Voltage. The typical value of VOX(ac) is expected to be about 0.5 x VDDQ of the transmitting device and VOX(ac) is expected to track variations in VDDQ . VOX(ac) indicates the voltage at which differential output signals must cross. This test requires probing each half of a differential signal. This is only available in the configurations using 4 probes.

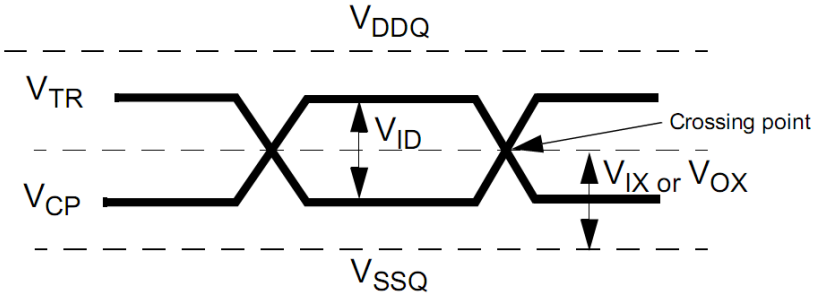


Figure 16. Differential signal levels [JESD79-2E figure 74]

Timing Tests on Read Bursts (Outputs)

Tests on Bits (no interpolation)

tDQSQ

DQS-DQ Skew for DQS and associated DQ signals, the maximum skew between the DQS line and the associated DQ line within a read burst. Measures timing from DQS at VREF to DQ rising at VIH(ac)min and falling at VIL(ac)max.

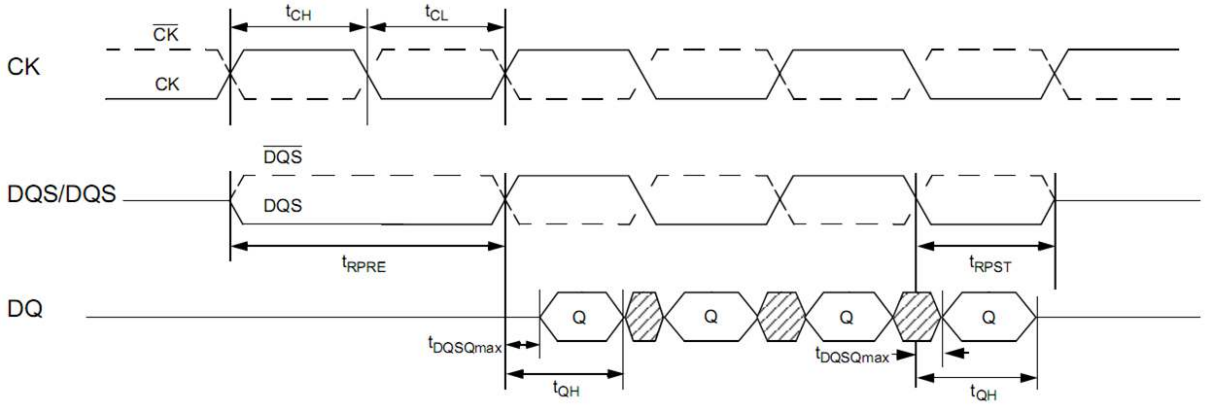


Figure 17. Data output (read) timing [JESD79-2E figure 32]

tHP

Clock half pulse width test. Result of tCL and tCH Clock Tests is prerequisite. tHP refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). tHP is the minimum of the absolute half period of the actual input clock.

tHP is an input parameter but not an input specification parameter, hence no limits are applied, it is reported as informational only. It is used in conjunction with tQHS to derive the DRAM output timing tQH.

tHP = Min (tCH(abs), tCL(abs))

where,

tCH(abs) is the minimum of the actual instantaneous clock HIGH time;

tCL(abs) is the minimum of the actual instantaneous clock LOW time;

tQHS

DQ hold skew factor. This measures the sum of CK at VREF to DQS at VREF and DQ at VIH(dc) or VIL(dc) to DQS at VREF

tQH

DQ/DQS output hold time from DQS. This measures the timing from DQS at VREF to DQ at VIH(dc) (rising edge) or VIL(dc) (falling edge). tHP result is prerequisite:to compute the limit.

tDQSCK

DQS output access time from CK/CK #time from CK at VREF level to DQS at VREF level. This is a measure similar to tDQSS but on the Read frame and on both edges (the result can be negative). tERR(6-10per) is preprequisite. A derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only.

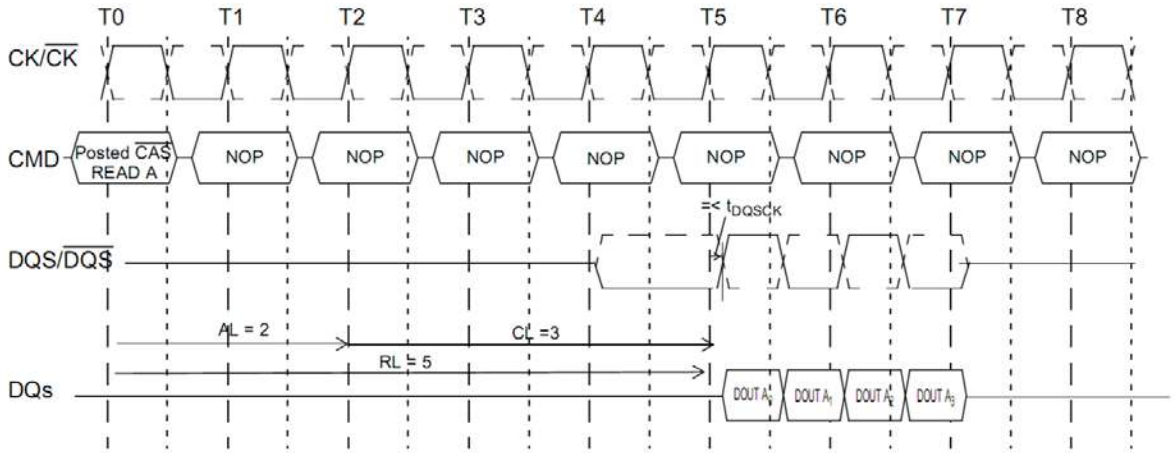


Figure 18. Burst read operation [JESD79-2E figure 33]

tAC

DQ output access time from CK/CK#. Time from CK at VREF level to DQ at VIH(ac) or VIL(ac) level. tERR(6-10per) is prerequisite. a derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only.

PrePostAmble Tests (using interpolation)

tHZ(DQ)

DQ high impedance time from CK/CK#. This is the time from Vref of the CK/CK# signal to the point when the DQ is not being driven anymore (at the end of the burst)

tLZ(DQ)

DQ low impedance time from CK/CK#. This is the time from when the DQ begins to be driven (at the beginning of the burst) to the nearest CK/CK# edge.

tLZ(DQS)

DQS low impedance time from CK/CK#. This is the time from when the DQS begins to be driven (at the beginning of the preamble) to the nearest CK/CK# edge.

tRPRE

Read Preamble, time from when DQS begins to be driven (at the beginning of the preamble) to when it crosses Vref. This is only measured on a read cycle. tJIT(per) is prerequisite. A derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only.

tRPST

Read Postamble, time from when DQS crosses Vref (at the beginning of the postamble) to when DQS stops being driven (at the end of the postamble). This is only measured on a read cycle. tJIT(duty) is prerequisite. A derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only.

Timing Tests on Write Bursts

Tests on Bits (no interpolation)

tDQSS

DQS latching rising transitions to associated CK edge. CK rising edge at VREF level to DQS rising edge at VREF level, see Figure 19.

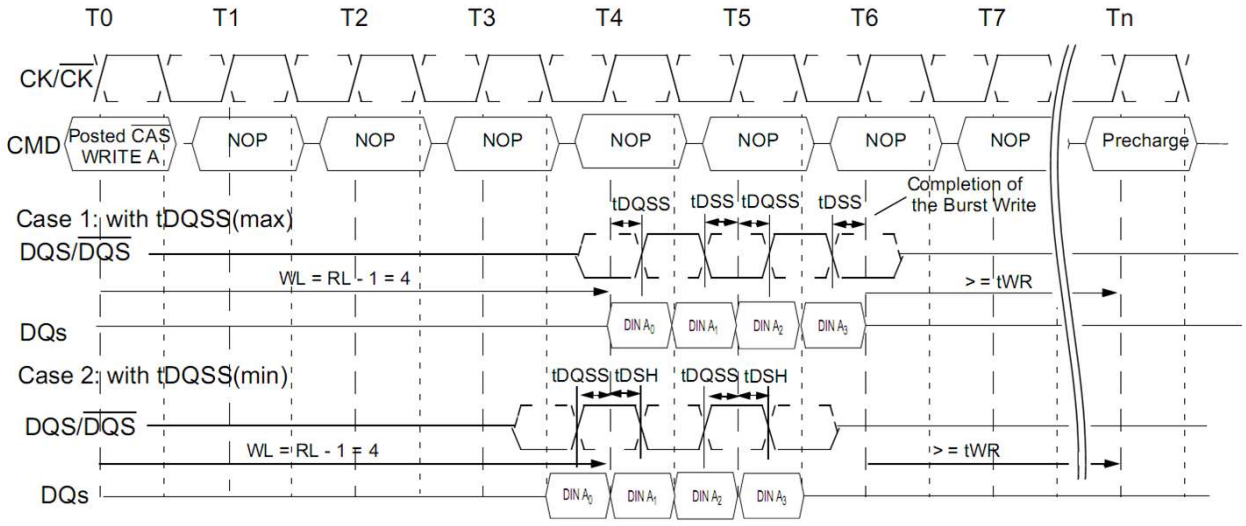


Figure 19. Burst write operation [JESD79-2E figure 39]

tDQSH

DQS input high pulse width at VREF level, see Figure 20.

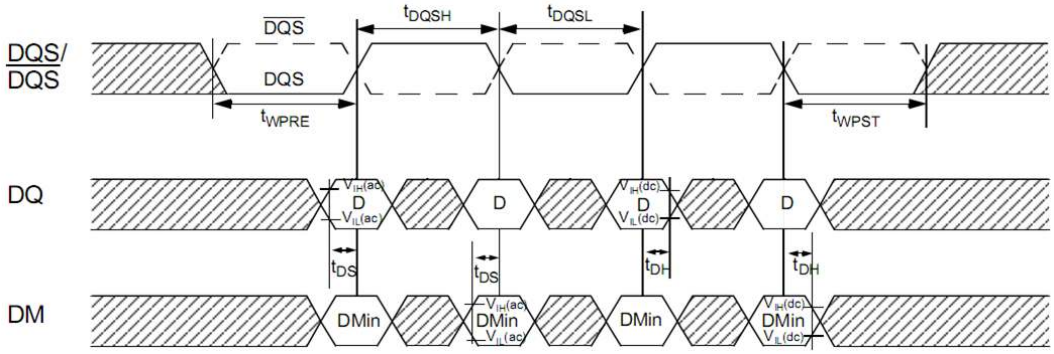


Figure 20. Data input (write) timing [JESD79-2E figure 38]

tDQSL

DQS input low pulse width at VREF level, see Figure 20.

tDSS

Time from DQS falling edge at VREF level to CK rising edge at VREF level, see Figure 20.

tDSH

DQS Falling Edge Hold Time from CK, time from CK rising edge at VREF level to DQS falling edge at VREF level, see Figure 20.

tDS1(base)

Single-Ended DQ and DM Input Setup Time, This is referenced from the input signal crossing at the VIH(ac)min level to the single-ended data strobe crossing VIH(dc)min or VIL(dc)max at the start of its transition for a rising signal, and from the input signal crossing at the VIL(ac)max level to the single-ended data strobe crossing VIH(dc)min or VIL(dc)max at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between VIL(dc)max and VIH(dc)min. See Figure 26 below.

Jedec JESD79-2E Specific Note 8 (page 85 to 94) with table 45 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

This test is only applicable only to 400 and 533 MHz devices, and only in configurations using four probes.

tDH1(base)

Single-Ended DQ and DM Input Hold Time. This is referenced from the input signal crossing at the VIH(dc)min level to the single-ended data strobe crossing VIH(ac)min or VIL(ac)max at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc)max level to the single-ended data strobe crossing VIH(ac)min or VIL(ac)max at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between VIL(dc)max and VIH(dc)min. See Figure 26 below.

Jedec JESD79-2E Specific Note 8 (page 85 to 94) with table 45 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

This test is only applicable only to 400 and 533 MHz devices, and only in configurations using four probes.

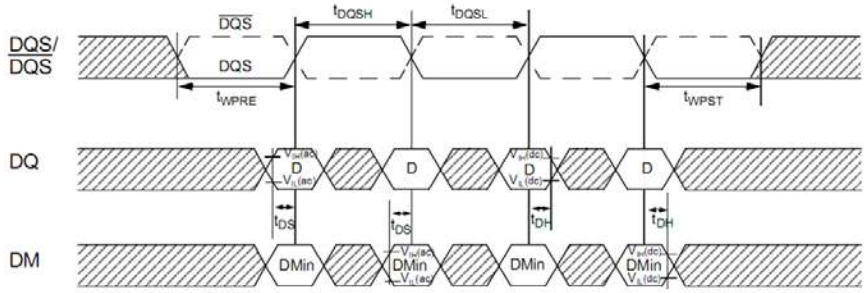


Figure 21. Data input (write) timing [JESD79-2E figure 38]

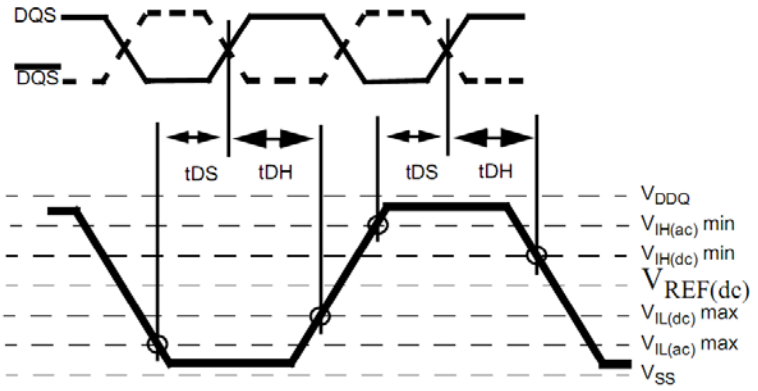


Figure 22. Differential input waveform timing - tDS and tDH [JESD79-2E figure 98]

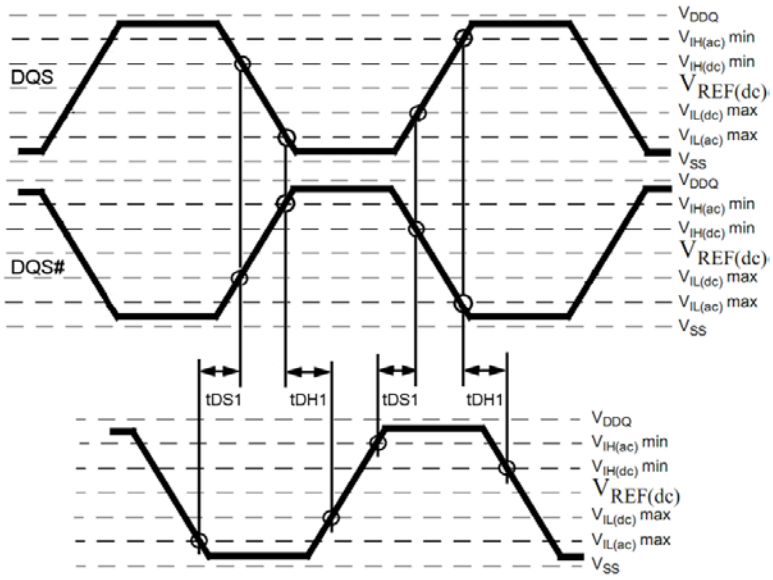


Figure 23. Single-ended input waveform timing - tDS1 and tDH1

tDS(base+derated)

DQ and DM Input Setup Time. Input waveform timing tDS with differential data strobe enabled, is referenced from the input signal crossing at the VIH(ac)min level to the differential data strobe crosspoint at VREF for a rising signal, and from the input signal crossing at the VIL(ac)max level to the differential data strobe crosspoint at VREF for a falling signal applied to the device under test. DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

JESD79-2E Specific Note 8 (page 85 to 94) with tables 43 and 44 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the delta tDS and delta tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + delta tDS. For example:

data sheet tDS(base) = 100 ps minimum
delta tDS = 100 ps
total tDS (setup time) required = 200 ps
measured: min = 567 ps (no derating)
measured: min = 467 ps (derated)

tDH(base+derated)

DQ and DM Input Hold Time. Input waveform timing tDH with differential data strobe enabled, is referenced from the differential data strobe crosspoint at VREF to the input signal crossing at the VIH(dc)min level for a falling signal and from the differential data strobe crosspoint at VREF to the input signal crossing at the VIL(dc)max level for a rising signal applied to the device under test. DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

JESD79-2E Specific Note 8 (page 85 to 94) with tables 43 and 44 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tIS(base+derated)

Address and Control Input Setup Time. Input waveform timing is referenced from the input signal crossing at the VIH(ac)min level to the differential clock crosspoint at VREF for a rising signal, and from the input signal crossing at the VIL(ac)max level to the differential clock crosspoint at VREF for a falling signal applied to the device under test. See Figure 24.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

Jedec JESD79-2E Specific Note 9 (page 95 to 100) with tables 46 and 47 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tIH(base+derated)

Address and Control Input Hold Time. Input waveform timing is referenced from the input signal crossing at the VIL(dc)max level to the differential clock crosspoint at VREF for a rising signal, and from the input signal crossing at the VIH(dc)min level to the differential clock crosspoint at VREF for a falling signal applied to the device under test. See Figure 24.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

Jedec JESD79-2E Specific Note 9 (page 95 to 100) with tables 46 and 47 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

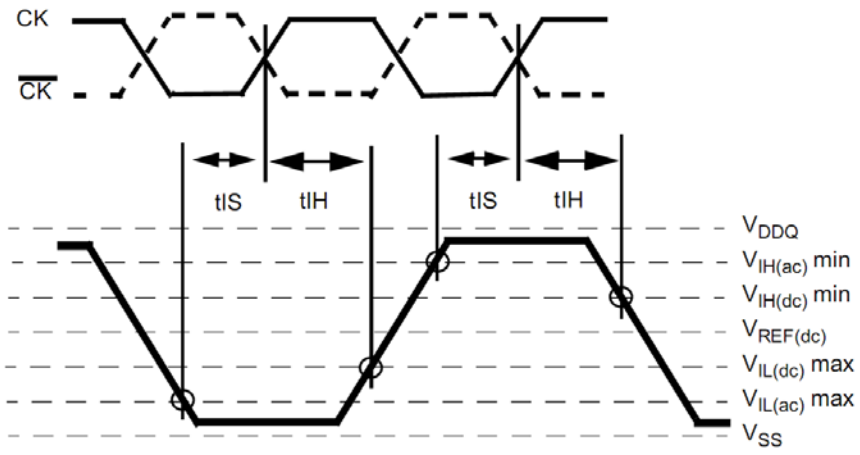


Figure 24. Differential input waveform timing - tIS and tIH [JESD79-2E figure 99]

Tests on PrePostamble (using interpolation)

tWPRE

Write Preamble, time from when DQS begins to be driven (at the beginning of the preamble) to when it crosses Vref. This is only measured on a write cycle.

tWPST

Write Postamble, time from when DQS crosses Vref (at the beginning of the postamble) to when DQS stops being driven (at the end of the postamble). This is only measured on a write cycle. SLEW of DQ and DQS is prerequisite. A derating factor is applied to the limit depending on the signals slewrate. This is applicable for the following four tests.

QPHY-DDR2 Variables

Main Settings

The following variables are used by all configurations. They can be used in conjunction with the test selection and limit set selection to create custom configurations.

Custom Speed Grade in MT/s

Custom Speed Grade of the DUT (Data Rate). Used to set the oscilloscope timebase and sampling rate. See Clock Period Per Screen Division for more explanation. Automatically updated from limit set when default value is set (0 MT/s). Value can be also any custom Speed Grade.

DQ Signal Name

Select name of data (DQ) SUT. Choose between available DDR signal names. Default is DQ0.

DQS Signal Name

Select name of strobe (DQS) SUT. Choose between available DDR signal names. Default is DQS0.

Clock Signal Name

Select name of clock (CK) SUT. Choose between available DDR signal names. Default is CK.

DUT Power Supply VDDQ

Value of VDDQ used to compute test limits as specified by Jedec standard. Default is 1.8 V.

4th Probe Names

DQSp Signal Name

Select the name of the positive strobe (DQSp) SUT. Choose between available DDR signal names. Default is DQS0p.

DQSn Signal Name

Select the name of the negative strobe (DQSn) SUT. Choose between available DDR signal names. Default is DQS0n.

ADD/CTRL signal name

Select the name of the Address or Control SUT. Choose between available DDR signal names. Default is A0.

Clock Negative Signal Name

Select the name of the negative clock (CKn) SUT. Choose between available DDR signal names. Default is CKn.

Clock Positive Signal Name

Select the name of the positive clock (CKp) SUT. Choose between available DDR signal names. Default is CKp.

DM Signal Name

Select the name of the Data Mask SUT. Choose between available DDR signal names. Default is DM0.

Script Settings

Enable Prompt Before Signal Acquisition

Enables/disables prompt to begin signal acquisition, allowing user to generate read/write bursts at the start of the acquisition or to modify the trigger conditions before signal acquisition. Set to “True” to enable. Default is False.

Save Acquired Waveforms

Saved waveforms can be used later in demonstration or optimized version of script. Choose between Yes or No. The default is No. This setting is ignored (no save) if using stored waveforms is enabled and in Demo mode.

Silent Mode Control

No more interaction with the user when silent mode is on. Choose between Yes or No. Default is No. This is useful to let the test run without interruption in the background.

Stop on Test to Review Results

When set to Yes, the script stops after each test allowing you to view the results. The setup is saved so the oscilloscope settings can be modified by the user. On resume, the setup is recalled. Any new acquisition done may cause the script to produce unexpected results.

Waveform Path

Full path to the oscilloscope folder in which to save/recall waveforms. When not in Demo Mode and when Save acquired waveforms is enabled, the waveforms are saved in this folder. When set to Demo Mode or when Use stored trace for pixel clock measure, waveforms are also available from this folder. The default location is D:\Waveforms\DDR2.

Demo Settings

Use Stored Waveforms
When enabled, previously stored DDR2 waveforms are used. Default is No for compliance test configurations, Yes for Demo configurations.

Recalled Waveform File Index (5 digits)
Five digit number corresponding to the index of the file you want to recall. Default is 00000.

Define Format Used to Set Trace Names
Naming method for saving waveforms. LeCroy composes waveform names automatically from signal names (e.g., C1-00000.trc). **Dialog** prompts the user for custom waveform names. The default setting is LeCroy.

Use Stored Trace for Speed Grade
This is an optimization used specifically to measure the clock frequency only once. Choose from **Yes** or **No** values, The default selection is No.

Advanced Settings

Clock Period per Screen Division
Oscilloscope timebase and sampling rate is set to acquire the given number of clock cycle per display horizontal division at a given Custom (DUT) Speed Grad in MT/s and for a Max. Number of Samples Per Clock Period. The default is 3341 clock periods (a 10us/div timebase at 667 MT/s and 3.3MS max for 100 samples per period).

Timebase = [Clock Period Per Screen Division] / ([DUT Speed Grade in MT/s] / 2 * 1e6)

Maximum Samples = [Max. Number Of Samples Per Clock Period] * [Clock Period Per Screen Division] * 10

Number of Cycles for Clock Test
Jedec standard requires 200 cycles for the Clock compliance test. Any positive number can be entered. Default is 200.

Check for Valid Pre and Postambles
If set to Yes, all the bursts with invalid preamble and/or postambles (not standard pre/postamble shape as defined by the spec) are ignored (not included in tests). If set to No, the user is warned when the preamble and/or postamble are detected as having a non-standard shape. Default is No.

Max. Number of Samples Per Clock Period
The oscilloscope timebase and sampling rate is set to acquire the given number of points per clock period. The oscilloscope is always set to at least acquire at 20GS/s. Additionally, if an oscilloscope with greater than 6GHz bandwidth is used, the bandwidth is limited to 6GHz. See the Clock Period Per Screen Division variable for more details. Choose from 10;20;50;100;200;500 or 1000. The default value is 100.

Probe Setup <type> Variables

The following variables are specific to the different probe setups that may appear in different configurations. Some of these setups appear under multiple configurations.

Probe Tip Selection
Specifies probe tip used (e.g., SI, PT, SMA/SMP, SP or HighTemp). Applies to all probes in the setup.

<Signal> Channel Gain
Allows the user to manually specify the vertical scale in V/div. Signal can be Clock, DQ, DQS, DQSn, ADD/CTRL, or DM. Default is 0 for auto-scale.

<Signal> Channel Index
Oscilloscope input channel used for the respective signal. For example, when the Clock is input to C1, Clock Channel Index is 1.

<Signal> Channel Invert
Inverts the respective signal. For example, to invert the Clock signal, set Clock Channel Invert to True. Default is False.

<Signal> Channel Offset
Specifies the offset in Volts to apply to the respective signal. Default value of 0 applies auto-scale. Only used if Gain is > 0.

<Signal> Signal Type
Specifies whether respective signal is probed Differential or Single-ended. For example, if the DQS signal is probe differential, DQS Signal Type variable is Diferential.

Select Signal Under Test If Many
Specifies which signals to test for particular tests. The default state for this variable includes all pertinent signals. For example, when testing input slew rate, the Slew Signal Under Test if many defaults to DQ, DQS, CK.

Use Vref Level for DQ Read Timings
Specifies whether or not to use Vref level for DQ Read timing tests of tDQSQ and TQH, instead of VIL/VIH (ac/dc)

Previously Measured tHP in Seconds
tHP is usually computed from the result of test tCH/tCL. However if a result is not available, the value entered here is used. If this variable is set to 0, then tHP is computed from the Custom Speed Grade in MT/s.

Max Overshoot Peak Amplitude
For address and control signals, the maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Default value is 0.5 V.

Note: Register vendor data sheets specify the maximum over/undershoot induced in specific RDIMM applications. DRAM vendor data sheets also specify the maximum overshoot/undershoot that their DRAM can tolerate. This allows the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register induces in the specific RDIMM.

QPHY-DDR2 Limit Sets

DDR2-400

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 400 MT/s.

DDR2-533

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 533 MT/s.

DDR2-667

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 667 MT/s.

DDR2-800

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 800 MT/s.

DDR2-1066

This corresponds to the JEDEC JESD208 DDR2 standard specification limits for 1066 MT/s.

Appendix A: Manual Deskewing Procedures

Cable Deskewing Using the Fast Edge Output

The following procedure demonstrates how to manually deskew two oscilloscope channels and cables using the fast edge output, with no need for any T connector or adapters.

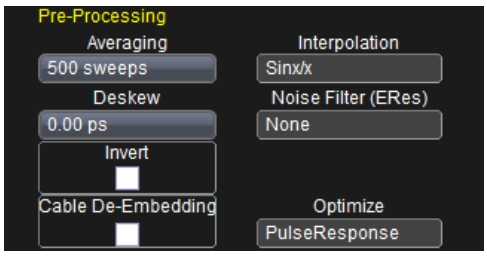
Note: This procedure only applies to the oscilloscope and cables connected directly to oscilloscope channels. Fast Edge output is available only on some models. If your oscilloscope does not have Fast Edge output, see Cable Deskewing Without Using the Fast Edge Output.

This can be done once the temperature of the oscilloscope is stable. The oscilloscope must be warmed up for at least 20 min. before proceeding. This procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

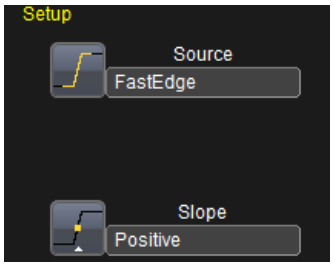
For the purpose of this procedure, the two channels being deskewed are referred to as Channel X and Channel Y. The reference channel is Channel X and the channel being deskewed is Channel Y.

1. Begin by recalling the Default Oscilloscope Setup.
2. Configure the oscilloscope as follows:
    - Timebase
        i. Fixed Sample Rate
        ii. Set the Sample Rate to 40 GS/s
        iii. Set the Time/Division to 1 ns/div

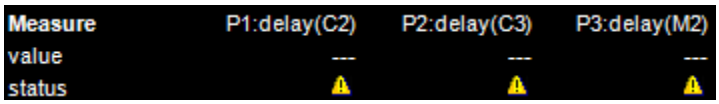
    - Channels
        i. Turn on Channel X and Channel Y.
        ii. Set V/div for Channel X and Channel Y to 100mV/div.
        iii. Set the Averaging of Channel X and Channel Y to 500 sweeps.
        iv. Set the Interpolation of Channel X and Channel Y to Sinx/x.



- Trigger
    i. Configure to **Source** to be **FastEdge**.
    ii. Set the **Slope** to **Positive**.



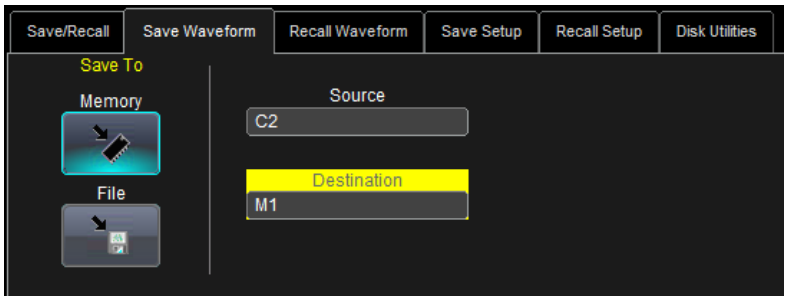
- Parameter Measurements:
    i. Set the **source** for P1 to CX and the **measure** to Delay.
    ii. Set the **source** for P2 to CY and the **measure** to Delay.
    iii. Set the **source** for P3 to M1 and the **measure** to Delay.



3. Set the display to Single Grid.
    - Click **Display → Single Grid**.
4. Using the appropriate adapter, connect Channel X to the Fast Edge Output of the oscilloscope.
5. Adjust the Trigger Delay so that the Channel X signal crosses at the center of the screen.
6. Change the **Timebase** to 50 ps/div.

7. Fine tune the Trigger Delay so that the Channel X signal crosses at the exact center of the screen.
8. Press the **Clear Sweeps** button on the front panel to reset the averaging.
9. Allow multiple acquisitions to occur until the waveform is stable on the screen.

10. Save Channel X to M1.
    - Click **File → Save Waveform**.
    - Set **Save To Memory**.
    - Set the **Source** to **CX**.
    - Set the **Destination** to **M1**.
    - Click **Save Now**.



11. Disconnect Channel X from the Fast Edge Output and connect Channel Y to the Fast Edge Output.
12. Press the **Clear Sweeps** button on the front panel to reset the averaging.
13. Allow multiple acquisitions to occur until the waveform is stable on the screen.
14. From the Channel Y menu, adjust the **Deskew** of Channel Y until Channel Y is directly over the M1 trace.
15. Ensure that P3 and P2 are reasonably close to the same value. (Typically < 5ps difference)

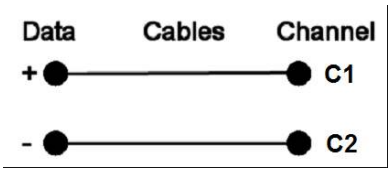
Cable Deskewing Without Using the Fast Edge Output

The following procedure demonstrates how to manually deskew two oscilloscope channels and cables using the differential data signal, with no need for any T connector or adapters.

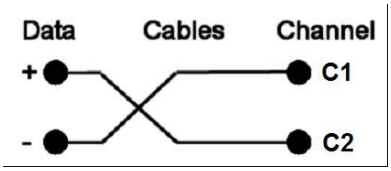
Note: This procedure only applies to the oscilloscope and cables connected directly to oscilloscope channels.

Warm the oscilloscope for at least a half-hour before proceeding. This procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

1. Connect a differential data signal to C1 and C2 using two approximately matching cables. Set up the oscilloscope to use the maximum sample rate. Set the timebase for a few repetitions of the pattern (at least a few dozen edges).



2. On the C3 menu, check **Invert**. Now C1 and C2 should look the same.
3. Using the **Measure Setup**, set P1 to measure the Skew of C1, C2. Turn on **Statistics** (**Measure** menu). Write down the mean skew value after it stabilizes. This mean skew value is the addition of Data skew + cable skew + channel skew.
4. Swap the cable connections on the Data source side (on the test fixture), and then press the **Clear Sweeps** button on the oscilloscope (to clear the accumulated statistics; since we changed the input).



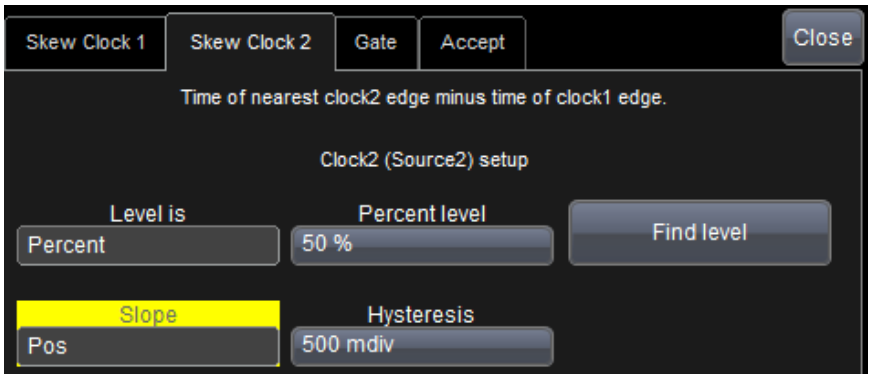
5. Write down the mean skew value after it stabilizes. This mean skew value is the addition of (-Data skew) + cable skew + channel skew.
6. Add the two mean skew values and divide the sum in half:

$$\frac{\text{[cable skew + channel skew]}}{2}$$

7. Set the resulting value as the Deskew value in C1 menu.
8. Restore the cable connections to their Step 1 settings (previous). Press the **Clear Sweeps** button on the oscilloscope. The mean skew value should be approximately zero - that is the data skew. Typically, results are <1ps given a test fixture meant to minimize skew on the differential pair.
9. On the C2 menu, clear the **Invert** checkbox and turn off the parameters.

In the previous procedure, we used the default setup of the Skew parameter (which is detecting positive edges on both signals at 50%). We also inverted C2 in order to make C1 and C2 both have positive edges at the same time.

Alternately, we clearly could have not inverted C2 and instead selected the Skew clock 2 tab in the P1 parameter menu and set the oscilloscope to look for negative edges on the second input (C2). However, we believe that the previous procedure looks much more aesthetically pleasing from the display as it shows C2 and C3 with the same polarity.



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