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December 2015

FSB70625 Motion SPM[®] 7 Series

Features

- UL Certified No. E209204 (UL1557)
- High Performance PQFN Package
- 250 V $R_{DS(on)} = 0.8 \Omega(\text{Max})$ FRFET MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- HVIC for Gate Driving with Under-Voltage Protection and Interlock Function
- Isolation Rating: 1500 V_{rms} / min.
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

Application

- 3-Phase Inverter Driver for Small Power AC Motor Drives

Related Source

- [AN-9077 - Motion SPM[®] 7 Series User's Guide](#)
- [AN-9078 - Surface Mount Guidelines for Motion SPM[®] 7 Series](#)

General Description

The FSB70625 is an advanced Motion SPM[®] 7 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET[®] technology) to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, thermal monitoring, fault reporting and interlock function. The built-in one HVIC translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.



3D Package Drawing (Click to Activate 3D Content)

Package Marking & Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|----------|---------|-----------|------------|------------|
| FSB70625 | FSB70625 | PQFN27A | 13" | 24 mm | 1000 units |

Absolute Maximum Ratings

Inverter Part (each MOSFET unless otherwise specified.)

| Symbol | Parameter | Conditions | Rating | Unit |
|--------------|---------------------------------------|---|--------|------|
| V_{DSS} | Drain-Source Voltage of Each MOSFET | | 250 | V |
| $*I_{D\ 25}$ | Each MOSFET Drain Current, Continuous | $T_{CB} = 25^{\circ}\text{C}$ (1st Note 1) | 6.9 | A |
| $*I_{D\ 80}$ | Each MOSFET Drain Current, Continuous | $T_{CB} = 80^{\circ}\text{C}$ | 5.2 | A |
| $*I_{DP}$ | Each MOSFET Drain Current, Peak | $T_{CB} = 25^{\circ}\text{C}$, $PW < 100\ \mu\text{s}$ | 13.9 | A |
| $*P_D$ | Maximum Power Dissipation | $T_{CB} = 25^{\circ}\text{C}$, For Each MOSFET | 81 | W |

Control Part (each HVIC unless otherwise specified.)

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------|-------------------------------|----------------------------------|--------------------------|------|
| V_{DD} | Control Supply Voltage | Applied Between V_{DD} and COM | 20 | V |
| V_{BS} | High-side Bias Voltage | Applied Between V_B and V_S | 20 | V |
| V_{IN} | Input Signal Voltage | Applied Between IN and COM | $-0.3 \sim V_{DD} + 0.3$ | V |
| V_{FO} | Fault Output Supply Voltage | Applied Between FO and COM | $-0.3 \sim V_{DD} + 0.3$ | V |
| I_{FO} | Fault Output Current | Sink Current FO Pin | 5 | mA |
| V_{CSC} | Current Sensing Input Voltage | Applied Between Csc and COM | $-0.3 \sim V_{DD} + 0.3$ | V |

Total System

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------|--------------------------------|---|----------------|--------------------|
| T_J | Operating Junction Temperature | | $-40 \sim 150$ | $^{\circ}\text{C}$ |
| T_{STG} | Storage Temperature | | $-40 \sim 125$ | $^{\circ}\text{C}$ |
| V_{ISO} | Isolation Voltage | 60 Hz, Sinusoidal, 1 Minute, Connection Pins to Heat Sink Plate | 1500 | V_{rms} |

1st Notes:

- T_{CB} is pad temperature of case bottom.
- Marking "*" is calculation value or design factor.

Pin descriptions

| Pin Number | Pin Name | Pin Description |
|------------|------------|---|
| 1 | /FO | Fault Output |
| 2 | V_{TS} | Voltage Output of HVIC Temperature |
| 3 | Cfod | Capacitor for Duration of Fault Output |
| 4 | Csc | Capacitor (Low-pass Filter) for Short-circuit Current Detection Input |
| 5 | V_{DD} | Supply Bias Voltage for IC and MOSFETs Driving |
| 6 | IN_UH | Signal Input for High-side U Phase |
| 7 | IN_VH | Signal Input for High-side V Phase |
| 8 (8a) | COM | Common Supply Ground |
| 9 | IN_WH | Signal Input for High-side W Phase |
| 10 | IN_UL | Signal Input for Low-side U Phase |
| 11 | IN_VL | Signal Input for Low-side V Phase |
| 12 | IN_WL | Signal Input for Low-side W Phase |
| 13 | Nu | Negative DC-Link Input for U Phase |
| 14 | U | Output for U Phase |
| 15 | Nv | Negative DC-Link Input for V Phase |
| 16 | V | Output for V Phase |
| 17 | W | Output for W Phase |
| 18 | Nw | Negative DC-Link Input for W Phase |
| 19 | $V_{S(W)}$ | High-side Bias Voltage Ground for W phase Mosfet driving |
| 20 | P_W | Positive DC-Link Input for W Phase |
| 21 | P_V | Positive DC-Link Input for V Phase |
| 22 | P_U | Positive DC-Link Input for U Phase |
| 23 (23a) | $V_{S(V)}$ | High-side Bias Voltage Ground for V phase Mosfet driving |
| 24 (24a) | $V_{S(U)}$ | High-side Bias Voltage Ground for U phase Mosfet driving |
| 25 | $V_{B(U)}$ | High-side Bias Voltage for U phase Mosfet driving |
| 26 | $V_{B(V)}$ | High-side Bias Voltage for V phase Mosfet driving |
| 27 | $V_{B(W)}$ | High-side Bias Voltage for W phase Mosfet driving |

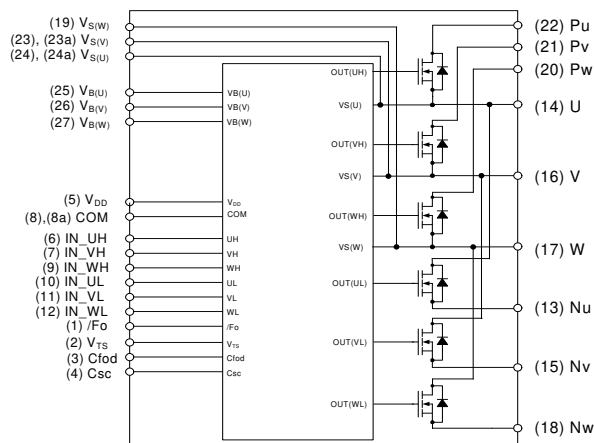


Figure 1. Pin Configuration and Internal Block Diagram

1st Notes:

- Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM® 7 product. External connections should be made as indicated in Figure 2.
- The suffix -a pad is connected with same number pin. ex) 8 and 8a is connected inside.

Electrical Characteristics (T_J = 25°C, V_{DD} = V_{BS} = 15 V unless otherwise specified.)

Inverter Part (each MOSFET unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|---|-----|-----|-----|------|
| BV _{DSS} | Drain - Source Breakdown Voltage | V _{IN} = 0 V, I _D = 1 mA (2nd Note 1) | 250 | - | - | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{IN} = 0 V, V _{DS} = 250 V | - | - | 1 | mA |
| R _{DS(on)} | Static Drain - Source Turn-On Resistance | V _{DD} = V _{BS} = 15 V, V _{IN} = 5 V, I _D = 1.0 A | - | 0.7 | 0.8 | Ω |
| V _{SD} | Drain - Source Diode Forward Voltage | V _{DD} = V _{BS} = 15V, V _{IN} = 0 V, I _D = -1.0 A | - | 0.9 | 1.2 | V |
| t _{ON} | Switching Times | V _{PN} = 150 V, V _{DD} = V _{BS} = 15 V, I _D = 1.0 A V _{IN} = 0 V ↔ 5 V, Inductive Load L = 3 mH Low-Side MOSFET Switching (2nd Note 2) | - | 495 | - | ns |
| t _{D(ON)} | | | - | 415 | - | ns |
| t _{OFF} | | | - | 370 | - | ns |
| t _{D(OFF)} | | | - | 275 | - | ns |
| I _{rr} | | | - | 1.8 | - | A |
| t _{rr} | | | - | 70 | - | ns |
| E _{ON} | | | - | 20 | - | μJ |
| E _{OFF} | | | - | 1.7 | - | μJ |

Control Part (each HVIC unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|----------------------|--|---|---|------|-----|--------|---|
| I _{QDD} | Quiescent V _{DD} Current | V _{DD} =15V, V _{IN} =0V | V _{DD} - COM | - | 1.7 | 3.0 mA | |
| I _{QBS} | Quiescent V _{BS} Current | V _{BS} =15V, V _{IN} =0V | V _{B(X)} -V _{S(X)} , V _{B(V)} -V _{S(V)} , V _{B(W)} -V _{S(W)} | - | 45 | 70 μA | |
| I _{PDD} | Operating V _{DD} Current | V _{DD} =15V, F _{PWM} =20kHz, duty=50%, PWM signal input for Low side | V _{DD} - COM | - | 1.9 | 3.2 mA | |
| I _{PBS} | Operating V _{BS} Current | V _{BS} =15V, F _{PWM} =20kHz, duty=50%, PWM signal input for High side | V _{B(U)} -V _{S(U)} , V _{B(V)} -V _{S(V)} , V _{B(W)} -V _{S(W)} | - | 300 | 400 μA | |
| UV _{DDD} | Low-side Undervoltage Protection (Figure 6) | V _{DD} Undervoltage Protection Detection Level | 7.4 | 8.0 | 9.4 | V | |
| UV _{DDR} | | V _{DD} Undervoltage Protection Reset Level | 8.0 | 8.9 | 9.8 | V | |
| UV _{BSD} | High-side Undervoltage Protection (Figure 7) | V _{BS} Undervoltage Protection Detection Level | 7.4 | 8.0 | 9.4 | V | |
| UV _{BSR} | | V _{BS} Undervoltage Protection Reset Level | 8.0 | 8.9 | 9.8 | V | |
| V _{TS} | HVIC Temperature sensing voltage output | V _{DD} =15V, T _{HVIC} =25°C (2nd Note 3) | 580 | 675 | 770 | mV | |
| V _{IH} | ON Threshold Voltage | Logic High Level | IN - COM | - | - | 2.4 | V |
| V _{IL} | OFF Threshold Voltage | Logic Low Level | | 0.8 | - | - | V |
| V _{SC(ref)} | SC Current Trip Level | V _{DD} =15V | C _{SC} - COM | 0.45 | 0.5 | 0.55 | V |
| t _{FOD} | Fault-out Pulse Width | C _{FOD} =33nF (2nd Note 4) | 1.0 | 1.4 | 1.8 | ms | |

2nd Notes:

- BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM® 7 product. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{PN} should not exceed BV_{DSS} in any case.
- t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 3 for the switching time definition with the switching test circuit of Figure 4.
- V_{TS} is only for sensing-temperature of module and cannot shutdown MOSFETs automatically.
- The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : C_{FOD} = 24 × 10⁻⁶ × t_{FOD} [F]

Recommended Operating Condition

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|--|--|------|------|------|------------|
| V_{PN} | Supply Voltage | Applied Between P and N | - | 150 | 200 | V |
| V_{DD} | Control Supply Voltage | Applied Between V_{DD} and COM | 13.5 | 15.0 | 16.5 | V |
| V_{BS} | High-Side Bias Voltage | Applied Between V_B and V_S | 13.5 | 15.0 | 16.5 | V |
| dV_{DD}/dt , dV_{BS}/dt | Control Supply Variation | | -1.0 | - | 1.0 | V/ μ s |
| t_{dead} | Blanking Time for Preventing Arm-Short | $V_{DD} = V_{BS} = 13.5 \sim 16.5$ V, $T_J \leq 150^\circ\text{C}$ | 500 | - | - | ns |
| f_{PWM} | PWM Switching Frequency | $T_J \leq 150^\circ\text{C}$ | - | 15 | - | kHz |

Thermal Resistance

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------|--|---|------|------|------|---------------------------|
| $R_{\theta JCB}$ | Junction to Case Bottom Thermal Resistance | Single MOSFET Operating Condition (3rd Notes 1) | - | 1.2 | - | $^\circ\text{C}/\text{W}$ |

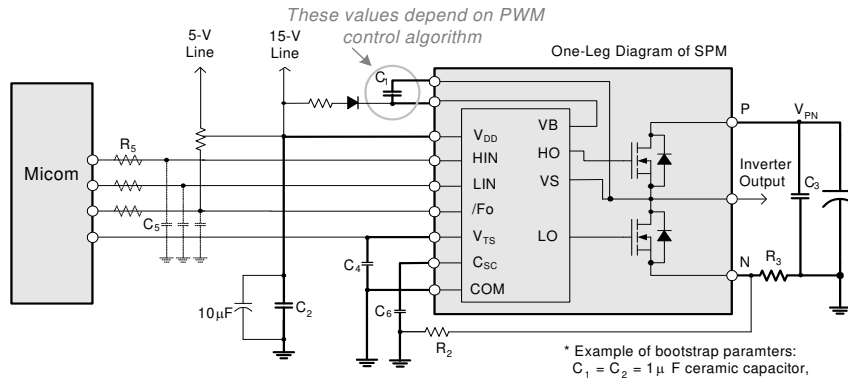


Figure 2. Recommended MCU Interface and Bootstrap Circuit with Parameters

3rd Notes:

- $R_{\theta JCB}$ is simulation value with application board layout. (Please refer user's guide SPM7 series)
- Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- RC coupling (R_5 and C_5) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM® is compatible with standard CMOS or LSTTL outputs.
- Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage.

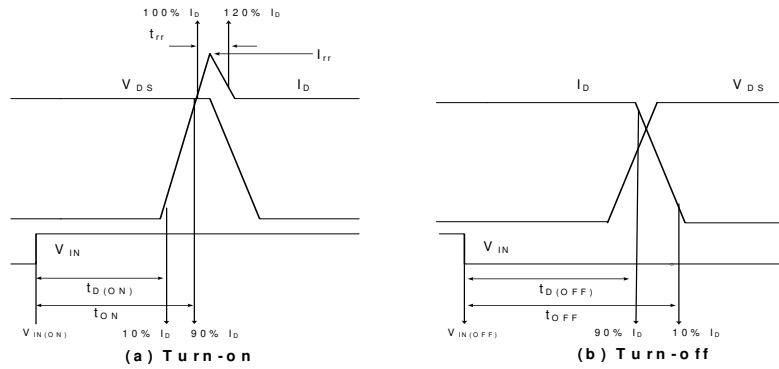


Figure 3. Switching Time Definition

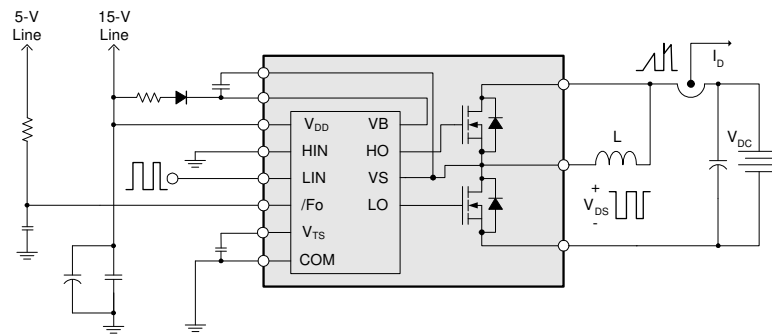


Figure 4. Switching Test Circuit (Low-side)

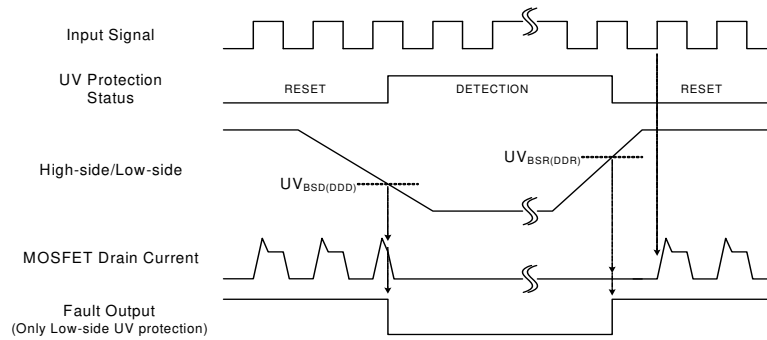


Figure 5. Under Voltage Protection

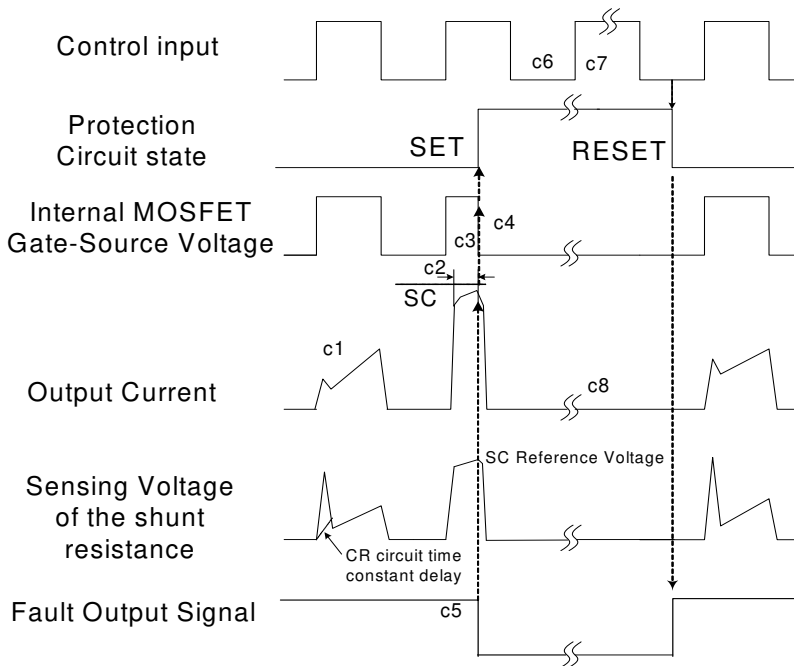


Figure 6. Short-Circuit Current Protection

(with the external shunt resistance and CR connection)

- c1 : Normal operation: MOSFET ON and carrying current.
- c2 : Short circuit current detection (SC trigger).
- c3 : Hard MOSFET gate interrupt.
- c4 : MOSFET turns OFF.
- c5 : Fault output timer operation start : Fault-out width (t_{FOD})
- c6 : Input "L" : MOSFET OFF state.
- c7 : Input "H": MOSFET ON state, but during the active period of fault output the MOSFET doesn't turn ON.
- c8 : MOSFET OFF state

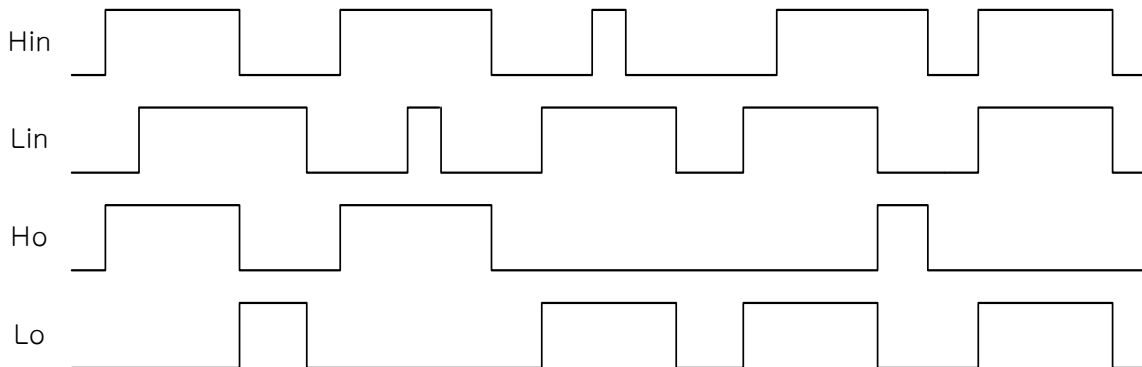


Figure 7. Timing Chart of Interlock Function

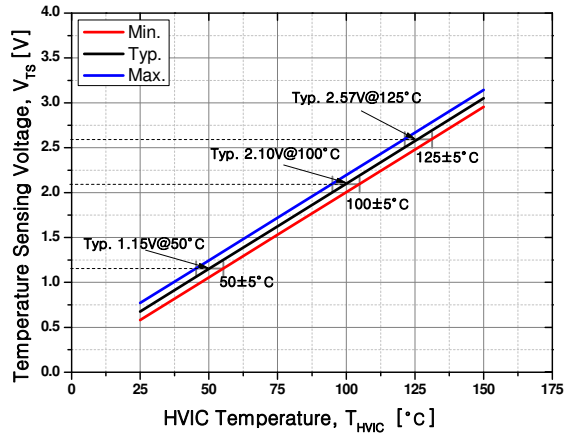


Figure 8. Temperature profile V_{TS} vs. T_{HVIC}

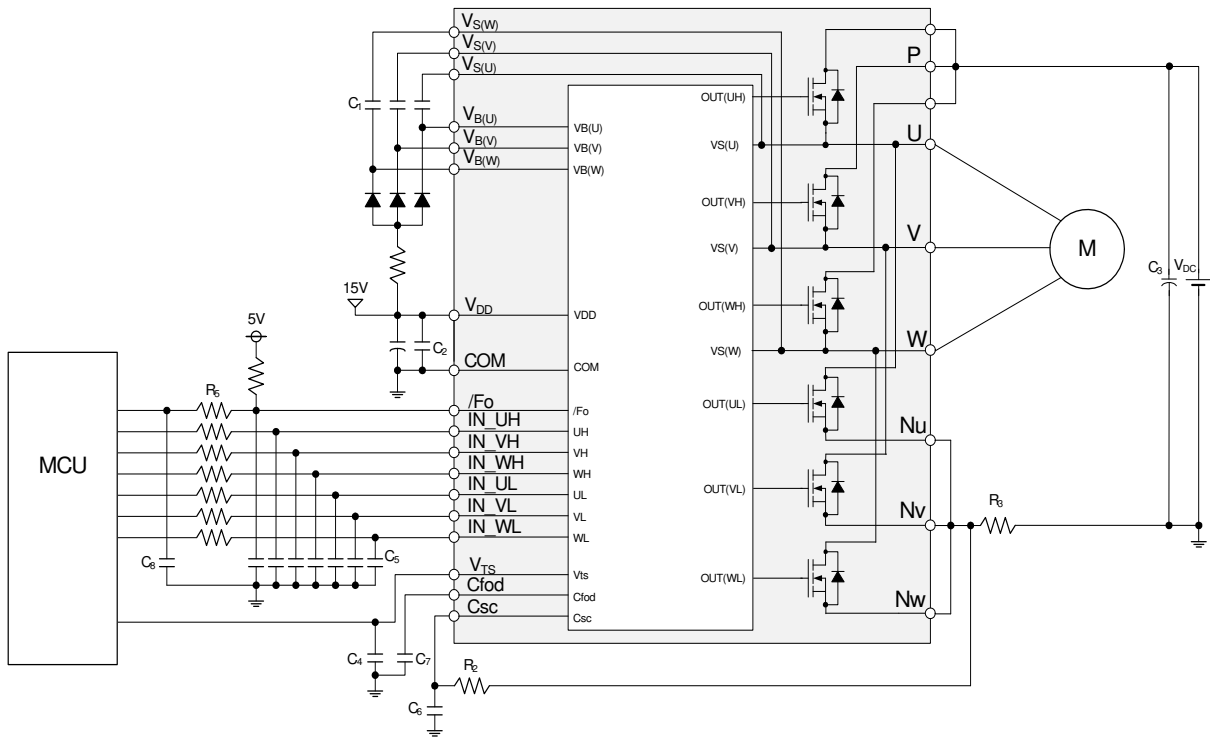
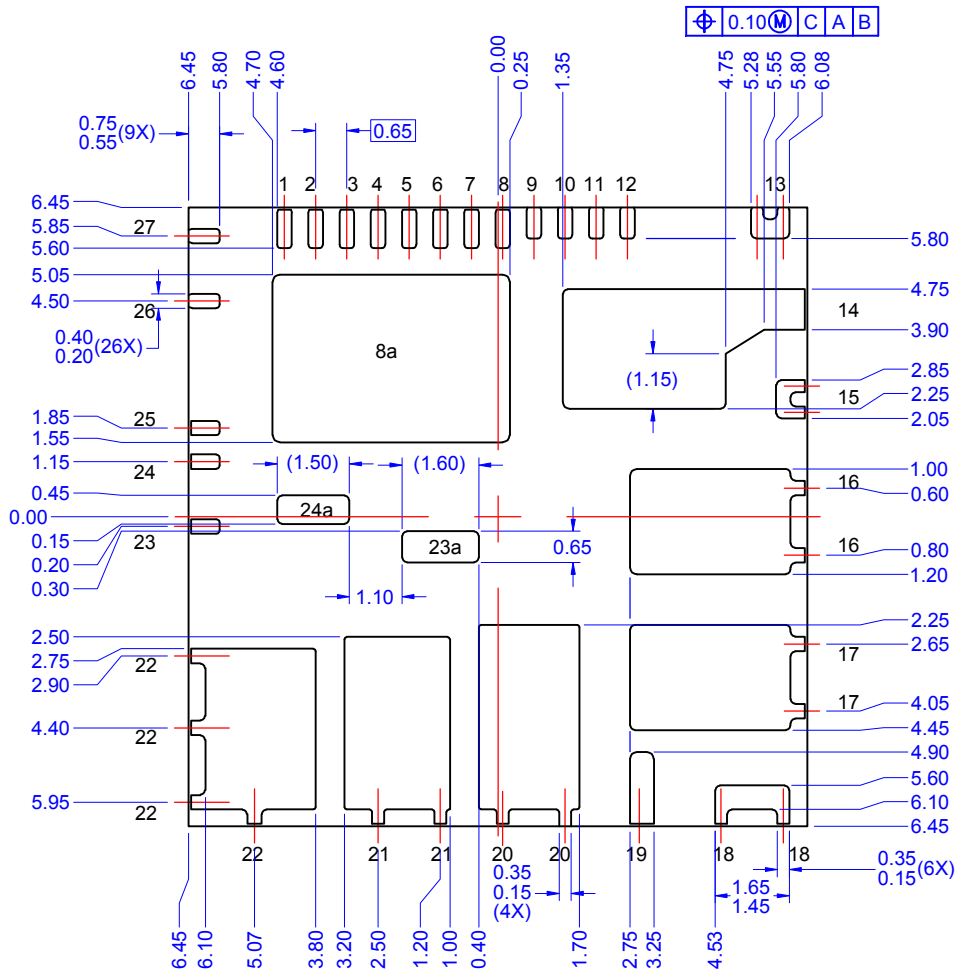


Figure 9. Example of Application Circuit

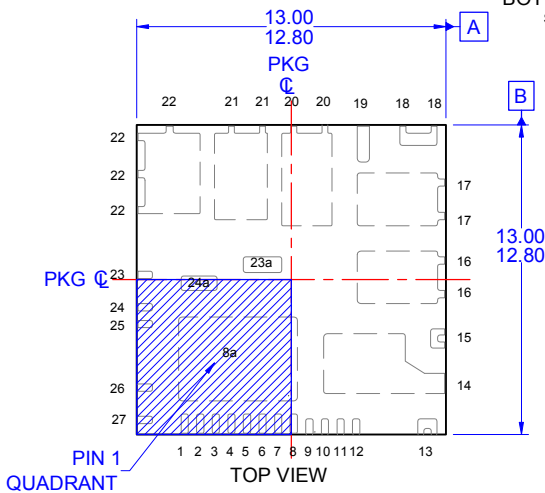
4th Notes:

1. RC-coupling (R_5 and C_5 , R_2 and C_6) and C_1 , C_5 , C_7 , C_8 at each input of Motion SPM® 7 product and MCU are useful to prevent improper input signal caused by surge-noise.
2. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
3. All the filter capacitors should be connected close to Motion SPM 7 product, and they should have good characteristics for rejecting high-frequency ripple current.

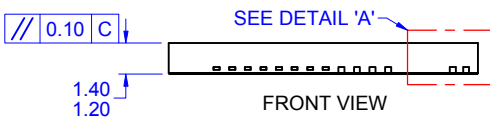


BOTTOM VIEW

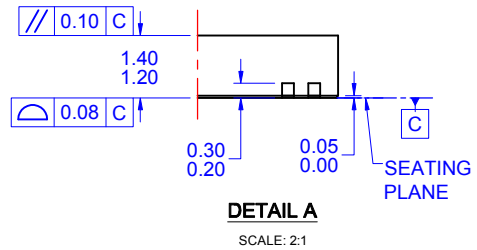
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TOP VIEW

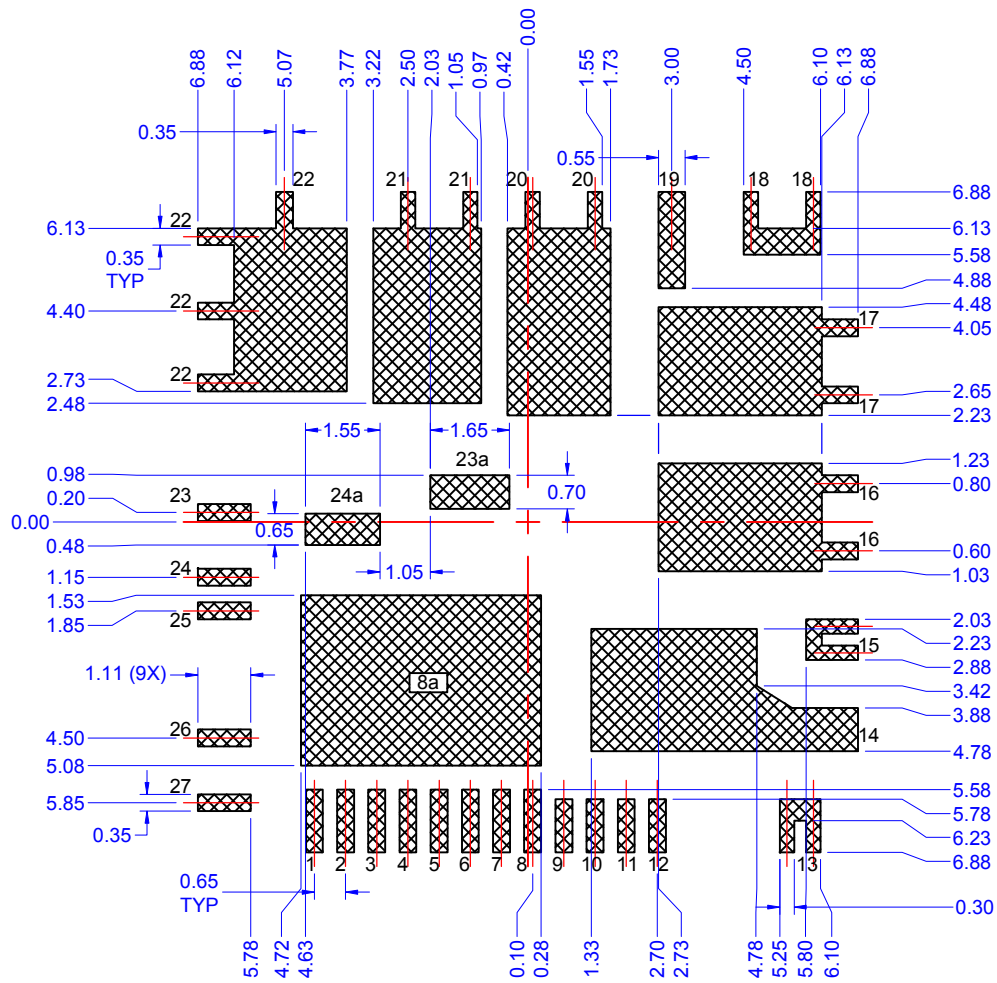


FRONT VIEW



DETAIL A

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LAND PATTERN
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