



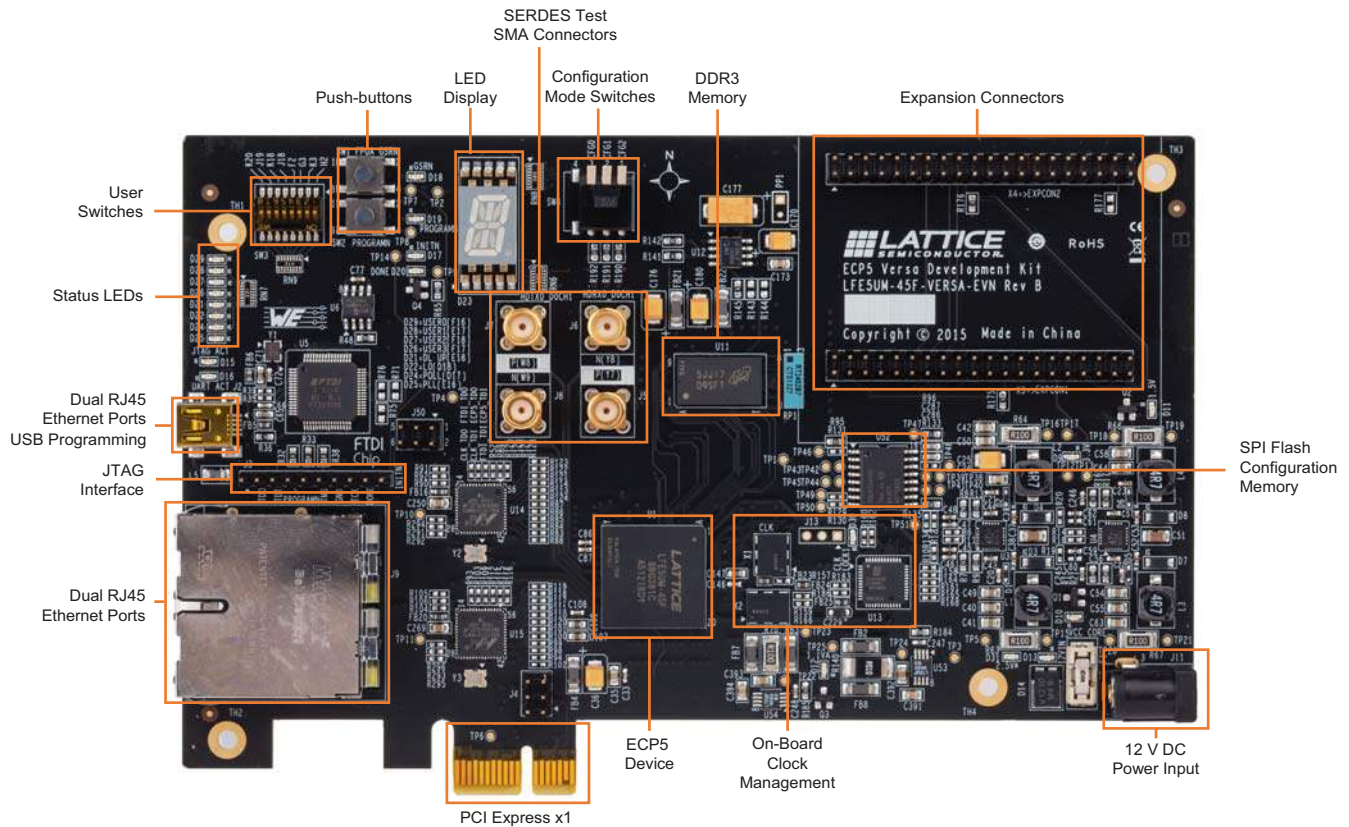
ECP5 Versa Development Board User Guide

FPGA-EB-02021 Version 2.3, September 2018

Introduction

The ECP5™ Versa Development Board allows designers to investigate and experiment with the features of the ECP5 Field-Programmable Gate Array. The features of the ECP5 Versa Development Board can assist engineers with rapid prototyping and testing of their specific designs. The ECP5 Versa Development Board is part of the ECP5 Versa Development Kit. The guide is intended to be referenced in conjunction with demo user guides to demonstrate the ECP5 FPGA.

Figure 1. ECP5 Versa Development Board, Top Side



Features

- Half-length PCI Express form-factor
 - Allows demonstration of PCI Express x1 interconnection
- Electrical testing of one full-duplex SERDES channel via SMA connections
- USB-B connection for UART and device programming
- Two RJ45 interfaces to 10/100/1000 Ethernet to RGMII
- On-board Boot Flash
 - 128M Serial SPI Flash
- DDR3-1866 memory components (64Mb/x16)*
- Expansion mezzanine interconnection for prototyping
- 14-segment alpha-numeric display
- Switches, LEDs and displays for demo purposes
- Diamond® programming support
- On-board reference clock sources

The contents of this user guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics.

**Note: The ECP5 FPGA supports DDR3 memory at data rates up to 800 Mbps.*

Caution: The ECP5 Versa Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the evaluation board.

ECP5 Device

This board features an ECP5 FPGA with a 1.1 V core supply. It can accommodate all pin-compatible ECP5 devices in the 381 ball caBGA package. A complete description of this device can be found in FPGA-DS-02012, [ECP5 Family Data Sheet](#).

Note: The connections referenced in this document refer to the LFE5UM-45F-8BG381C device.

Applying Power to the Board

The ECP5 Versa Development Board is ready to power on. The board can be supplied with power from a PCI Express host system or standalone with an external wall power module.

The 12 V DC input power source is fused with a surface mounted fuse, as noted in Table 1.

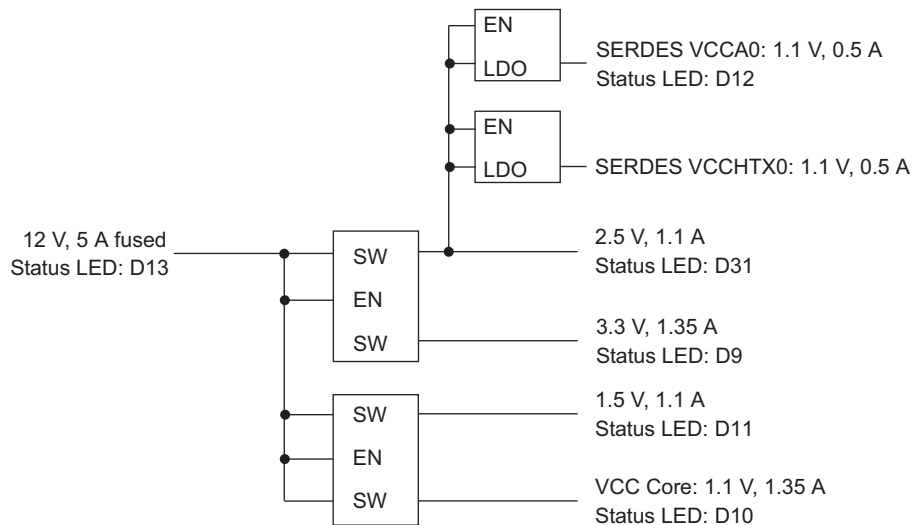
Table 1. Board Power Supply Fuses (See Appendix A, Sheet 2, Figure 11- Voltage Regulators)

| Fuse Designator | Description |
|-----------------|------------------------|
| F1 | 12 V Input Supply Fuse |

The board may be plugged into a host PC. Only plug the board into a PCI Express slot when the system is powered off. Once inserted, the PC can be safely powered on.

Using the evaluation board outside of a PC chassis supply requires the factory-supplied wall supply module. Use of other supplies is not suggested.

Figure 2. Power Distribution Scheme (See Appendix A, Sheet 2, Figure 11- Voltage Regulators)



Programming/FPGA Configuration

The ECP5 Versa Development Board has a built-in download controller for programming the ECP5 FPGA. The built-in module consists of a USB Type-B connector and a USB UART device. To use the built-in download cable, simply connect a standard USB cable (a USB-B to USB-A cable is included with the ECP5 Versa Development Kit) from J2 to your PC (with Diamond programming software installed). The USB hub on the PC will detect the addition of the USB function, making the built-in cable available for use with the Diamond programming software. The USB cable is connected in parallel to J3.

Alternate Programmer Download Interface

J3 is a 10 pin JTAG connector that is provided for use with an external Lattice download cable (available separately). A USB download cable can be attached to the board using J3 to interface with the FPGA (U1).

Note: Resistors R38, R33, R32 and R36 need to be removed for programming with J3.

The same interface can be used to access the ispClock 5406D clock device (U13) by reconfiguring the jumpers on J50 (See Appendix A, Sheet 3, Figure 12 - Programming). U13 is factory-programmed for use with the reference designs and should only be altered for customized designs.

Table 2. JTAG Connector Pinout (J3) (See Appendix A, Sheet 3, Figure 12 - Programming)

| Pin | Function |
|-----|----------|
| 1 | PWR |
| 2 | TDO |
| 3 | TDI |
| 4 | PROGRAMn |
| 5 | N/C |
| 6 | TMS |
| 7 | GND |
| 8 | TCK |
| 9 | DONE |
| 10 | INITn |

Diamond Programmer Requirements

Note: This board includes the built-in download module and only requires the USB cable included with the board. After initial board setup, use the following procedure to program the board. Instructions assume that Diamond Programmer software has been installed on a local PC.

Requirements:

- PC with Diamond Programmer 3.5.1 (or later) programming software, installed with appropriate drivers (USB driver for USB cable).

Note: An option to install these drivers is included as part of the Diamond Programmer setup.

Setting the Configuration Mode

The ECP5 device on the ECP5 Versa Development Board supports a variety of configuration modes, including 1149.1 JTAG and Master SPI. Refer to TN1260, [ECP5 sysCONFIG Usage Guide](#). On the PCB version Rev B, use the CFG Setting Dip Switch SW4 described in Table 3.

Table 3. CFG[2:0] Selection – Rev B

| Configuration Mode | CFG[2:0] | SW4.3 | SW4.2 | SW4.1 |
|----------------------|----------|-------|-------|-------|
| 1149.1 JTAG only | 000 | Down | Down | Down |
| Slave SPI | 001 | Down | Down | Up |
| Master SPI | 010 | Down | Up | Down |
| SCM (Slave_Serial) | 101 | Up | Down | Up |
| SCM (Slave_Parallel) | 111 | Up | Up | Up |

Board Programming

Configuration Status Indicators

(See Appendix A, Sheet 3, Figure 12 - Programming)

Figure 3. ECP5 Status LEDs and Push-button Controls



The LEDs indicate the configuration status of the ECP5 FPGA.

- **D17 (red)** illuminated indicates that programming was aborted or reinitialized, driving the INITN output low.
- **D20 (green)** illuminated indicates the successful completion of configuration by releasing the open collector DONE output pin.
- **D19 (red)** illuminated indicates that PROGRAMN is low.
- **D18 (red)** illuminated indicates that GSRN is low.

PROGRAMN and GSRN

These push-button switches assert/de-assert the logic levels on PROGRAMN (SW2) and GSRN (SW1). Depressing the button drives a logic level “0” to the device.

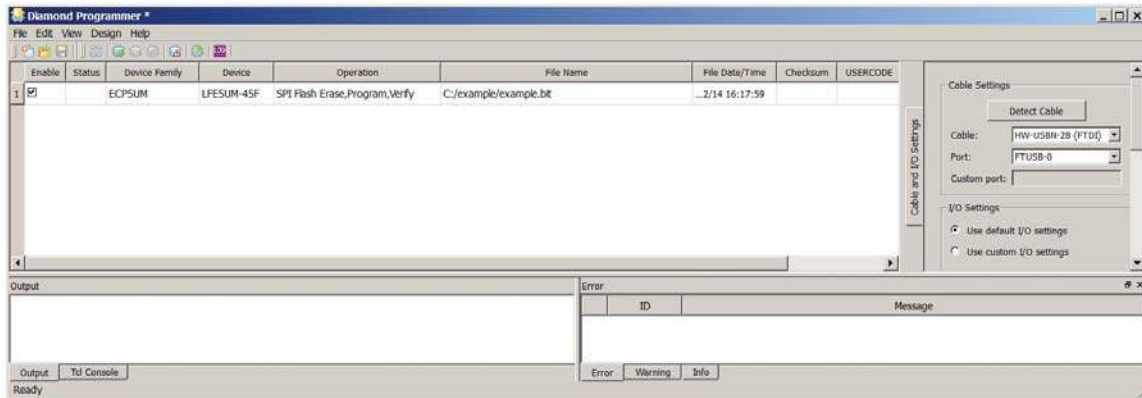
Programming Serial SPI Flash Memory

A serial SPI (16-pin TSSOP, 128M) Flash memory device (U52) is on-board for non-volatile configuration memory storage. A Micron N25Q128A device is populated on-board.

The Serial SPI Flash memory device can be configured easily via the ECP5 JTAG port. This mode enables the FPGA to be programmed at power-up or assertion of PROGRAMN with a bitstream stored in the memory device.

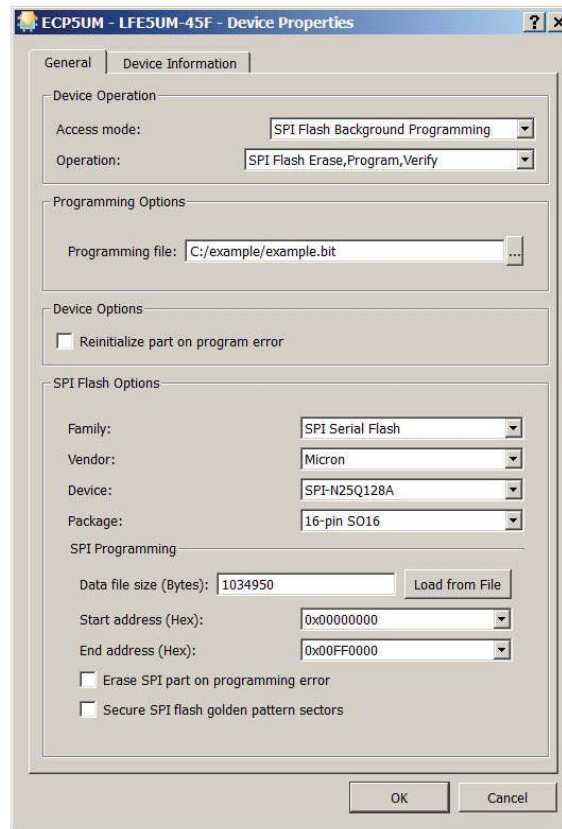
1. Connect the ECP5 Versa Development Board.
2. Scan the board or select the **LFE5UM-45F** device in the ECP5UM device family.
3. From the Edit pull down menu select **Device Properties**. Set the Access mode to **SPI Flash Background Programming** and Operation to **SPI Flash Erase, Program, Verify**.

Figure 4. Diamond Programmer Main Screen



4. Under the SPI Flash Options, select Family to **SPI Serial Flash**, Vendor to **Micron**, Device to **SPI-N25Q128A**, Package to **16-pin SO16**.

Figure 5. Device Properties Dialog Box



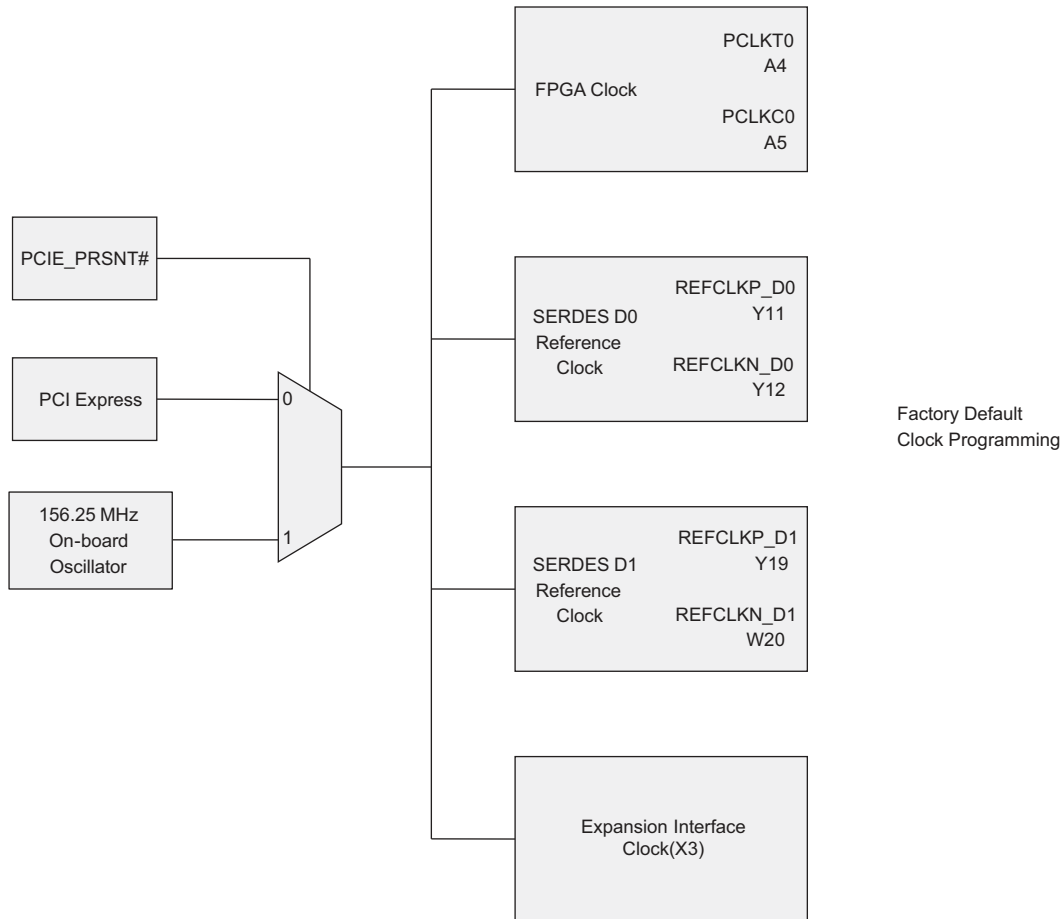
5. Click **OK** in the Device Properties dialog box. You will return to the main configuration screen.
6. Set J50 jumper to ECP5 programming (see Appendix A, sheet 3 "Programming").
7. Ensure the Configuration Mode is set to Master SPI using DIP Switch SW4 (see Table 3).
8. From the main programming window, select **Program** from the top toolbar. This begins the SPI Serial Flash programming. Note that the SPI Flash Background Programming operation is only possible when the ECP5 device is either erased or the active design has the MASTER_SPI_PORT mode enabled. For more details see TN1260, [ECP5 sysCONFIG Usage Guide](#).

On-Board Clock Capabilities

(See Appendix A, Sheet 9, Figure 18 - Reference Clock Generator)

The ECP5 Versa Development Board allows for several clock source options. Some of these options are controlled via the ispClock5406D programmable clock manager device. The ispClock5406D enables the reference clock from the PCI Express interface to provide a reference clock to the SERDES. This is true only when the board is in a PCI Express host socket. When the board is not in a PCI Express host socket, the clock will be supplied by a 156.25 MHz clock on-board oscillator. Both clock inputs can be fanned out to the dedicated SERDES reference inputs, FPGA inputs, and to the expansion connectors. The factory default programming only connects the SERDES reference clock inputs. Factory-defined demonstration designs will control and manage the clock.

Figure 6. Clock Controller Scheme

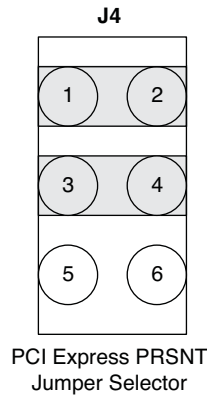


General Purpose Clock Source

An on-board 100 MHz LVDS oscillator is provided for general purpose use. This clock source is connected to differential inputs P3 and P4 and must be used as LVDS inputs to the FPGA. This pin pair also provides optimal interface to the FPGA PLL for customized use.

The PCI Express add-in card specification requires add-in boards to include capabilities to tell the host of its presence. The ECP5 Versa Development Board allows this optional connection via a board jumper. Using the board with a PCI Express host requires the setting shown in Figure 7 below.

Figure 7. PCI Express PRSNT Control Connection



SERDES

The ECP5 Dual Channel Unit (DCU) SERDES FPGA is utilized on the board for several purposes. DCU0, Channel 0 is provisioned to provide a single, full-duplex PCI Express channel. The high-speed signals are connected to the PCI Express edge connection. DCU0, Channel 1 is connected to the SMA connectors for external electrical demonstrations.

Table 4. PCI Express Channel Interconnections

| Signal Name | SERDES Port | FPGA Ball Number |
|-------------|--------------|------------------|
| PETp0 | HDRXP0_D0CH0 | Y5 |
| PETn0 | HDRXN0_D0CH0 | Y6 |
| PERp0 | HDTXP0_D0CH0 | W4 |
| PERn0 | HDTXN0_D0CH0 | W5 |

Table 5. SMA Test Interconnections

| Connector | SERDES Port | FPGA Ball Number |
|-----------|--------------|------------------|
| J5 | HDRXP0_D0CH1 | Y7 |
| J6 | HDRXN0_D0CH1 | Y8 |
| J7 | HDTXP0_D0CH1 | W8 |
| J8 | HDTXN0_D0CH1 | W9 |

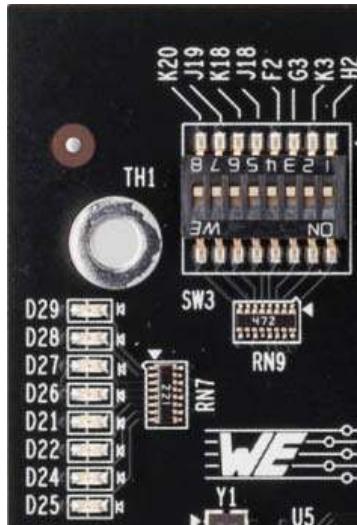
FPGA Test Pins

(See Appendix A, Sheet 8, Figure 17 - LEDs and Switches)

General Purpose DIP Switches

General purpose FPGA pins are available for user applications. FPGA pins are connected to switch SW3, a SPST slide-actuated DIP switch. The switches are connected to logic level 0 when moved to the ON position. Switch position 1 is indicated with an arrow. *Inputs 1-4 are within a 1.5 V bank and inputs 5-8 are within a 2.5 V bank.* The user must program inputs 1-4 to be the LVC MOS15 type and inputs 5-8 to be the LVC MOS25 type in the design. Figure 9 shows the switches. Note the silk marking associated with SW3-7 is incorrect in revision B, SW3-7 is mapped to K19, per Table 6.

Figure 8. ECP5 Versa Development Board LEDs and Switches



The designated pins are connected according to Table 6.

Table 6. FPGA Ball to DIP Switch Position

| FPGA Ball Number | SW3 DIP Switch Position |
|------------------|-------------------------|
| H2 | 1 |
| K3 | 2 |
| G3 | 3 |
| F2 | 4 |
| J18 | 5 |
| K18 | 6 |
| K19 | 7 |
| K20 | 8 |

General Purpose LEDs

(See Appendix A, Sheet 8, Figure 17 - LEDs and Switches)

The LEDs provided on the ECP5 Versa Development Board are connected to general purpose FPGA I/Os. These LEDs provide status for user designs and must be included in the design. The LEDs illuminate when the FPGA output is driven LOW. Table 7 shows the LED and associated FPGA pins. These pins are within an I/O bank connected to 2.5 V and the user should program these to be LVCMOS25 type outputs in the design.

Table 7. LED Definitions

| LED Designator | FPGA Ball Number | LED Color |
|----------------|------------------|-----------|
| D25 | E16 | Yellow |
| D24 | D17 | Yellow |
| D22 | D18 | Green |
| D21 | E18 | Green |
| D26 | F17 | Red |
| D27 | F18 | Red |
| D28 | E17 | Red |
| D29 | F16 | Red |

Alpha-numeric LED Display

(See Appendix A, Sheet 8, Figure 17 - LEDs and Switches)

A 14-segment alpha-numeric display is provided on the board (D23). These LED segments are connected to general-purpose FPGA I/Os. The LEDs must be included in the FPGA design. The LEDs illuminate when the FPGA output is driven LOW. Table 8 shows the LED and associated FPGA pins. These pins are within an I/O bank connected to 2.5 V and the user should program these to be LVCMOS25 outputs in the design.

Figure 9. 14-Segment Display

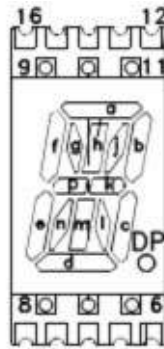


Table 8. Alpha-numeric LED Definitions

| Display | FPGA Ball Number | Display | FPGA Ball Number |
|---------|------------------|---------|------------------|
| A | M20 | J | N18 |
| B | L18 | K | P17 |
| C | M19 | L | N17 |
| D | L16 | M | P16 |
| E | L17 | N | R16 |
| F | M18 | P | R17 |
| G | N16 | DP | U1 |
| H | M17 | | |

DDR3 Memory Device

(See Appendix A, Sheet 7, Figure 16 - DDR3 Memory)

- The ECP5 Versa Development Board is equipped with an SDRAM memory device (1.5 V, 64 Mb/x16, 96-ball FBGA, 933 MHz, DDR3-1866) such as the Micron MT41K64M16TW-107:J device.
- The DDR3 memory includes a 16-bit wide memory controller interface.
- The board includes termination of data, address and command signals. It includes all power and external components needed to demonstrate the memory controller of the ECP5 device.
- A 100 MHz on-board clock oscillator is available to provide a DDR3 reference clock.

Table 9. DDR3 Memory Controller Interconnections

| DDR3 Signal | FPGA Ball Number |
|-------------|------------------|
| DQ0 | L5 |
| DQ1 | F1 |
| DQ2 | K4 |
| DQ3 | G1 |
| DQ4 | L4 |
| DQ5 | H1 |
| DQ6 | G2 |
| DQ7 | J3 |
| DQ8 | D1 |
| DQ9 | C1 |
| DQ10 | E2 |
| DQ11 | C2 |
| DQ12 | F3 |
| DQ13 | A2 |
| DQ14 | E1 |
| DQ15 | B1 |
| DQS0 | K2 |
| DQS0# | J1 |
| DQS1 | H4 |
| DQS1# | G5 |
| CE0 | N2 |
| RAS# | P1 |
| CLKP | P3 |
| CLKN | P4 |
| RST# | N4 |

| DDR3 Signal | FPGA Ball Number |
|-------------|------------------|
| A0 | P2 |
| A1 | C4 |
| A2 | E5 |
| A3 | F5 |
| A4 | B3 |
| A5 | F4 |
| A6 | B5 |
| A7 | E4 |
| A8 | C5 |
| A9 | E3 |
| A10 | D5 |
| A11 | B4 |
| A12 | C3 |
| K_0 | M4 |
| K_0# | N5 |
| CAS# | L1 |
| BA0 | P5 |
| BA1 | N3 |
| BA2 | M3 |
| ODT | L2 |
| CS0# | K1 |
| WE# | M1 |
| VREF | K5 |
| DM0 | J4 |
| DM1 | H5 |

Ethernet Interfaces

(See Appendix A, sheets 5 and 6 "10/100/1000-T PHY#x/RJ45")

Two Marvell 88E1512 Gigabit Ethernet transceiver devices (U14 and U15) are included on the board. These physical layer devices support 1000BASE-T, 100BASE-TX, and 10BASE-T applications via a standard media interface to a dual RJ45 connection. The RJ45 connection includes network magnetics providing the proper signal conditioning, electro-magnetic interference suppression and signal isolation. Each connector includes two LEDs which are controlled by the 88E1512 devices. Detailed descriptions are available in the Marvell device data sheet.

Table 10. PHY Status Indicators

| LED | Status Description |
|---------------------|--------------------|
| RJ45 (Yellow) | Data RX/TX |
| RJ45 (Green/Orange) | Link State |

Each Marvell 88E1512 device communicates via a RGMII interface to the ECP5 device.

Table 11. FPGA GPIO to RGMII Interfaces

| Signal | Phy1 | Phy2 |
|-----------|------|------|
| CLK125 | L19 | J20 |
| CLK125Pll | U16 | C18 |
| Config | T17 | G20 |
| Resetrn | U17 | F20 |
| TXCLK | P19 | C20 |
| TX_D0 | N19 | J17 |
| TX_D1 | N20 | J16 |
| TX_D2 | P18 | D19 |
| TX_D3 | P20 | D20 |
| TXCTRL | R20 | E19 |
| RXCLK | L20 | J19 |
| RX_D0 | T20 | G18 |
| RX_D1 | U20 | G16 |
| RX_D2 | T19 | H18 |
| RX_D3 | R18 | H17 |
| RXCTRL | U19 | F19 |
| MDIO | U18 | H20 |
| MDC | T18 | G19 |

Table 12. Expansion Connections


| X3 Expansion Connector | | |
|------------------------|--------|------------------|
| Pin | Signal | FPGA Ball Number |
| 1 | GND | — |
| 2 | NC | — |
| 3 | 2V5 | — |
| 4 | IO29 | B19 |
| 5 | IO30 | B12 |
| 6 | IO31 | B9 |
| 7 | IO32 | E6 |
| 8 | IO33 | D6 |
| 9 | IO34 | E7 |
| 10 | IO35 | D7 |
| 11 | IO36 | B11 |
| 12 | IO37 | B6 |
| 13 | IO38 | E9 |
| 14 | IO39 | D9 |
| 15 | IO40 | B8 |
| 16 | IO41 | C8 |
| 17 | IO42 | D8 |
| 18 | IO43 | E8 |
| 19 | IO44 | C7 |
| 20 | IO45 | C6 |
| 21 | 5VIN | — |
| 22 | GND | — |
| 23 | 2V5 | — |
| 24 | GND | — |
| 25 | 3V3 | — |
| 26 | GND | — |
| 27 | 3V3 | — |
| 28 | GND | — |
| 29 | OSC | — |
| 30 | GND | — |
| 31 | CLKIN | A10 |
| 32 | GND | — |
| 33 | CLKOUT | E11 |
| 34 | GND | — |
| 35 | 3V3 | — |
| 36 | GND | — |
| 37 | 3V3 | — |
| 38 | GND | — |
| 39 | 3V3 | — |
| 40 | GND | — |

| X4 Expansion Connector | | |
|------------------------|----------|------------------|
| Pin | Signal | FPGA Ball Number |
| 1 | RESOUT# | A8 |
| 2 | GND | — |
| 3 | IO0 | A12 |
| 4 | IO1 | A13 |
| 5 | IO2 | B13 |
| 6 | IO3 | C13 |
| 7 | IO4 | D13 |
| 8 | IO5 | E13 |
| 9 | IO6 | A14 |
| 10 | IO7 | C14 |
| 11 | IO8 | D14 |
| 12 | IO9 | E14 |
| 13 | IO10 | D11 |
| 14 | IO11 | C10 |
| 15 | IO12 | A9 |
| 16 | IO13 | B10 |
| 17 | IO14 | D12 |
| 18 | IO15 | E12 |
| 19 | GND | — |
| 20 | 3V3 | — |
| 21 | IO16 | B15 |
| 22 | GND | — |
| 23 | IO17 | C15 |
| 24 | GND | — |
| 25 | IO18 | D15 |
| 26 | GND | — |
| 27 | IO19 | E15 |
| 28 | IO20 | A16 |
| 29 | IO21 | B16 |
| 30 | GND | — |
| 31 | IO22 | C16 |
| 32 | IO23 | D16 |
| 33 | IO24 | B17 |
| 34 | GND | — |
| 35 | IO25 | C17 |
| 36 | IO26 | A17 |
| 37 | IO27 | B18 |
| 38 | CARDSEL# | A7 |
| 39 | IO28 | A18 |
| 40 | GND | — |

References

- FPGA-DS-02012, [ECP5 and ECP5-5G Family Data Sheet](#)
- FPGA-UG-02006, [PCI Express Demos for the ECP5 and ECP5-5G Versa Development Board](#)
- UG97, [DDR3 Demo for the ECP5 Versa Development Board](#)
- UG93, [SERDES Eye Demo for the ECP5 Versa Development Board](#)
- UG92, [SEU \(Single Event Upset\) Demo for the ECP5 Versa Development Board](#)

Ordering Information

| Description | Ordering Part Number | China RoHS Environment-Friendly Use Period (EFUP) |
|------------------------------|----------------------|---|
| ECP5 Versa Development Board | LFE5UM-45F-VERSA-EVN |  |

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

| Date | Version | Change Summary |
|----------------|---------|--|
| September 2018 | 2.3 | Updated document number from EB98 to FPGA-EB-02021. Updated ECP5 and ECP5-5G Family Data Sheet number to FPGA-DS-02012. Updated PCI Express Demos for the ECP5 and ECP5-5G Versa Development Board number to FPGA-UG-02006. |
| March 2017 | 2.2 | Updated Features section. Added note to the “DDR3-1866 memory components (64Mb/x16)” feature. Updated Programming Serial SPI Flash Memory section. Added step 7 to the procedure. |
| November 2015 | 2.1 | Updated Introduction section. Indicated Dual RJ45 Ethernet ports and corrected USB Programming callout in Figure 1, ECP5 Versa Development Board, Top Side. Updated General Purpose LEDs section. Revised FPGA ball numbers in Table 7, LED Definitions. Updated Appendix A. Schematics section. Revised LEDs signal map in Figure 17, LEDs and Switches. Updated Appendix B. Bill of Materials section. Revised description of item 111. Updated Setting the Configuration Mode section in Appendix C. Changed Figure 20, CFG[2:0] Setting Resistor Field – Revision A. |
| August 2015 | 2.0 | Updated to support Rev B of development board. |
| July 2015 | 1.1 | Added Setting the Configuration Mode section. Updated Technical Support Assistance section. Added ECP5 Versa Development Board Bill of Materials section. |
| March 2015 | 1.0 | Initial release. |

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Appendix A. Schematics

Figure 10. Board Block Design

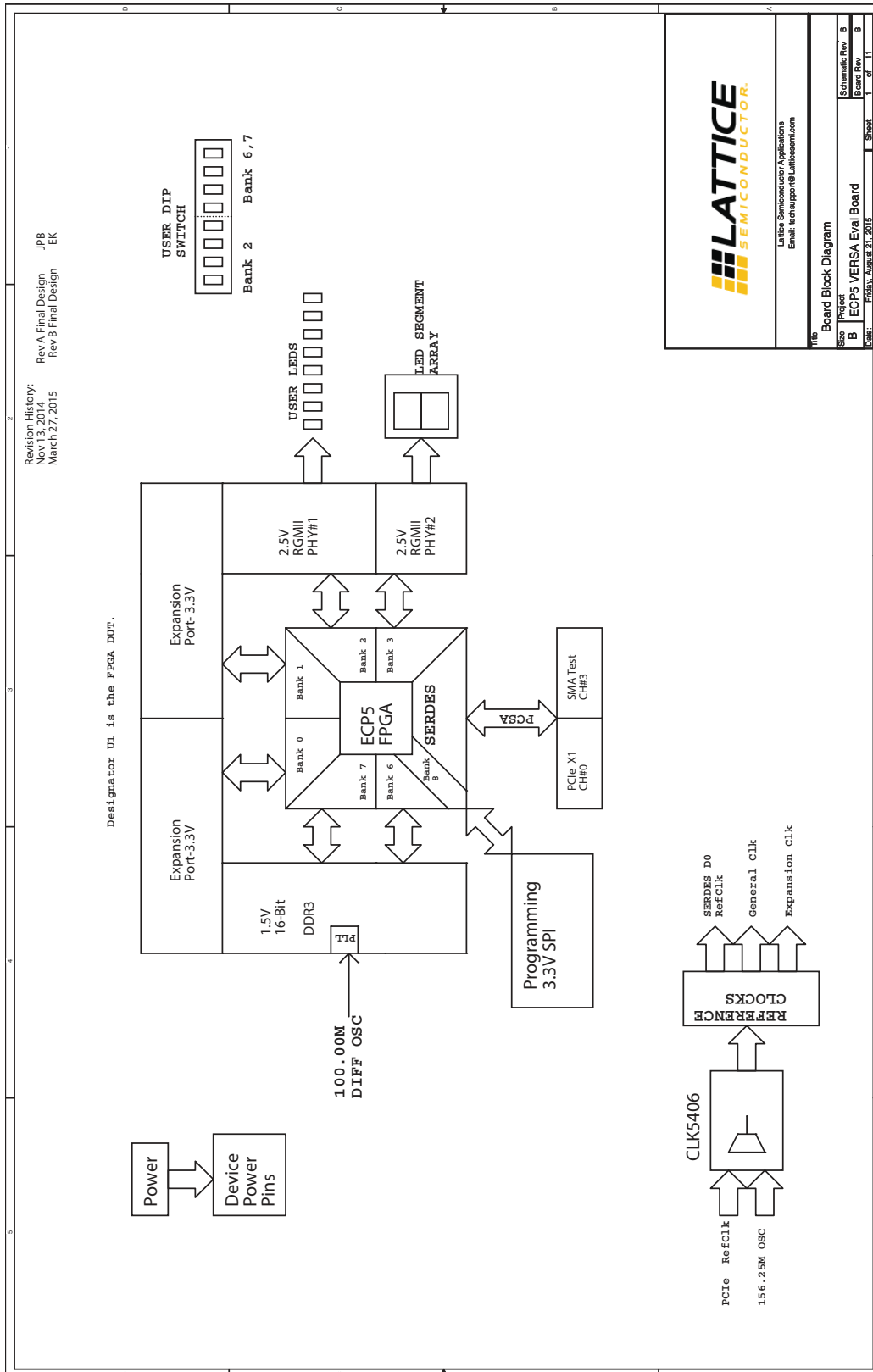


Figure 12. Programming

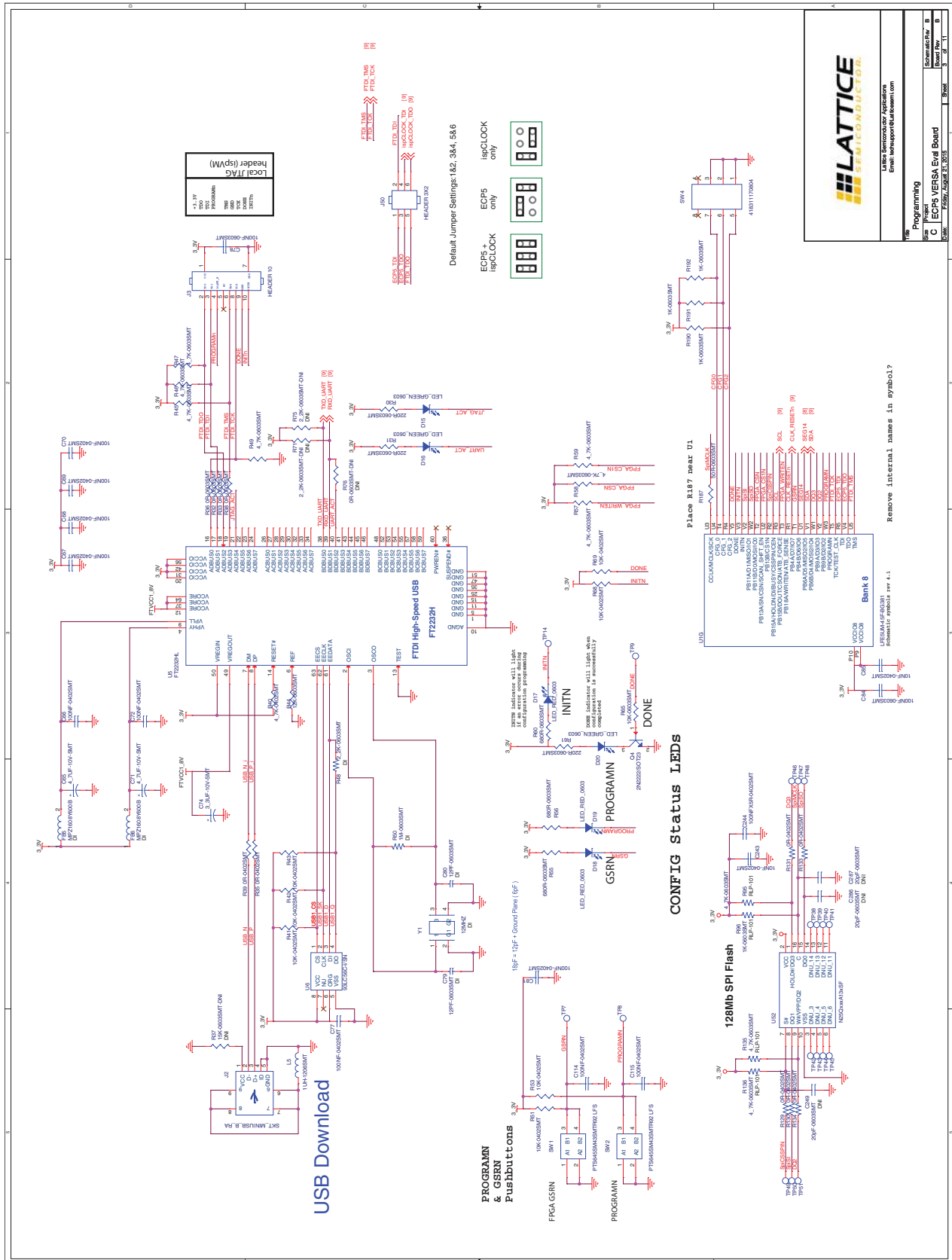
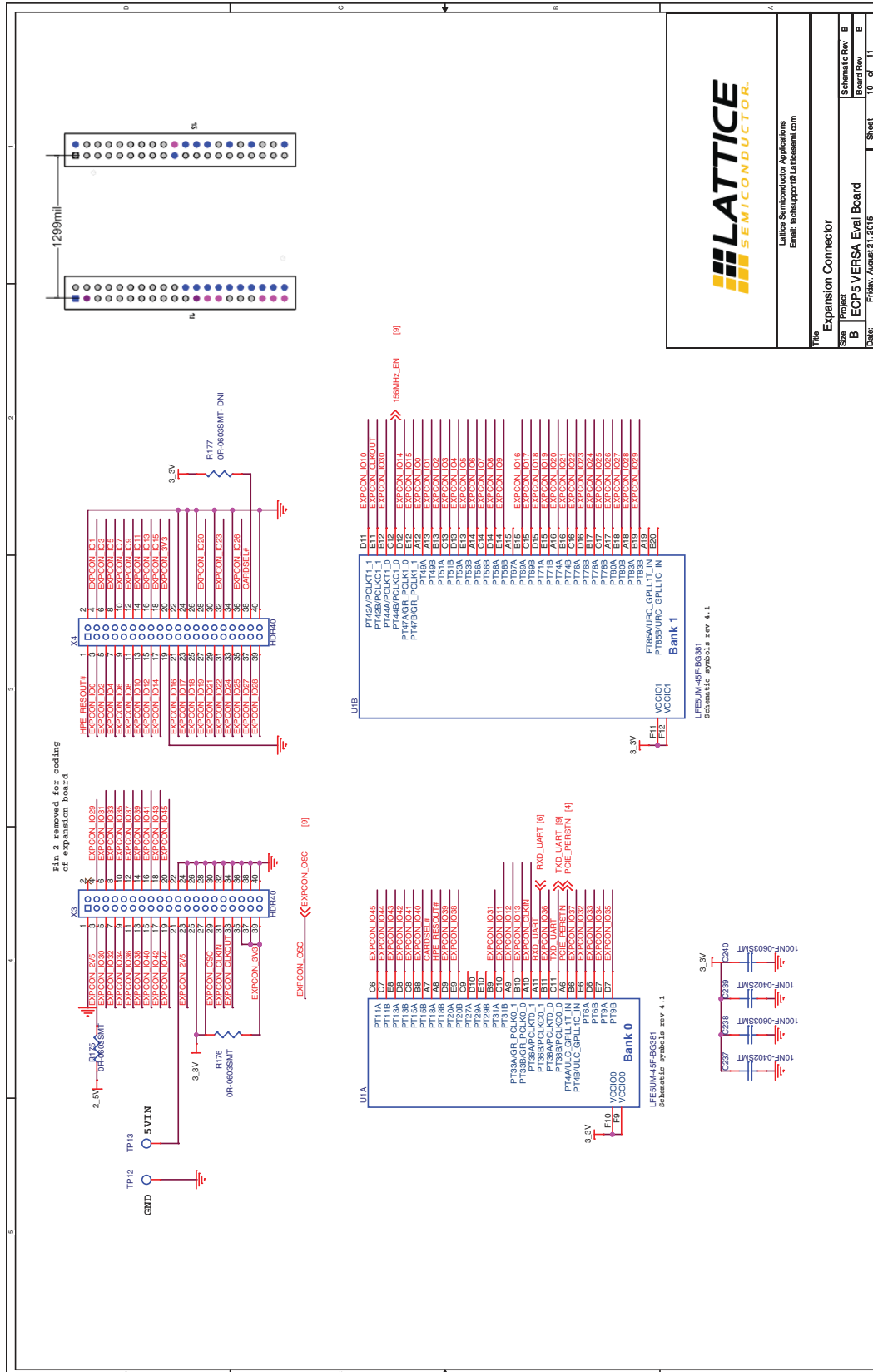


Figure 19. Expansion Connector



Appendix B. Bill of Materials

Table 13. ECP5 Versa Development Board Bill of Materials

| Item | Quantity | Reference | Part | Manufacturer | Part Number | Description |
|------|----------|--|----------------------------------|-----------------|---------------------|---------------------------------|
| 1 | 1 | CN1 | PCI Express x1 Edge Finger Conn. | | | |
| 2 | 31 | C1,C2,C3,C4,C5,C20,C21,C29,C33,C85,C89,C92,C95,C108,C110,C113,C146,C202,C203,C206,C237,C239,C243,C396,C398,C401,C404,C408,C410,C413,C417 | 10NF-0402SMT | Panasonic | ECJ0EB1E103K | CAP .01UF 25V CERAMIC X7R 0402 |
| 3 | 32 | C6,C7,C8,C9,C11,C22,C23,C28,C30,C34,C66,C67,C68,C69,C70,C72,C77,C81,C88,C91,C106,C111,C114,C115,C395,C399,C402,C405,C407,C412,C414,C416 | 100NF-0402SMT | Panasonic | ECJ-0EB1A104K | CAP .1UF 10V CERAMIC X5R 0402 |
| 4 | 8 | C18,C25,C26,C36,C102,C104,C176,C180 | 22UF-16V-TANTBSMT | Kemet | T491B226M016AT | CAPACITOR TANT 22UF 16V 20% SMD |
| 5 | 12 | C19,C24,C27,C35,C101,C103,C171,C173,C178,C181,C391,C394 | 1UF-16V-0805SMT | Panasonic | ECJ-2FB1C105K | CAP 1UF 16V CERAMIC 0805 X5R |
| 6 | 7 | C31,C32,C90,C93,C94,C105,C112 | 1NF-0402SMT | TDK Corporation | C1005C0G1E102J | CAP CER 1000PF 25V C0G 5% 0402 |
| 7 | 2 | C37,C51 | 10uF,25V-1206SMT | TDK Corporation | C3216Y5V1E106Z | CAP CER 10UF 25V Y5V 1206 |
| 8 | 6 | C38,C39,C52,C53,C255,C273 | 220NF-0402SMT | TDK Corporation | C1005X7R1C224K050BC | CAP CER 0.22UF 16V X7R 10% 0402 |
| 9 | 10 | C40,C41,C42,C49,C50,C54,C55,C58,C63,C64 | 22uF,6.3V-0805SMT | TDK Corporation | C2012X5R0J226M | CAP CER 22UF 6.3V X5R 20% 0805 |
| 10 | 12 | C43,C44,C56,C57,C397,C400,C403,C406,C409,C411,C415,C418 | 1000pF-0402SMT | Panasonic | ECJ-0EB1E102K | CAP 1000PF 25V CERAMIC X7R 0402 |
| 11 | 4 | C45,C48,C59,C62 | 330pF-0402SMT | TDK Corporation | C1005C0G1H331J | CAP CER 330PF 50V C0G 5% 0402 |
| 12 | 2 | C46,C47, | 10pF-0402SMT | TDK Corporation | C1005C0G1H100D | CAP CER 10PF 50V C0G 0402 |
| 13 | 2 | C60,C61 | 10pF-0402SMT | DNI | | |
| 14 | 2 | C65,C71 | 4_7UF-10V-SMT | TDK Corporation | C1608X5R1A475K | CAP CER 4.7UF 10V X5R 0603 |
| 15 | 1 | C74 | 3_3UF-10V-SMT | TDK Corporation | C1608X5R1A335K | CAP CER 3.3UF 10V X5R 0603 |
| 16 | 33 | C78,C84,C107,C109,C145,C147,C172,C174,C175,C183,C185,C186,C188,C189,C191,C193,C195,C197,C199,C201,C205,C218,C220,C222,C224,C225,C227,C231,C232,C233,C238,C240,C242 | 100NF-0603SMT | Panasonic | ECJ-1VF1C104Z | CAP .1UF 16V CERAMIC Y5V 0603 |
| 17 | 2 | C79,C80 | 12PF-0603SMT | TDK Corporation | C1608C0G1H120J | CAP CER 12PF 50V C0G 5% 0603 |
| 18 | 25 | C86,C87,C244,C247,C248,C256,C258,C260,C261,C262,C263,C264,C265,C266,C267,C274,C275,C278,C279,C280,C281,C282,C283,C284,C285 | 100NFx5R-0402SMT | Kemet | C0402C104K8PACTU | CAP .10UF 10V CERAMIC X5R 0402 |
| 19 | 1 | C170 | 47UF-16V-TANTBSMT | Kemet | B45196H2476K209 | CAP TANTALUM 47UF 10V 10% SMD |
| 20 | 1 | C177 | 100UF-D3POSCAP | Sanyo | 6TPE100MI | 100UF,6.3V ,D2E. POSCAP |
| 21 | 1 | C179 | 10UF-16V-TANTBSMT | AVX | TAJB106K016R | CAP TANTALUM 10UF 16V 10% SMD |

| Item | Quantity | Reference | Part | Manufacturer | Part Number | Description |
|------|----------|--|----------------------------|-----------------|---------------------|--|
| 22 | 19 | C182,C184,C187,C190, C192,C194,C196,C198, C200,C204,C217,C219, C221,C223,C226,C228, C234,C236,C241 | 10NF-0603SMT | Kemet | C0603C103K5RACTU | CAP .01UF 50V CERAMIC X7R 0603 |
| 23 | 1 | C229 | 6.8UF-TAN-0805SMT | Kemet | T494R685K006AS | CAP TANT 6.8UF 6.3V 10% SMD |
| 24 | 1 | C235 | 560PF-0603SMT | Kemet | C0603C561K5RACTU | CAP 560PF 50V CERAMIC X7R 0603 |
| 25 | 2 | C245,C246 | 100pF-0402SMT | Panasonic | ECJ-0EB1E101K | CAP 100PF 25V CERAMIC X7R 0402 |
| 26 | 3 | C249,C286,C287 | 20pF-0603SMT | TDK Corporation | C1608C0G1H200J | CAP CER 20PF 50V C0G 5% 0603 |
| 27 | 6 | C250,C251,C268,C269, C392,C393 | 10uF-6.3V-0805SMT | AVX | 08056C106KAT2A | CAP CER 10UF 6.3V X7R 10% 0805 |
| 28 | 4 | C253,C254,C271,C272 | 27pF-0603SMT | Kemet | C0603C270J5GACTU | CAP CERAMIC 27PF 50V NPO 0603 |
| 29 | 2 | C257,C276 | 4.7uF-16-0805SMT | TDK Corporation | C2012Y5V1C475Z/0.85 | CAP CER 4.7UF 16V Y5V 0805 |
| 30 | 4 | D1,D2,D5,D6 | 1N4448W | Fairchild | 1N4448WT | DIODE 75V 200MA SOD523F |
| 31 | 4 | D3,D4,D7,D8 | DFLS220L | Diodes Inc | DFLS220L | DIODE SCHOTTKY 2A 20V PWRDI 123 |
| 32 | 11 | D9,D10,D11,D12,D15,D16, D20,D21,D22,D30,D31 | LED_GREEN_0603 | Würth | 150060VS75000 | LED 1.6X0.8MM 568NM GRN CLR SMD |
| 33 | 1 | D13 | LED_BLUE_0603 | Würth | 150060BS75000 | LED 1.6X0.8 470NM BL WTR CLR SMD |
| 34 | 1 | D14 | SCHOTTKY/VISHAY- V12P10 | Vishay | V12P10-M3/86A | DIODE SCHOTTKY 12A 100V SMPC TO-277A |
| 35 | 7 | D17,D18,D19,D26,D27, D28,D29 | LED_RED_0603 | Würth | 150060RS75000 | LED 1.6X0.8MM 625NM RED CLR SMD |
| 36 | 1 | D23 | 14-SEGMENT | Kingbright | ACPSA04-41SRWA | LED Display |
| 37 | 2 | D24,D25 | LED_YELLOW_0603 | Würth | 150060YS75000 | LED 1.6X0.8MM 588NM YLW CLR SMD |
| 38 | 7 | FB2,FB3,FB4,FB7,FB8, FB21,FB22 | BLM41PG600SN1 | Würth | 742792410 | FERRITE CHIP 60 OHM 6000MA 1806 |
| 39 | 5 | FB5,FB6,FB23,FB24,FB25 | MPZ1608Y600B | Würth | 742792602 | FERRITE CHIP 60 OHM 2.3A 0603 |
| 40 | 4 | FB16,FB17,FB19,FB20 | Z-600 ohm / 7427926 | Würth | 74279265 | FERRITE BEAD 600 OHM .2A 0603 |
| 41 | 1 | F1 | F1251CT-ND | Littlefuse | 0154010.DR | FUSEBLOCK WITH 10A FUSE SMD |
| 42 | 1 | J2 | SKT_MINIUSB_B_RA | NELTRON | 5075BMR-05-SM-CR | CONN MINI USB RCPT RA TYPE B SMD |
| 43 | 1 | J3 | HEADER 10 | Würth | 61301011121 | 10x1-0.25 Header |
| 44 | 2 | J4,J50 | HEADER 3X2 | Würth | 61300621121 | 3x2-0.25 Header |
| 45 | 4 | J5,J6,J7,J8 | SMA | Molex | 73391-0060 | CONN JACK SMA STR 50 OHM PCB |
| 46 | 1 | J9 | 0826-1X2T-23-F | Bellfuse | 0826-1X2T-23-F | CONN MAGJACK 2PORT GIGABIT GO/Y |
| 47 | 1 | J11 | PJ-002A | Würth | 694106301002 | |
| 48 | 1 | J13 | HEADER 3(DNP) | DNI | TSW-103-07-T-S | 3x1-0.25 Header |
| 49 | 4 | L1,L2,L3,L4 | 4.7uH-SPD62R-472M | API Delavan | SPD62R-472M | 6.60mm x 6.20mm x 3.00mm, 4.7uH Power inductor |
| 50 | 1 | L5 | 1UH-1206SMT | Murata | LQM31PN1R0M00L | INDUCTOR 1.0UH 1.2A 1206 |
| 51 | 1 | PP1 | PROBEPOINT | DNI | | |
| 52 | 4 | Q1,Q2,Q3,Q4 | 2N2222/SOT23 | Diodes Inc | MMBT2222A-7 | TRANS NPN 40V 350MW SMD SOT-23 |
| 53 | 2 | RN6,RN8 | EXB2HV680JV | Panasonic | EXB2HV680JV | RES ARRAY 68 OHM 5% 8 RES SMD |

| Item | Quantity | Reference | Part | Manufacturer | Part Number | Description |
|------|----------|--|-----------------|--|---------------|----------------------------------|
| 54 | 1 | RN7 | EXB2HV221JV | Panasonic | EXB2HV221JV | RES ARRAY 220 OHM 5% 8 RES SMD |
| 55 | 1 | RN9 | EXB2HV472JV | Panasonic | EXB2HV472JV | RES ARRAY 4.7K OHM 5% 8 RES SMD |
| 56 | 1 | RP1 | CTS-RT1402B7 | CTS Corporation Resistor/Electrocomponents | RT2402B7 | RES NET DDR SDRAM 50 OHM 3X9 BGA |
| 57 | 4 | R6,R10,R12,R14 | 51K-0402SMT | Panasonic | ERJ-2RKF5102X | RES 51.0K OHM 1/10W 1% 0402 SMD |
| 58 | 1 | R7 | 21_5K-0603SMT | Panasonic | ERJ-3EKF2152V | RES 21.5K OHM 1/10W 1% 0603 SMD |
| 59 | 1 | R8 | 35_7K-0603SMT | Panasonic | ERJ-3EKF3572V | RES 35.7K OHM 1/10W 1% 0603 SMD |
| 60 | 6 | R9,R21,R27,R28,R29,R65 | 10K-0603SMT | Panasonic | ERJ-3EKF1002V | RES 10.0K OHM 1/10W 1% 0603 SMD |
| 61 | 1 | R11 | 34K-0402SMT | Panasonic | ERJ-2RKF3402X | RES 34.0K OHM 1/10W 1% 0402 SMD |
| 62 | 1 | R13 | 11_5K-0603SMT | Panasonic | ERJ-3EKF1152V | RES 11.5K OHM 1/10W 1% 0603 SMD |
| 63 | 1 | R15 | 3_83K-0603SMT | Panasonic | ERJ-3EKF3831V | RES 3.83K OHM 1/10W 1% 0603 SMD |
| 64 | 1 | R16 | 15K-0603SMT | Panasonic | ERJ-3EKF1502V | RES 15.0K OHM 1/10W 1% 0603 SMD |
| 65 | 1 | R17 | 16_9K-0603SMT | Panasonic | ERJ-3EKF1692V | RES 16.9K OHM 1/10W 1% 0603 SMD |
| 66 | 1 | R18 | 63_4K-0402SMT | Panasonic | ERJ-2RKF6342X | RES 63.4K OHM 1/10W 1% 0402 SMD |
| 67 | 1 | R19 | 30_1K-0402SMT | Panasonic | ERJ-2RKF3012X | RES 30.1K OHM 1/10W 1% 0402 SMD |
| 68 | 1 | R20 | 20K-0402SMT | Panasonic | ERJ-2RKF2002X | RES 20.0K OHM 1/10W 1% 0402 SMD |
| 69 | 4 | R22,R23,R24,R25 | 1_8K-1206SMT | Panasonic | ERJ-8ENF1801V | RES 1.80K OHM 1/4W 1% 1206 SMD |
| 70 | 5 | R26,R30,R31,R61,R179 | 220R-0603SMT | Panasonic | ERJ-3EKF2200V | RES 220 OHM 1/10W 1% 0603 SMD |
| 71 | 11 | R32,R33,R36,R38,R141, R145,R146,R169,R170, R175,R176 | 0R-0603SMT | Panasonic | ERJ-3GEY0R00V | RES 0.0 OHM 1/10W 0603 SMD |
| 72 | 42 | R35,R39,R52,R83,R84, R86,R87,R88,R89,R93, R94,R98,R100,R101,R102, R103,R109,R110,R112, R113,R115,R116,R117, R118,R119,R120,R121, R122,R123,R124,R125, R126,R127,R128,R129, R130,R131,R133,R134, R160,R298,R300 | 0R-0402SMT | Panasonic | ERJ-2GE0R00X | RES 0.0 OHM 1/10W 0402 SMD |
| 73 | 1 | R37 | 15K-0603SMT-DNI | DNI | | |
| 74 | 10 | R40,R90,R92,R104,R106, R162,R180,R181,R274, R275 | 4_7K-0402SMT | Panasonic | ERJ-2RKF4701X | RES 4.70K OHM 1/10W 1% 0402 SMD |
| 75 | 8 | R41,R42,R43,R51,R53, R68,R69,R157 | 10K-0402SMT | Panasonic | ERJ-2RKF1002X | RES 10.0K OHM 1/10W 1% 0402 SMD |
| 76 | 1 | R44 | 12K-0603SMT | Panasonic | ERJ-3EKF1202V | RES 12.0K OHM 1/10W 1% 0603 SMD |
| 77 | 12 | R45,R46,R47,R49,R57, R58,R59,R72,R95,R135, R136,R142 | 4_7K-0603SMT | Panasonic | ERJ-3EKF4701V | RES 4.70K OHM 1/10W 1% 0603 SMD |
| 78 | 1 | R48 | 2_2K-0603SMT | Panasonic | ERJ-3EKF2201V | RES 2.20K OHM 1/10W 1% 0603 SMD |
| 79 | 1 | R50 | 1M-0603SMT | Panasonic | ERJ-3EKF1004V | RES 1.00M OHM 1/10W 1% 0603 SMD |
| 80 | 3 | R55,R56,R60 | 680R-0603SMT | Panasonic | ERJ-3EKF6800V | RES 680 OHM 1/10W 1% 0603 SMD |

| Item | Quantity | Reference | Part | Manufacturer | Part Number | Description |
|------|----------|---|----------------------|------------------|----------------------|--|
| 81 | 5 | R63,R64,R66,R67,R70 | 0.1 | Vishay Dale | WSL2010R1000FEA | RES .1 OHM 1/2W 1% 2010 SMD |
| 82 | 2 | R71,R75 | 2_2K-0603SMT-DNI | DNI | | |
| 83 | 5 | R73,R74,R107,R108,R156 | 100R-0402SMT | Panasonic | ERJ-2RKF1000X | RES 100 OHM 1/10W 1% 0402 SMD |
| 84 | 1 | R76 | 0R-0603SMT-DNI | DNI | | |
| 85 | 4 | R85,R99,R111,R114 | 20 | Vishay | CRCW040220R0FKED | RES 20.0 OHM 1/16W 1% 0402 SMD |
| 86 | 2 | R91,R105 | 4_7K-0402SMT-DNI | DNI | | |
| 87 | 4 | R96,R190,R191,R192 | 1K-0603SMT | Panasonic | ERJ-3EKF1001V | RES 1.00K OHM 1/10W 1% 0603 SMD |
| 88 | 1 | R140 | 0.01 | Vishay Dale | WSL2512R0100FEA18 | RES .01 OHM 2W 1% 2512 SMD |
| 89 | 5 | R143,R144,R148,R149,R178 | OPEN-0603SMT | DNI | | |
| 90 | 1 | R147 | 240R-0603SMT | Panasonic | ERJ-3EKF2400V | RES 240 OHM 1/10W 1% 0603 SMD |
| 91 | 10 | R150,R151,R152,R153,R154,R155,R291,R292,R293,R295 | 50R-0402SMT | Vishay | FC0402E50R0FST1 | RES 50 OHM 50MW +/- 1% 0402 SMD |
| 92 | 7 | R158,R161,R164,R165,R168,R183,R186 | 10R-0402SMT | Panasonic | ERJ-2RKF10R0X | RES 10.0 OHM 1/10W 1% 0402 SMD |
| 93 | 2 | R159,R166 | 220R-0402SMT | Panasonic | ERJ-2RKF2200X | RES 200 OHM 1/10W 1% 0402 SMD |
| 94 | 1 | R163 | 680R-0402SMT | Panasonic | ERJ-2RKF6800X | RES 680 OHM 1/10W 1% 0402 SMD |
| 95 | 1 | R167 | 470R-0402SMT | Panasonic | ERJ-2RKF4700X | RES 470 OHM 1/10W 1% 0402 SMD |
| 96 | 1 | R177 | 0R-0603SMT- DNI | DNI | | |
| 97 | 1 | R184 | 121K-0603SMT | Panasonic | ERJ-3EKF1213V | RES 121K OHM 1/10W 1% 0603 SMD |
| 98 | 1 | R185 | 110K-0603SMT | Panasonic | ERJ-3EKF1103V | RES 110K OHM 1/10W 1% 0603 SMD |
| 99 | 1 | R187 | 50R-0603SMT | Panasonic | ERJ-3EKF49R9V | RES 49.9 OHM 1/10W 1% 0603 SMD |
| 100 | 2 | R294,R296 | 4.99k | Panasonic | ERJ-2RKF4991X | RES 4.99K OHM 1/10W 1% 0402 SMD |
| 101 | 2 | R299,R301 | 0R-0402SMT-DNI | DNI | | |
| 102 | 2 | SW1,SW2 | PTS645SM43SMTR92 LFS | Würth | 430483031816 | SPST SMD |
| 103 | 1 | SW3 | TDA DIP-8 | Würth | 416131160808 | 8-DIP |
| 104 | 1 | SW4 | 418311170804 | Würth | 418311170804 | 4 poles raised SMT |
| 105 | 4 | TH1,TH2,TH3,TH4 | ThruHole | DNI | | |
| 106 | 39 | TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP38,TP39,TP40,TP41,TP42,TP43,TP44,TP45,TP46,TP47,TP48,TP49,TP50,TP51 | TestPoint | DNI | | |
| 107 | 1 | U1 | LFE5UM-45F-BG381 | LATTICE SUPPLIED | LFE5UM-45F-8BG381IES | |
| 108 | 2 | U3,U4 | LT3508EUF | LATTICE SUPPLIED | LT3508EUF#PBF | Dual Monolithic 1.4A Step-Down Switching Regulator |
| 109 | 1 | U5 | FT2232HL | FTDI | FTD2232HL | USB-UART/JTAG |
| 110 | 1 | U6 | 93LC56C-I/SN | MicroChip | 93LC56C-I/SN | IC EEPROM 2KBIT 3MHZ 8SOIC |
| 111 | 1 | U11 | ddr3-96bga | Micron | MT41K64M16TW-107.J | 64Mb/x16, 1.5V, 96-ball FBGA, 667 MHz, DDR3-1866 |

| Item | Quantity | Reference | Part | Manufacturer | Part Number | Description |
|------|----------|-----------|------------------|------------------|---------------------------|--|
| 112 | 1 | U12 | LP2998-SO8 | National | LP2998MAX/NOPB | Termination regulator |
| 113 | 1 | U13 | ispCLOCK5406D | LATTICE SUPPLIED | ISPPAC-CLK5406D-01SN48I | |
| 114 | 2 | U14,U15 | 88E1512_56QFN | Marvell | 88E1512-A0-NNP2C000 | SINGLE-PORT EEE GIGABIT ETHER |
| 115 | 2 | U44,U45 | R0_1-3 | Panasonic | ERJ-3GEY0R00V | RES 0.0 OHM 1/10W 0603 SMD |
| 116 | 1 | U52 | N25QxxxA13xSF | Micron | N25Q128A13ESF40G | Serial Flash |
| 117 | 2 | U53,U54 | LT3085 | LATTICE SUPPLIED | LT3085EMS8E#PBF | Adjustable 500mA Single Resistor Low Dropout Regulator |
| 118 | 1 | X1 | 100_00MHz_LVDS | SiTime | SIT9120AC-2D2-33E100.000 | 100MHz Low-Jitter LVDS Clock Osc., 7mm x 5mm, 50ppm |
| 119 | 1 | X2 | 156.25MHz_LVCMOS | SiTime | SIT8256AI-83-33E-156.250T | 156.25MHz Single ended CMOS Clock Osc., 7mm x 5mm |
| 120 | 2 | X3,X4 | HDR40 | Würth | 61304021121 | HEADER 40POS .100" DL TIN |
| 121 | 1 | Y1 | 12MHZ | TXC | 7M-12.000MAAJ-T | CRYSTAL 12.0000MHZ 18PF SMD |
| 122 | 2 | Y2,Y3 | 25MHZ | TXC | 7M-25.000MAAJ-T | CRYSTAL 25.0000MHZ 18PF SMD |

Appendix C. Demo Board Rev A Information

ECP5 Versa Development Board – Working with Revision A

This document covers the Revision B of ECP5 Versa. To work with Revision A there are several items to be aware of:

Setting the Configuration Mode

On the Rev A, setting the Configuration Mode requires modifying the resistor population in the CFG[2:0] Setting Resistor Field (see Figure 3) as described in Table 3. This requires adding and/or removing 0603 size SMT resistors as necessary. Some soldering skill and the correct equipment is necessary to perform this rework.

Figure 20. CFG[2:0] Setting Resistor Field – Revision A



Table 14. CFG[2:0] Selection – Revision A

| Configuration Mode | CFG[2:0] | Rev A | | | | | |
|----------------------|----------|-----------------------|-----------------------|-----------------------|----------------------|----------------------|----------------------|
| | | R190 (1K-4.7 kOhm) | R191 (1K-4.7 kOhm) | R192 (1K-4.7 kOhm) | R182 (0 - 1 kOhm) | R188 (0 - 1 kOhm) | R189 (0 - 1 kOhm) |
| 1149.1 JTAG only | 000 | removed | removed | removed | placed | placed | placed |
| Slave SPI | 001 | removed | removed | placed | placed | placed | removed |
| Master SPI | 010 | removed | placed | removed | placed | removed | placed |
| SCM (Slave_Serial) | 101 | placed | removed | placed | removed | placed | removed |
| SCM (Slave_Parallel) | 111 | placed | placed | placed | removed | removed | removed |

1. Removing all six resistors is equivalent to Slave Parallel mode due to internal weak Pull-up resistors on CFG[2:0] pins.

ECP5 Pin Assignment Changes

The following pins (Table 15) have changed assignment between the Rev A and Rev B board. These functions would need to be remapped for use between the two boards.

Table 15. Pin Assignment Updates - Rev A vs Rev B

| Pin Signal / Function | Rev A ECP5 Ball Location | Rev B ECP5 Ball Location |
|------------------------------|--------------------------|--------------------------|
| SEG1 (Character LED) | L19 | L18 |
| Switch 3-7 | J19 | K19 |
| Phy1_CLK125 (Ethernet Phy 1) | L18 | L19 |
| Phy2_RxCLK (Ethernet Phy 2) | K19 | J19 |