AS3953B

14443 High Speed Passive Tag Interface

General Description

The AS3953B NFC interface IC (NFiC) delivers low cost, ultra low power NFC forum functionality to multiple different applications. The AS3953B is a analog front-end with integrated 14443A data framing and SPI interface. It is designed to create a fast data link between an ISO 14443A reader device (PCD) and a microcontroller. The AS3953B is **passively powered** meaning that it can be supplied from the PCD magnetic field, eliminating the need of a continual external supply. This makes the AS3953B perfect for wireless communication to a low-power battery powered device.

The AS3953B is used with an appropriate antenna coil connected to the terminals LC1 and LC2, and behaves as a normal passive ISO 144443A tag (PICC). After the anti-collision protocol is passed, the PCD sends a **Wake-Up** command, which wakes up the microcontroller by sending an interrupt. From this point onwards, the AS3953B serves as a data link between the microcontroller and the PCD. AS3953B can also operate as NFCIP-1 target at 106kbit/s.

The AS3953B includes an onboard EEPROM that can be accessed either from the PCD or from the microcontroller via the SPI interface. This built-in flexibility makes it ideal for two types of applications:

- Where personalization data is programmed by the PCD (even in case the SPI side is not powered) and it is later read by microcontroller through SPI interface.

- Where log data is stored periodically by the microcontroller and can then be read by the PCD even when the microcontroller is not powered.

A regulated power supply voltage extracted from the PCD field is also available on a pin and can be used as power supply for external circuitry. For example, an external microcontroller and a sensor could be powered from the PCD field combined with pass through data rates up to 848kbit/s, which means the AS3953B is ideal for contactless passive programming of MCU systems. The AS3953B can also operate as a stand-alone ISO 14443A tag.

The AS3953B supports ISO 14443A up to Level-4, meaning a contactless smart card or an NFC forum compatible tag (Tag Type 4) can be built. Having a NFC Forum compatible tag interface allows the AS3953B to be used in an application where a standard NFC enabled phone is used as a PCD.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3953B,14443 High Speed Passive Tag Interface are listed below:

Figure 1:
Added Value of Using AS3953B

Benefits	Features
• NFC Forum compliance for full interoperability	• ISO 14443A compliant to Level-4
• Data rate transmission up to the maximum allowed by ISO 14443A compliance	• Bit rates from 106 kbit/s till 848 kbit/s • 7 byte UID
• ECMA-340 / ISO/IEC_18092 compliance	• NFCIP-1 target at 106 kbit/s
• Internal user memory for standalone application	• 1k bit EEPROM (108 bytes of user memory)
• Allows zero-power standby	• Configurable wake-up interrupt (after tag is selected or using proprietary command)
• Enables long battery life time, or battery-less designs	• Powered from external magnetic field with the possibility to draw up to 5mA
• Allows supply of external circuitry	• User configurable regulated voltage extracted from external magnetic field
• Easy and fast antenna design and impedance matching	• Integrated resonant capacitor
• Guarantees no reset during reader (PCD) modulation	• Integrated buffer capacitor
• Design flexibility, easy integration. • Fits requirements for various embedded applications and manage of external microcontroller	• 4-wire Serial Peripheral Interface (SPI) with 32 byte FIFO
• Fits supply requirements for various applications, including industrial	• Wide SPI power supply range (1.65V to 3.6V)
• Flexibility for wide range of applications	• Wide temperature range: -40ºC to 85ºC
• Small outline, compatibility to common inlay and card manufacturing lines, surface-mount assembly	• Available as sorted wafer and Thin Wafer Level Chip Scale Package

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Applications

The device is ideal for applications like

- Passive wake-up

- Multipurpose HF interface to a controller

- Low power or passive programming

- Ultra low power data logger

- RFID programmable configuration EEPROM, ISO 14443A smart card, NFC Forum tag type 4

- Bluetooth and Wi-Fi pairing

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS3953B Block Diagram
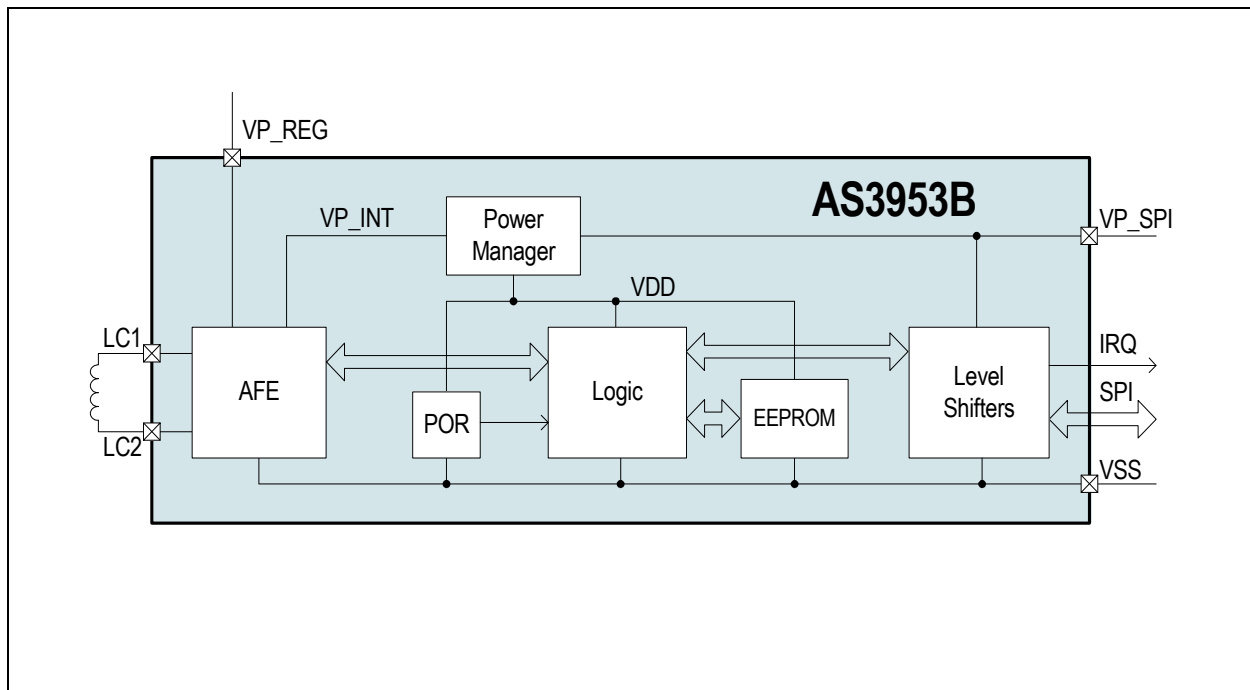
Pin Assignment

Figure 3:
Pin Assignment (Bottom View)
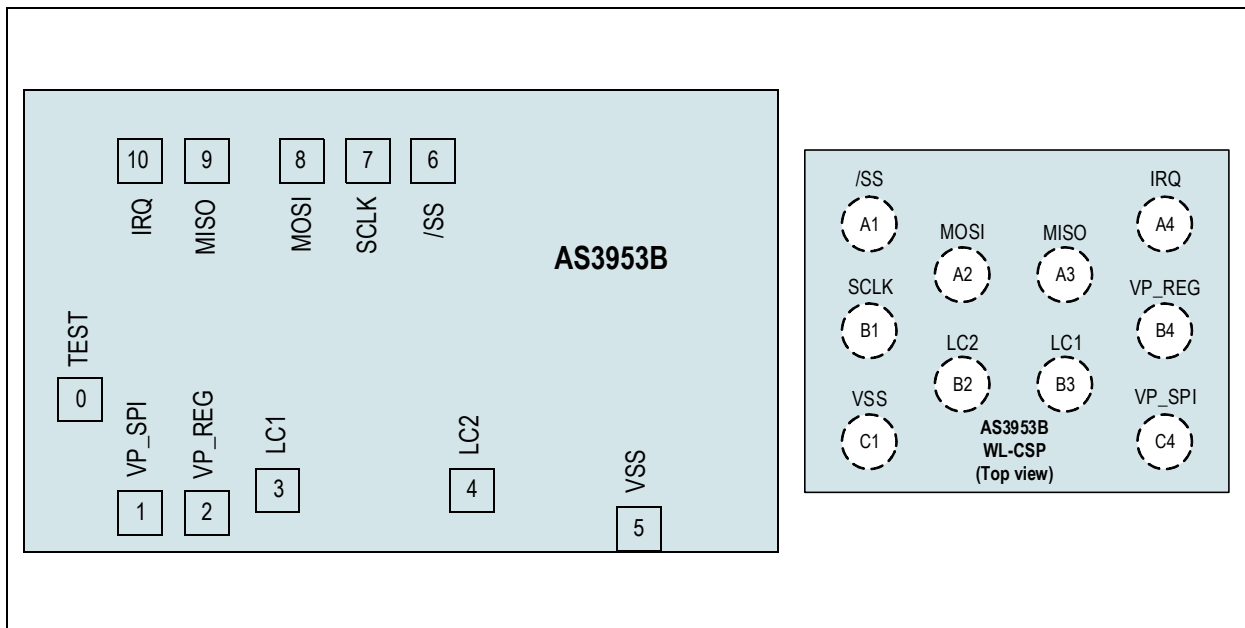
Figure 4:
Pin Description

Pin Number			
Sorted Die	**Pin Name**	**Pin Type**	**Description**
0	TEST	Internal use	No connection
1	VP_SPI	Supply pad	Positive supply of SPI interface
2	VP_REG	Analog output	Regulator output
3	LC1	Analog I/O	Connection to tag coil
4	LC2		
5	VSS	Supply pad	Ground, die substrate potential
6	/SS	Digital input	Serial Peripheral Interface enable (active low)
7	SCLK		Serial Peripheral Interface clock
8	MOSI		Serial Peripheral Interface data input
9	MISO	Digital output / tristate	Serial Peripheral Interface data output
10	IRQ	Digital output	Interrupt request output (active high)
-	Exposed Pad	Supply	Exposed pad to be connected to ground (optional)

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	DC supply voltage	-0.5	5	V	
V_{IN}	Input pin voltage except LC1 and LC2	-0.5	5	V	
	Input pin voltage pins LC1 and LC2	-0.5	6.5	V	
	Peak current induced on pins LC1 and LC2		100	mA	
I_{scr}	Input current (latchup immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge (human body model)	±2		kV	Norm: MIL 883 E method 3015
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	125	ºC	
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	1			Maximum floor life time of unlimited hours
t_{strg_DOF}	Storage time for DOF/dies or wafers on foil	3		months	Refer to indicated date of packing
T_{strg_DOF}	Storage temperature for DOF/dies or wafers on foil	18	24	ºC	
RH_{open_DOF}	Relative humidity for DOF/dies or wafers on foil in open package		15	%	Opened package
RH_{Unopen_DOF}	Relative humidity for DOF/dies or wafers on foil in closed package	40	60	%	Unopened package

Electrical Characteristics

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Figure 6:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
I_{lim}	Limiter current			30	mA	Till this current limiter clamps VLC1-LC2 to 5.0V
V_{VP_SPI}	SPI power supply	1.65		3.6	V	When logic powered from RFID interface
		1.8		3.6	V	When logic powered from VP_SPI interface
T_{AMB}	Ambient temperature	-40		85	ºC	

DC/AC Characteristics for Digital Inputs and Outputs

Figure 7:
CMOS Inputs, Valid for Input Pins /SS, MOSI, SCLK

Symbol	Parameter	Min	Typ	Max	Units	Note
V_{IH}	High level input voltage	0.7 * VP_SPI			V	
V_{IL}	Low level input voltage			0.3 * VP_SPI	V	
I_{LEAK}	Input leakage current			1	µA	

Figure 8:
CMOS Outputs, Valid for Output Pins MISO, IRQ

| Symbol	Parameter	Min	Typ	Max	Units	Note
V_{OH}	High level output voltage	0.85 * VP_SPI			V	I_{SOURCE} = 1mA VP_SPI = 3V
V_{OL}	Low level output voltage			0.15* VP_SPI	V	
C_L	Capacitive load			50	pF	
R_O	Output resistance		200	400	Ω	
R_{PD}	Pull-down resistance pad MOSI		10		kΩ	Pull-down can be enabled while MISO output is in tristate. The activation is controlled by register setting

Electrical Specification

Figure 9:
VP_SPI = 3.0 V, Temperature 25ºC (unless noted otherwise)

Symbol	Parameter	Min	Typ	Max	Units	Note
I_{SB_SPI}	Standby consumption on VP_SPI		65	100	nA	@ 25ºC; RF field not applied
		1.8	2.2	2.7	µA	@ 25ºC; RF field applied
V_{LIM}	Limiter voltage		5.2	5.7	V	I_{LC} = 30mA (DC)
I_S	Supply current		250		µA	Internal supply current measured in test mode on VREC, 13.56 MHz alternative pulses with amplitude 2Vpp, negative peak at VSS, forced to LC1 and LC2
V_{VP_REG}	Regulated supply voltage	1.65	1.8	2.01	V	Set to 1.8V in EEPROM Configuration word
V_{HF_PON}	HF_PON threshold (rising VREG)		2.3		V	Guaranteed by design only
V_{POR_HY}	HF_PON hysteresis		0.8		V	
V_{MOD}	Modulator ON voltage drop		1.2		V	I_{LC} = 1mA
			3.3			I_{LC} = 30mA
C_R	Resonance capacitor	25.2	28	30.8	pF	Measured at 10MHz, 3.0Vpp (2.5Vpp)
EE_{EN}	EEPROM endurance	100000			cycles	@ 125ºC
EE_{RET}	EEPROM retention	10			years	

Detailed Description

Figure 10:
System Block Diagram
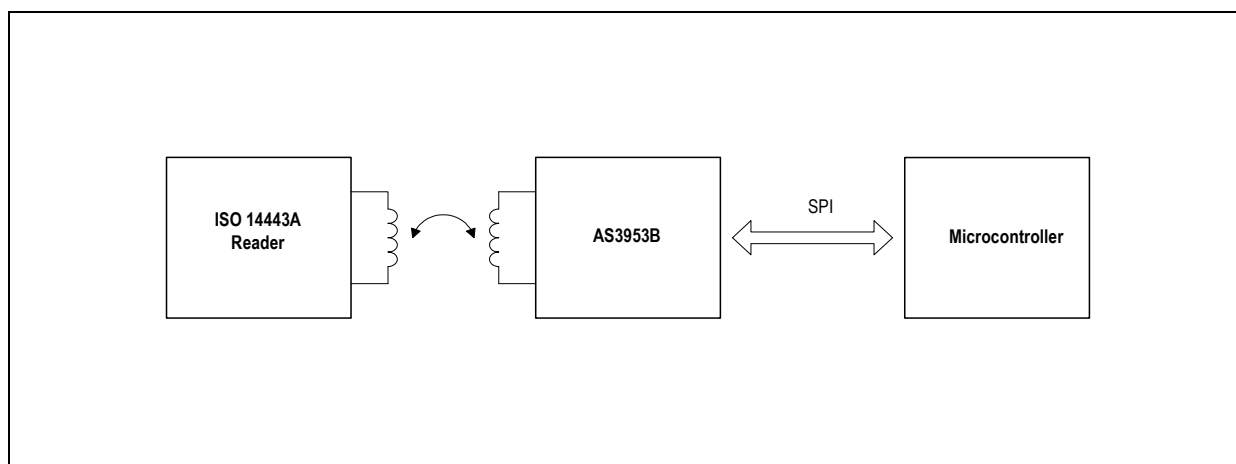
Circuit

The AS3953B is composed of ISO 14443A PICC Analog Front-end (PICC AFE), the ISO 14443A PICC Logic (PICC Logic), EEPROM, SPI Interface, Level Shifters and Power Supply Manager Block (Power Manager).

The PICC AFE is connected to an external tag coil, which forms together with integrated resonant capacitor an LC tank with a resonance at the external electromagnetic field frequency of 13.56 MHz. The PICC AFE has a built in rectifier and regulators. Output of internal regulator is called VP_INT. It is used to supply the PICC AFE and usually also the LOGIC and EEPROM (through Power Supply Manager). Output of external regulator VP_REG is available on a pin to supply some external circuitry.

Power Manager is controlling power supply of Logic and EEPROM. The two blocks can be supplied either from VP_INT or from VP_SPI (SPI power supply). In order to save current on VP_SPI, VP_INT is used as power supply whenever it is available. VP_SPI is only used when some activity is started over the SPI and the VP_INT is too low to be used as a power supply.

The PICC Logic is responsible for PICC-to-PCD communication up to the Level-4 (block transmission) of ISO 14443A. This means that anti-collision and other low-level functionality are implemented there.

The SPI Interface logic contains a 32 byte FIFO for block transmission data which is exchanged on Level-4 of ISO 14443A communication. It also contains some control and display registers.

The EEPROM is used to store the UID, the housekeeping data (configuration and control bits) and user data. It can be accessed from both sides (RFID and SPI).

PICC AFE

Figure 11 depicts main PICC AFE building blocks.

The PICC AFE is connected to external tag coil, which together with the integrated resonant capacitor forms an LC tank with resonance at external electromagnetic field frequency (13.56 MHz). Figure 11 depicts the main PICC AFE building blocks.

Rectifier: Extracts DC power supply from AC voltage induced on coil terminals.

Limiter: Limits the maximum voltage on coil terminals to protect PICC AFE from destruction. At voltages that exceed limiter voltage it starts to absorb current (acts as some sort of shunt regulator).

Modulator Switch: Is used for communication PICC-to-PCD. When switched on, it will draw current from coil terminals. This mechanism is called load modulation. Variation of current in the modulator switch (ON and OFF state) is seen as modulation by the PCD.

Demodulator: Is used for communication PICC-to-PCD. It detects AM modulation of the PCD magnetic field. The demodulator is designed to accept modulation according to ISO 14443A; all standard bit rates from 106 kbit/s to 848 kbit/s are supported. The modulation for bit rate 106 kbit/s is 100%, whereas for other bit rates it may be less.

Clock Extractor: The clock extractor extracts a digital clock signal from the PCD carrier field frequency which is used as clock signal by logic blocks.

HF_PON: Observes rectified regulated voltage VREC. When the supply voltage is sufficiently high it enables operation of the PICC AFE and the digital tag logic. A buffer capacitor and HF_PON hysteresis guarantees that there is no reset during reader (PCD) modulation.

Internal Regulator: Provides regulated voltage VP_INT to the PICC AFE and in most cases also to EEPROM and logic blocks. Typical regulated voltage VP_INT is 2.0V. A buffer capacitor is also integrated.

External Regulator: Provides regulated voltage on external pin VP_REG where it can be used to supply some external circuitry. The regulated voltage and output resistance can be adjusted using EEPROM settings (see Figure 36). Appropriate external buffer capacitor is needed in case VP_REG is used in the application. The current to be provided depends on reader field strength, antenna size and Q factor, but it is limited to maximum 5mA.

Bias: Provides bias currents and reference voltages to PICC AFE analog blocks.

**Figure 11:**
PICC AFE Block Diagram
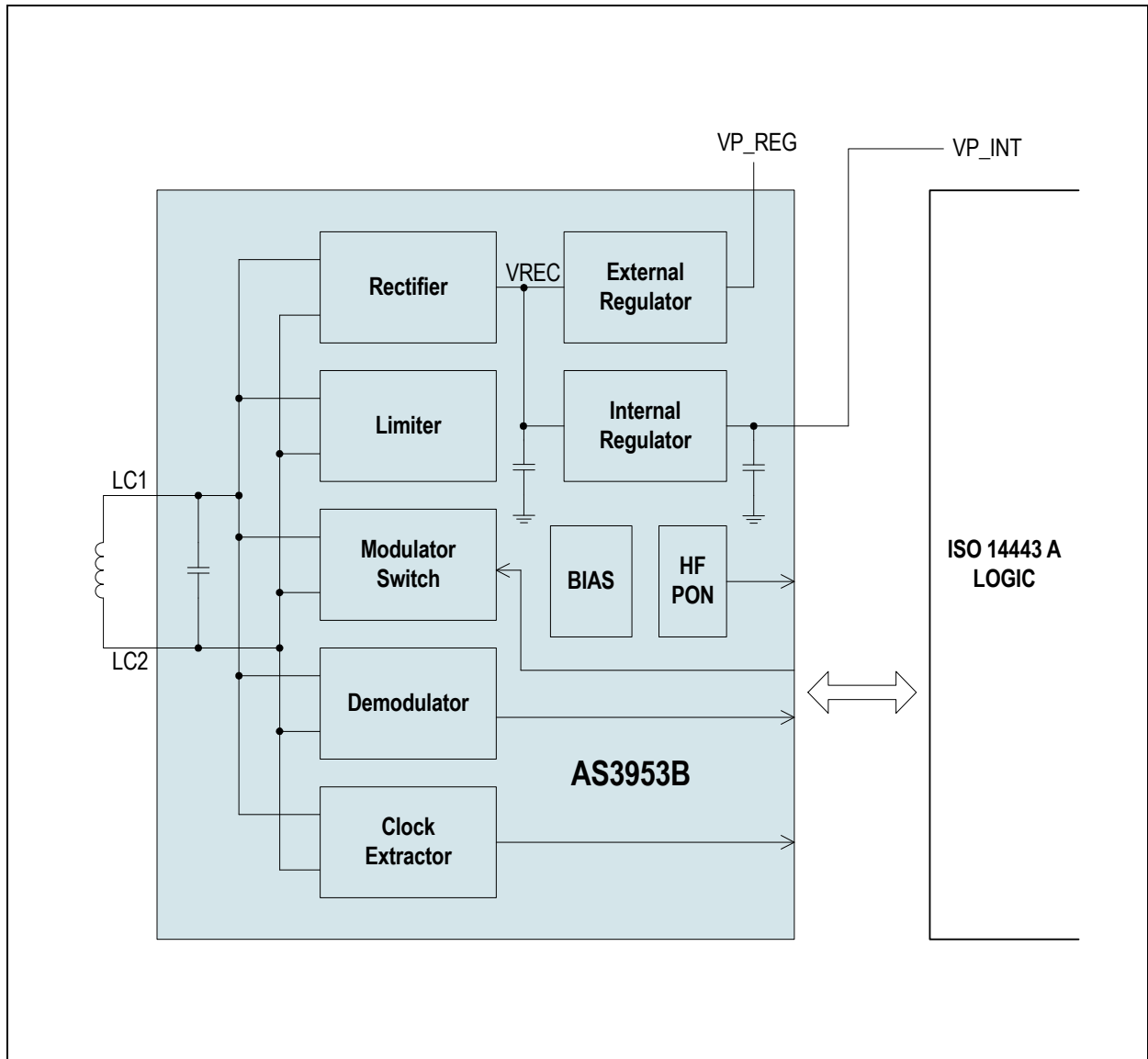
Power Manager

Power manager is controlling the positive supply voltage of the PICC Logic, EEPROM and SPI Interface (VDD). Its inputs are VP_INT (rectified and regulated supply extracted from PCD field) and the VP_SPI (SPI power supply from external).

In standby mode, when the AS3953B is not in a PCD field (condition is that rectified supply voltage is below HF_PON threshold) and the SPI is not active (/SS is high) the VDD supply is disconnected not to consume on VP_SPI. The only consumption on VP_SPI is leakage of level shifters and SPI pins.

When the AS3953B is placed in a PCD field the VDD is connected to VP_INT. This happens once the VP_INT level is above the HF_PON threshold.

VP_SPI is connected to VDD only when the AS3953B is not in the PCD field (rectified supply voltage is below HF_PON threshold) and the SPI interface is activated by pulling /SS signal low. The switch to VP_SPI is controlled by /SS signal. The deactivation is delayed by 0.7ms min., thus the switch stays on in case the time between successive SPI activations is short. During EEPROM writing, which is activated over the SPI, the switch is also active.

At activation of the switch the time between the falling edge of /SS signal and rising edge of SCLK has to be at least 50µs to allow charging of internal VDD buffer capacitor and expiration of POR signal. Please note that the only SPI operations, which are allowed in this mode, are reading and writing of the EEPROM and registers.

Figure 12:
Power Manager Concept
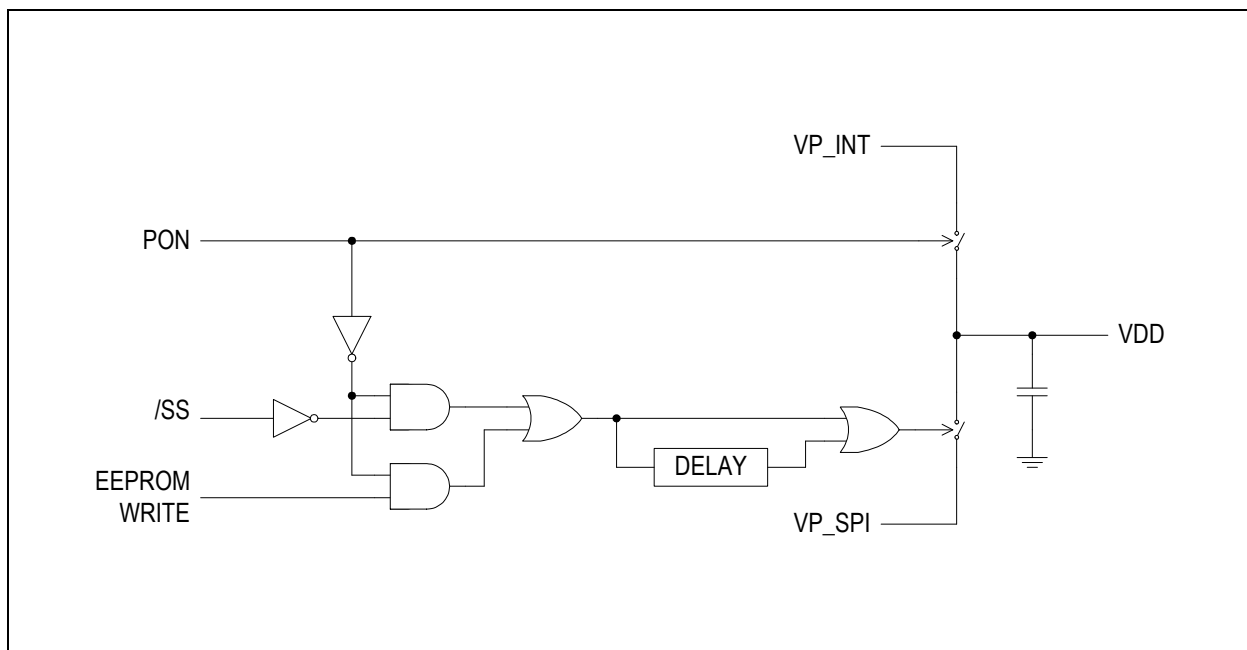
ISO 14443A Framing Mode

When Framing mode is selected the PICC logic performs receive and transmit framing according to the selected ISO 14443A bit rate.

During reception it recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from FIFO, generates parity and CRC bits, adds SOF and EOF and performs data encoding.

Default bit rate in the Framing mode is fc/128 (~106 kbit/s). Higher data rates may be configured by controller by writing the Bit Rate Definition Register.

In order to respect the PCD-to-PICC frame delay according to ISO14443-3 at data rate fc/128 bit the PICC logic synchronizes the response to the beginning of the next response window, but not earlier than window with n=9.

In this mode the EEPROM can be accessed via SPI when the RF field is active.

ISO 14443A Level-4 Protocol Mode

When Level-4 Protocol mode is selected the PICC Logic autonomously execute complete ISO 14443A Level-3 communication and certain commands of Level-4. This also includes the anti-collision sequence during which the AS3953B UID number is read by the PCD (7 bytes UID is supported), the AS3953B is brought in the selected state (ISO14443-4) in which data exchange between the AS3953B and the PCD can start. On this level also a reading and writing of the AS3953B EEPROM is possible.

In case the configuration bit *irq_l4* is set an interrupt is automatically sent to controller once the PICC Logic enters in ACTIVE(*) state (after sending SAK on Cascade Level 2).

Support of ISO 14443A Level-4

ISO 14443A-4 commands **RATS**, **PPS** and **DESELECT** are implemented in the PICC Logic. **RATS** and **PPS** define communication parameters, which are going to be used in the following data exchange by using the block transmission protocol. The advantage of implementing *PPS* that defines the bit rate used for communication, is that all bit rate issues are handled by the PICC Logic. The MCU gets the information about the actual receive and transmit bit rate by reading a dedicated display register. It has to be fast enough to serve receive and transmit at the maximum bit rate.

Execution of the block transmission protocol is left to the controller. In case of receiving the block data from the PCD the PICC Logic provides support by detecting and removing start bit, stop bit, parity bits and CRC. Parity bits and CRC are also checked. When the block data is sent to the PCD the PICC Logic calculates and inserts start bit, parity bits, CRC and stop bit.

DESELECT puts the PICC Logic in HALT state. An interrupt is sent to controller upon reception of **DESELECT** command to inform it that PCD stopped the Level-4 communication.

Additionally to supporting the ISO14443-4 transmitting protocol the PICC Logic accepts also proprietary commands. Proprietary commands are identified by setting the two MSB bits of first transmitted byte to '01' (This combination is not used by ISO 14443A Level-4 protocol). The following custom commands are implemented:

- **Wake-Up:** Sends a wake-up interrupt to controller
- **Read EEPROM:** Reads data from EEPROM
- **Write EEPROM:** Writes data to EEPROM

Support of ISO 14443A Optional Features

- CID is supported
- NAD is not supported
- Historical bytes are not supported
- Power level indication is not supported

Coding of UID

Anti-collision procedure is based on Unique Identification Number (UID). The AS3953B supports double UID size (7 bytes). First three bytes of UID are hard-wired inputs to the PICC Logic (*uid<23:0>*). Last 4 bytes of UID are stored in EEPROM UID word.

First Byte of UID (uid0)

First byte of UID is according to [ISO3] ISO/IEC 7816-6 IC Manufacturer ID. It is coded on bits *uid<7:0>*. **ams** IC Manufacturer ID is 3F(hex).

Second Byte of UID (uid1)

Second byte of UID – *uid<15:8>* is reserved for **ams** chip type (IC Type). Every **ams** RFID tag IC has its own chip type attributed. Therefore PCD which has read the RFID tag UID knows to which tag IC it is talking.

The AS3953B IC type is 10(hex).

Third Byte of UID (uid2)

Third byte of UID – *uid<23:16>* is set to 00(hex). Figure below defines the coding of the first three bytes of UID.

Figure 13:
Coding of First Three Bytes of UID

UID Byte	FL Signal Name	Value (hex)
uid0	uid<7:0>	3F
uid1	uid<15:8>	10
uid2	uid<23:16>	00

The last 4 bytes of UID are read from EEPROM (UID word).Figure below defines the last four bytes of UID.

Figure 14:
Coding of Last Four Bytes of UID

UID Byte	UID Word Bits
uid3	b7-b0
uid4	b15-b8
uid5	b23-b16
uid6	b31-b24

Coding of ATQA, SAK and ATS

Several bits of responses ATQA, SAK and ATS are defined as "don't care" in the ISO 14443A standard. Some others are defined by optional choices in standard protocol. This section defines how these bits are set by the AS3953B.

ATQA

ATQA is response to **REQA** and **WUPA** commands. Figure below defines the ATQA coding.

Figure 15:
ATQA Coding

b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1
0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
								UID size			Bit frame anti-collision				

Bits *b16* to *b13* are RFU bits which must be set to '0'.

Bits *b12* to *b9* are proprietary coding and are set to '0'.

Bits *b8* and *b7* indicate double size UID.

Bit *b6* is 'RFU' bit and is set to '0'.

For bit frame anti-collision, the code 00100 is chosen.

SAK

SAK is response to **SELECT** command. AS3953B UID has double size, which defines SAK responses for Cascade Level 1 and Cascade Level 2.

Cascade Level 1: According to ISO 14443-3, all bits except *b3* are "don't care" for Cascade Level 1. Figure below defines Cascade Level 1 coding.

Figure 16:
Cascade Level1 Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
0	0	As b6 in SAK CL2	0	0	1	0	0	Cascade bit set: UID not complete

Bit *b6* in Cascade Level 1 is always set as bit *b6* in Cascade Level 2. This is done in accordance to EMVCo Level – 1 Contactless Digital Test specifications.

Cascade Level 2: According to ISO 14443-3 all bits except *b6* and *b3* are "don't care" for Cascade Level 2.

If configuration *bit16 [nl4]* is set to logic '0' (default state), the SAK on Cascade Level 2 reports that tag is compliant to level4 (see figure below).

Figure 17:
Cascade Level 2 Coding (ISO/IEC14443-4 compliant)

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
0	0	1	0	0	0	0	0	UID complete, tag is compliant to ISO/IEC14443-4

If configuration *bit16 [nl4]* is set to logic '1', the SAK on Cascade Level 2 reports that tag is NOT compliant to Level-4 (see figure below).

Figure 18:
Cascade Level 2 Coding (NOT ISO/IEC14443-4 compliant)

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
0	0	0	0	0	0	0	0	UID complete, tag is **NOT** compliant to ISO/IEC14443-4

ATS

ATS is response to ISO 14443-4 command **RATS**. The content of the ATS is used to inform the PCD about PICC capability (like the maximum frame size, support of higher bit rates, etc.)

Several response fields of ATS are stored in EEPROM configuration word. The AS3953B ATS is composed of following 5 bytes according to [ISO4]: TL, T0, TA(1), TB(1) and TC(1).

TL: This is the length byte. Since ATS is composed of 5 bytes, its content is 0x05. Figure below defines the coding of the TL byte.

Figure 19:
TL Byte Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
0	0	0	0	0	1	0	1	Coding of ATS byte TL

T0: This is the format byte. Figure below defines the coding of the T0 byte.

Figure 20:
T0 Byte Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
0	1	1	1	fsci<3>	fsci<2>	fsci<1>	fsci<0>	Coding of ATS byte T0
	TC(1)	TB(1)	TA(1)	FCSI				

Bit *b8* is set to '0'.

Bits *b7* to *b5* indicate presence of bytes TA(1), TB(1) and TC(1) and hence are all set to '1'.

Bits *b4* to *b1* are called FCSI and codes FCS. The FCS is maximum size of a frame defined by PICC. It is defined by configuration bits *fsci<3:0>*.

TA(1): This codes the bit rate capability of PICC. Supported higher bit rates of AS3953B are 212, 424 and 848 kbit/s. However in specific applications, it is advised to report lower capability to PCD (for example, due to the usage of slow controller or low power application). Due to this reason the TA(1) response is configurable using configuration bits.

Figure 21:
TA(1) Byte Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
dr_sdr	dr_picc_8	dr_picc_4	dr_picc_2	0	dr_pcd_8	dr_pcd_4	dr_pcd_2	Coding of ATS byte TA(1)
	DS (PICC to PCD)				DR (PCD to PICC)			

Bit *b8* set to '0' codes possibility of having different data rates for each direction.

TB(1): The interface byte TB(1) conveys information to define the frame waiting time and the start-up frame guard time. The interface byte TB(1) consists of two parts:

- The most significant half-byte *b8* to *b5* is called FWI and codes frame waiting time (FWT).

- The least significant half byte *b4* to *b1* is called SFGI and codes a multiplier value used to define the SFGT. The SFGT defines a specific guard time needed by the PICC before it is ready to receive the next frame after it has sent the ATS. SFGI is coded in the range from 0 to 14. The value of '0' indicates 'No SFGT needed'.

- The SFGT bits are fixed to default value which is 0x0, while the FWI bits are defined by configuration bits *fwi<3:0>*. Figure below defines the coding of the TB(1) byte.

Figure 22:
TB(1) Byte Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
fwi<3>	fwi<2>	fwi<1>	fwi<0>	0	0	0	0	Coding of ATS byte TB(1)
	FWI				SFGI			

- **TC(1):** The interface byte TC(1) specifies a parameter of the protocol. The interface byte TC(1) consists of two parts:

- The most significant bits *b8* to *b3* are set to 000000, all other values are 'RFU'.

- The bits *b2* and *b1* define which optional fields in the prologue field are supported by the PICC. The PCD is allowed to skip fields that are supported by the PICC. Bit *b2* indicates support of CID and *b1* indicates support of NAD. The AS3953B value is '10' indicating "CID supported" and "NAD not supported".

Figure below defines the coding of the TC(1) byte.

Figure 23:
TC(1) Byte Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
0	0	0	0	0	0	1	0	Coding of ATS byte TC(1)
						CID	NAD	

Proprietary Commands

Proprietary commands have the same format as blocks defined in ISO 14443-4 with the difference that optional NAD field is abandoned since NAD is not supported by the AS3953B. The same format is used for commands sent by PCD and AS3953B responses. Figure below defines the coding of the Proprietary commands.

Figure 24:
Proprietary Commands Coding

Prologue Field		Information Field	Epilogue Field
PCB	[CID]	INF	EDC
1 byte	1 byte		2 bytes

Prologue field consists of the mandatory Protocol Control Byte and an optional Card Identifier Byte. Card identifier byte is according to ISO 14443-4 definition. Epilogue field contains CRC over transmitted block.

Prologue Field for Proprietary Commands

Figure below defines the coding of Prologue field for Proprietary commands.

Figure 25:
Prologue Field (proprietary commands)

Bit	Value	Function
b8	0	01 indicates proprietary command
b7	1	
b6	0	Shall be set to this value, other values are 'RFU'
b5	1	
b4		CID following if bit is set to '1'
b3	1	Shall be set to this value, other values are 'RFU'
b2	0	
b1	1	

The following proprietary commands are implemented:

- **Wake-Up:** Sends a wake-up interrupt to controller
- **Read EEPROM:** Reads data from EEPROM
- **Write EEPROM:** Writes data to EEPROM

Wake-Up Command

Information field of **Wake-Up** command consists of one byte only (see figure below). The AS3953B echoes back the same information field.

Figure 26:
Wake-Up Command

01h
1byte

Figure below defines the coding of the AS3953B reply INF to **Wake-Up** command.

Figure 27:
Wake-Up Reply

01h
1byte

Word Address Byte

Both proprietary commands related to EEPROM (Read and Write) use Word Address byte to define the address of EEPROM word that is accessed. Seven MSB bits of the Address Byte are used to define the address, while the last bit is "don't care".

Note(s): The valid range for the Word Address byte is from 0000 000xb to 0011 111xb (EEPROM words from 00h to 1Fh).

Read EEPROM

The **Read EEPROM** command is used to read data from the EEPROM. The request information field contains the following three bytes:

• Command code byte (02h)

• Address of the first word to be read

• Number of words to be read

Figure below defines coding of **Read EEPROM** command information field.

Figure 28:
Read EEPROM Command

02h	Address of First Word to Be Read	Number of Words (≤ 8) to Be Read
1byte	1byte	1byte

If the request is normally processed, the reply information field contains the status word *90h* followed by the data. In case of error, the information field only contains the error status byte. The following rules apply:

• In case the number of words to be read is higher than 8, first eight words are read.

• In case the read protected word (its read lock bit is set) is accessed, an all '0' data is sent out.

• In case the reading starts at valid address and the number of words to read is such that the reading would be done beyond the EEPROM addressing space, all '0' data is returned for non-existing addresses.

• In case the reading starts at non-existing address, error information field is returned.

Figure below defines the coding of the AS3953B reply information field to **Read EEPROM** command, if command is normally processed.

Figure 29:
Read EEPROM Reply (successful)

90h	Data
1byte	4 to 32 bytes

Figure below defines the coding of the AS3953B reply information field to **Read EEPROM** command, in case of an error.

Figure 30:
Read EEPROM Reply (error code)

Information Field	Comment
61h	Error (no diagnostic)

Write EEPROM

The **Write EEPROM** command is used to write one EEPROM word (32 bits). The request information field contains 6 bytes:

- Command code byte (04h)
- Address of the word to be written
- Four bytes (32 bits) of data to be written

Figure below defines coding of **Write EEPROM** command information field.

Figure 31:
Write EEPROM Command

04h	Address of Word to Be Written	Data
1 byte	1 byte	4 bytes

The AS3953B reply contains one byte informing whether the writing of EEPROM was executed or whether there was an error. Prior to actual programming of data in EEPROM, the control logic checks whether there is enough power available. This is done by performing so called power check during which a dummy EEPROM programming is started. If the power check fails, EEPROM programming is not performed and an error code is sent. The EEPROM programming is a time consuming operation.

Therefore, if the EEPROM programming is executed, the AS3953B reply comes after 8ms typical. Figure below defines the coding of the AS3953B reply to **Write EEPROM** command.

Figure 32:
Write EEPROM Reply

Information Field	Comment
90h	Writing is normally processed
61h	Writing is not done due to coding error (error in parity, CRC, nonexistent address…)
62h	Writing is not done since the word is locked
64h	Writing is not done due to power check fail

Passing of Block Data to Controller

After the PICC Logic has passed the anti-collision procedure and replied with SAK on Cascade Level 2 it passes in ACTIVE(*) state. On this level it expects that blocks received from the PCD have the format according to ISO 14443A-4. The ISO 144443A Logic recognizes the command by observing the first received byte. Based on content of this byte command is either processed by the AS3953B or the complete block data is put in the FIFO for further processing by the controller. The figure below displays the decision criteria.

Figure 33:
First Byte of the ISO 14443-4 PCD Block

First Byte	Comment	Action of PICC Logic
1110 0000	RATS	Replies with ATS [1]
1110 not(0000)		Block is put in FIFO
1101 xxxx	PPS	Replies with PPS response (second character is CID)[1]
1100 x 010	DESELECT	Replies and go to Halt
1100 x not(010)	See note [2]	Block is put in FIFO
1111 xxxx	WTX, S(PARAMETERS), RFU [1]	Block is put in FIFO since controller needs it to implement chaining
01xx xxxx	Proprietary command	Proprietary command is processed
00xx xxxx	I-block	Block is put in FIFO
10xx xxxx	R-block	

Note(s):

1. RATS and PPS are only processed by the AS3953B logic in case they are sent according to the ISO 14443-4 specification (RATS is first command sent after entry in ACTIVE(*) state, optionally followed by PPS). In case RATS or PPS are sent once the AS3953B logic is in PROTOCOL state the information received is saved into FIFO and not acted upon.

2. Compatible with old and new S(PARAMETERS) definition: Old: 1100 x000 is S(PARAMETERS) block according to the ISO 14443-4/AM2. **New**: 1111 x000 is S(PARAMETERS) block according to the modification SC17/WG8.

As shown in Figure 33, the block data is put in the FIFO whenever the two MSB bits are 00 or 10 and also in the case when the four MSB bits are 1111. Therefore the implemented communication between the PCD and a tag implemented by the AS3953B and a controller does not need to follow the Block transmission protocol defined in the ISO 14443-4.

Use of CID

As mentioned above the AS3953B decides depending on content of the first byte of received message to either execute received message as a command or to put it in the FIFO. The second byte of the message comprises a CID number which is attributed by PCD. PCD will use CID number in case more PICCs are brought to Level-4 of communication at the same time.

CID is only checked for messages (commands) that are executed by the AS3953B. In case CID does not match such a command is rejected (no action is taken).

Messages that are based on first byte are put in FIFO and are not filtered by CID. It is left to controller to check for the CID and decide whether or not to reply (CID number is stored in the RATS Register).

ISO 14443A Level-3 Protocol Mode

Level-3 Protocol mode is intended for implementation of custom protocols for which coding on Level-4 of ISO 14443A communication according to Figure 33 is not appropriate. In this mode Level-2 and Level-3 behavior of the PICC logic is identical to ISO 14443A Level-4 Protocol mode, while on Level-4 all received data blocks are put in FIFO.

In case the configuration bit *irq_l4* is set an interrupt is automatically sent to controller once the PICC Logic enters in ACTIVE(*) state (after sending SAK on Cascade Level 2).

In this mode the EEPROM can be accessed via SPI when the RF field is active.

Transparent Mode

In the Transparent Mode the AS3953B logic is bypassed, AFE input and output signals are directly available on SPI interface pins when /SS signal is high.

- Modulator switch is controlled by pin MOSI (high is modulator on)

- Clock extractor output is sent to pin MISO

- Demodulator output is sent to pin IRQ

When /SS signal is low the SPI interface pins resume its normal functionality. In this mode the EEPROM can be accessed via SPI when the RF field is active.

EEPROM

The AS3953B contains an EEPROM block which can be accessed from both RFID and SPI interface. EEPROM contains 1024 bits (128 bytes) organized in 32 words of 32 bits. Words in EEPROM are number from 0 to 31(1F[hex]). Bits in a word are numbered from 0 to 31.

Most of the EEPROM is used to store user data (27 words – 864 bits), five words are used to store some housekeeping information (part of the AS3953B UID, configuration bits which define the AS3953B operating options, lock bits, which control the possibility to write EEPROM words).

Figure 34:
EEPROM Organization

Word Address [hex]	Content	Access Properties
0	UID	RO
1	Fabrication Data	RO
2	Configuration Word	RW
3	Write Lock Word	OTP
4	Read Lock Word	OTP
5: 1F	User Data	RW

Access Properties:

RO: Read only, writing to this word is not possible

RW: Reading and writing to this word is possible, writing is disabled once the lock bit is set

OTP: One time programmable. A bit of this word once set to '1' cannot be set back to '0'.

UID Word

The UID word contains four LSB bytes of 7 byte UID which is used during anti-collision and selection process. Every IC is programmed by a unique number during fabrication process at **ams**. For details on UID, please refer to Coding of UID.

Fabrication Data Word

This word stores some IC manufacturer data which is programmed and locked during fabrication process at **ams**.

Configuration Word

The Configuration word is used to define the AS3953B operating options. It is delivered by **ams** with default setting.

Figure 35:
Configuration Word (Bits 31 to 16)

Configuration Bit	Name	Default	Function
b31	fsci<3>	0	FSCI. Default value (2h) codes maximum size of frame accepted by PICC to 32 bytes which is the size of the FIFO. Please note that the AS3953B can support larger frame sizes in case FIFO is read during the receiving.
b30	fsci<2>	0	
b29	fsci<1>	1	
b28	fsci<0>	0	
b27	fwi<3>	0	FWI (default value (6h) defines frame waiting time of ~19.3ms)
b26	fwi<2>	1	
b25	fwi<1>	1	
b24	fwi<0>	0	
b23	dr_sdr	0	**1:** Only the same bit rate for both directions supported (TA(1) of ATS)
b22	dr_picc_8	0	**1:** DR=8 PICC-to-PCD supported (848kbit/s) (TA(1) of ATS)
b21	dr_picc_4	0	**1:** DR=4 PICC-to-PCD supported (424kbit/s) (TA(1) of ATS)
b20	dr_picc_2	0	**1:** DR=2 PICC-to-PCD supported (212kbit/s) (TA(1) of ATS)
b19	dr_pcd_8	0	**1:** DR=8 PCD-to-PICC supported (848kbit/s) (TA(1) of ATS)
b18	dr_pcd_4	0	**1:** DR=4 PCD-to-PICC supported (424kbit/s) (TA(1) of ATS)
b17	dr_pcd_2	0	**1:** DR=2 PCD-to-PICC supported (212kbit/s) (TA(1) of ATS)
b16	nl4	0	**1:** SAK on Cascade Level 2 reports that tag is not ISO 14443-4 compatible
b15	nfc	0	**1:** SAK on Cascade Level 2 reports that tag is NFC passive target

Note(s):

1. Configuration bits *b31* to *b15* define AS3953B response to **SAK** and **ATS** command in ISO 14443A Protocol modes, while bits *b14* to *b0* actually change performance.

2. Incase both *nl4* and *nfc* are set, the *nl4* setting prevails.

Figure 36:
Configuration Word (Bits 14 to 0)

Configuration Bit	Name	Default	Function	
b14	irq_pu	0	**1:** Send a power-up IRQ (after power-up initialization is finished)	
b13	irq_l4	0	**1:** Send an IRQ at entry in ACTIVE(*) state (after sending SAK on Cascade Level 2) [2]	
b12	mod_1	0	**00:** ISO 14443A Level-4 Protocol mode **01:** ISO 14443A Level-3 Protocol mode	
b11	mod_0	0	**10:** Framing mode **11:** Transparent mode	
b10	rxncrc	0	**1:** Rx – CRC is not checked, CRC part of message is also put in FIFO [3]	
b9	rxbs	0	**1:** Rx – Bit stream mode, received bits are put in FIFO (no parity and CRC check) [3]	
b8	txncrc	0	**1:** Tx – Do not generate CRC [3]	
b7	txbs	0	**1:** Tx – Bit stream mode, bits put in FIFO are sent without parity and CRC generation [3]	
b6	fdel<1>	0	PCD-to-PICC delay adjustment [4]	
b5	fdel<0>	0		
b4	vreg<1>	0	**00:** 1.8V **10:** 2.7V **01:** 2.0V **11:** 3.3V	External Regulated voltage (VP_REG) setting
b3	vreg<0>	0		
b2	rreg<1>	0	**00:** disabled **10:** 50Ω **01:** 100Ω **11:** 25Ω	External Regulator enable and output resistance setting
b1	rreg<0>	0		
b0	dr8	0	Reserved for internal use	

Note(s):

1. Configuration bits *b31* to *b15* define AS3953B response to **SAK** and **ATS** command in ISO 14443A Protocol mode, while bits *b14* to *b0* actually change performance.

2. Applicable in ISO 14443A Level-3 and Level-4 Protocol modes.

3. Applicable in ISO 14443A Level-3 Protocol mode and Framing mode, in Protocol mode applicable for frames which are put in FIFO.

4. Configuration bits *fdel<1:0>* are used to adjust frame delay time PCD-to-PICC. Delays caused by reader and tag resonant tanks and AFE processing are compensated by PICC logic.Figure below defines PCD-to-PICC frame delay compensation using *fdel* bits.

Figure 37:
PCD-to-PICC Frame Delay Compensation

fdel<1:0>	Delay [ns]	Delay [number of 13.56 MHz periods]
00	442.5	6
01	295.0	4
10	147.5	2
11	590.0	8

OTP Words

Write and Read Lock Words are OTP (One Time Programmable). This means that once they are set to '1', they cannot be reset back to '0'. Since setting of OTP bits is an irreversible operation, it is strongly recommended to perform it in controlled environment.

Write Lock Word

The Write Lock Word contains write lock bits. Each EEPROM word has a corresponding lock bit in the Write Lock Word. Once a certain lock bit is set to '1', the content of corresponding word cannot be modified any more (it becomes read only), EEPROM write commands issued either through PICC interface or through SPI interface are rejected. The lock bit of a certain number protects the word with the same number (e.g. $b5$ of lock word protects word 5). Since lock bits are OTP they cannot be reset back to '0' once they are set to '1'. Therefore once a certain word is locked it cannot be unlocked any more. The lock bits for page 0 is "don't care" since word 0 is always read only. Please note that setting lock bit $b2$ locks the Lock Word itself, therefore once this bit is set the lock configuration cannot be modified any more.

Read Lock Word

The Read Lock Word contains read lock bits. Each EEPROM word has a corresponding lock bit in the Read Lock Word. Once a certain lock bit is set to '1', the content of corresponding word cannot be read through PICC interface, it can only be read through SPI interface. The lock bit of a certain number protects the word with the same number (e.g. $b5$ of lock word protects word 5). Since lock bits are OTP they cannot be reset back to '0' once they are set to '1'. Therefore once a certain word is locked it cannot be unlocked any more. The lock bits for pages 0 to 4 are "don't care"; these pages can be read through PICC interface even in case their corresponding lock bits are set.

Application Information

SPI Interface

Communication between the AS3953B and controller is done through a 4-wire Serial Peripheral Interface (SPI) and additional interrupt signal. The AS3953B is an SPI slave device; it requests controller attention by sending an interrupt (IRQ pin).

Figure 38:
SPI and Interrupt Signals

Name	Signal	Signal Level	Description
/SS	Digital input with pull-up	CMOS	SPI enable (active low)
MOSI	Digital input	CMOS	Serial data input
MISO	Digital output with tristate	CMOS	Serial data output
SCLK	Digital input	CMOS	Clock for serial communication
IRQ	Digital output	CMOS	Interrupt output pin

While signal /SS is high the SPI interface is in reset, while it is low the SPI interface is enabled. It is recommended to keep signal /SS high whenever the SPI interface is not in use. MOSI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). First three bits of first byte transmitted after high to low transition of /SS define SPI operation mode. MSB bit is always transmitted first (valid for address and data). Read and Write modes support address auto incrementing, which means that in case after the address and first data byte some additional data bytes are sent (read), they are written to (read from) addresses incremented by '1'.

SPI interface supports the following modes:

- Read and write of the SPI Interface internal registers
- Read and write of the EEPROM
- Read and write of the FIFO
- Sending direct commands

Please note that the only SPI operations, which are allowed when logic and EEPROM are supplied from VP_SPI, are reading and writing of EEPROM and registers (see also Power Manager)

Figure 39:
SPI Modes

| MODE | MODE Pattern (communication bits) | | | | | | | | MODE Related Data | |
| | MODE | | | Trailer | | | | | | |
	M2	M1	M0	C4	C3	C2	C1	C0		
Register Write	0	0	0	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto incrementing)	
Register Read	0	0	1	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto incrementing)	
EEPROM Write	0	1	0	0	0	0	0	0	Word Address byte	4 bytes of word data
EEPROM Read	0	1	1	1	1	1	1	1	Word Address byte	4 bytes of word data (or multiple words in case of auto incrementing
FIFO Load	1	0	0	0	0	0	0	0	One or more bytes of FIFO data	
FIFO Read	1	0	1	1	1	1	1	1	One or more bytes of FIFO data	
COMMAND Mode	1	1	C5	C4	C3	C2	C1	C0		

MISO output is usually in tristate, it is only driven when output data is available. Due to this the MOSI and the MISO can be externally shorted to create a bidirectional signal.

During the time the MISO output is in tristate, it is possible to switch on a 10 kΩ pull-down by activating option bits *miso_pd1* and *miso_pd2* in IO Configuration Register.

Figure 40:
Signal to Controller
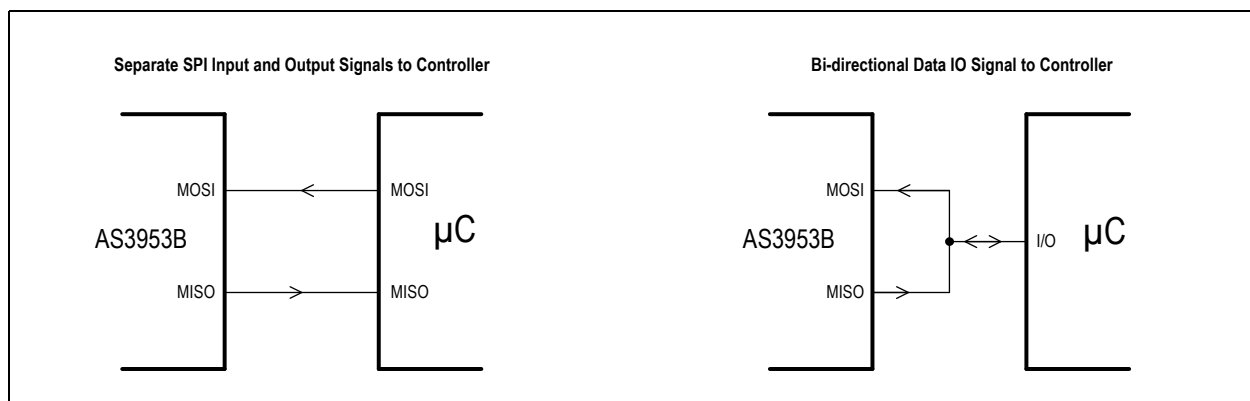
Writing of Data to Addressable Registers (Register Write Mode)

Following figures show cases of writing a single byte and writing multiple bytes with auto-incrementing address. After the SPI operation mode bits, the address of register to be written is provided. Then one or more data bytes are transferred from the SPI, always from the MSB to the LSB. The data byte is written in register on falling edge of its last clock. In case the communication is terminated by putting /SS high before a packet of 8 bits composing one byte is sent, writing of this register is not performed. In case the register on the defined address does not exist or it is a read only register no write is performed.

Note(s): When the AS3953B is powered via vp_SPI and not via field; the registers and EEPROM can be readout. When CS is set to low, after 50us of the falling edge, the Registers and the EEPROM can be readout. Nevertheless, if there is no activity for 1ms, there is a timeout and the logic goes to sleep, hence losing the values in the registers. (EEPROM values are retained).

Figure 41:
Writing of a Single Register
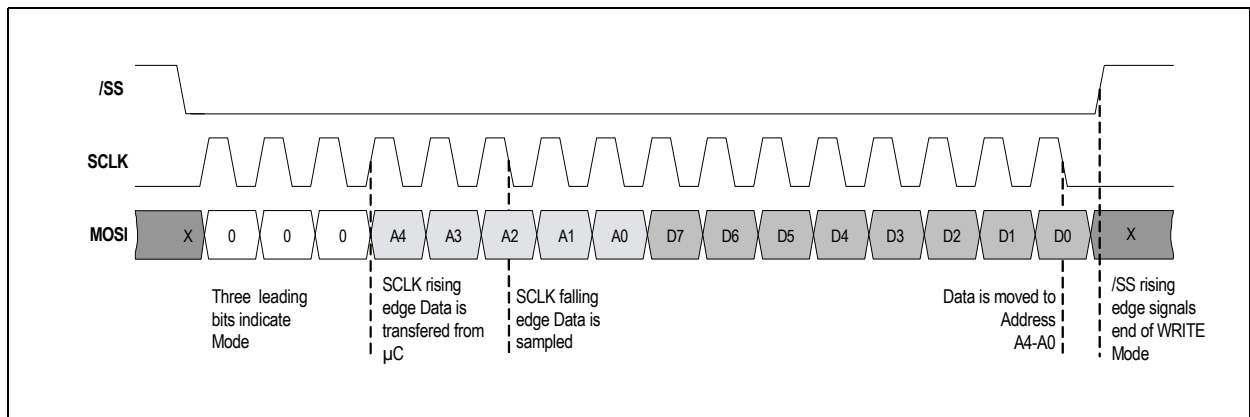
Figure 42:
Writing of Register Data with Auto-Incrementing Address
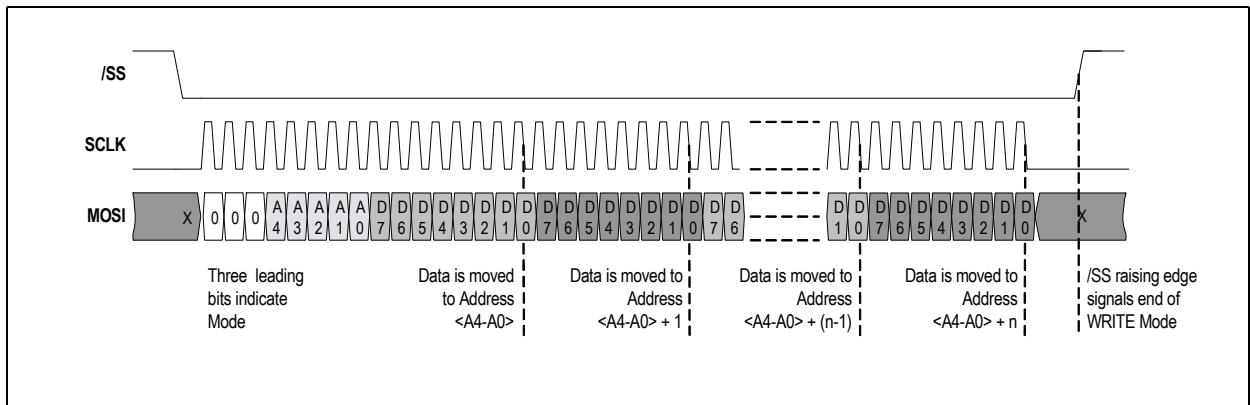
Reading of Data from Addressable Registers (Register Read Mode)

After the SPI operation mode bits the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes are transferred to MISO output, always from the MSB to the LSB. As in case of the write mode also the read mode supports auto-incrementing address.

MOSI is sampled at the falling edge of SCLK (like shown in the following diagrams); data to be read from the AS3953B internal register is driven to MISO pin on rising edge of SCLK and is sampled by the master at the falling edge of SCLK.

In case the register on defined address does not exist all '0' data is sent to MISO.

In the following figure example for reading of single byte is given.

Figure 43:
Reading of a Single Register
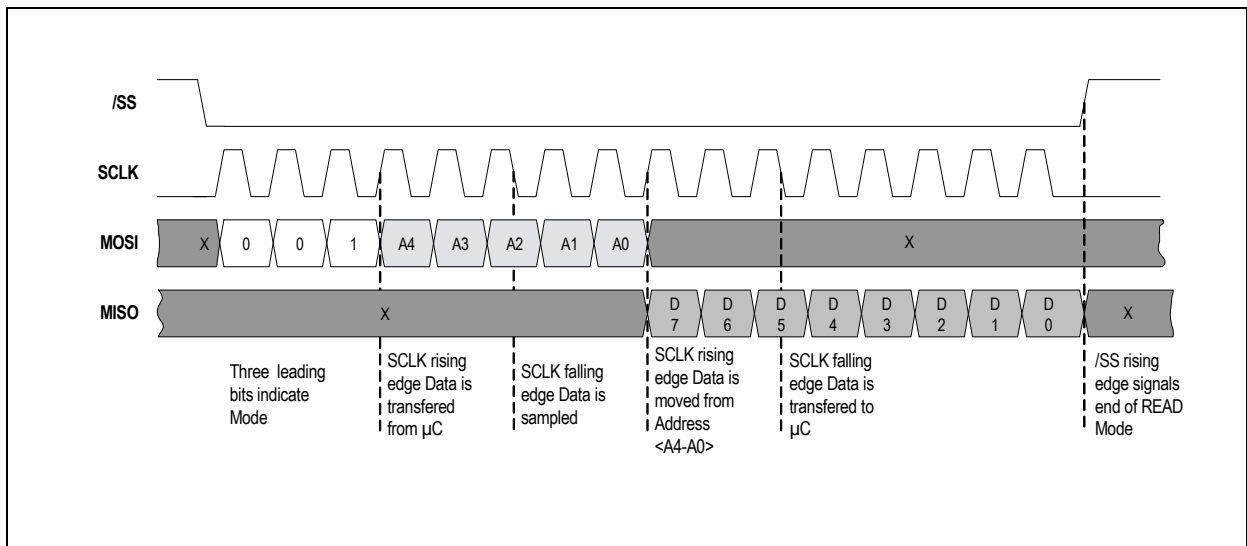
Writing and Reading of EEPROM Through SPI

EEPROM data can be read and written also through SPI interface. Due to possible conflict with RFID interface trying to access the EEPROM in ISO 14443A - level4 mode, access is granted to SPI only in case the PICC AFE is not active.

In all other modes defined in Mode Definition Registers, the EEPROM can be accessed via SPI when the RF field is active.

Activity of the PICC AFE can be checked by observing *hf_pon* bit of RFID Status Display Register. In case PICC AFE is activated while the EEPROM writing or reading operation is going on, this operation is interrupted, and *I_ee_spi* IRQ is sent.

Word Address Byte

Both EEPROM modes (Read and Write) use Word Address byte to define the address of EEPROM word which is accessed. 7 MSB bits of the Address Byte are used to define the address; while the last bit is "don't care" (utilized to synchronize EEPROM access).

Note(s): The valid range for the Word Address byte is from 0000 000xb to 0011 111xb (EEPROM words from 00h to 1Fh).

Figure below defines the EEPROM Word Address byte.

Figure 44:
EEPROM Word Address Byte

	B7	B6	B5	B4	B3	B2	B1	B0
EEPROM Word Address	WA6	WA5	WA4	WA3	WA2	WA1	WA0	x

EEPROM Write

In order to program an EEPROM word six bytes have to be sent (mode byte, word address byte and 4 bytes of word data, all of them MSB first)). Actual programming of EEPROM is started with rising edge of /SS signal which terminated the **EEPROM Write** command. During EEPROM programming the controller is not allowed to start another SPI activity. Controller is informed about the end of EEPROM programming by sending an interrupt (an interrupt flag is set in the Auxiliary Interrupt Register). *I_eew* flag is set in case EEPROM programming is normally finished; in case of an error (writing to write protected word, writing to non-existent address) an error flag (*I_er_eew*) is set. Typical EEPROM programing time for one word is 8ms.

Note(s): Word data is sent MSB first which is opposite to RFID EEPROM programming where LSB is sent first.

EEPROM Read

In order to read data from EEPROM first a mode byte is sent, followed by the word address byte (MSB first). Then one or more words of data with address auto incrementing (packets of 4 bytes) are transferred to MISO output, always from the MSB to the LSB. MOSI is sampled at the falling edge of SCLK; data to be read from the AS3953B EEPROM is driven to MISO pin on rising edge of SCLK and is sampled by the master at the falling edge of SCLK. In case the word on defined address does not exist all '0' data is sent to MISO.

Please note that SCLK frequency should not exceed 1MHz during EEPROM Read (limited by EEPROM read access time).

Figure 45:
Reading of EEPROM Page
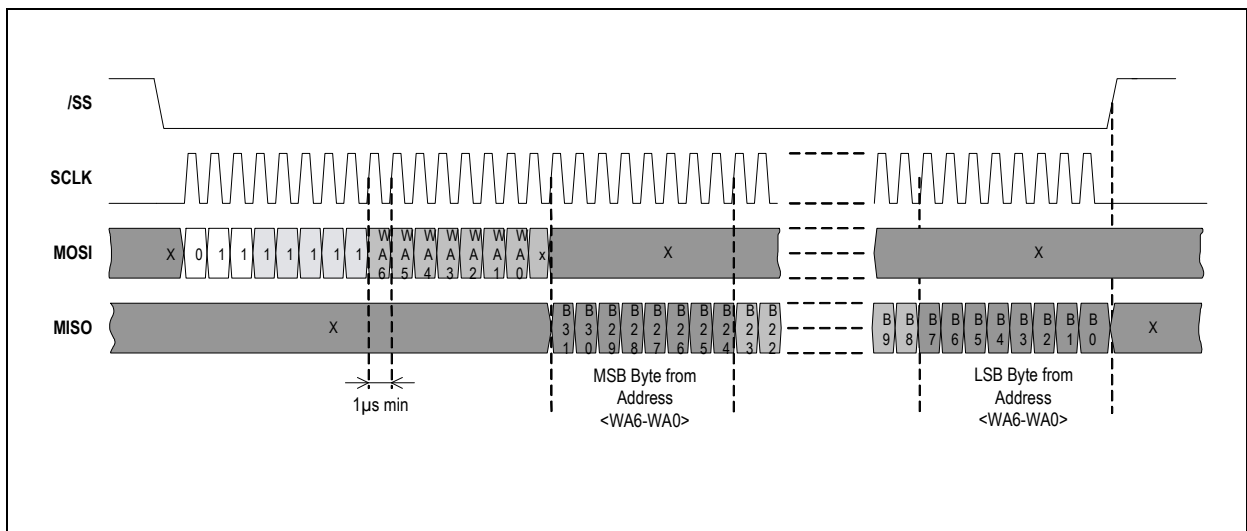
Loading Transmitting Data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. Difference is that in case of loading more bytes all bytes go to the FIFO. The command mode code 10 indicates FIFO operations. In case of loading transmitting data into FIFO all bits <C5 – C0> are set to '0'. Then a bit-stream, the data to be sent (1 to 32 bytes), can be transferred.

Figure 46 shows how to load the transmitting data into the FIFO.

Figure 46:
Loading of FIFO
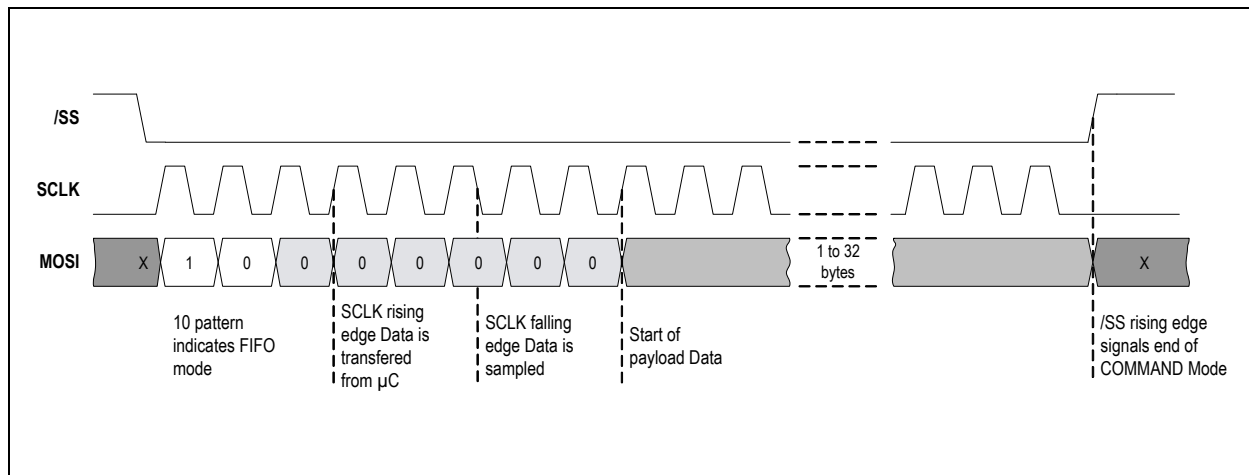
Reading Received Data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. Difference is that in case of reading more bytes they all come from the FIFO. The command mode code 10 indicates FIFO operations. In case of reading the received data from the FIFO all bits <C5 – C0> are set to '1'. On the following SCLK rising edges the data from FIFO appears as in case of read data from addressable registers. In case the command is terminated by putting /SS high before a packet of 8 bits composing one byte is read that particular byte is considered read.

Direct Command Mode

Direct Command Mode has no arguments, so a single byte is sent. SPI operation mode bits 11 indicate Direct Command Mode. The following six bits define command code, sent MSB to the LSB. The command is executed on falling edge of last clock.

Figure 47:
Sending a Direct Command
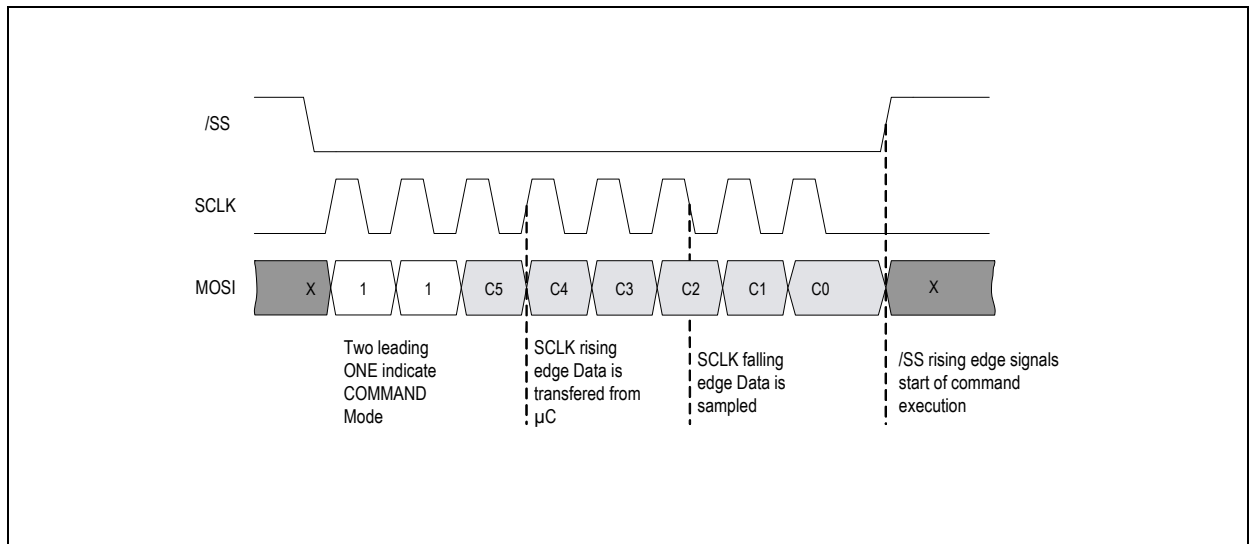
SPI Timing

Figure 48:
Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Note
General Timing (VDD = VDD_IO = VDD_D = 3.3V, Temperature 25°C)						
T_{SCLK}	SCLK period	200			ns	$T_{SCLK}=T_{SCLKL}+T_{SCLKH}$, during EEPROM read the SCLK period has to be increased to 1µs (this limitation is imposed by EEPROM read access time)
T_{SCLKL}	SCLK low	80			ns	
T_{SCLKH}	SCLK high	80			ns	
T_{SSH}	SPI reset (/SS high)	50			ns	
T_{NCSL}	/SS falling to SCLK rising	25			ns	first SCLK pulse
T_{NCSH}	SCLK falling to /SS rising	80			ns	last SCLK pulse
T_{DIS}	Data in setup time	10			ns	
T_{DIH}	Data in hold time	10			ns	
Read Timing (VDD = VDD_IO = VDD_D = 3.3V, Temperature 25°C, $C_{LOAD} \leq 50pF$)						
T_{DOD}	Data out delay		20		ns	
T_{DOHZ}	Data out to high impedance delay		20		ns	

Figure 49:
SPI General Timing
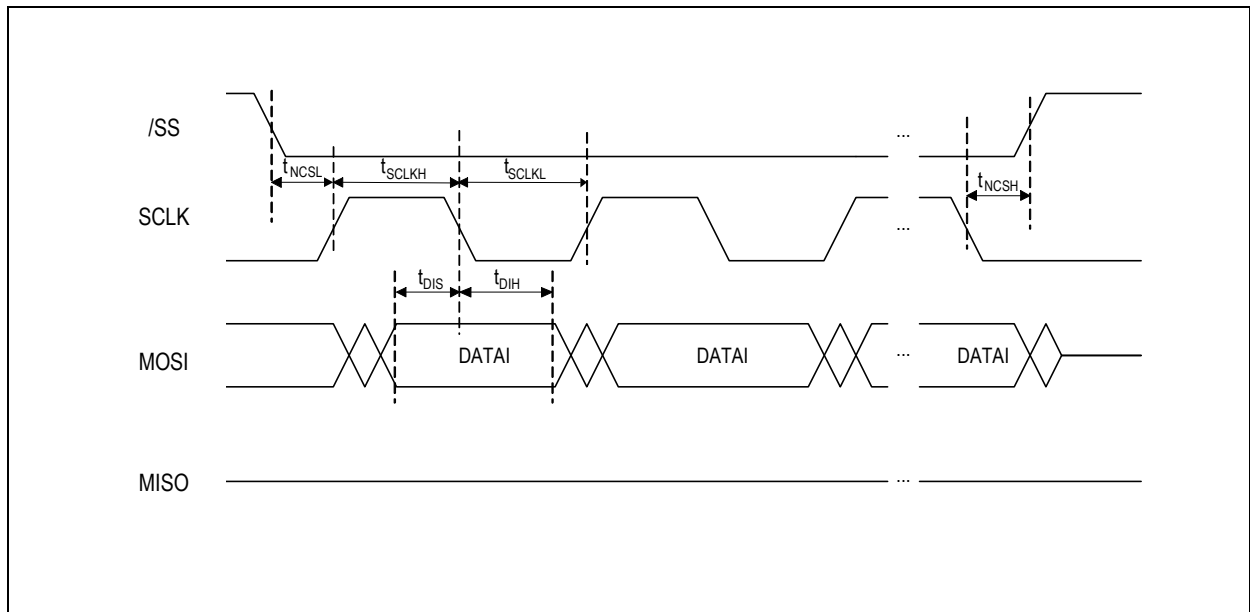
Figure 50:
SPI Read Timing
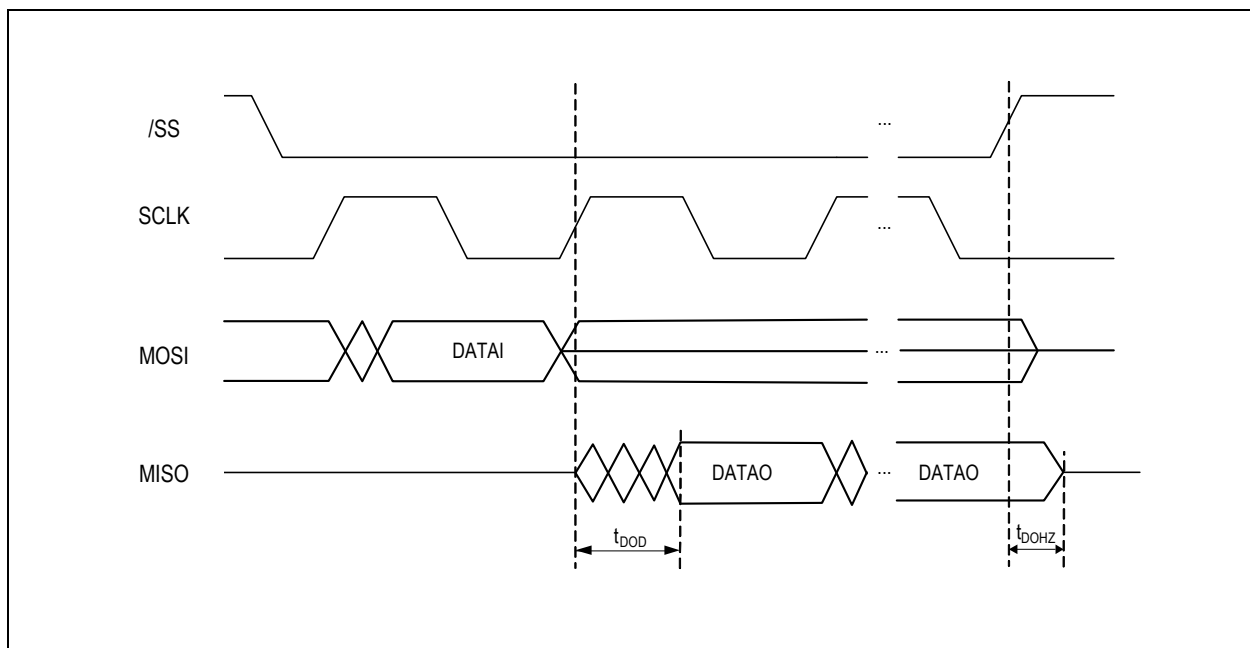
Interrupt Interface

There are two interrupt registers implemented in the AS3953B (Main Interrupt Register and Auxiliary Interrupt Register). Main Interrupt Register contains information about seven interrupt sources, while one bit references to interrupt sources detailed in Auxiliary Interrupt Register.

When an interrupt condition is met the source of interrupt bit is set in the Main Interrupt Register and the IRQ pin transitions to high.

The controller then reads the Main Interrupt Register to distinguish between different interrupt sources. In case the bit *I_aux* is pointing to the Auxiliary Interrupt Register, this register also needs to be read. After an interrupt register (main or auxiliary) is read its content is reset to '0'. Exception to this rule is the bit pointing to auxiliary register. This bit is only cleared when the auxiliary interrupt register is read. IRQ pin transitions to high after the interrupt bit(s) which caused its transition to high has been read. Please note that there may be more than one interrupt register bit set in case the controller did not immediately read the Interrupt registers after the IRQ signal is set and another event causing interrupt occurred.

FIFO Water Level and FIFO Status Register

The AS3953B contains a 32 byte FIFO. In case of transmitting the Control logic shifts data which was previously loaded by the external controller to the Framing Block and further to the Transmitter. During reception, the demodulated data is stored in the FIFO and the external controller can download received data.

Transmit and receive capability of the AS3953B is not limited by of the FIFO size due to a FIFO water level interrupt system. During transmission an interrupt is sent (interrupt due to FIFO water level in the Main Interrupt Register) when the content of data in the FIFO which still need to be sent is lower than the FIFO water level for transmit. The external controller can now add more data in the FIFO. The same stands for receive mode. In case the number of received bytes increases over the FIFO water level for receive an interrupt is sent to inform the external controller that data has to be downloaded from FIFO.

The external controller has to serve the FIFO faster than data is transmitted or received. A general rule is that the SCLK frequency has to be at least double than the actual data rate in receive or transmit.

FIFO water level is set to ¾ of FIFO for reception and to ¼ of FIFO for transmission. This means that in case of getting an interrupt during reception there are already 24 bytes in the FIFO, which have to be read out to liberate space for following data bytes. Same stands for transmission, water level interrupt is sent when there are 8 bytes left in FIFO, therefore up to 24 additional bytes can be loaded.

During FIFO operation (FIFO read or FIFO load) the water level detection system is blocked to avoid spurious water level interrupts (these might occur when for example number of bytes has increased above water level during loading and immediately after that dropped again below water level due to Tx process which runs in parallel). Due to this the FIFO loading/reading rate has to be higher than Tx / Rx bit rate, once FIFO loading/reading is finished the /SS pin has to be pulled to VDD (logic remains in FIFO load/read mode as long as /SS remains low).

In case loading/reading of FIFO is not much faster than Tx / Rx processes low the following two cases have to be considered:

- FIFO underflow IRQ is not blocked, in case loading in FIFO is slower than transmission process the FIFO underflow IRQ is produced.

- In case of slow FIFO loading it is possible that the content of FIFO is increased above water level but it is below when FIFO loading is finished. In such case a water level IRQ is issued after termination of FIFO loading. Same stands for FIFO reading.

- In case of slow FIFO loading it is possible that the content of FIFO stays below water level during complete FIFO loading operation. In such case water level IRQ is not issued after termination of FIFO loading. Same stands for FIFO reading.

- In case it is known that the receive data frame is smaller than the FIFO size the water level interrupt does not have to be served. In such case the water level interrupt can be masked.

- After data is received the external controller needs to know how long the receive data string was before downloading data from the FIFO: This information is available in the FIFO Status Register 1 and FIFO Status Register 2 which display number of bytes in the FIFO which were not read out.

The FIFO Status Register 2 additionally contains two bits which indicate that the FIFO was not correctly served during reception or transmission process (FIFO overflow and FIFO underflow).

FIFO overflow is set when too much data is written in FIFO. In case this bit is set during reception the external controller did not react on time on water level IRQ and more than 32 bytes were written in the FIFO. The received data is corrupted in such a case. During transmission this means that controller has written more data than FIFO size. The data to be transmitted is corrupted.

FIFO underflow is set when data was read from empty FIFO. In case this bit is set during reception the external controller read more data than was actually received. During transmission this means that controller has failed to provide the quantity of data defined in number of transmitted bytes registers on time.

ISO 14443A Frame Data in FIFO

Data in ISO 14443A frames is organized in bytes; each byte is terminated by parity bit. Data bits in a byte are numbered from *b1* to b8 where *b1* is LSB bit, LSB is sent first.

Data sent over SPI is also organized in bytes, bits in a byte are marked *D0* to *D7*, where *D0* is LSB bit, MSB is sent first.

During receive the framing engine checks the parity bit and removes it from data frame, only the data bytes are put in FIFO. During transmission the process is inversed, only the data bytes are put in FIFO, while the framing engine adds the parity bits.

The ISO 14443A data bits *b1* to *b8* are mapped to FIFO data bits *D0* to *D7*, which means that the order of receiving/transmitting bits in a byte is inversed (the ISO 14443A bytes are sent LSB first while the SPI bytes are sent MSB first).

The only exceptions to this rule are the Rx and Tx bit stream modes. In these modes the meaning of byte is lost. In order to simplify processing the order of bits is the same on ISO 14443A and FIFO side.

This means that during reception with bit *rxbs* set the first received bit is also the first bit read out of FIFO. In case the last FIFO byte is not complete the bits which are not part of received data are padded with '0'.

The same stands for transmission with bit *txbs* set: the first bit written in FIFO is also the first bit sent.

Direct Commands

Figure 51:
List of Direct Commands

Command Byte Value [hex]	Command	Comments
C2, C3	Set Default	Puts the AS3953B in default state
C4, C5	Clear	Stops all activities and clears FIFO
C8	Transmit	Starts a transmit sequence
D0	Go2halt	Puts PICC logic in HALT state

Set Default

This direct command puts the AS3953B in the same state as power-up initialization. All registers are initialized to the default state.

Clear

This direct command stops all current activities (transmission or reception) and clears FIFO.

Transmit

This direct command transmits the data stored in the FIFO. In Protocol modes it is only accepted on Level-4 of communication. Before triggering transmission using Transmit command direct command Clear has to be sent, followed by definition of number of transmitted bytes and writing data to be transmitted in FIFO.

Execution of this direct command is only enabled when the AS3953B antenna coil is in a PCD field (VP_INT is above HF_PON threshold).

Go2halt

Puts PICC logic in HALT state.

Execution of this direct command is only enabled when the AS3953B antenna coil is in a PCD field (VP_INT is above HF_PON threshold) and PICC Logic is in one of the two ISO 14443A Protocol modes.

Registers

The 6-bit register addresses below are defined in the hexadecimal notation. The possible address range is from 00h to 3Fh.

There are two types of registers implemented in the AS3953B: configuration registers and display registers. The configuration registers are used to configure the AS3953B. They can be written and read through the SPI (RW). The display registers are read only (RO); they contain information about the AS3953B internal state, which can be accessed through the SPI.

Overview of Registers

Figure 52:
List of the SPI Interface Internal Registers

Address [hex]	Content	Type
00	IO Configuration Register	RW
01	Mode Definition Register	RW
02	Bit Rate Definition Register	RW
04	RFID Status Display Register	RO
05	RATS Register	RO
08	Mask Main Interrupt Register	RW
09	Mask Auxiliary Interrupt Register	RW
0A	Main Interrupt Register	RO
0B	Auxiliary Interrupt Register	RO
0C	FIFO Status Register 1	RO
0D	FIFO Status Register 2	RO
10	Number of Transmitted Bytes Register 1	RW
11	Number of Transmitted Bytes Register 2	RW

IO Definition Register

Figure 53:
IO Configuration Register

Address# 00h : IO Configuration				Type: RW	
Bit	**Name**	**Default**	**Function**	**Comments**	
7	miso_pd2	x	**1:** Pull-down on MISO, when \SS is low and MISO is not driven by the AS3953B	
6	miso_pd1	x	**1:** Pull-down on MISO when \SS is high	
5			RFU	
4			RFU	
3			RFU	
2			RFU	
1			RFU	
0			RFU	

Note(s):

1. This register is directly supplied by VP_SPI. Its initial state is unknown.

Mode Definition Registers

Figure 54:
Mode Definition Register

Address# 01h : Mode Definition				Type: RW	
Bit	**Name**	**Default**	**Function**	**Comments**	
7			RFU		
6			RFU		
5	r_mod_1	See note (1)	**00:** ISO 14443A Level-4 Protocol mode	ISO mode in case of register control; If ISO 14443A Protocol mode is selected through registers, logic is forced in Level-4 mode.	
4	r_mod_2	See note (1)	**01:** ISO 14443A Level-3 Protocol mode **10:** Framing mode **11:** Transparent mode		
3	r_rxncrc	See note (1)	**1:** Rx – CRC is not checked, CRC part of message is also put in FIFO	Applicable in ISO 14443A Level-3 Protocol mode and Framing mode. In Protocol mode, applicable for frames which are put in FIFO.	
2	r_rxbs	See note (1)	**1:** Rx – Bit stream mode, received bits are put in FIFO (no parity and CRC check)		
1	r_txncrc	See note (1)	**1:** Tx – Do not generate CRC		
0	r_txbs	See note (1)	**1:** Tx – Bit stream mode, bits put in FIFO are sent without parity and CRC generation		

Note(s):

1. Default value is loaded from EEPROM configuration word bits *b12* to *b7* during power-up initialization.

Figure 55:
Bit Rate Definition Register

Address# 02h : Bit Rate Definition				Type: RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	tx_rate3	0	Bit rate for Tx For coding see Figure 56	
6	tx_rate2	0		
5	tx_rate1	0		
4	tx_rate0	0		
3	rx_rate3	0	Bit rate for Rx For coding see Figure 56	
2	rx_rate2	0		
1	rx_rate1	0		
0	rx_rate0	0		

Note(s):

1. Default setting is set at power-up and after **Set Default** command. In ISO 14443A Level-4 Protocol mode, this value is rewritten after receiving **PPS** command.

Figure below defines the coding of the Bit Rate.

Figure 56:
Bit Rate Coding

Rate3	Rate2	Rate1	Rate0	Bit Rate [kbit/s]	Comments
0	0	0	0	fc/128 (~106)	
0	0	0	1	fc/64 (~212)	
0	0	1	0	fc/32 (~424)	
0	0	1	1	fc/16 (~848)	
					Other combinations RFU

Note(s):

1. In case a bit rate which is not supported is selected, the Tx / Rx operation is disabled.

Display Registers

Figure 57:
RFID Status Display Register

Address# 04h : RFID Status Display			Type: R
Bit	**Name**	**Function**	**Comments**
7	hf_pon	**1:** PICC AFE is active	AFE Power-on signal
6	state<2>	**000:** POWER OFF **001:** IDLE **010:** READY 011 – ACTIVE **101:** HALT **110:** READYX **111:** ACTIVEX **100:** L4	PICC Logic state
5	state<1>		
4	state<0>		
3		RFU	
2		RFU	
1		RFU	
0		RFU	

Note(s):

1. The information read from this register can be false during reception (the logic state change during reception and the readout of status can be done just at the moment when the status is changing).

2. The RFID Status Display Register is not a real register. By reading this register, controller has access to specific RFID logic internal signals in order to observe its internal state.

Address# 05h : RATS			Type: R
Bit	**Name**	**Function**	**Comments**
7	fsdi3	RATS FSDI bits	Displays maximum frame size that PCD can handle (set by PCD in **RATS** command)
6	fsdi2		
5	fsdi1		
4	fsdi0		
3	cid3	RATS CID bits	Displays attributed CID number (set by PCD in **RATS** command)
2	cid2		
1	cid1		
0	cid0		

Note(s):

1. At power-up and after *Set Default*, content of this register is set to '0'.

2. The RATS Register is used only in ISO 14443A-4 Protocol mode. It contains information sent by PCD in **RATS** command. The register informs the controller about maximum frame size that the PCD can handle and the attributed CID number.

Interrupt Register and Associated Registers

Figure 59:
Mask Main Interrupt Register

Address# 08h : Mask Main Interrupt					Type: RW
Bit	Name	Default	Function	Comments	
7	M_pu	1	Mask power-up IRQ	This bit is set to '0' during power-up initialization in case EEPROM configuration bit *irq_pu* is set to '1'	
6	M_wu_l4	1	Mask wake-up IRQ at entry in ACTIVE(*) state	This bit is set to '0' during power-up initialization in case EEPROM configuration bit *irq_l4* is set to '1'	
5	M_wu	0	Mask wake-up IRQ triggered by sending **Wake-Up** command		
4	M_rxs	0	Mask IRQ due to start of receive		
3	M_rxe	0	Mask IRQ due to end of receive		
2	M_txe	0	Mask IRQ due to end of transmission		
1	M_wl	0	Mask IRQ due to FIFO water level		
0		0	RFU		

Note(s):

1. Default setting is set at power-up and after **Set Default** command.

Figure 60:
Mask Auxiliary Interrupt Register

Address# 09h : Mask Auxiliary Interrupt				Type: RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	M_des	0	Mask IRQ due to reception of **DESELECT** command	
6	M_er_fr	0	Mask Framing error IRQ	
5	M_er_par	0	Mask Parity error IRQ	
4	M_er_crc	0	Mask CRC error IRQ	
3	M_er_fifo	0	Mask FIFO error IRQ	
2	M_eew	0	Mask IRQ due to successful termination of EEPROM programming	
1	M_er_eew	0	Mask error during EEPROM programming IRQ	
0	M_ee_spi	0	Mask IRQ due to interruption of EEPROM access due to PICC interface activation	

Note(s):

1. Default setting is set at power-up and after **Set Default** command.

Figure 61:
Main Interrupt Register

Address# 0Ah : Main Interrupt			Type: R
Bit	**Name**	**Function**	**Comments**
7	I_pu	Power-up IRQ	
6	I_wu_l4	Wake-up IRQ at entry in ACTIVE(*) state	
5	I_wu	Wake-up IRQ triggered by sending **Wake-Up** command	
4	I_rxs	IRQ due to start of receive	Applicable when receive frame is put in FIFO
3	I_rxe	IRQ due to end of receive	Applicable when receive frame is put in FIFO
2	I_txe	IRQ due to end of transmission	Applicable when data from FIFO is sent
1	I_wl	IRQ due to FIFO water level	During receive informing that FIFO is almost full and has to be read out. During transmit informing that FIFO is almost empty and that additional data has to be send
0	I_aux	IRQ due to event displayed in the Auxiliary Interrupt Register	

Note(s):

1. At power-up and after **Set Default** command, content of this register is set to '0'.

2. After Main Interrupt Register is read, with the exception of bit0, the register content is set to '0'. The bit0 is set to '0' only after the corresponding interrupt register is read.

Figure 62:
Auxiliary Interrupt Register

Address# 0Bh : Auxiliary Interrupt			Type: R
Bit	**Name**	**Function**	**Comments**
7	I_des	IRQ due to reception of **DESELECT** command	
6	I_er_fr	Framing error	
5	I_er_par	Parity error	In case of parity or/and CRC error the receive data is still put in FIFO, error IRQ is additionally send.
4	I_er_crc	CRC error	
3	I_er_fifo	FIFO error (overflow/underflow)	See FIFO Status Register 2
2	I_eew	IRQ due to successful termination of EEPROM programming	In case **EEPROM write** command was sent through SPI
1	I_er_eew	Error during EEPROM programming (writing to write protected word, writing to nonexistent address)	In case **EEPROM write** command was sent through SPI
0	I_ee_spi	IRQ due to interruption of EEPROM access due to PICC interface activation	

Note(s):

1. At power-up and after **Set Default** command content of this register is set to 0.

2. After Auxiliary Interrupt Register has been read its content is set to 0.

Figure 63:
FIFO Status Register 1

Address# 0Ch : FIFO Status 1			Type: R
Bit	**Name**	**Function**	**Comments**
7		RFU	
6		RFU	
5	fifo_b5	Number of data bytes (binary coded) in the FIFO which were not read out	Valid range is from 000000 to 100000 000000 means that there are no data bytes to be read out
4	fifo_b4		
3	fifo_b3		
2	fifo_b2		
1	fifo_b1		
0	fifo_b0		

Note(s):

1. At power-up and after direct commands **Set Default** and **Clear** content of this register is set to 0.

Figure 64:
FIFO Status Register 2

Address# 0Dh: FIFO Status 2			Type: R
Bit	**Name**	**Function**	**Comments**
7		RFU	
6	fifo_unf	FIFO underflow	Set when more bytes than the actual content of FIFO are read
5	fifo_ovr	FIFO overflow	
4	fifo_ncp	Last FIFO byte is not complete	
3	fifo_lb2	Number of bits in last FIFO byte in case it was not complete (fifo_npc=1)	MSB bits valid
2	fifo_lb1		
1	fifo_lb0		
0	np_lb	Parity bit is missing in last byte	This is a framing error

Note(s):

1. At power-up and after direct commands **Set Default** and **Clear** content of this register is set to 0.

Definition of Number of Transmitted Bytes

Figure 65:
Number of Transmitted Bytes Register 1

Address# 10h : Number of Transmitted Bytes 1				Type: RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RFU			
6	RFU			
5	RFU			
4	ntx9	0	Number of full bytes to be transmitted in one command, MSB bits	Maximum supported number of bytes is 1023
3	ntx8	0		
2	ntx7	0		
1	ntx6	0		
0	ntx5	0		

Note(s):

1. Default setting is set at power-up and after **Set Default** command.

Figure 66:
Number of Transmitted Bytes Register 2

Address# 11h: Number of Transmitted Bytes 2				Type: RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	ntx4	0	Number of full bytes to be transmitted in one command, LSB bits	Maximum supported number of bytes is 1023
6	ntx3	0		
5	ntx2	0		
4	ntx1	0		
3	ntx0	0		
2	nbtx2		Number of bits in the split byte 000 means that all bytes all full	Applicable in Level-3 Protocol mode in case configuration bit *txbs* is set (bit stream Tx) Framing mode
1	nbtx1			
0	nbtx0			

Note(s):

1. Default setting is set at power-up and after **Set Default** command.

Package Drawings & Markings

Figure 67:
Thin WL-CSP 10-Bumps Package Diagram

Top through view   Bottom view (Ball side)
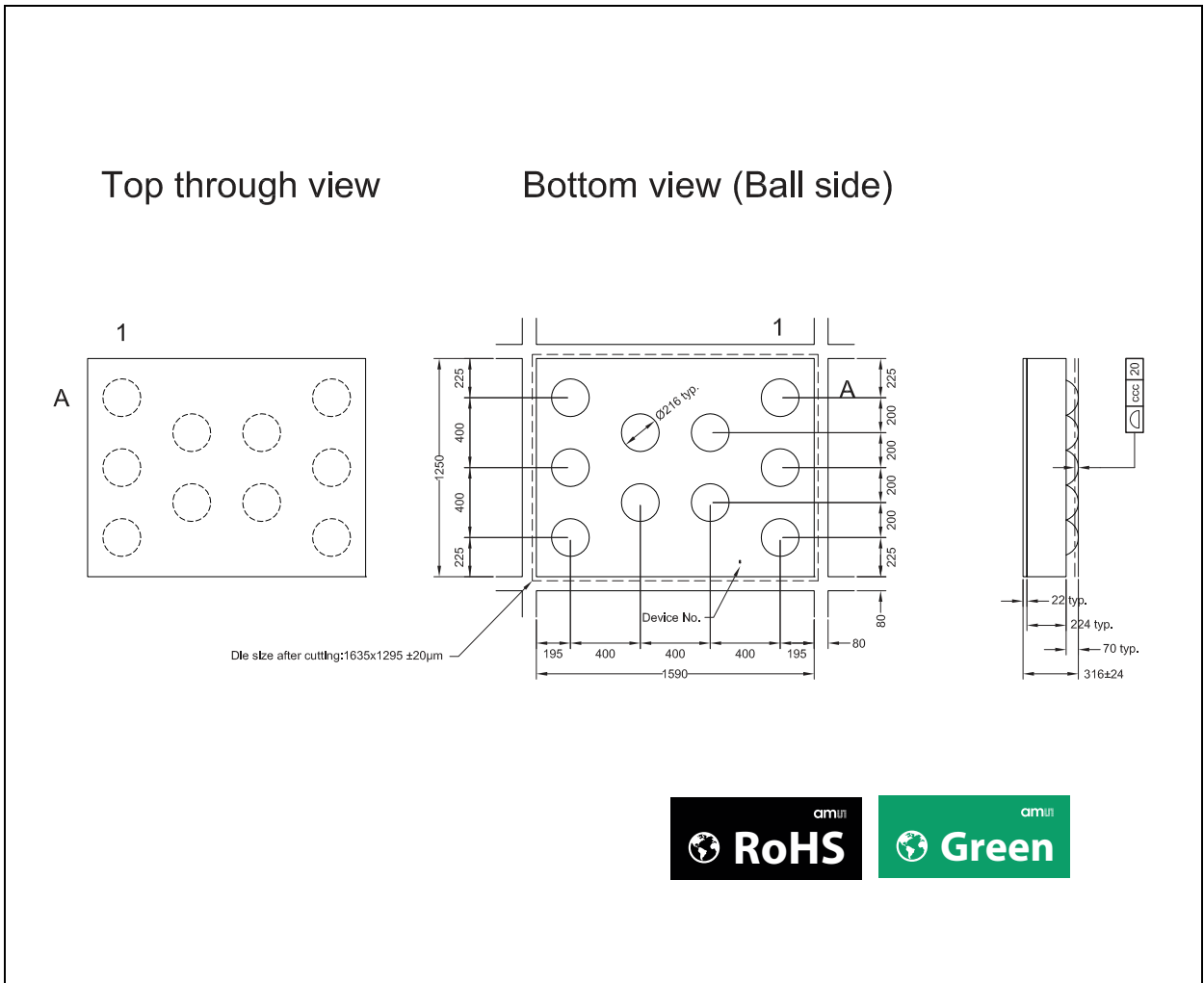
Note(s):

1. Pin1=A1.

2. ccc coplanarity.

3. All dimensions are in m.

Figure 68:
Package Marking
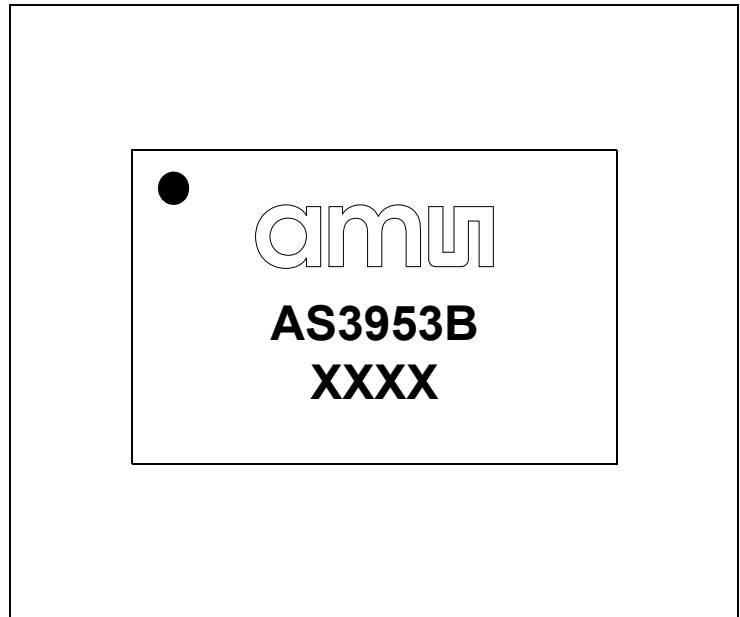
Figure 69:
Package Code

XXXX
Tracecode
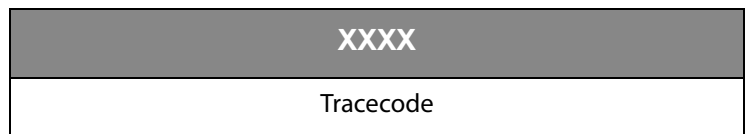
Ordering & Contact Information

The devices are available as standard products shown in figure below.

Figure 70:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS3953B-BTWM	Thin WL-CSP	AS3953B	Mini Reel	1000 pcs/reel
AS3953B-BTWT	Thin WL-CSP	AS3953B	Tape & Reel	12000 pcs/reel
AS3953B-BSWB	Sorted Wafer	NA	Wafer Box	

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Revision Information

Changes from 1.1 to current revision 1-04 (2016-Jan-07)	Page
1.1 to 1-02 (2015-Nov-20)	
Content was updated to the latest **ams** design	
Added benefits to the Key Features	2
Updated Figure 4	4
Updated Figure 9	8
Added Package Drawings & Markings section	56
Updated Figure 68	58
1-02 (2015-Nov-20) to 1-03 (2015-Nov-24)	
Updated Figure 5	5
Updated text under Figure 33	24
Updated text under ISO 14443A Level-3 Protocol Mode	25
1-03 (2015-Nov-24) to 1-04 (2016-Jan-07)	
Updated Figure 67	56

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.

2. Correction of typographical errors is not explicitly mentioned.

Content Guide