CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX655D/CMX655A
Ultra Low Power Voice Codec

D/655/3 October 2018 Provisional

Features

- Analogue and digital microphone support
- High efficiency Class-D amplifier
- Ultra Low power consumption
- 16 bit audio data
- Supports conventional telephony and HD voice (300Hz - 3.4kHz and 50Hz -7kHz bandwidths)
- Supports audio bandwidths up to 21kHz
- Supports 8/16/32/48 ksps sample rates
- Flexible serial audio interface
- SPI™/TWI control interface[1]
- Small 24-lead VQFN Package

Applications

- Security alarm panels
- Glass break detection
- Intercom and access systems
- Mobile radio and accessories
- Wired telephony
- Voice controlled equipment

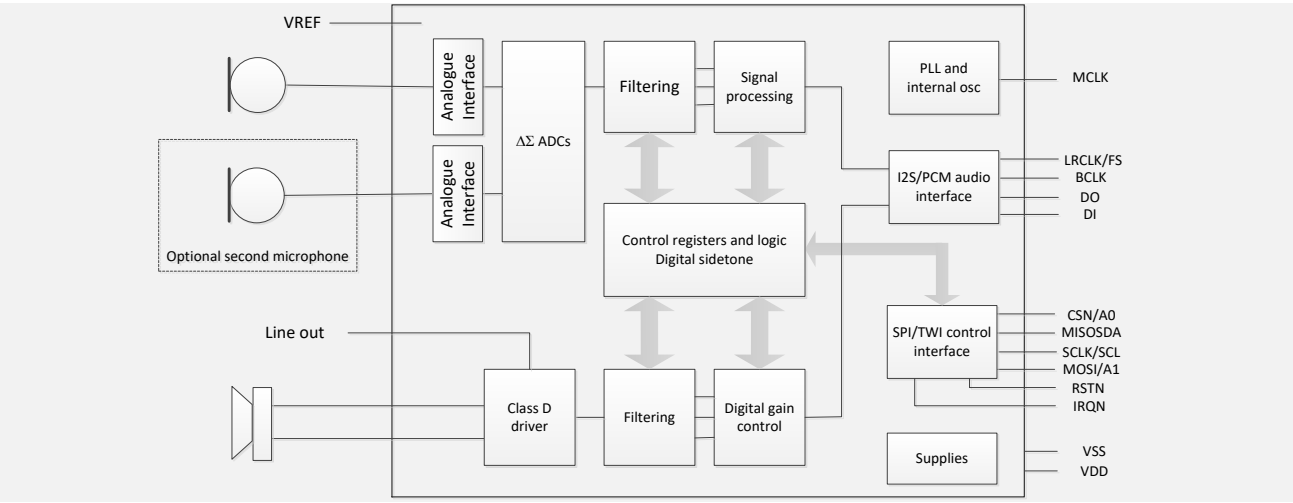

Figure 1 CMX655A Simplified Block Diagram

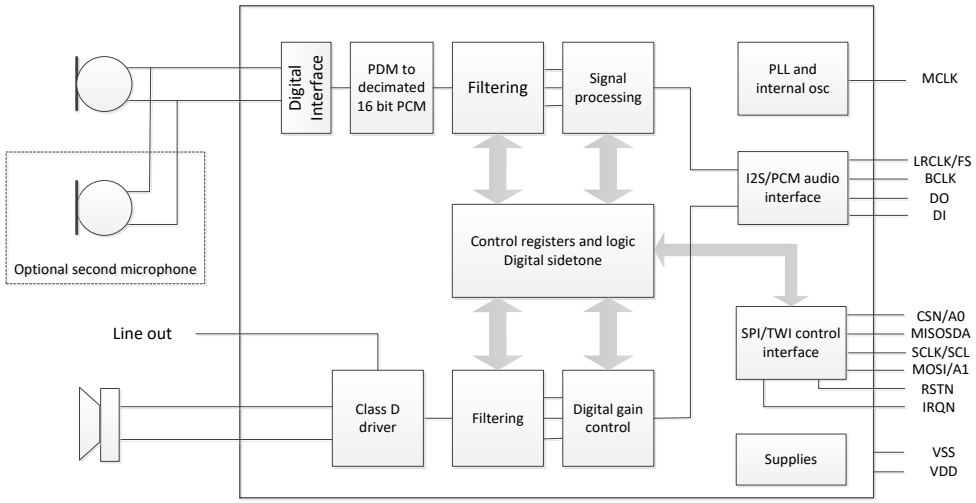

Figure 2 CMX655D Simplified Block Diagram

[1] SPI™ is a trademark of Motorola Inc.

1 Brief Description

Traditionally audio codecs have interfaced to electret microphones and speakers providing A-to-D and D-to-A functions using precision oversampling data converters. Recent advances in microphone design using MEMS techniques are now changing this, along with higher efficiency speaker drivers such as Class-D topologies. Both of these advances enable significant reductions in power consumption which is needed to address new applications such as voice control, that require 'always-on' operation. Such applications are often battery powered, driving the need for minimal power consumption. The CMX655D and CMX655A address these needs providing an update to the traditional audio codec that is both very low power and small in size.

The CMX655D has a digital microphone interface that connects single or dual microphones to the device and the same parallel processing streams.

The CMX655A has two independent input channels that support analogue microphones, with parallel processing of each data stream to maintain phase alignment between the two channels. The device supports programmable on-chip filtering, with digital gain control and an AGC function.

A 1-Watt mono Class-D amplifier drives differential audio outputs for a filterless speaker. A separate single-ended analogue lineout is also provided for a headphone. The Class-D amplifier features programmable filtering and digital gain control. This architecture operates with far higher efficiency than conventional speaker drivers.

The device interfaces via standard serial busses that are commonly found on many microcontrollers, DSPs and low cost radio transceivers.

Note that text shown in pale grey indicates features that will be available in future versions of the device.

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History

Version	Changes	Date
1	Document title changed to “CMX655D/CMX655A Ultra Low-Power Codec” Section 7.2 – Typical Performance Characteristics graphs added Section 5.6.7 – Automatic Level Control: description and associated register tables “greyed out” pending further revision	8th August 2018
2	Revised performance figures	3rd September 2018
3	First public release	19th October 2018

This is Provisional Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.

2 Block Diagram

2.1 CMX655A

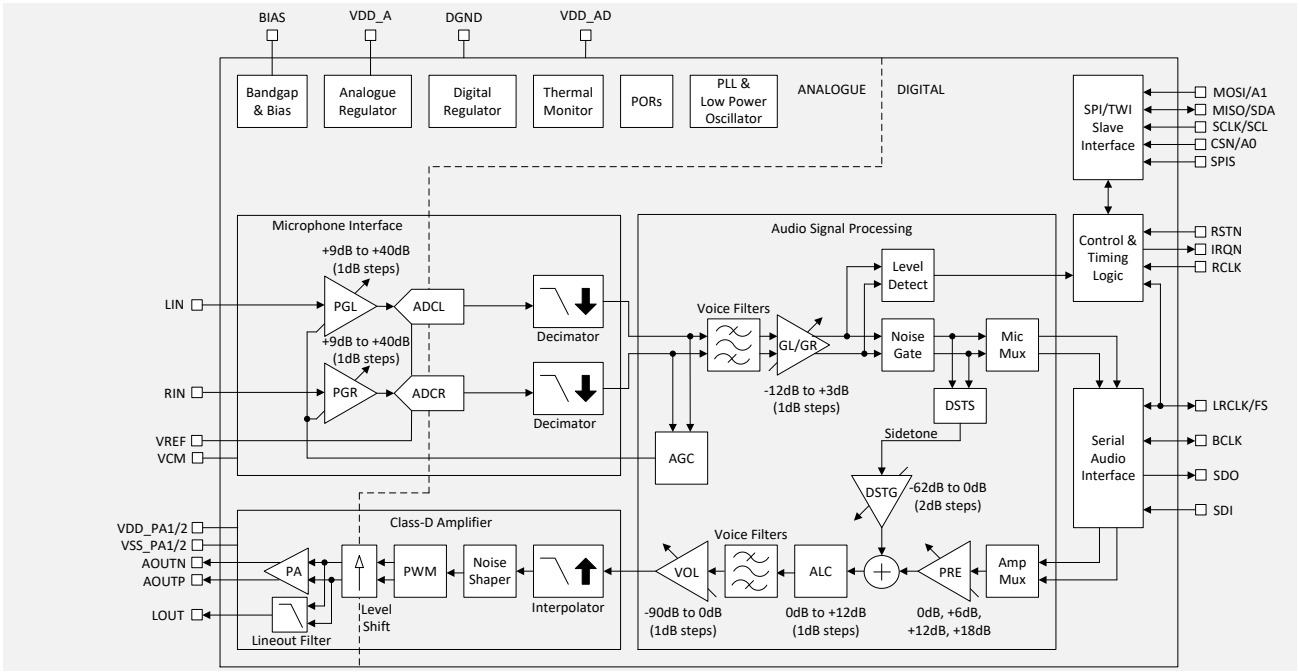


Figure 3 CMX655A Block Diagram

2.2 CMX655D

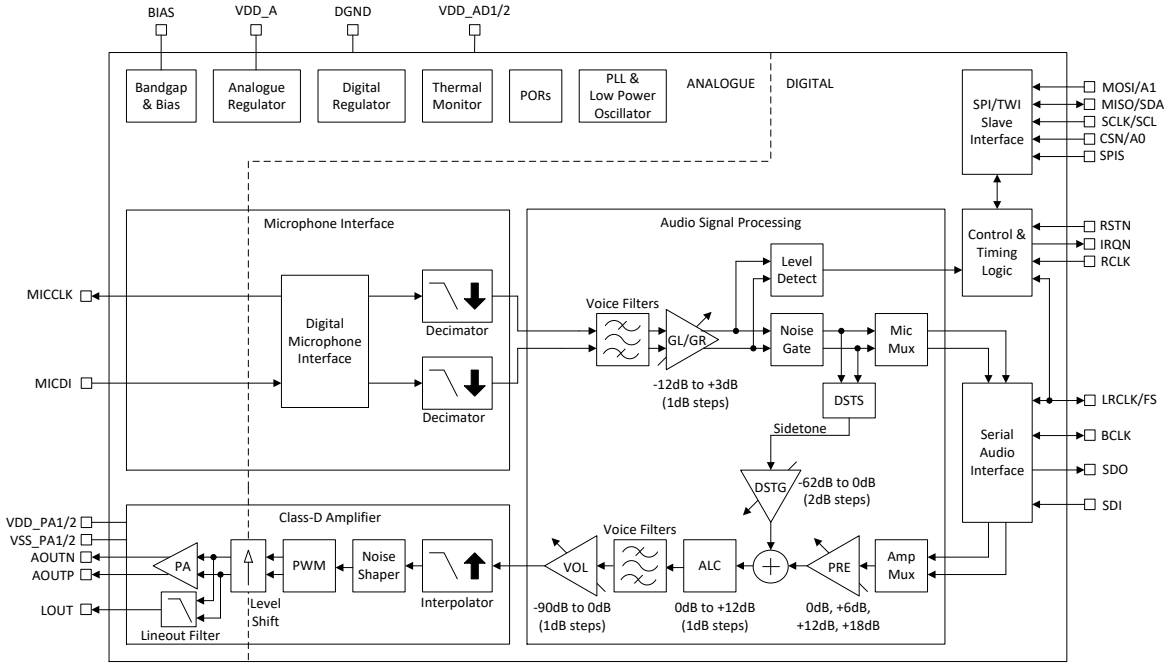


Figure 4 CMX655D Block Diagram

3 Pin List

3.1 CMX655A

Table 1 CMX655A Pin List by Number

Pin No.	Pin Name	Type	Pin Function
1	AOUTN	AO	Class-D Amplifier Output Negative
2	VDD_PA	VDD	Class-D Supply: 2.7-3.6V (high current)
3	LOUT	AO	Lineout
4	VDD_A	AO	1.2V Regulator Decouple
5	BIAS	AO	Bias Current Resistor
6	VCM	AO	Common Mode Voltage Decouple
7	VREF	AO	ADC Reference Voltage Decouple
8	LIN	AI	Analogue Microphone Left Input
9	RIN	AI	Analogue Microphone Right Input
10	VDD_AD	VDD	Analogue/Digital Supply 2.7-3.6V (1.75-3.6V if VDD_PA unused)
11	RSTN	DI	Active Low Reset
12	RCLK	DI	PLL Reference/Main clock
13	LRCLK/FS	DIO	Left-Right Clock/PCM Frame Sync/PLL Reference
14	SDI	DI	Serial Audio Data Input
15	SDO	DO	Serial Audio Data Output
16	BCLK	DIO	Serial Audio Data Clock
17	SPIS	DI	SPI Select: 0=TWI, 1=SPI
18	IRQN	DO	Active Low Interrupt. Open-drain – connect to VDD_AD via pull up
19	SCLK/SCL	DI	SPI SCLK/TWI SCL
20	MISO/SDA	DIO	SPI MISO/TWI SDA
21	MOSI/A1	DI	SPI MOSI/TWI A1
22	CSN/A0	DI	SPI CSN/TWI A0
23	AOUTP	AO	Class-D Amplifier Output Positive
24	VSS_PA	GND	Class-D Ground
PADDLE	DGND	GND	Digital and Analogue Ground

AIO	Analogue Input / Output	DIO	Digital Input / Output
AI	Analogue Input	DI	Digital Input
AO	Analogue Output	DO	Digital Output
VDD	Supply	GND	Ground

Table 2 CMX655A Pin List by Group

Number	Name	Type	Function
Power			
2	VDD_PA	VDD	Class-D Supply: 2.7-3.6V (high current)
4	VDD_A	VDD	1.2V Analogue Regulator Decouple
10	VDD_AD	VDD	Analogue/Digital Supply 2.7-3.6V (1.75-3.6V if VDD_PA unused)
24	VSS_PA	GND	Class-D Ground
PADDLE	DGND	GND	Digital and Analogue Ground
Reference and Bias			
5	BIAS	AI	Bias Current Resistor
6	VCM	AO	Common Mode Voltage Decouple
7	VREF	AO	ADC Reference Voltage Decouple
Class-D Amplifier Outputs			
1	AOUTN	AO	Class-D Amplifier Output Negative
3	LOUT	AO	Lineout
23	AOUTP	AO	Class-D Amplifier Output Positive
Microphone Interface			
8	LIN	AI	Analogue Microphone Left Input
9	RIN	AI	Analogue Microphone Right Input
General System & Control			
11	RSTN	DI	Active Low Reset
12	RCLK	DI	PLL Reference/Main clock
18	IRQN	DO	Active Low Interrupt. Open-drain - connect to VDD_AD via pull-up
Control Interface			
17	SPIS	DI	SPI Select: 0=TWI, 1=SPI
19	SCLK/SCL	DI	SPI SCLK/TWI SCL
20	MISO/SDA	DIO	SPI MISO/TWI SDA
21	MOSI/A1	DI	SPI MOSI/TWI A1
22	CSN/A0	DI	SPI CSN/TWI A0
Serial Audio Interface			
13	LRCLK/FS	DIO	Left-Right Clock/PCM Frame Sync/PLL Reference
14	SDI	DI	Serial Audio Data Input
15	SDO	DO	Serial Audio Data Output
16	BCLK	DIO	Serial Audio Data Clock

AIO	Analogue Input / Output	DIO	Digital Input / Output
AI	Analogue Input	DI	Digital Input
AO	Analogue Output	DO	Digital Output
VDD	Supply	GND	Ground

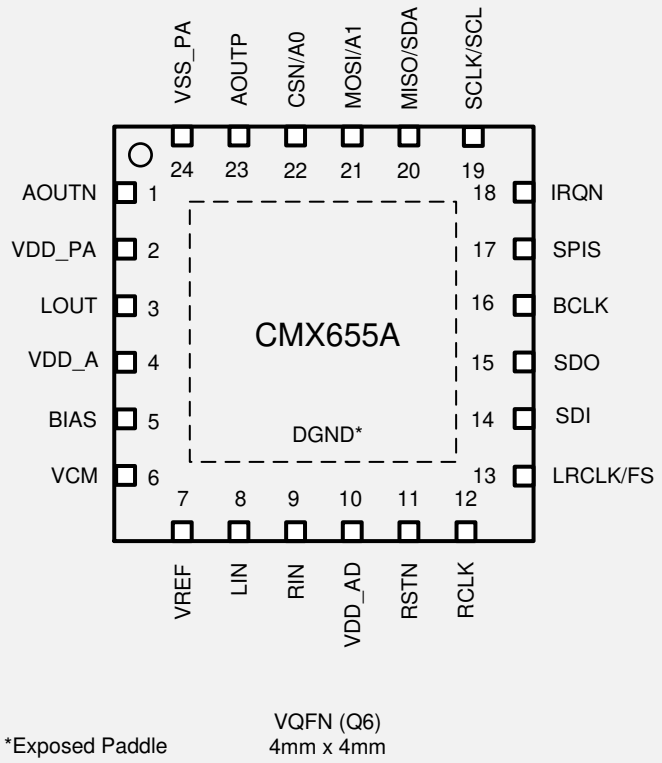


Figure 5 CMX655A Pin Arrangement

3.2 CMX655D

Table 3 CMX655D Pin List by Number

Number	Name	Type	Function
1	AOUTN	AO	Class-D Amplifier Output Negative
2	VDD_PA	VDD	Class-D Supply: 2.7-3.6V (high current)
3	LOUT	AO	Lineout
4	VDD_A	VDD	1.2V Regulator Decouple
5	BIAS	AO	Bias Current Resistor
6	NC1	NC	No Connection
7	VDD_AD1	VDD	Analogue/Digital Supply 2.7-3.6V (1.75-3.6V if VDD_PA unused)
8	VDD_AD2	VDD	Analogue/Digital Supply 2.7-3.6V (1.75-3.6V if VDD_PA unused)
9	RSTN	DI	Active Low Reset
10	MICCLK	DO	Digital Microphone Clock Output
11	MICDI	DI	Digital Microphone Data Input
12	RCLK	DI	PLL Reference/Main clock
13	LRCLK/FS	DIO	Left-Right Clock/PCM Frame Sync/PLL Reference
14	SDI	DI	Serial Audio Data Input
15	SDO	DO	Serial Audio Data Output
16	BCLK	DIO	Serial Audio Data Clock
17	SPIS	DI	SPI Select: 0=TWI, 1=SPI
18	IRQN	DO	Active Low Interrupt. Open-drain – connect to VDD_AD via pull up
19	SCLK/SCL	DI	SPI SCLK/TWI SCL
20	MISO/SDA	DIO	SPI MISO/TWI SDA
21	MOSI/A1	DI	SPI MOSI/TWI A1
22	CSN/A0	DI	SPI CSN/TWI A0
23	AOUTP	AO	Class-D Amplifier Output Positive
24	VSS_PA	GND	Class-D Ground
PADDLE	DGND	GND	Digital and Analogue Ground

AIO	Analogue Input / Output	DIO	Digital Input / Output
AI	Analogue Input	DI	Digital Input
AO	Analogue Output	DO	Digital Output
NC	Not Connected	VDD	Supply
GND	Ground		

Table 4 CMX655D Pin List by Group

Number	Name	Type	Function
Power			
2	VDD_PA	VDD	Class-D Supply: 2.7-3.6V (high current)
4	VDD_A	VDD	1.2V Analogue Regulator Decouple
7	VDD_AD1	VDD	Analogue/Digital Supply 2.7-3.6V (1.75-3.6V if VDD_PA unused)
8	VDD_AD2	VDD	Analogue/Digital Supply 2.7-3.6V (1.75-3.6V if VDD_PA unused)
24	VSS_PA	GND	Class-D Ground
PADDLE	DGND	GND	Digital and Analogue Ground
Reference and Bias			
5	BIAS	AI	Bias Current Resistor
Class-D Amplifier Outputs			
1	AOUTN	AO	Class-D Amplifier Output Negative
3	LOUT	AO	Lineout
23	AOUTP	AO	Class-D Amplifier Output Positive
Microphone Interface			
10	MICCLK	DO	Digital Microphone Clock Output
11	MICDI	DI	Digital Microphone Data Input
General System & Control			
9	RSTN	DI	Active Low Reset
12	RCLK	DI	PLL Reference/Main clock
18	IRQN	DO	Active Low Interrupt. Open-drain - connect to VDD_AD via pull-up
Control Interface			
17	SPIS	DI	SPI Select: 0=TWI, 1=SPI
19	SCLK/SCL	DI	SPI SCLK/TWI SCL
20	MISO/SDA	DIO	SPI MISO/TWI SDA
21	MOSI/A1	DI	SPI MOSI/TWI A1
22	CSN/A0	DI	SPI CSN/TWI A0
Serial Audio Interface			
13	LRCLK/FS	DIO	Left-Right Clock/PCM Frame Sync/PLL Reference
14	SDI	DI	Serial Audio Data Input
15	SDO	DO	Serial Audio Data Output
16	BCLK	DIO	Serial Audio Data Clock

AIO	Analogue Input / Output	DIO	Digital Input / Output
AI	Analogue Input	DI	Digital Input
AO	Analogue Output	DO	Digital Output
NC	Not Connected	VDD	Supply
GND	Ground		

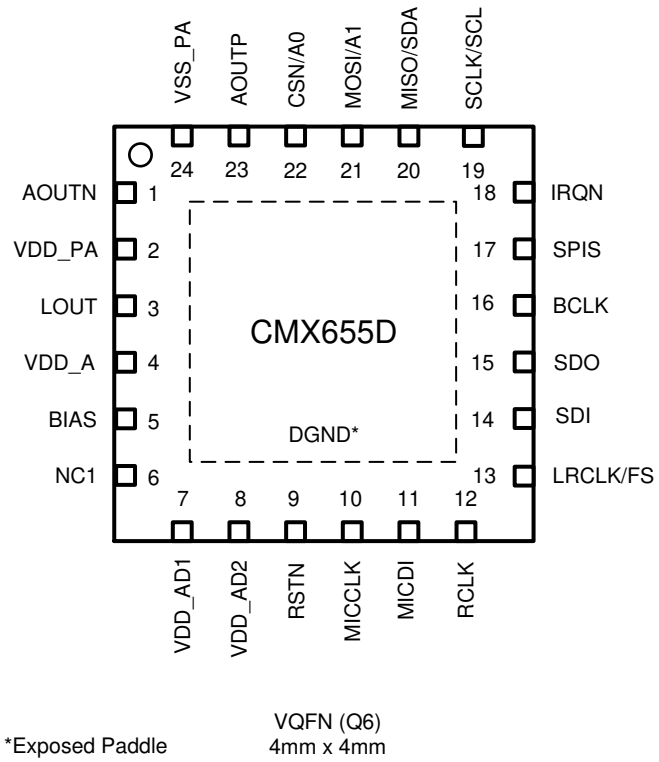


Figure 6 CMX655D Pin Arrangement

4 External Components

4.1 CMX655A

4.1.1 Power Supply and Pin Decoupling

The CMX655A has two supply pins, VDD_AD and VDD_PA, which should be connected to the same nominal supply voltage of 3V. If the Class-D amplifier is not required, VDD_PA may be disconnected from the supply and connected to ground allowing VDD_AD to operate from a minimum supply voltage of 1.75V.

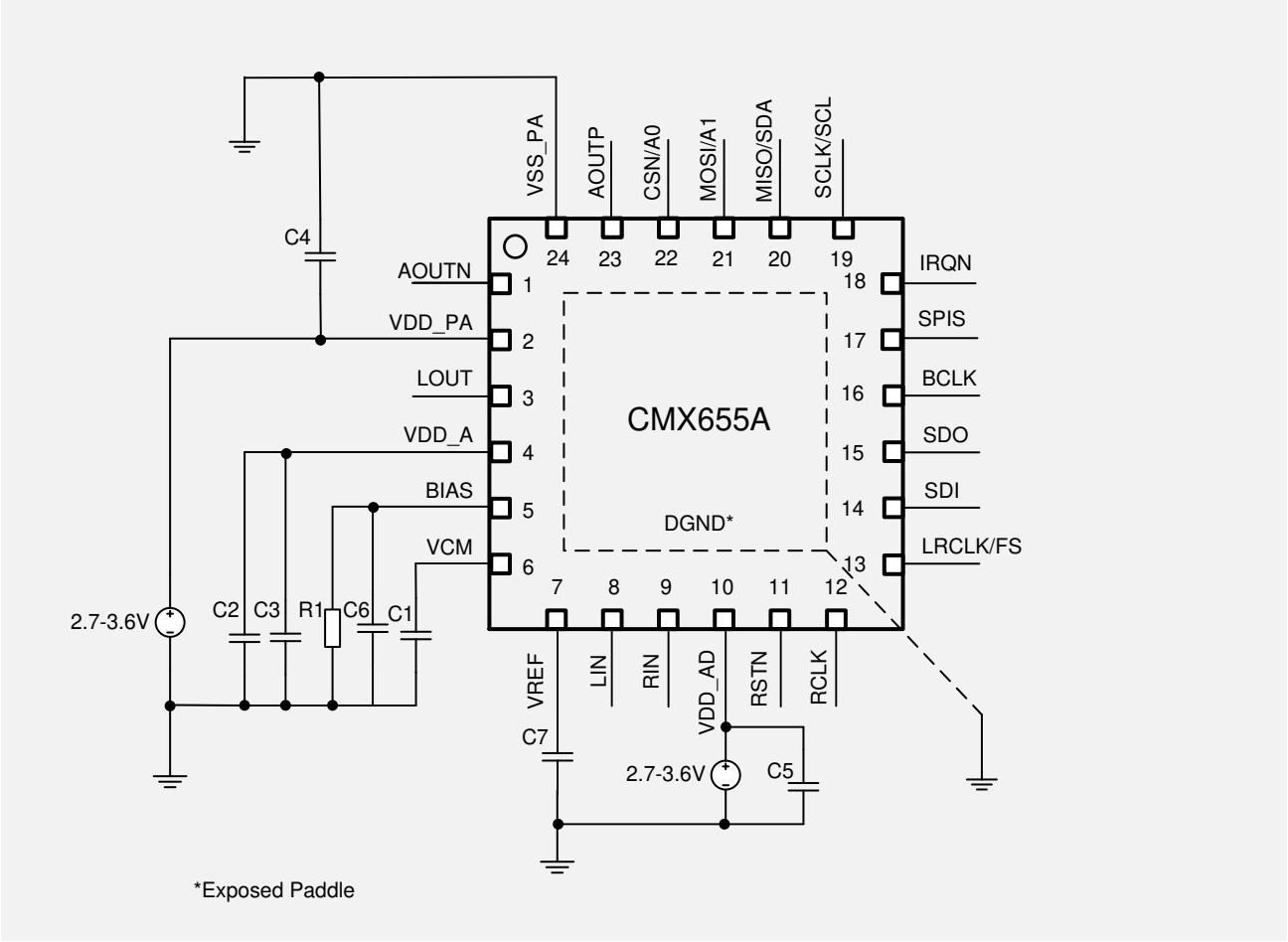


Figure 7 CMX655A Power Supply and Pin Decoupling

Table 5 CMX655A Component Values

C1	10nF
C2	100nF
C3	100pF
C4	10nF
C5	10nF
C6	10pF
C7	100nF
R1	60kΩ

Capacitors ±5%, Resistors ±1%

4.1.2 SPI

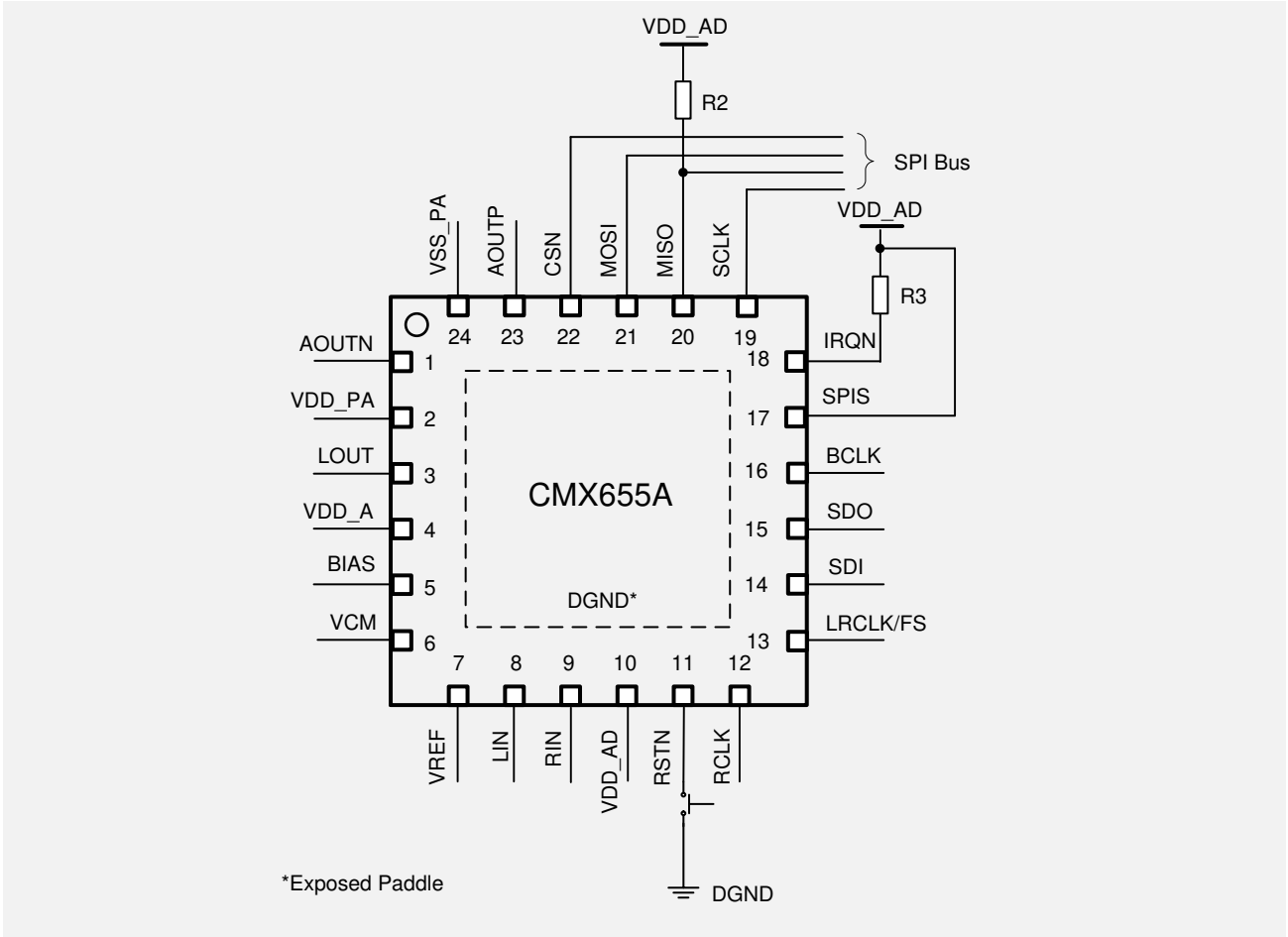


Figure 8 CMX655A SPI Connections

Table 6 CMX655A SPI Component Values

R2	10kΩ
R3	47kΩ

Resistors ±1%

4.1.3 TWI

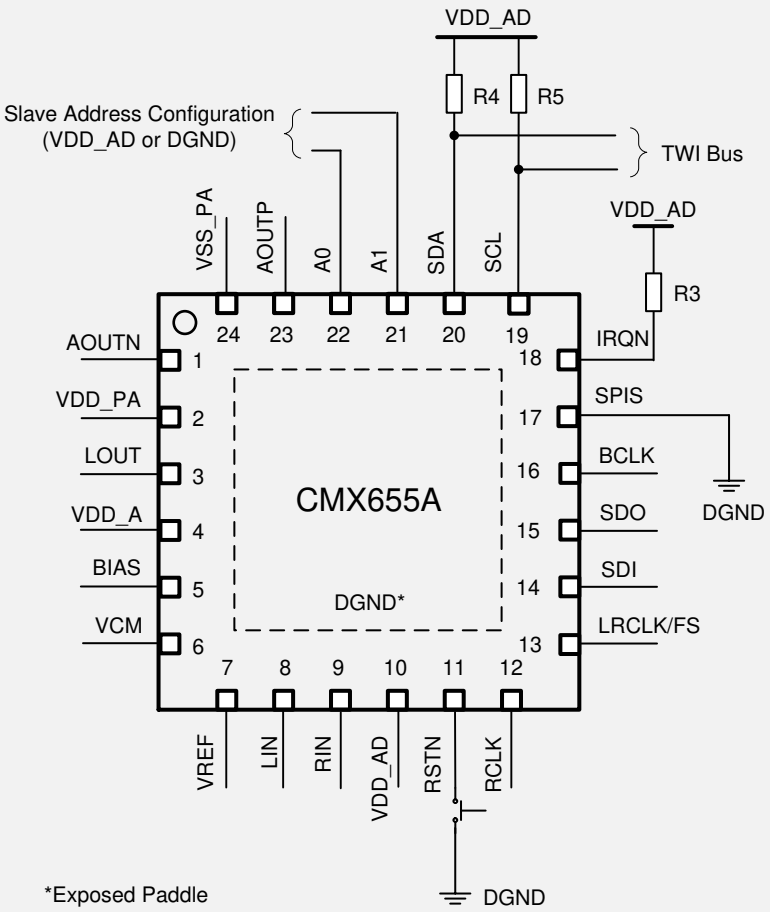


Figure 9 CMX655A TWI Connections

Table 7 CMX655A TWI Component Values

R3	47kΩ
R4	R_p
R5	R_p

Resistors ±1%

The value of R_p is given in Table 20.

4.1.4 Speaker and Microphone

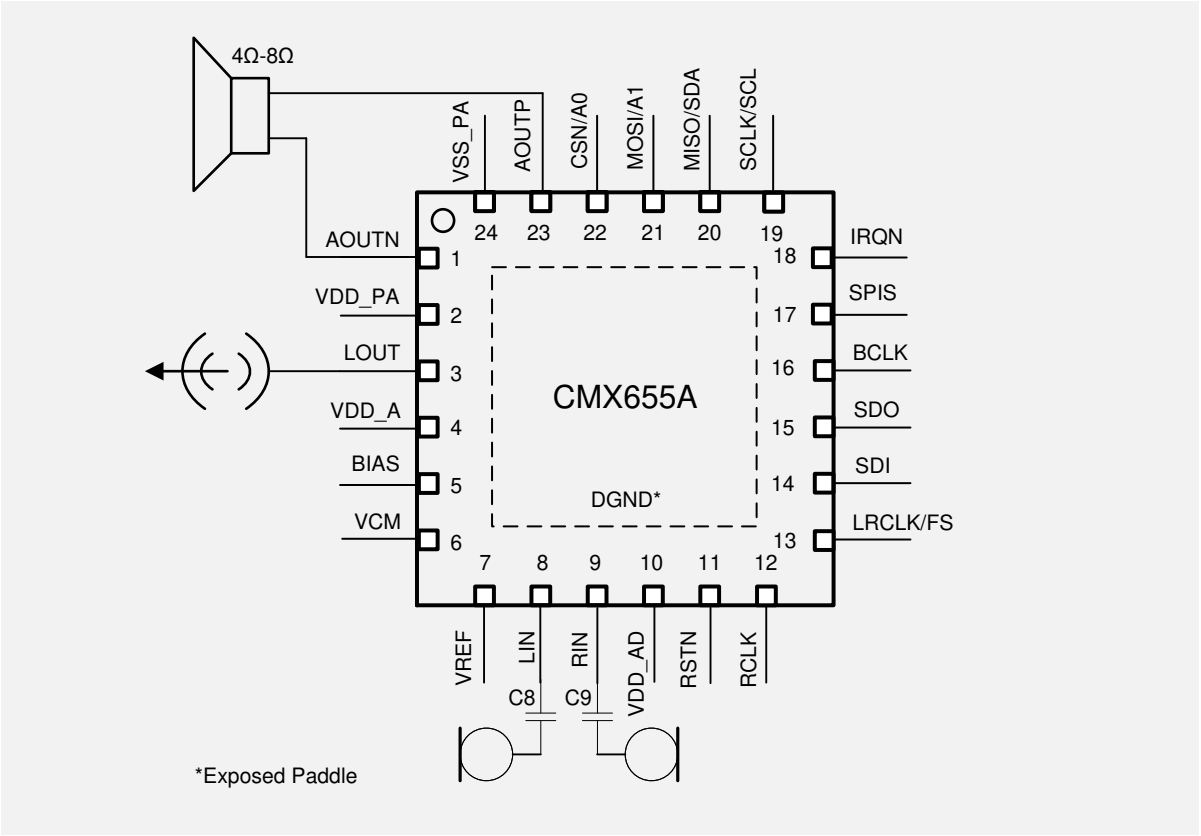


Figure 10 CMX655A Speaker and Microphone Connections

Table 8 CMX655A AC Coupling Component Values

C8	390nF
C9	390nF

Capacitors ±5%

4.2 CMX655D

4.2.1 Power Supply and Pin Decoupling

The CMX655B has two supply pins, VDD_AD and VDD_PA, which should be connected to the same nominal supply voltage of 3V. If the Class-D amplifier is not required, VDD_PA may be disconnected from the supply and connected to ground allowing VDD_AD to operate from a minimum supply voltage of 1.75V.

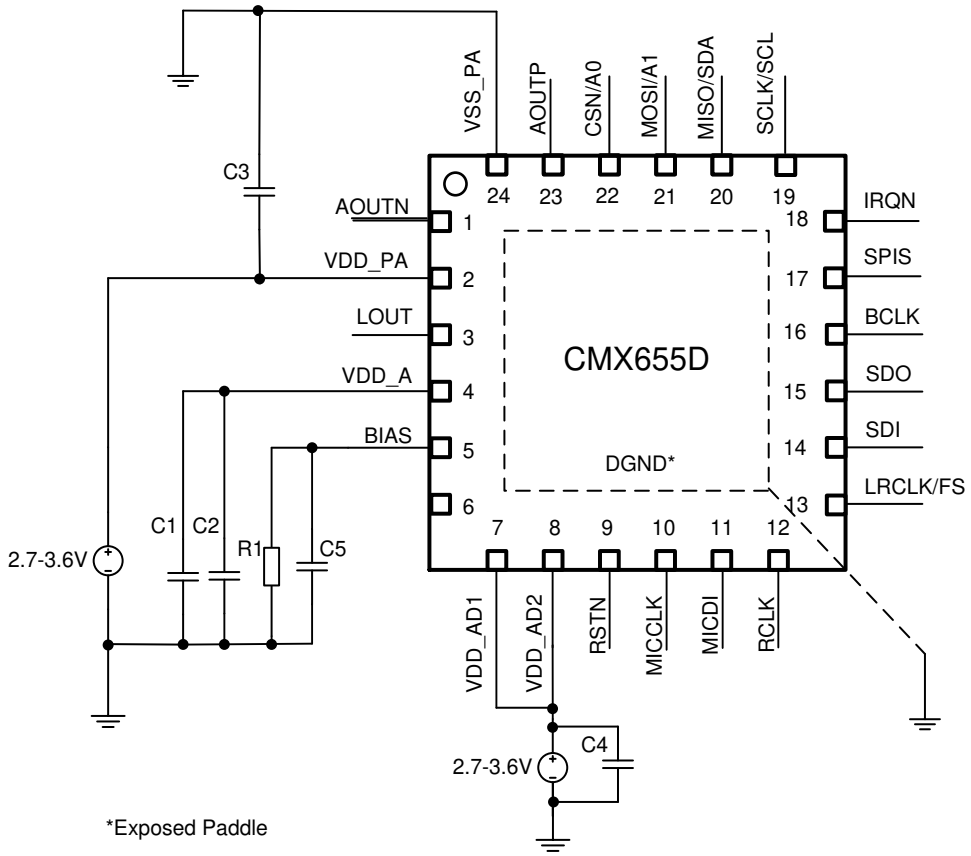


Figure 11 CMX655D Power Supply and Pin Decoupling

Table 9 CMX655D Component Values

C1	100nF
C2	100pF
C3	10nF
C4	10nF
C5	10pF
R1	60kΩ

Capacitors ±5%, Resistors ±1%

4.2.2 SPI

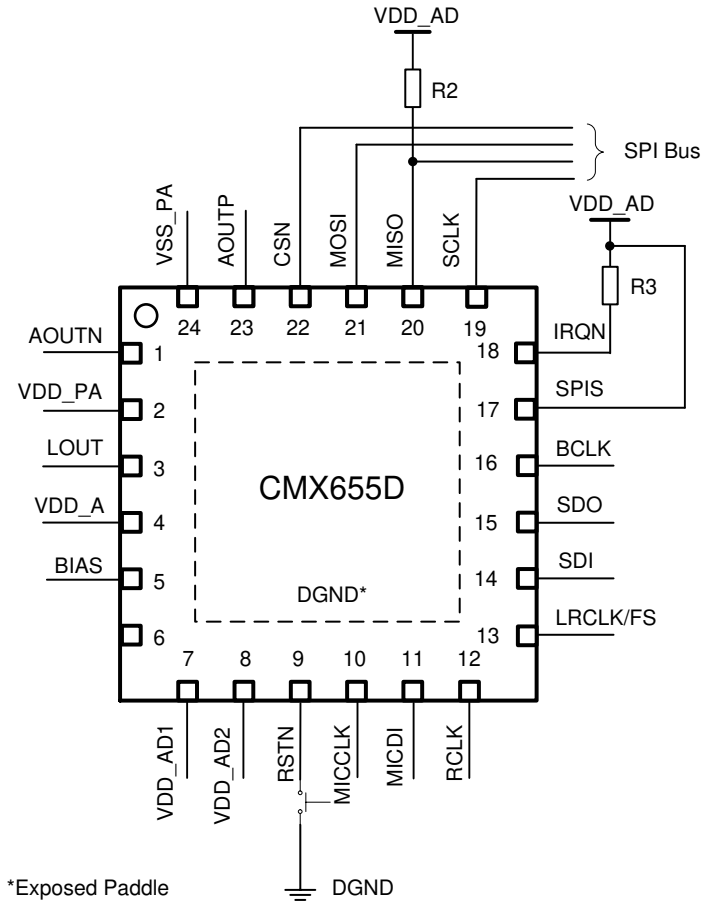


Figure 12 CMX655D SPI Connections

Table 10 CMX655D SPI Component Value

R2	10kΩ
R3	47kΩ

Resistors ±1%

4.2.3 TWI

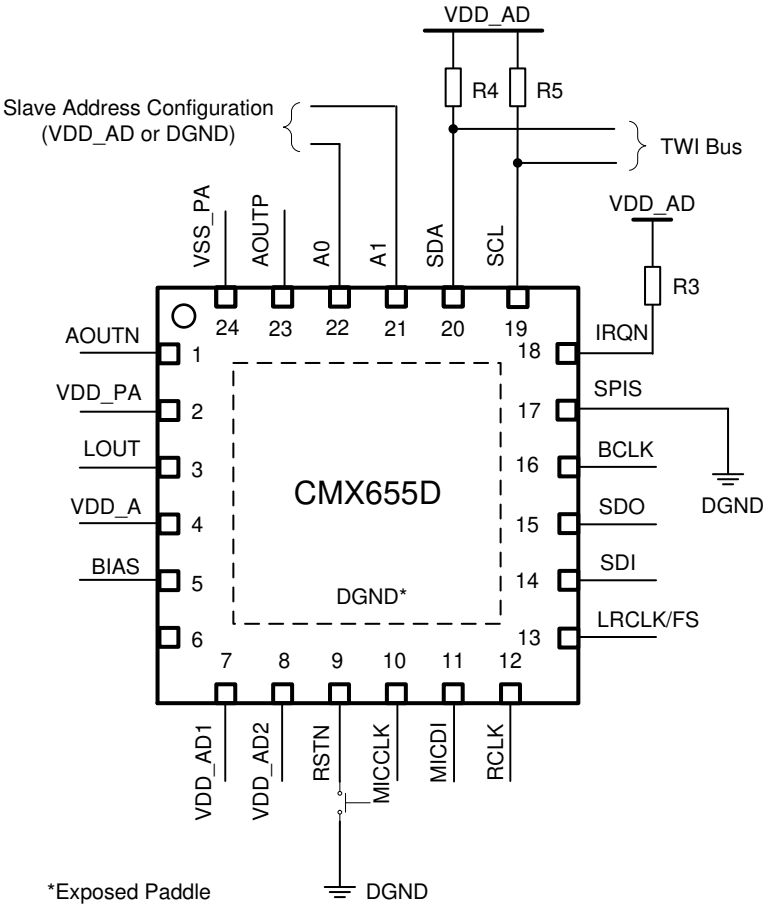


Figure 13 CMX655D TWI Connections

Table 11 CMX655D TWI Component Values

R3	47kΩ
R4	R_p
R5	R_p

Resistors ±1%

The value of R_p is given in Table 20.

4.2.4 Speaker and Microphone

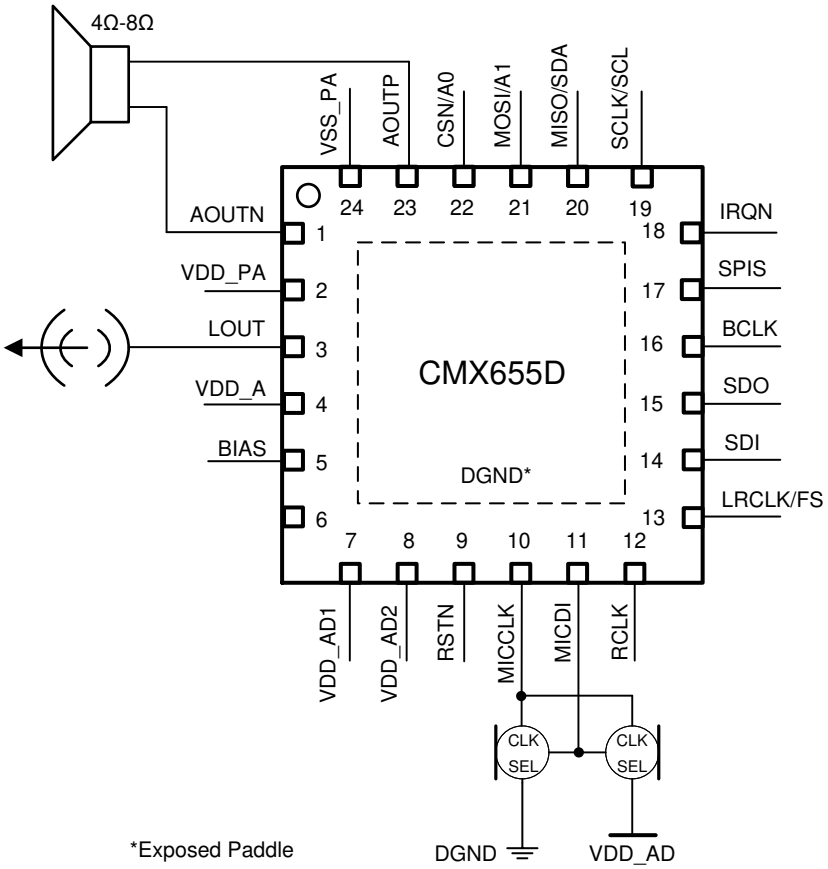


Figure 14 CMX655D Speaker and Microphone Connections

5 General Description

5.1 Power Management

5.1.1 External Supplies

The external unregulated supplies required by the CMX655D/CMX655A are VDD_AD connected to the VDD_AD pin and VDD_PA connected to the VDD_PA1 pin. The VDD_PA2 pin on the 28-pin part should also be connected to the VDD_PA supply. The power amplifier analogue ground pin is VSS_PA1. The VSS_PA2 pin on the 28-pin part should also be connected to analogue ground. The exposed paddle on the underside of the package is the digital and analogue ground.

VDD_PA solely powers the Class-D power-amplifier output stage that drives the AOUTN and AOUTP pins. VDD_AD powers the Class-D lineout output stage and the remaining analogue and digital circuits.

When the CMX655D/CMX655A Class-D power-amplifier is in use, the VDD_PA and VDD_AD supplies must operate at the same voltage between 2.7-3.6V. If the CMX655D/CMX655A Class-D power-amplifier is not required, the VDD_PA supply may be connected to analogue ground and the VDD_AD supply may operate between 2.7V-3.6V. If both the Class-D power-amplifier and lineout are not required, the VDD_AD supply may operate between 1.75-3.6V, see Table 10 below.

Table 12 External Supply Voltages

Class-D PA In Use	Class-D Lineout In Use	VDD_AD	VDD_PA
Yes	Yes	2.7 to 3.6V	Same as VDD_AD
Yes	No	2.7 to 3.6V	Same as VDD_AD
No	Yes	2.7 to 3.6V	Not Required
No	No	1.75 to 3.6V	Not Required

5.1.2 Regulated Supplies

The CMX655D/CMX655A contains integrated voltage regulators powered from VDD_AD that generate 1.2V regulated supply rails for the digital (VDD_D) and analogue (VDD_A) circuits in the device. The regulated analogue supply rail is externally decoupled via the VDD_A pin.

5.2 Device Reset

The CMX655D/CMX655A device reset is activated by the integrated power-on-reset (POR) generator on the VDD_D voltage domain and the active low reset pin RSTN. The CMX655D/CMX655A SPI/TWI interface must not be accessed and remain in their idle state while the device reset is in progress.

5.2.1 Power-On-Reset

The CMX655D/CMX655A POR voltage thresholds are listed in Table 13.

Table 13 Supply and POR Threshold Voltages

Supply	Nominal Voltage (V)	POR Voltage (V)
VDD_A	1.2	0.93
VDD_D	1.2	0.93

The reset signal produced by each POR generator is asserted within 1µs of the power-on-reset threshold voltage being exceeded.

Once the VDD_D power-on-reset threshold voltage has been exceeded the device will be released from reset and this will occur within 10µs of the VDD_AD supply reaching 1.75V.

5.2.2 Reset Pin

The CMX655D/CMX655A may be reset while the device remains powered-up by externally driving the RSTN pin low to DGND. A reset duration of 1µs minimum is recommended.

5.3 Main Clock

The control registers and functions associated with the audio signal processing, the Class-D amplifier, the microphone channels and the Serial Audio Interface require the main clock to be active before they may be modified.

5.3.1 Clock Frequency

The CMX655D/CMX655A are designed to operate with a main internal clock frequency of 24.576MHz.

5.3.2 Clock Generation

From reset, the device is in its lowest power state with the main clock (CLK) internally deactivated. The main clock must first be configured and activated before attempting to access and control other device functions.

The required main clock frequency of 24.576MHz may be directly applied to the CMX655D/CMX655A via the RCLK pin. If the exact main clock frequency cannot be supplied by the external system then the CMX655D/CMX655A integer-N PLL may be configured and enabled to generate the required main clock from either RCLK or the serial audio interface sample rate clock LRCLK/FS as shown in Figure 15.

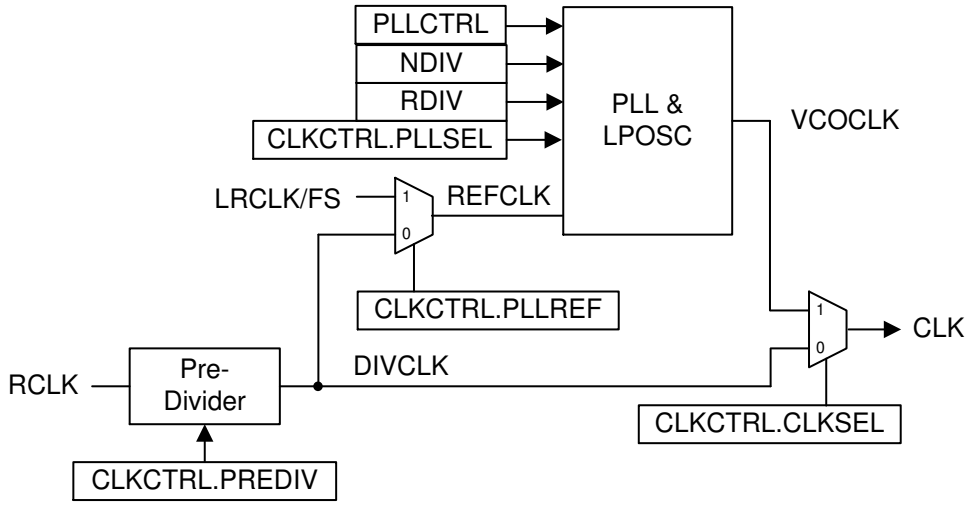


Figure 15 Main Clock Generation

The LRCLK/FS signal may only be selected as the PLL reference clock if the CMX655D/CMX655A Serial Audio Interface operates as a slave. In this operating mode, LRCLK/FS is generated by the external master and is an input to the CMX655D/CMX655A and the RCLK input is unused and may be tied low or high as appropriate.

If the CMX655D/CMX655A Serial Audio Interface (SAI) operates as the slave, the CMX655D/CMX655A main clock must be synchronous to LRCLK/FS to avoid audio sample slippage due to clock drift between the CMX655D/CMX655A internal sample rate (derived from the main clock) and the external sample rate indicated on LRCLK/FS and generated by the SAI master. If LRCLK/FS is not used as the PLL reference clock to derive the main clock when the CMX655D/CMX655A SAI operates as the slave, then the external system should ensure that LRCLK/FS is synchronous with respect to RCLK.

The **CLKCTRL**, **RDIVHI**, **RDIVLO**, **NDIVHI**, **NDIVLO** and **PLLCTRL** register settings should first be configured prior to activating the main clock.

Prior to activating the main clock, the IRQN pin may be configured to indicate when the main clock has successfully started by setting the CLKRDY bit in the **ISM** register. The main clock is activated by writing $01 (Clock Start command) to the **COMMAND** register. The CLKRDY bit in the **ISR** register is set when the clock goes ready. This bit is cleared on reading the **ISR** register. It is not possible to modify the **CLKCTRL** register after the main clock is activated. The **RDIVHI**, **RDIVLO**, **NDIVHI**, **NDIVLO** and **PLLCTRL** registers should not be modified if the main clock is active and generated by the PLL.

To return the device to its lowest power state, the **SYSCTRL** register should first be cleared after which the main clock may be deactivated by writing $00 (Clock Stop command) to the **COMMAND** register. The main clock will stop within four main clock cycles after the Clock Stop command has been transferred. If the main clock is derived from the PLL clock at

the time the main clock is deactivated, the external clock source used for the PLL reference (i.e. RCLK or LRCLK/FS) must only be disabled at least four REFCLK cycles after the Clock Stop command has been transferred.

After the main clock has stopped, the Microphone Interface, Class-D Amplifier, Audio Signal Processing and Serial Audio Interface are held in reset until the main clock is next restarted.

The CMX655D/CMX655A low-power oscillator, LPOSC, generates a nominal 24.576MHz clock. The LPOSC allows the CMX655D/CMX655A to perform record level detection without an external clock supplied to the device. When the LPOSC is used as the main clock source, the SAI and Class-D amplifier must be disabled because the LPOSC frequency is too low and not sufficiently accurate to support these functions. If the detected microphone audio level exceeds a programmable threshold an associated interrupt may be indicated on the IRQN pin. The interrupt may be used to wake-up a sleeping external controller that subsequently re-enables the external clock source (i.e. RCLK or LRCLK/FS) and places the CMX655D/CMX655A back into a fully featured operating mode that makes use of the active external clock to derive the main clock.

5.3.3 PLL

The basic integer-N PLL block diagram is shown in Figure 16.

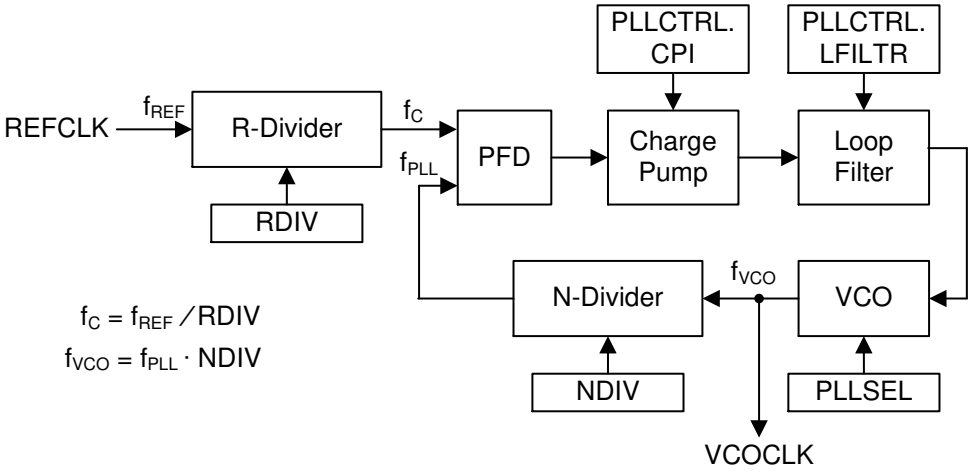


Figure 16 Integer-N PLL

The REFCLK is taken from RCLK (i.e. a common crystal oscillator frequency) or the sample rate clock input on LRCLK/FS (i.e. 8/16/32/48kHz). The frequency range of REFCLK is 8kHz–20MHz. The PLL is fully integrated within the CMX655D/CMX655A so there is no requirement for any external loop filter components. The PLL loop filter is shown in Figure 17.

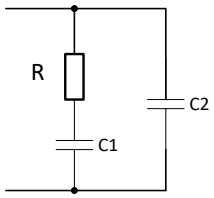


Figure 17 PLL Loop Filter

C1 is 54pF, C2 is 5.4pF and R is adjustable via bits 7-4 of the register PLLCTRL.

5.3.4 Low Power Oscillator

The LPOSC generates a nominal 24.576MHz clock. When the LPOSC is selected as the main clock source, the VCO operates as an open-loop ring oscillator and the remaining PLL components are disabled. The LPOSC supports record level detection without the requirement of an external clock source to be applied to the CMX655D/CMX655A.

5.3.5 Clock Control Registers

5.3.5.1 CLKCTRL ($03)

Clock Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0	SR		PLLREF	PLLSEL	CLKSEL	PREDIV	

SR	Sample Rate (f_s)
0	8ksps
1	16ksps
2	32ksps
3	48ksps

PLLREF	PLL Reference Clock Source
0	DIVCLK
1	LRCLK/FS - requires CMX655D/CMX655A Serial Audio Interface to operate as a slave

PLLSEL	PLL Select
0	Open-loop VCO (LPOSC)
1	Closed-loop PLL

CLKSEL	Clock Selection
0	Select DIVCLK
1	Select VCOCLK

PREDIV	Pre-divider
0	Divide by 1
1	Divide by 2
2-3	Divide by 4

5.3.5.2 RDIVHI ($04)

R-Divider High Byte (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0			RDIV[12:8]				

5.3.5.3 RDIVLO ($05)

R-Divider Low Byte (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
RDIV[7:0]							

RDIV[12:0]	Divide Value
0	Divide by 8192
1-8191	Divide by 1-8191

5.3.5.4 NDIVHI ($06)

N-Divider High Byte (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0			NDIV[12:8]				

5.3.5.5 NDIVLO ($07)

N-Divider Low Byte (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
NDIV[7:0]							

NDIV[12:0]	Divide Value
0	Divide by 8192
1-8191	Divide by 1-8191

5.3.5.6 PLLCTRL ($08)

PLL Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
R				CPI			

R	Loop Filter Resistor (Ω)
0	17.5 kΩ
1	25 kΩ
2	35 kΩ
3	50 kΩ
4	70 kΩ
5	100 kΩ
6	140 kΩ
7	200 kΩ
8	280 kΩ
9	400 kΩ
10	560 kΩ
11	800 kΩ
12	1.12 MΩ
13	1.6 MΩ
14	2.24 MΩ
15	3.2 MΩ

CPI	Charge Pump Current Gain (µA/cycle)
0	0.0
1	0.05
2	0.075
3	0.1
4	0.15
5	0.2
6	0.3
7	0.4
8	0.55
9	0.8
10	1.15
11	1.6
12	2.25
13	3.2
14	4.45
15	6.2

5.4 Microphone Interface

5.4.1 Digital Microphone Interface

The CMX655D drives the MICCLK pin which connects to the external microphone(s) clock input and receives a PDM bit-stream on MICDI from the microphone(s) data output. Digital MEMS microphones are configured to output the PDM bit-

stream for either positive or negative clock edge operation, with the data-line going high-impedance for the inactive clock edge. This allows two microphones to share a common clock and data line when configured to operate on opposite clock edges to support 2-channel audio. The CMX655D samples left channel data on the falling edge of MICCLK and right channel data on the rising edge of MICCLK as shown in Figure 18.

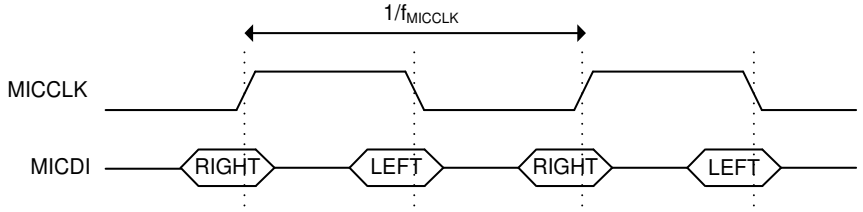


Figure 18 CMX655D Digital Microphone Interface

The CMX655D drives MICCLK with a 50% duty cycle at a frequency of f_{MICCLK}. If the sample rate is 48ksps, then f_{MICCLK} = 3.072MHz. For the remaining sample rates of 8/16/32ksps, f_{MICCLK} = 2.048MHz.

5.4.2 Analogue Microphone Interface

The CMX655A analogue microphone interface is shown in Figure 19.

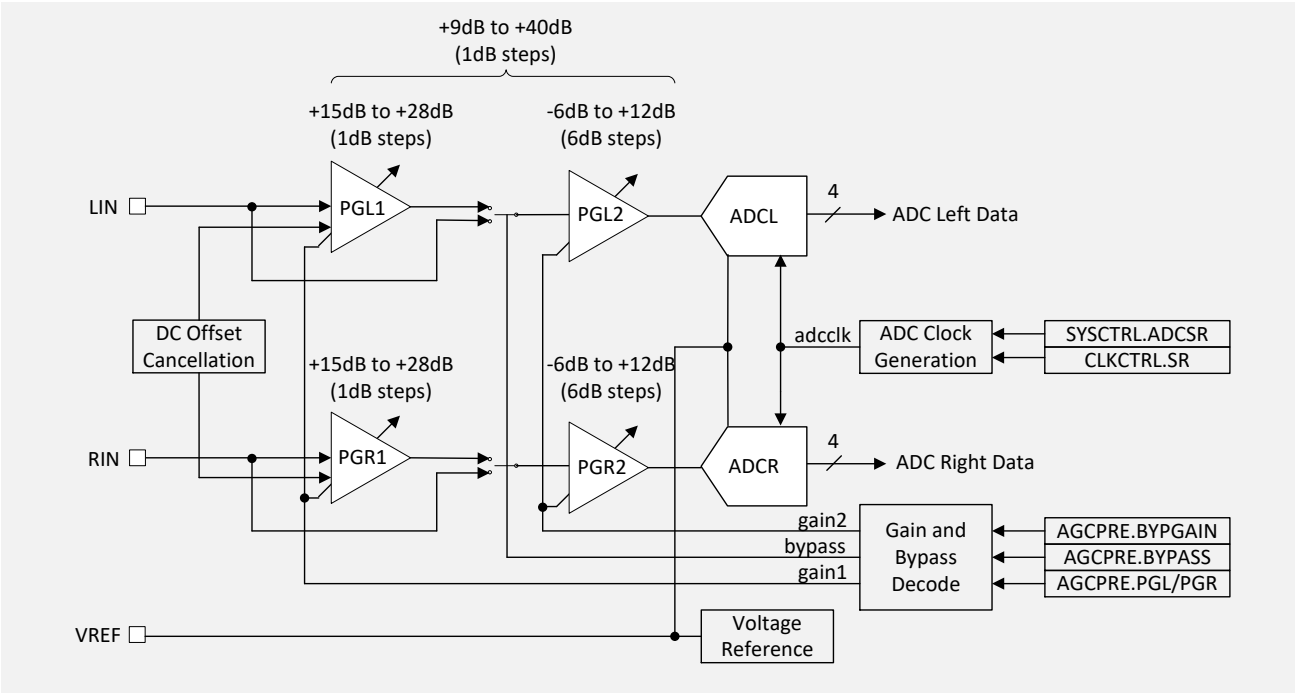


Figure 19 CMX655A Analogue Microphone Interface

The CMX655A receives externally AC coupled analogue record signals on the LIN and RIN input pins for the left and right record channels respectively. The VREF pin is used to externally decouple the on-chip generated voltage reference.

The LIN and RIN analogue record input signals are amplified by the programmable gain amplifiers PGL1/2 and PGR1/2 respectively. If AGC is disabled, the amplifier gains are manually controlled by writing to the PGL/PGR field in the **AGCPRE** register. If AGC is enabled, the amplifier gains are automatically controlled by the AGC unit and the gain setting may be read from the PGL/PGR field in the **AGCPRE** register.

The amplifiers PGL1 and PGR1 may be optionally bypassed to facilitate the use of an external microphone pre-amplifier in conjunction with amplifiers PGL2 and PGR2. This bypass mode of operation is controlled using the BYPASS and BYPGAIN fields in the **AGCPRE** register. In this mode of operation, the CMX655A microphone inputs LIN and RIN must be externally DC-biased to half the VDD_AD supply as shown in Figure 20 with component values listed in Table 14.

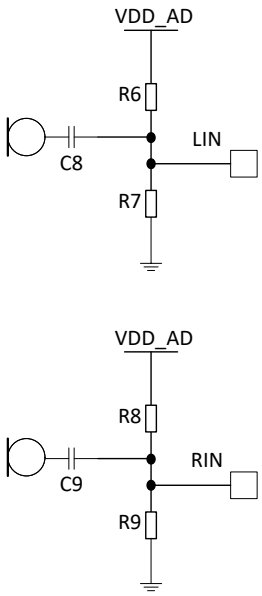


Figure 20 External Microphone Connections for Bypass Mode

Table 14 Bypass Mode Component Values

R6	10kΩ
R7	10kΩ
R8	10kΩ
R9	10kΩ
C8	390nF
C9	390nF

The CMX655A includes an on-chip DC-offset cancellation circuit that eliminates the DC-offset voltage at the PGL1/PGR1 pre-amplifier inputs. The analogue microphone channels require 150ms to stabilise after being enabled via the **SYSCTRL** register after which DC-offset voltage calibration may be initiated by writing to the CAL bit in the **ISE** register. DC-offset voltage calibration should not be performed when these pre-amplifiers are bypassed.

The CMX655A delta-sigma ADC modulators convert the analogue record signals into 4-bit pulse density modulated bit-streams that are subsequently decimated to produce 16-bit audio samples at the selected audio sample rate.

The standard sampling rate of the ADC is 2.048Msps for the 8/16/32ksps audio sample rates and 3.072Msps for the 48ksps audio sample rate. The ADC sample rate may be doubled to improve SNR for the 16/32/48ksps audio sample rates by setting the ADCSR bit to 1 in the **SYSCTRL** register.

5.5 Class-D Amplifier

5.5.1 Audio Outputs

The CMX655D/CMX655A Class-D amplifier provides differential power outputs (AOUTP, AOUTN) for driving a speaker with 4Ω-8Ω impedance and a single-ended lineout (LOUT) for driving a minimum load impedance of 18kΩ in parallel with 120pF.

5.5.2 Overload Current Protection

The CMX655D/CMX655A differential power outputs of the Class-D amplifier are protected against overload current conditions with an automatic shut-off protection circuit. Overload current protection is enabled when the **SYSCTRL** register PAMP bit is set to 1. The overload current condition may be configured to signal an interrupt via the IRQN pin as described in section 5.9.

5.5.3 Thermal Protection

The CMX655D/CMX655A includes an integrated thermal detection circuit which automatically powers-down the Class-D amplifier differential power outputs when the device temperature reaches a critical level. Thermal protection is enabled when the **SYSCTRL** register PAMP bit is set to 1. The thermal protection event may be configured to signal an interrupt via the IRQN pin as described in section 5.9.

5.5.4 Clipping Detection

A clipping detection circuit within the CMX655D/CMX655A Class-D amplifier monitors if the differential power output stage is in saturation and distorting the playback signal. The clipping detection circuit is enabled when the **SYSCTRL** register PAMP bit is set to 1. The clipping detection interrupt generation is enabled using the **ISE** register. The clipping detection circuit may be configured to signal an interrupt via the IRQN pin as described in section 5.9.

5.6 Audio Signal Processing

5.6.1 Record Level Control

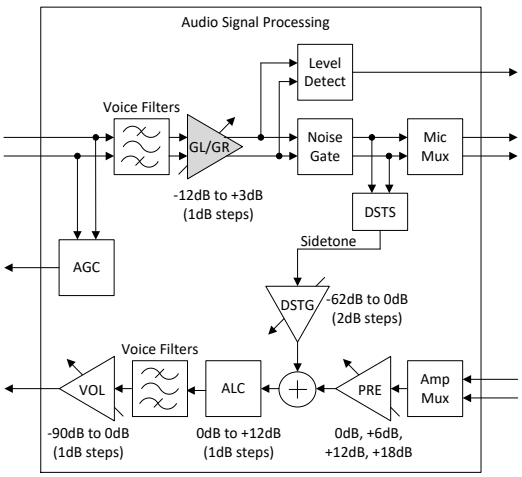


Figure 21 Audio signal processing block diagram with gain level block highlighted

The record levels of the left and right channels are controlled by the gain settings in the **LEVEL** register. The gain applied to each channel may be independently set from -12dB to +3dB in 1dB steps.

5.6.1.1 Record Level Control Register

LEVEL ($0F)
Record Level (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
GL				GR			

GL	Gain Left channel
0-15	-12dB to +3dB (+1dB steps)

GR	Gain Right channel
0-15	-12dB to +3dB (+1dB steps)

5.6.2 Automatic Gain Control

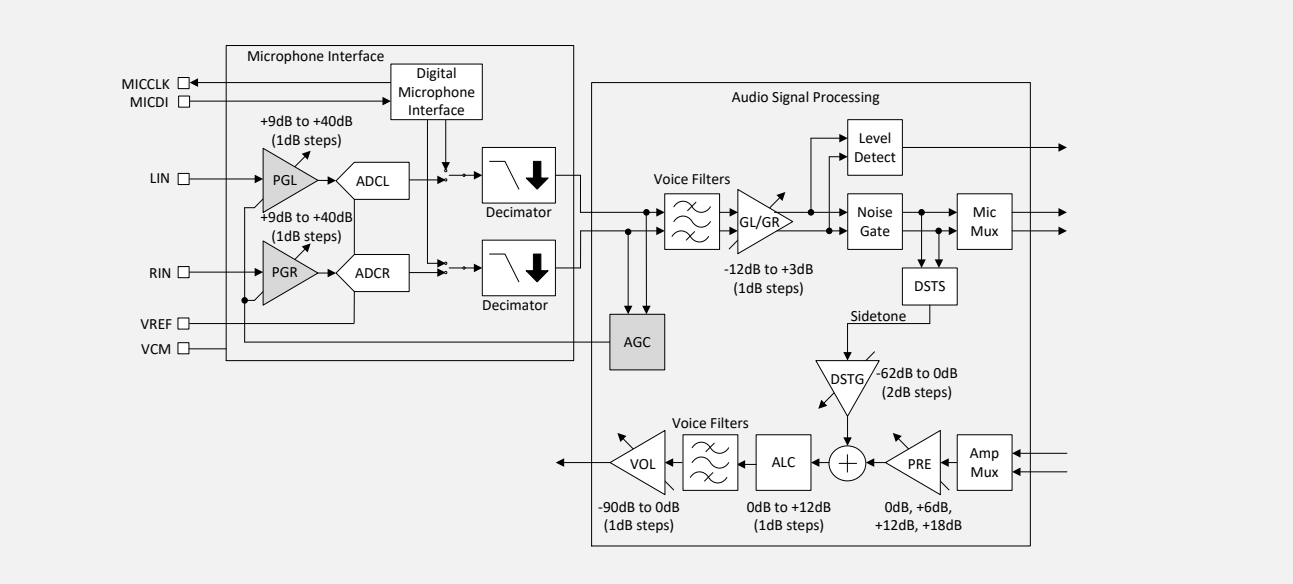


Figure 22 Microphone interface and Audio signal processing block diagrams, showing AGC control blocks highlighted

The AGC function dynamically controls the gain of the analogue microphone amplifiers to best utilise the available ADC dynamic input range. The amplifier gains PGL and PGR are each composed of two separate gain stages PGL1/2 and PGR1/2 as shown in Figure 19.

The AGC algorithm starts with the amplifier gain at the centre of the configured gain control range. If the signal level is above the pre-programmed threshold, the AGC circuit reduces the gain until the signal falls within 1dB of the threshold. The attack time determines how long the AGC circuit takes to reduce the gain by one time-constant of the exponential response when the signal is above the threshold. One time-constant of the exponential response is equivalent to ~63% of the total gain reduction.

If the signal falls below the threshold, the gain is maintained for the pre-programmed hold time before initiating the release phase where the gain is increased. During the hold time, if the signal rises above the threshold the hold time counter is reset. Once the hold time has expired, the AGC circuit increases the gain until the signal is within 1dB of the threshold. The release time determines how long the AGC circuit takes to increase the gain by one time-constant of the exponential response which is equivalent to ~63% of the total gain increase.

The AGC algorithm is controlled by the **AGCRANGE**, **AGCPRE**, **AGCCTRL** and **AGCTIME** registers. If the AGC function is disabled, the gain of the microphone amplifiers may be directly controlled by the user.

5.6.2.1 AGC Registers

AGCRANGE ($18)
AGC Range Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
SPAN				MINGAIN			

SPAN	AGC Span
0-7	20-27dB (+1dB steps)
8-15	12-19dB (+1dB steps)

The SPAN field may be considered as a 4-bit two's complement number (-8 to +7) which added to 20 produces the AGC Span in decibels. The AGC Span is the difference between the highest and the lowest microphone amplifier gain settings utilised by the AGC algorithm. For typical applications, 20dB of span is sufficient (i.e. SPAN=0).

MINGAIN	AGC Minimum Gain
0-15	9-24dB (+1dB steps)

The AGC Minimum Gain is the lowest microphone amplifier gain setting utilised by the AGC algorithm. The highest microphone amplifier gain setting utilised by the AGC algorithm equals the AGC Minimum Gain plus the AGC Span. The maximum microphone amplifier gain setting is 40dB. Therefore, to avoid gain saturation, the AGC Minimum Gain plus the AGC Span must not exceed 40dB.

The selection of the MINGAIN value is partly determined by the sensitivity of the external microphone transducer and the typical distance between the sound source and the external microphone required by the target application.

AGCPRE ($19)
AGC Pre-amplifier Gain (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
BYPGAIN		BYPASS	PGL/PGR				

BYPGAIN	Bypass Mode Gain (BYPASS = 1)
0	-6dB
1	0dB
2	+6dB
3	+12dB

BYPASS	Bypass Mode
0	Amplifier PGL1/PGR1 in signal path - combined amplifier gain is controlled by PGL/PGR
1	Amplifier PGL1/PGR1 bypassed - amplifier PGL2/PGR2 gain is controlled by BYPGAIN

PGL/PGR	Programmable Gain Left/Right (BYPASS=0)
0-31	+9dB to +40dB (+1dB steps)

If the AGC function is disabled (i.e. SOURCE=0 in AGCCTRL) and BYPASS=0, the value written to the PGL/PGR field controls the composite microphone amplifier gain.

If the AGC function is enabled (i.e. SOURCE≠0 in AGCCTRL) then BYPASS must be set to 0 and the PGL/PGR field is read only and reflects the gain setting applied by the AGC algorithm.

AGCCTRL ($1A)
AGC Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0		SOURCE		THRESH			

SOURCE	AGC Input Source
0	None - AGC disabled
1	Left channel
2	Right channel
3	Maximum of left or right channel

THRESH	Threshold
0-15	-18dBFS to -3dBFS (+1dB steps)

AGCTIME ($1B)
AGC Time (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
ATTACK			HOLD		RELEASE		

ATTACK	Attack Time (ms)
0	0.125 (only use if fs = 48ksps)
1	0.25 (only use if fs >= 32ksps)
2	0.5 (only use if fs >= 16ksps)
3	1
4	4
5	16
6	64
7	256

HOLD	Hold Time (ms)
0	50
1	100
2	200
3	400

RELEASE	Release Time (s)
0	0.064
1	0.128
2	0.256
3	0.512
4	1.024
5	2.048
6	4.096
7	8.192

5.6.3 Noise Gate

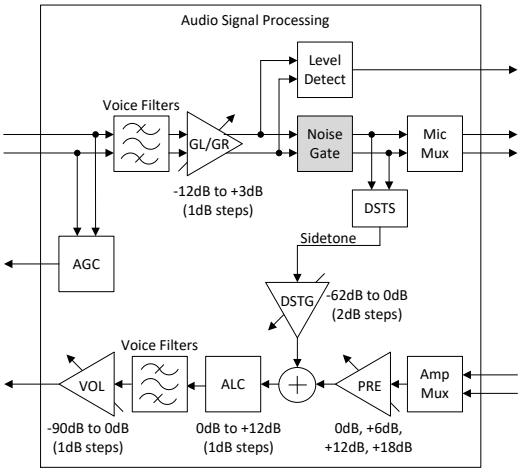


Figure 23 Audio signal processing block diagram with Noise Gate block highlighted

The noise gate function is designed to attenuate low-level record signals that fall below a pre-programmed noise threshold. Noise gating is implemented using downward expansion such that the output signal level is attenuated in proportion to the degree in which the peak input signal level is below the expansion threshold. Downward expansion results in a soft noise gating response due to the gradual attenuation applied to the input signal. The input-to-output

signal level ratio below the threshold may be programmed as 1:2, 1:3 or 1:4. The noise gate is controlled by the **NGCTRL** register. The ideal expansion attenuation A_{EXP} (dB) when the input signal (dBFS) is below the expansion threshold (dBFS) for a given an expansion ratio of 1:E is:

$$A_{EXP} = (E-1)*(\text{Threshold} - \text{Input})$$

However, it should be noted that A_{EXP} is only controlled using 1dB of resolution and that the maximum attenuation applied by the noise gate is limited to 31dB. Figure 24 shows the ideal noise gate response for these ratios with the threshold set to -50dBFS. The 1:1 ratio is effective when the noise gate is disabled.

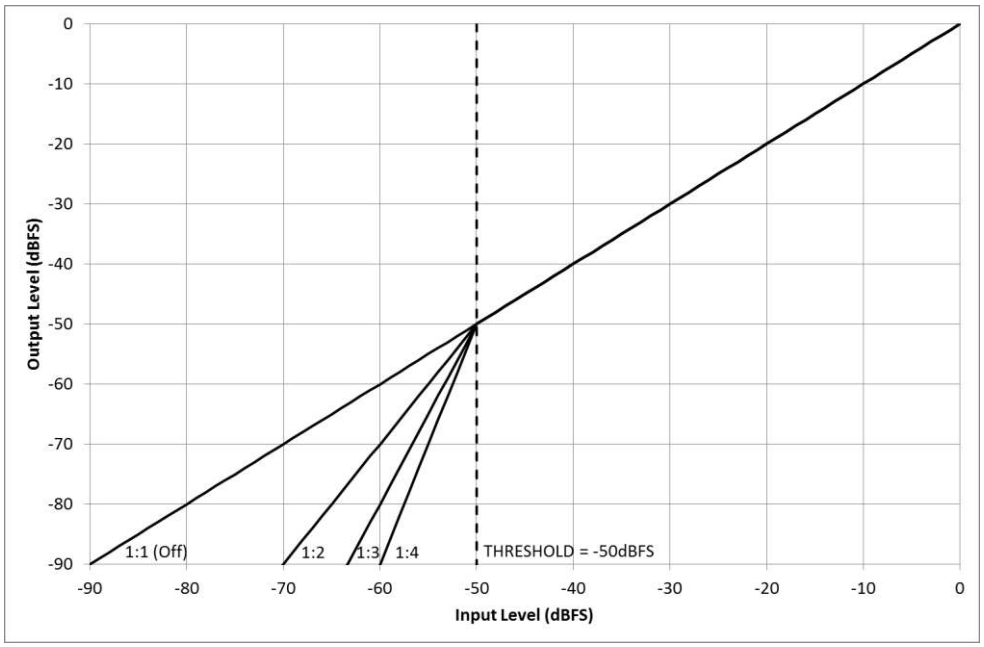


Figure 24 Noise Gate Response

When enabled, the noise gate function operates independently on the left and right record channel. The noise gate response time is programmed using the **NGTIME** register. The release time determines how long it would take for the noise gate to apply 12dB of downwards expansion when the input signal falls below the threshold. The attack time determines how long it would take the noise gate to remove 12dB of downwards expansion once the signal rises back above the threshold. The release and attack times therefore determine the rate at which expansion is applied and removed. The attenuation applied to the left and right record channel may be read from **NGLSTAT** and **NGRSTAT** registers respectively.

5.6.3.1 Noise Gate Registers

NGCTRL ($1C)
Noise Gate Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
EN	RATIO		THRESH				

EN	**Enable**
0	Noise Gate disabled (1:1 ratio)
1	Noise Gate enabled

RATIO	**Input-to-output signal level ratio below Threshold when Noise Gate enabled**
0	1:2
1	1:3
2-3	1:4

THRESH	**Threshold**
0-31	-63dBFS to -32dBFS (+1dB steps)

NGTIME ($1D)
Noise Gate Time (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0	ATTACK			0	RELEASE		

ATTACK	Attack Time (ms)
0	1.5
1	3
2	4.5
3	6
4	12
5	24
6	48
7	96

RELEASE	Release Time (s)
0	0.06
1	0.12
2	0.24
3	0.48
4	0.96
5	1.92
6	3.84
7	7.68

NGLSTAT ($1E)
Noise Gate Left Channel Status (R)
Reset Value: $00

7	6	5	4	3	2	1	0
0			ATTEN				

ATTEN	Attenuation
0-31	0dB to +31dB (+1dB steps)

NGRSTAT ($1F)
Noise Gate Right Channel Status (R)
Reset Value: $00

7	6	5	4	3	2	1	0
0			ATTEN				

ATTEN	Attenuation
0-31	0dB to +31dB (+1dB steps)

5.6.4 Record Level Detection

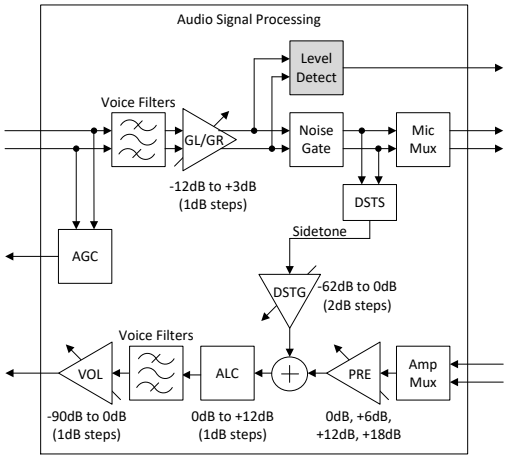


Figure 25 Audio signal processing block diagram with Level Detect block highlighted

The record level detection function continuously monitors the record signal level and can be configured to trigger an interrupt when the record signal level exceeds a pre-programmed detection threshold. This feature is useful in low-power listening mode applications, such as a voice activated switch (VOX), where the CMX655D/CMX655A record level interrupt signal is used to wake-up a sleeping external host. The record level detection function interrupt enable bits are set in the **ISM** register and the record level detection thresholds for the left and right channels are independently set by the **LDCTRL** and **RDCTRL** registers respectively.

Each of left and right level detectors operates in a one-shot manner; a detector is automatically disabled when triggered and cannot be enabled again until its corresponding MICL or MICR bit in the **ISR** is cleared by a read of the **ISR** register.

5.6.4.1 Record Level Detection Registers

LDCTRL ($0D)
Left Channel Detection Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
LEN	LTHRESH						

LEN	**Left Channel Detection Enable**
0	Disable left channel interrupt detection.
1	Enable left channel interrupt detection. LEN is automatically cleared to 0 if the **ISR** MICL bit is set to 1. The LEN bit is equivalent to and its state is always the same as that of the MICL **ISE** register bit.

LTHRESH	**Left Channel Detection Threshold**
0-89	-90dBFS to -1dBFS (+1dB steps)
90-127	-1dBFS

RDCTRL ($0E)
Right Channel Detection Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
REN	RTHRESH						

REN	**Right Channel Detection Enable**
0	Disable right channel interrupt detection.
1	Enable right channel interrupt detection. REN is automatically cleared to 0 if the **ISR** MICR bit is set to 1. The REN bit is equivalent to and its

state is always the same as that of the MICR **ISE** register bit.

RTHRESH	**Right Channel Detection Threshold**
0-89	-90dBFS to -1dBFS (+1dB steps)
90-127	-1dBFS

5.6.5 Playback Preamplifier Gain

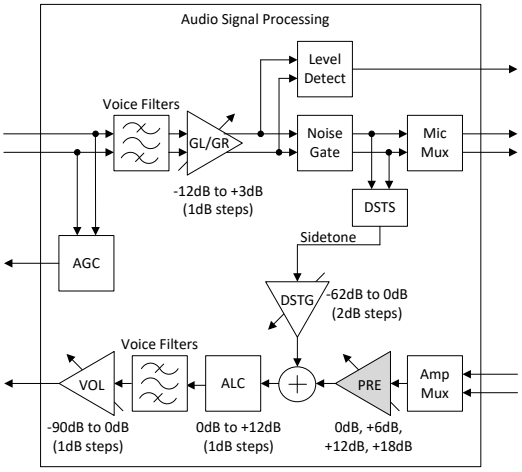


Figure 26 Audio signal processing block diagram with preamp block highlighted

The **PREAMP** register sets the playback preamplifier gain to 1/2/4/8 (approximately 0/6/12/18dB).

5.6.5.1 Playback Preamplifier Gain Register

PREAMP ($29)
Playback Preamp Gain (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0						PRE	

PRE	**Pre-amplifier Gain**
0	1 (0dB)
1	2 (6dB)
2	4 (12dB)
3	8 (18dB)

5.6.6 Playback Volume Control

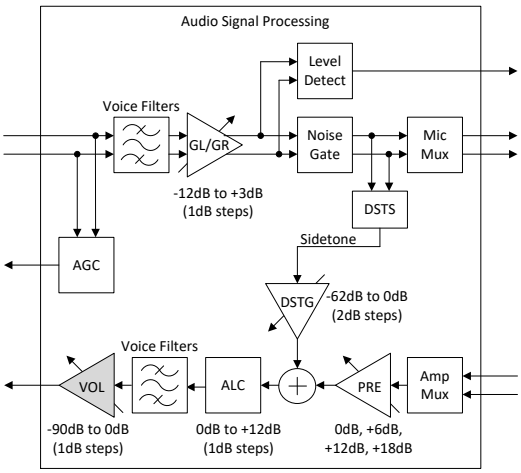


Figure 27 Audio signal processing block diagram with the volume block highlighted

The **VOLUME** register sets the playback amplifier gain between 0dB and -90dB in 1dB steps.

5.6.6.1 Playback Volume Register

VOLUME ($2A)
Playback Volume (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
SMOOTH	VOL						

SMOOTH	**Volume Smoothing**
0	Volume smoothing disabled - the VOL setting is applied immediately
1	Volume smoothing enabled - the VOL setting is applied gradually using intermediate gain steps near zero-crossings or after a 5ms timeout if no zero-crossing is detected

VOL	**Volume Gain Setting**
0	Mute
1-91	-90dB to 0dB (+1dB steps)
92-127	0dB

The generation of the VOL interrupt status bit in the **ISR** bit register is enabled by setting the VOL interrupt enable bit in the **ISE** register. The VOL **ISR** bit indicates that volume gain adjustment has completed, which occurs 32 sample periods after the applied volume gain equals the volume gain setting. To avoid the immediate generation of a VOL interrupt, the VOL **ISE** bit should only be set following a change in the volume gain setting.

To reduce click-and-pop artefacts, it is recommended to mute the volume and wait for volume gain adjustment completion before clearing the PAMP bit in the **SYSCTRL** register when disabling the Class-D power amplifier.

5.6.7 Automatic Level Control

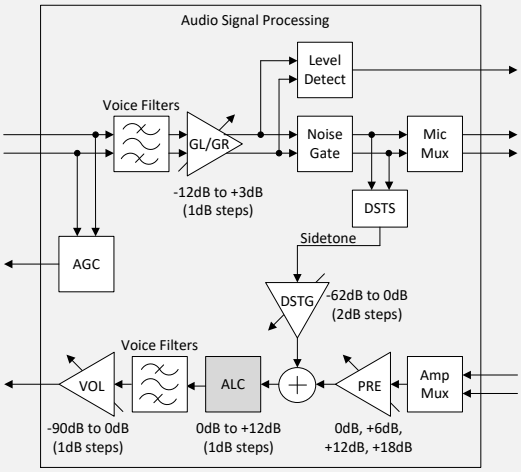


Figure 28 Audio signal processing block diagram with ALC block highlighted

The ALC function is designed to enhance low-level playback signals by reducing the dynamic range of the output signal with respect to the input signal. The ALC is implemented using downward compression such that the output signal level is attenuated in proportion to the degree in which the peak input signal level is above the compression threshold. The ALC is controlled using the **ALCCTRL** register where the input-to-output signal level ratio above the compression threshold may be programmed as 1.5:1, 2:1, 4:1 or ∞:1. The ideal compression attenuation A_{COM} (dB) when the input signal (dBFS) is above the compression threshold (dBFS) for a given a compression ratio of C:1 is:

$$A_{COM} = (C-1)*(Input – Threshold)/C$$

However, it should be noted that A_{COM} is only controlled using 1dB of resolution. Figure 29 shows the ideal ALC response for these ratios with the threshold set to -30dBFS. The 1:1 ratio is effective when the ALC is disabled.

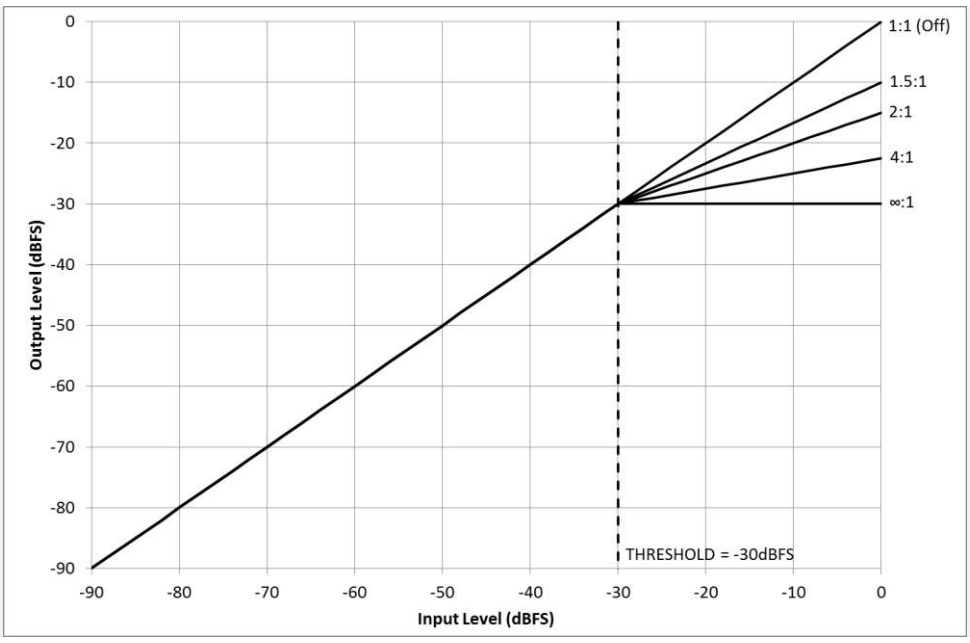


Figure 29 ALC Response

The ALC response time is programmed using the **ALCTIME** register. The attack time determines how long it would take the ALC to apply 12dB of downwards compression when the input signal rises above the threshold. The release time determines how long it would take the ALC to remove 12dB of downwards compression once the signal falls back below the threshold. The attack and release times therefore determine the rate at which compression is applied and removed.

To make-up for lost gain due to the downwards compression, up to 12dB of make-up gain is selectable using the **ALCGAIN** register. The make-up gain is applied regardless of whether the ALC is enabled. The compression attenuation applied by the ALC excluding the make-up gain may be read from the **ALCSTAT** register.

5.6.7.1 ALC Registers

ALCCTRL ($2B)
ALC Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
EN	RATIO			THRESH			

EN	Enable
0	ALC disabled (1:1 ratio)
1	ALC enabled

RATIO	Input-to-output signal level ratio above Threshold when ALC enabled
0	1.5:1
1	2:1
2	4:1
3	∞:1

THRESH	Threshold
0-31	-31dBFS to 0dBFS (+1dB steps)

ALCTIME ($2C)
ALC Time (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0	ATTACK			0	RELEASE		

ATTACK	Attack Time (ms)
0	1.5
1	3
2	4.5
3	6
4	12
5	24
6	48
7	96

RELEASE	Release Time (s)
0	0.06
1	0.12
2	0.24
3	0.48
4	0.96
5	1.92
6	3.84
7	7.68

ALCGAIN ($2D)
ALC Make-up Gain (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0				GAIN			

GAIN	Make-up Gain
0-12	0dB-12dB (+1dB steps)
13-15	12dB

ALCSTAT ($2E)
ALC Status (R)
Reset Value: $00

7	6	5	4	3	2	1	0
0			ATTEN				

ATTEN	ALC Attenuation
0-31	0dB to +31dB (+1dB steps)

5.6.8 Digital Sidetone

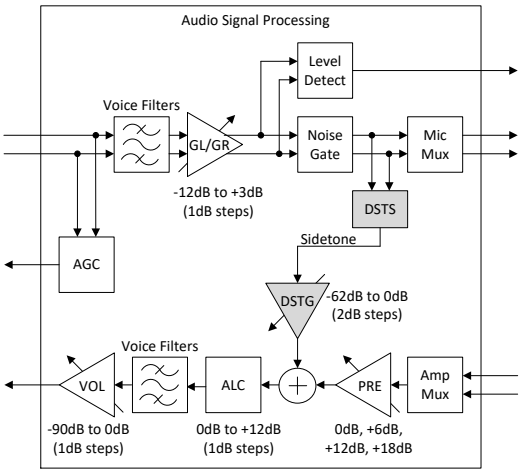


Figure 30 Audio signal processing block diagram with the Digital Side Tone path and block highlighted

Digital sidetone feeds a proportion of the microphone signal back into the playback signal path to provide audible feedback to the speaking user. The sidetone level and input source are controlled by the **DST** register which provides programmable signal attenuation of -62dB to 0dB in +2dB steps.

5.6.8.1 Digital Sidetone Register

DST ($2F)
Digital Sidetone Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
EN	DSTS			DSTG			

EN	Digital Sidetone Enable
0	Sidetone disabled (muted)
1	Sidetone enabled

DSTS	Digital Sidetone Source
0	Left microphone signal
1	Right microphone signal
2-3	Mean of left and right microphone signals

DSTG	Digital Sidetone Gain
0 to 31	-62dB to 0dB (+2dB steps)

5.6.9 Voice Filters

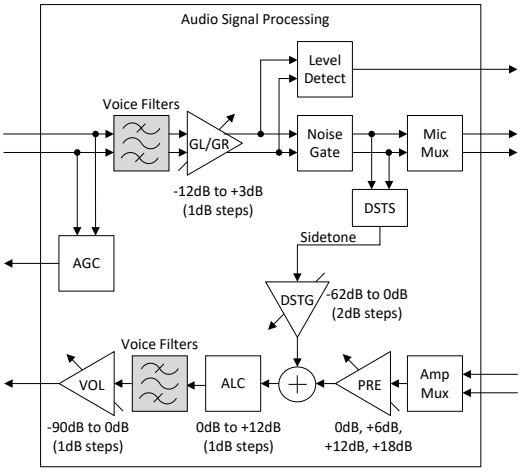


Figure 31 Audio signal processing block diagram with Voice Filter blocks highlighted

The voice filters provide narrow audio band filtering and may be optionally enabled as required.

5.6.9.1 Low Pass Filter

The low pass IIR filter has a 4th-order Butterworth response with a passband -3dB point of 0.4375 x f_s (i.e. 3500/7000/14000/21000Hz @ 8/16/32/48ksps). The low pass filter for the record and playback channels is enabled by the LPFEN bit in the **RVF** and **PVF** registers respectively. The frequency response of the low pass filter is shown in Figure 32.

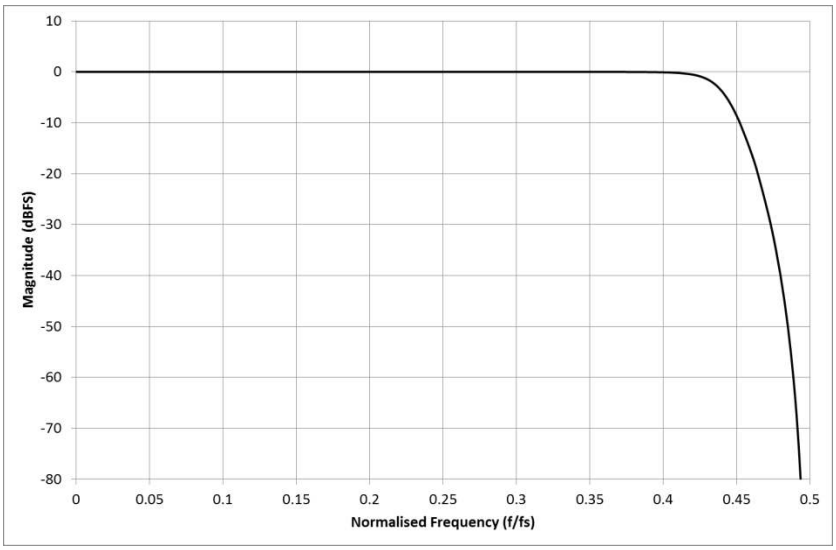


Figure 32 Low Pass Filter Frequency Response

5.6.9.2 DC Blocking Filter

The DC blocking filter provides 90dB of DC attenuation. The DC blocking filter for the record and playback channels is enabled by the DCBEN bit in the **RVF** and **PVF** registers respectively.

5.6.9.3 High Pass Filter

The high pass IIR filter has a 4th-order Butterworth response with three selectable -3dB points to accommodate different applications and may be optionally disabled. The high pass filter for the record and playback channels is controlled by the HPSEL bits in the **RVF** and **PVF** registers respectively. The frequency response of the high pass filters are shown in Figure 33.

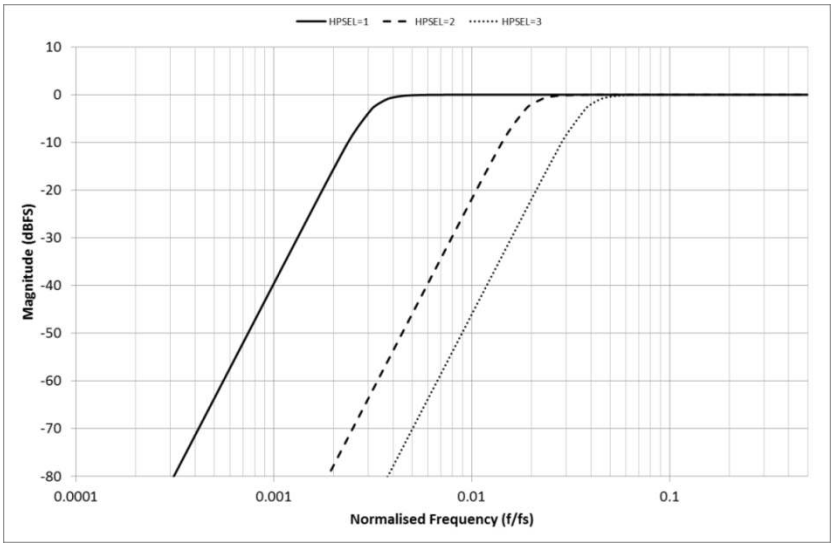


Figure 33 High Pass Filter Frequency Response

5.6.9.4 Voice Filters Registers

RVF ($0C)
Record Voice Filters (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0				LPFEN	DCBEN	HPSEL	

LPFEN	**Record Low Pass Filter Enable**
0	Low pass filter disabled
1	Low pass filter enabled

DCBEN	**Record DC Blocking Filter Enable**
0	DC blocking filter disabled
1	DC blocking filter enabled

HPSEL	**Record High Pass Filter Select**
0	High pass filter disabled
1	High pass filter with a -3dB point of 0.003125 x f_s (e.g. -3dB point of 50Hz @ 16ksps)
2	High pass filter with a -3dB point of 0.01875 x f_s (e.g. -3dB point of 300Hz @ 16ksps)
3	High pass filter with a -3dB point of 0.0375 x f_s (e.g. -3dB point of 300Hz @ 8ksps)

PVF ($28)
Playback Voice Filters (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0				LPFEN	DCBEN	HPSEL	

LPFEN	**Playback Low Pass Filter Enable**
0	Low pass filter disabled
1	Low pass filter enabled

DCBEN	Playback DC Blocking Filter Enable
0	DC blocking filter disabled
1	DC blocking filter enabled

HPSEL	Playback High Pass Filter Select
0	High pass filter disabled
1	High pass filter with a -3dB point of 0.003125 x f_s (e.g. -3dB point of 50Hz @ 16ksps)
2	High pass filter with a -3dB point of 0.01875 x f_s (e.g. -3dB point of 300Hz @ 16ksps)
3	High pass filter with a -3dB point of 0.0375 x f_s (e.g. -3dB point of 300Hz @ 8ksps)

5.6.10 Channel Multiplexing

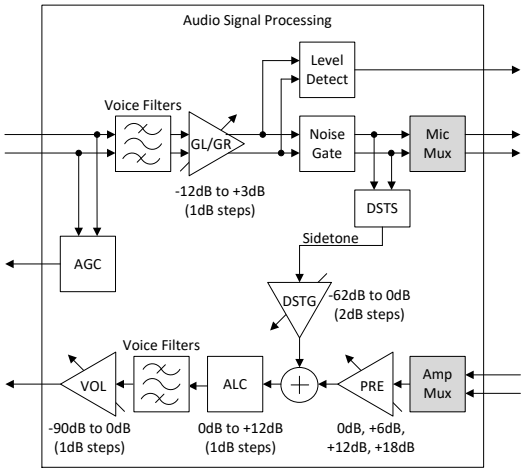


Figure 34 Audio signal processing block diagram with Mic Mux and Amp Mux block highlighted

The left and right microphone output channels may be interchanged or duplicated by appropriately setting the MIC control bits in the **SAIMUX** register defined in section 5.8.5.

The mono amplifier input channel may be selected from the left input or the right input or the mean of the left and right inputs by appropriately setting the AMP control bits in the **SAIMUX** register.

5.6.11 Click-and-Pop Reduction

The CMX655D/CMX655A provides a soft mute function that generates low-level background noise when the playback volume is muted which potentially reduces audible click-and-pop artefacts.

5.6.11.1 Click-and-Pop Reduction Register

CPR ($30)
Click-and-Pop Reduction (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
			0				SOFTM

SOFTM	Soft Mute
0	Soft mute disabled.
1	Soft mute enabled.

5.7 Control Interface

The CMX655D/CMX655A is configured and controlled via the Control Interface. The interface communicates as a SPI Slave when the external SPIS pin is tied high to VDD_AD or as a TWI Slave when the external SPIS pin is tied low to DGND. These interfaces allow communication with standard MCUs and DSPs and are commonly used by existing audio codecs.

5.7.1 SPI Slave

The CMX655D/CMX655A SPI Slave responds to activity on the SPI-bus when the chip-select pin CSN is driven low. Input data on MOSI is clocked in by the CMX655D/CMX655A SPI Slave on the rising edge of SCLK. Output data on MISO is clocked out by the CMX655D/CMX655A SPI Slave on the falling edge of SCLK when transferring read data.

The CMX655D/CMX655A SPI Slave only drives MISO when transferring read data from a valid device address. This feature allows the CMX655D/CMX655A SPI pin connections to be potentially shared with other CML C-BUS slave devices. An external pull-up resistor to VDD_AD (or pull-down resistor to DGND) must be connected to MISO to prevent the node from floating when not driven by the CMX655D/CMX655A SPI Slave or any other connected device. The CMX655D/CMX655A SPI Slave is insensitive to the polarity of SCLK at the start and end of each transfer and is compatible with SPI masters operating in SPI Mode 0 (CPOL=0, CPHA=0) or SPI Mode 3 (CPOL=1, CPHA=1).

The CMX655D/CMX655A communicates over the SPI interface using a transfer width of 16-bits. Figure 35 shows the SPI transfer protocol for performing a single-byte write to the CMX655D/CMX655A .

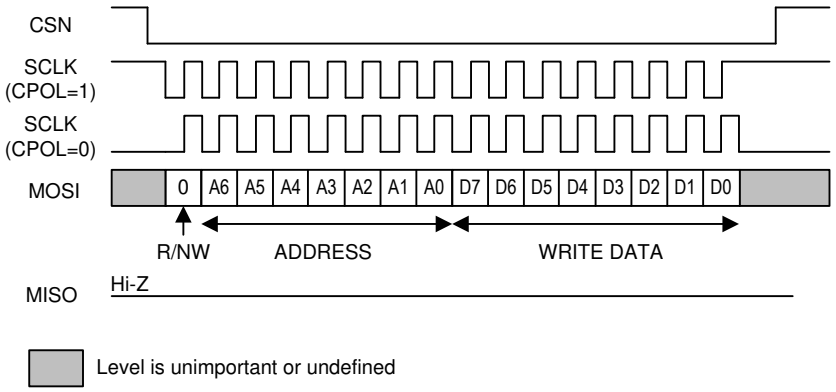


Figure 35 SPI Write Transfer

The first bit on MOSI is the Read/NotWrite bit (R/NW) and this is set to 0 to indicate a write transfer and the following 7-bits (A6 to A0) indicate the register address to be written (MSB first). The remaining 8-bits on MOSI (D7 to D0) indicate the data to be written (MSB first).

Figure 36 shows the SPI transfer protocol for performing a single-byte read from the CMX655D/CMX655A.

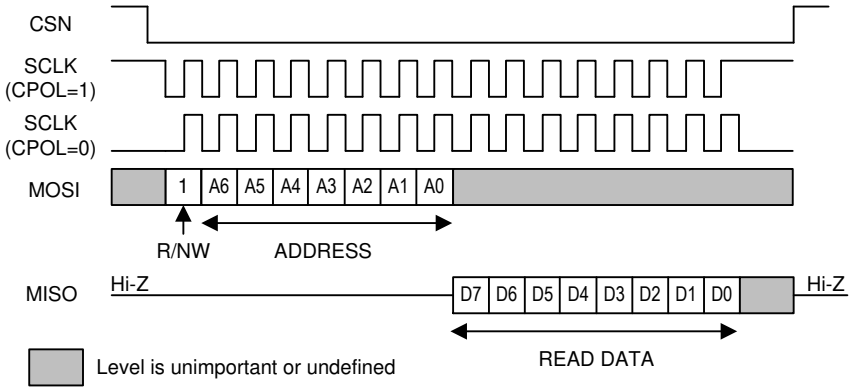


Figure 36 SPI Read Transfer

The R/NW bit is set to 1 to indicate a read transfer and the following 7-bits (A6 to A0) indicate the register address to be read (MSB first). The CMX655D/CMX655A drives the data read from the address onto MISO (D7 to D0) in the following 8 SCLK cycles (MSB first). The CMX655D/CMX655A will only drive read data onto MISO if the register address is defined or reserved by the CMX655D/CMX655A . Read transfers from unallocated register addresses will result in MISO remaining not driven by the CMX655D/CMX655A.

The CMX655D/CMX655A automatically increments the register address internally after each data byte is transferred. SPI masters capable of transfer widths in excess of 16-bits may take advantage of this feature to perform consecutive write (or read) address accesses within the same transfer with reduced addressing overhead as shown in Figure 37 and Figure 38.

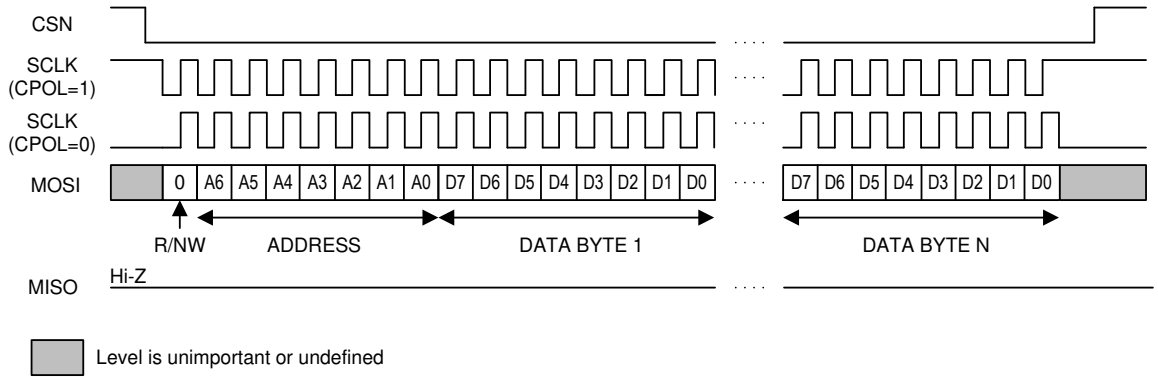


Figure 37 SPI N-Byte Write Transfer

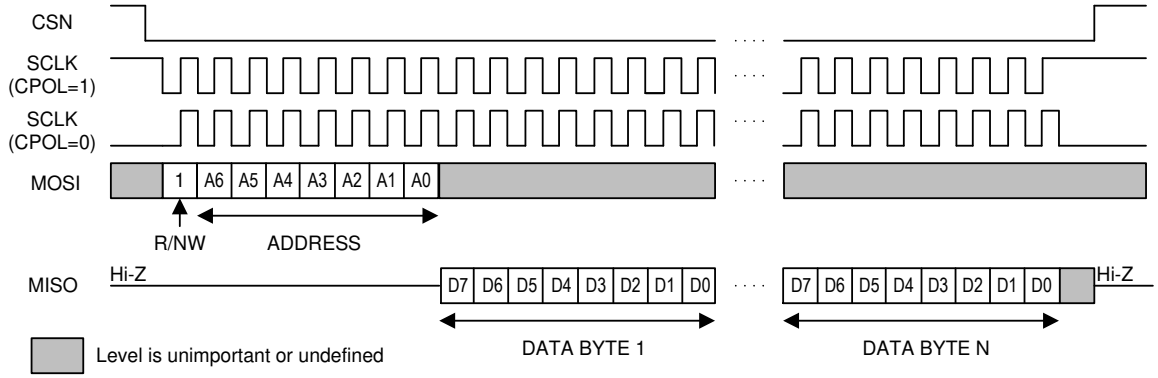


Figure 38 SPI N-Byte Read Transfer

It should be noted that the internal address saturates at $7F and does not auto-increment to wrap back around to $00.

5.7.2 TWI Slave

The CMX655D/CMX655A TWI Slave is compatible with the I^2C-bus Standard-mode (100 kHz) and Fast-mode (400 kHz) operating speeds. The TWI clock line is the SCL pin and the TWI data line is the SDA pin. External pull-up resistors to VDD_AD must be connected to the SDA and SCL pins.

The value of the A1 and A0 pins are address bits 1 and 0 respectively of the 7-bit Slave Address. The remaining upper 5-bits of the 7-bit Slave Address are hard-coded in the device as 10101 binary. The CMX655D/CMX655A TWI Slave may be configured to respond to the following 7-bit Slave Addresses listed in Table 15.

Table 15 CMX655D/CMX655A Slave Addresses

7-bit Slave Address	A1	A0
1010100 (0x54)	0	0
1010101 (0x55)	0	1
1010110 (0x56)	1	0
1010111 (0x57)	1	1

Figure 39 shows the TWI transfer protocol for performing a single-byte write to the CMX655.

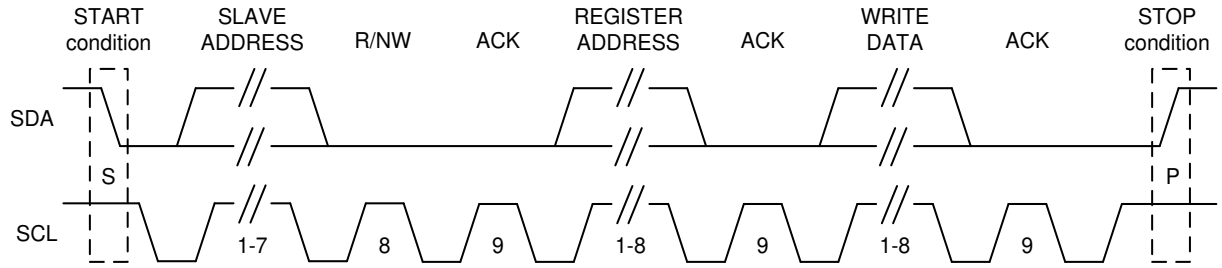


Figure 39 TWI Write Transfer

The TWI master initiates each transaction by generating a START (S) condition defined as a high-to-low transition on SDA while SCL is high. The TWI master terminates each transfer by generating a STOP condition (P) defined as a low-to-high transition on SDA while SCL is high. Each byte placed on the TWI-bus is transferred MSB first and is followed by an Acknowledge bit. The CMX655D/CMX655A TWI Slave does not perform clock-stretching and will not drive the SCL line.

Following the START condition, the first byte the master places on the TWI-bus consists of the 7-bit Slave Address of the target slave followed by the R/NW bit indicating a read (R/NW=1) or write (R/NW=0) transaction. The target slave will respond with an acknowledgement by driving the Acknowledgement bit (ACK) low. For writes (R/NW=0), the TWI master will drive the following data bytes (REGISTER ADDRESS) and the TWI slave will drive the Acknowledgement bit. For reads (R/NW=1), the TWI slave will drive the following data bytes (READ DATA) and the TWI master will drive the Acknowledgement bit.

If the 7-bit Slave Address does not match the CMX655D/CMX655A Slave Address (see Table 15) then the CMX655D/CMX655A TWI Slave will remain idle until a new START condition is generated. If the 7-bit Slave Address matches the CMX655D/CMX655A Slave Address then the CMX655D/CMX655A TWI Slave will respond by driving the SDA line low to indicate an Acknowledgement (ACK).

For a write transaction (R/NW=0), the next byte placed on the TWI-bus by the master consists of the 7-bit register address in the lower 7-bits; the MS bit of the byte is ignored and may be 0 or 1. The CMX655D/CMX655A TWI Slave will signal an ACK by driving the SDA line low. The next byte placed on the TWI-bus by the master is the data to be written and the CMX655D/CMX655A TWI Slave responds with an ACK. The TWI master terminates the transfer by generating the STOP condition.

To read from an arbitrary address, the TWI master must first perform a write transaction to establish the register address to be read followed a repeated START condition (Sr) as shown in Figure 40.

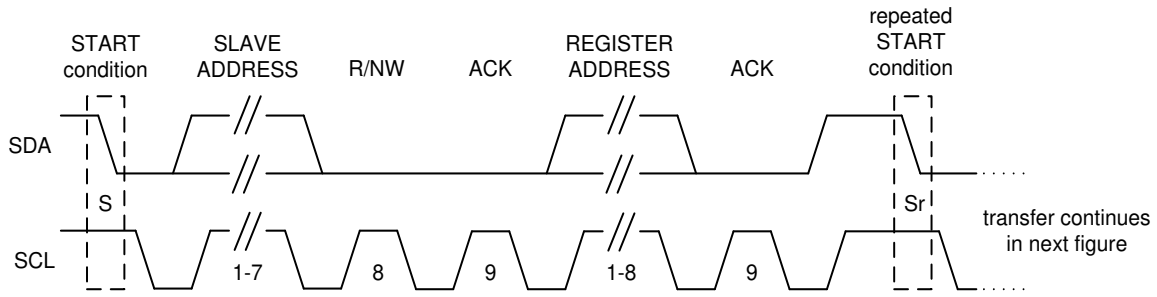


Figure 40 TWI Read Transfer Address Phase

The repeated START condition is functionally identical to the START condition. Following the repeated START condition, the TWI master proceeds to perform a read transaction and resends the 7-bit Slave Address with the R/NW bit set to 1 as shown Figure 41.

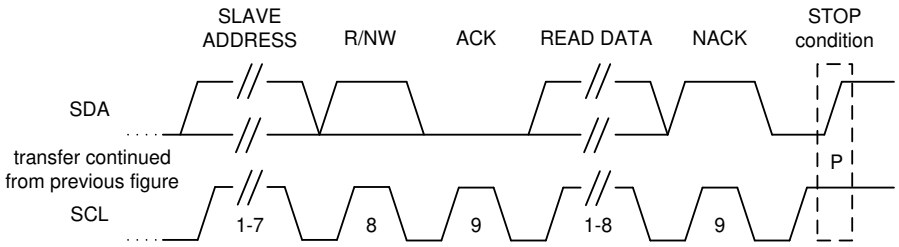


Figure 41 TWI Read Transfer Data Phase

The CMX655D/CMX655A TWI Slave responds with an ACK and drives the read data onto the TWI-bus in the next byte transferred. The CMX655D/CMX655A TWI Slave will send $FF as the data read from unallocated register addresses. The TWI master responds with a Not Acknowledgement (NACK) which indicates to the CMX655D/CMX655A TWI Slave that it should no longer drive the SDA line in this transfer. This subsequently enables the TWI master to terminate the transfer by generating a STOP condition.

The register address is internally reset by the CMX655D/CMX655A TWI Slave to 0 at the end of each transfer when the STOP condition is detected. This feature allows the CMX655D/CMX655A Interrupt Status Register (ISR) to be immediately read without performing a prior write transaction to establish the register address (Figure 42).

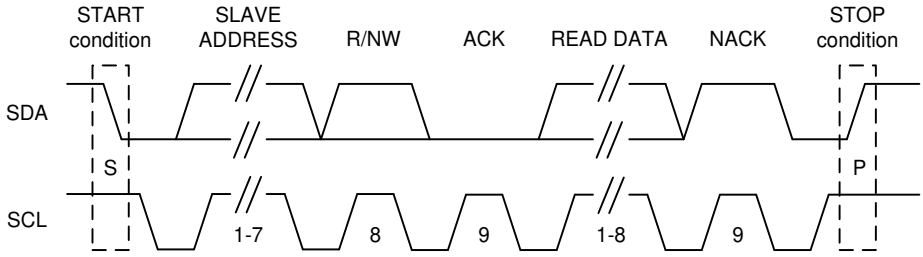


Figure 42 TWI Interrupt Status Register Read Transfer

The register address is automatically incremented by the CMX655D/CMX655A internally after each data byte is transferred to accommodate consecutive write (or read) address accesses within the same transfer with reduced protocol overhead as shown in Figure 43 and Figure 44.

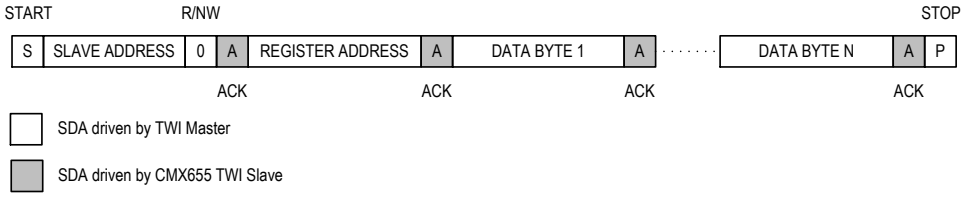


Figure 43 TWI N-Byte Write Transfer

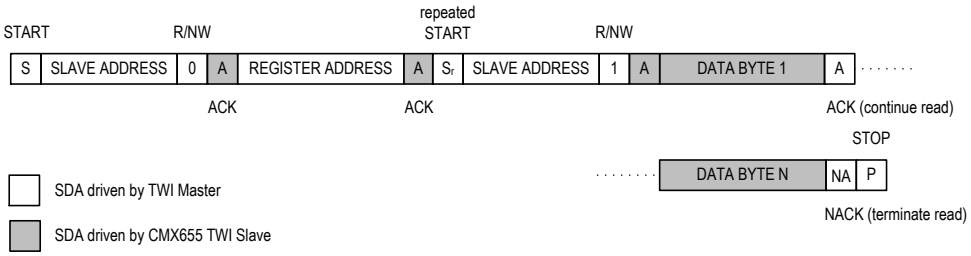


Figure 44 TWI N-Byte Read Transfer

It should be noted that the internal address saturates at $7F and does not auto-increment to wrap back around to $00.

5.8 Serial Audio Interface

The Serial Audio Interface (SAI) is used to transfer audio data between the CMX655D/CMX655A and an external device. The SAI is configured by the **SAICTRL** and **SAIMUX** registers and is enabled or disabled by the SAI bit in the **SYSCTRL** register. The **SAICTRL** register and the audio companding control bits in the **SAIMUX** register may only be changed while the SAI is disabled.

The CMX655D/CMX655A Serial Audio Interface may be configured to operate as either master or slave. If the CMX655D/CMX655A Serial Audio Interface is the master, the LRCLK/FS and BCLK pins are driven by the CMX655D/CMX655A as outputs. If the CMX655D/CMX655A Serial Audio Interface is the slave, the LRCLK/FS and BCLK pins are configured as inputs and both pins should be driven by the external device. The CMX655D/CMX655A Serial Audio Interface transmits serial audio data to the external device on the SDO output pin and receives serial audio data from the external device on the SDI input pin.

If the CMX655D/CMX655A Serial Audio Interface is disabled, the LRCLK/FS and BCLK pins as are configured as digital inputs with internal pull-up resistors connected to VDD_AD. The pull-up resistors are disabled when the CMX655D/CMX655A Serial Audio Interface is enabled by the external host. The CMX655D/CMX655A Serial Audio Interface may be configured to operate in several modes and supports the I2S, Left-Justified and PCM audio interface protocols.

Serial data is shifted MSB first in to the CMX655D/CMX655A on SDI and out of the CMX655D/CMX655A on SDO by a common bit clock BCLK. The CMX655D/CMX655A supports back-to-back data transfers in all audio transfer modes.

The standard audio data format is represented as a 16-bit signed number. If μ-law or A-law audio companding is selected then the audio data format transferred over the interface is an 8-bit compressed code. Audio companding is only permitted at a sample rate of 8ksps. The audio data output by the CMX655D/CMX655A for a disabled microphone channel is '0'.

By default, serial data changes on the falling edge of BCLK and is sampled on the rising edge of BCLK, though it is possible to configure the CMX655D/CMX655A to transfer data using the opposite edge of BCLK.

5.8.1 I2S Mode

The I2S interface consists of a Left/Right clock called LRCLK which has a frequency equal to the sample rate and is common to both input and output audio signal paths. The LRCLK low and high levels indicate if the audio data reflects the left or right channel. The Class-D amplifier is mono so only the left channel data on SDI is received. BCLK must have a frequency of at least 32xLRCLK for 16-bit signed audio data or at least 16xLRCLK for companded audio data. Serial data is in a left-justified format with the MSB being transmitted one clock cycle after LRCLK changes as shown in Figure .

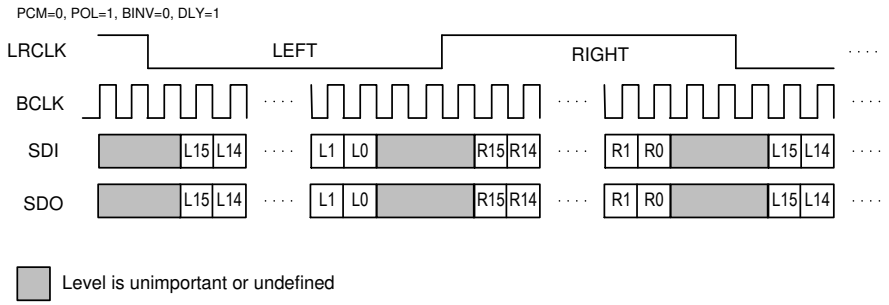


Figure 45 I2S Mode Data Transfer

5.8.2 Left-Justified Mode

Left-Justified mode is similar to I2S mode except that the polarity of the LRCLK signal is inverted and the MSB of the serial data in transferred in the first cycle following the LRCLK transition, one cycle earlier than I2S mode. Figure 46 shows a Left-Justified mode transfer.

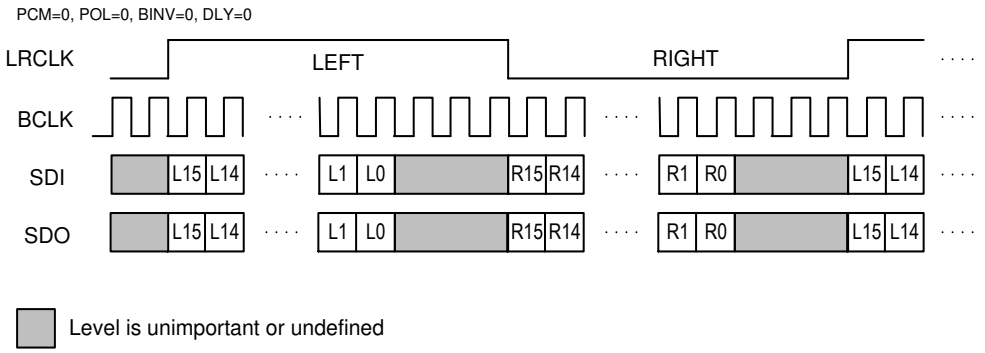


Figure 46 Left-Justified Mode Data Transfer

5.8.3 PCM Mode

The PCM Mode is a common interface protocol compatible with standard DSP devices for transferring PCM data. A frame sync signal (FS) is used to indicate the audio sample rate and serial data is transferred using a left-justified format. The FS signal is a single BCLK period wide and the MSB of left channel serial data may be configured to be transferred in the first or second cycle following the FS transition. When transferring two channels, the left channel data is first transferred followed by the right channel data. When transferring two channels, BCLK must have a frequency of at least 32xLRCLK for 16-bit signed audio data or at least 16xLRCLK for companded audio data. When transferring a single channel, BCLK must have a frequency of at least 16xLRCLK for 16-bit signed audio data or at least 8xLRCLK for companded audio data. Figure 47 shows an example 2-channel 16-bit PCM mode transfer with different configuration parameters.

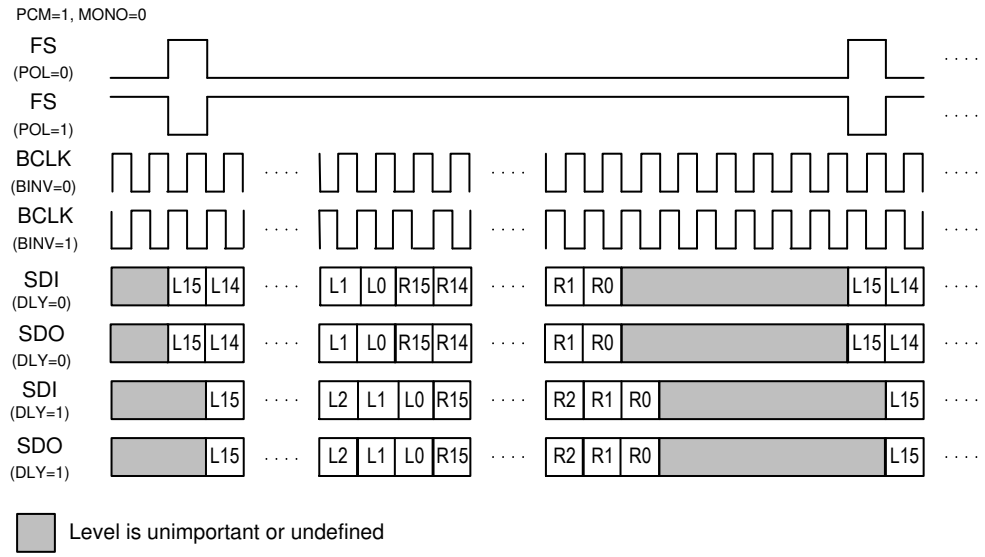


Figure 47 PCM Mode Dual-channel Data Transfer

Figure 48 shows an example of a single-channel 16-bit PCM mode transfer with different configuration parameters.

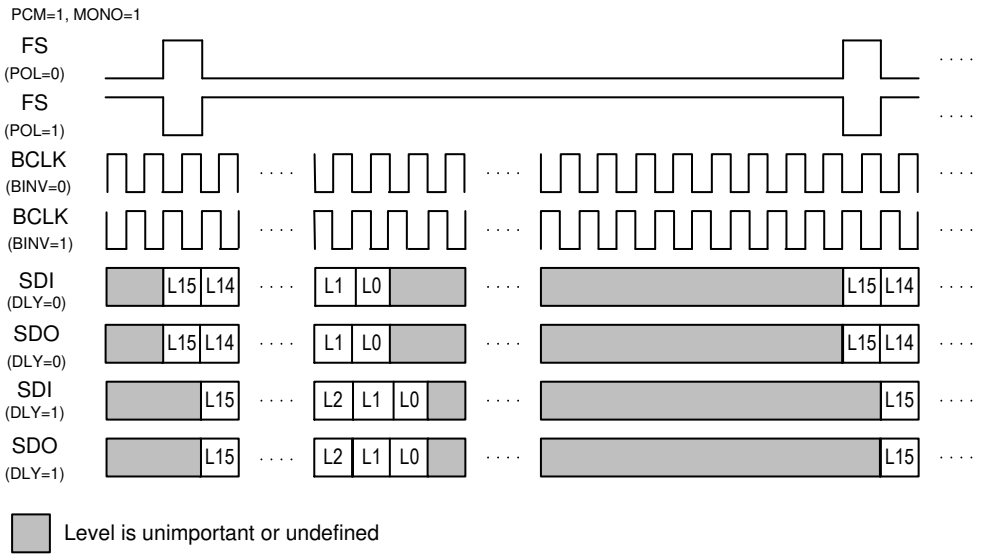


Figure 48 PCM Mode Single-channel Data Transfer

5.8.4 Audio Companding

If the audio sample rate is 8ksps, data may be optionally companded using 8-bit μ-law or A-law encoding by appropriately programming the COMP and ALAW control bits in the **SAIMUX** register. The 8-bit compressed audio data samples may be transported over the interface using half the number of BCLK cycles than standard 16-bit signed data. Any surplus LSBs transmitted by the CMX655D/CMX655A on SDO are set to '0'. The **SAIMUX** register companding control bits may only be modified while the SAI is disabled. An example of companded data transfer using the CMX655D/CMX655A as a PCM slave is shown in Figure 49.

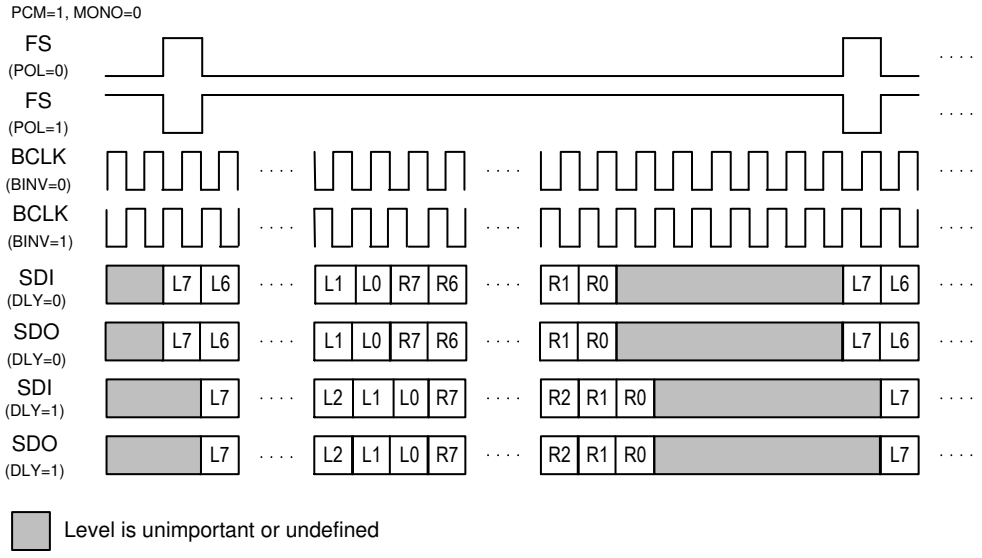


Figure 49 PCM Slave Mode Dual-channel Companded Data Transfer

5.8.5 Serial Audio Interface Registers

SAICTRL ($09)
Serial Audio Interface Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
MSTR	WL	MONO	DLY	POL	BINV	0	PCM

MSTR **Serial Audio Interface Master**
0 CMX655D/CMX655A is the slave and the external master drives LRCLK/FS and BCLK
1 CMX655D/CMX655A is the master and drives LRCLK/FS and BCLK

WL **Word length per channel transmitted by the CMX655D/CMX655A if MSTR=1**
0 16-bits for standard data or 8-bits for companded data
1 32-bits for standard data or 16-bits for companded data

MONO **Mono Data (only applicable if PCM=1)**
0 Frame contains both left and right data
1 Frame contains only left data

DLY **Data Delay**
0 SDI/SDO are latched/valid on the 1st BCLK edge following the LRCLK/FS transition
1 SDI/SDO are latched/valid on the 2nd BCLK edge following the LRCLK/FS transition

POL **Polarity**
0 If PCM=0, Left data if LRCLK=1 and right data if LRCLK=0.
If PCM=1, Start of frame indicated by FS=1.
1 If PCM=0, Left data if LRCLK=0 and right data if LRCLK=1.
If PCM=1, Start of frame indicated by FS=0.

BINV **BCLK Invert**
0 SDI/SDO and LRCLK/FS change on the negative edge of BCLK.
SDI/SDO latched/valid on the positive edge of BCLK.
1 SDI/SDO and LRCLK/FS change on the positive edge of BCLK.
SDI/SDO latched/valid on the negative edge of BCLK.

PCM **PCM Mode**
0 The LRCLK/FS phase is used to indicate Left or Right channel data
1 The LRCLK/FS is used for frame synchronization and serial data is always left-justified

The sample bit-width is 16-bits for standard data and 8-bits for companded data.

For non-PCM modes (PCM = 0) the transmitted word length may be greater than or less than or equal to the sample bit-width.

For PCM slave mode (PCM = 1, MSTR=0) the transmitted word length must be equal to the sample-bit width.

If the transmitted word length is less than the sample bit-width, the non-received input word LSBs are set to zero internally and the output word LSBs are not transmitted.
If the transmitted word length is greater than the sample bit-width, the surplus received input LSBs are ignored and the surplus transmitted output LSBs are set to zero.

SAIMUX ($0A)
Serial Audio Interface Mux (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0		ALAW	COMP	AMP		MIC	

ALAW	**Companding Law**
0	µ-Law
1	A-Law

COMP	**Companding Enable (requires CLKCTRL.SR=0)**
0	Companding disabled at 8ksps (16-bit data)
1	Companding enabled at 8ksps (8-bit data)

AMP	**Amplifier Input Data**
0	Left data
1	Right data
2-3	Mean of left and right data

MIC	**Microphone Output Data**
0	Left data is microphone left channel, right data is microphone right channel
1	Left data is microphone right channel, right data is microphone left channel
2	Left and right data are microphone left channel
3	Left and right data are microphone right channel

5.9 Interrupt Status and IRQN Pin

The active low IRQN pin is driven low when an interrupt status request bit in the **ISR** register is high and the associated interrupt status mask bit in the **ISM** register is set high. The **ISR** register interrupt status bits are cleared down when the **ISR** register is read. Some of the interrupt status events may be optionally enabled using the **ISE** register.

5.9.1 Interrupt Registers

ISR ($00)
Interrupt Status Register (R)
Reset Value: $00

7	6	5	4	3	2	1	0
CAL	VOL	THERM	CLKRDY	AMPCLIP	AMPOC	MICL	MICR

If a bit is set to 1, it indicates that the corresponding event has occurred.

CAL DC-offset calibration completed.
VOL Volume gain adjustment completed.
THERM Thermal warning indication (auto power amplifier shut-off).
CLKRDY Main clock ready – this bit is set once the clock status goes from inactive to active.
AMPCLIP Class-D amplifier output clipping (saturation) detected.
AMPOC Class-D amplifier overload current detected (auto power amplifier shut-off).
MICL Microphone left channel level has exceeded threshold.
MICR Microphone right channel level has exceeded threshold.

The ISR register is automatically cleared to 0 when read.

If CAL is set to 1, the CAL **ISE** register bit is automatically cleared to 0. The CAL **ISE** register bit may not be set again until the CAL **ISR** register bit has been cleared to 0.

If VOL is set to 1, the VOL bit in the **ISE** register is automatically cleared to 0 thereby preventing further VOL interrupt events from being generated. The VOL bit in the **ISE** register may not be set again until the VOL **ISR** register bit has been cleared to 0.

If THERM or AMPOC is set to 1, the PAMP **SYSCTRL** register bit is automatically cleared thereby disabling the power-amplifier and preventing further generation THERM or AMPOC interrupt events. The PAMP **SYSCTRL** register bit may not be set to 1 again until THERM and AMPOC **ISR** register bits have been cleared to 0.

If AMPCLIP is set to 1, the AMPCLIP **ISE** register bit is automatically cleared to 0 thereby preventing the clipping detection circuit from generating further AMPCLIP interrupt events. The AMPCLIP **ISE** register bit may not be set again until the AMPCLIP **ISR** register bit has been cleared to 0.

If MICL/MICR is set to 1, the MICL/MICR **ISE** register bit is automatically cleared to 0 thereby preventing the left/right channel record level detection block from generating further MICL/MICR interrupt events. The MICL/MICR **ISE** register bit may not be set again until the MICL/MICR **ISR** register bit has been cleared to 0.

ISM ($01)
Interrupt Status Mask (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
CAL	VOL	THERM	CLKRDY	AMPCLIP	AMPOC	MICL	MICR

Interrupt request mask for the interrupt status bits in the **ISR** register.
If a bit is set to 0, the corresponding **ISR** bit has no effect on the IRQN pin.
If a bit is set to 1, the IRQN pin will go low if the corresponding **ISR** bit is 1.

ISE ($02)
Interrupt Status Enable (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
CAL	VOL	0	0	AMPCLIP	0	MICL	MICR

CAL **DC-offset Calibration Interrupt Enable**
0 CAL interrupt disabled.
1 CAL interrupt enabled. The DC-offset calibration process is initiated and on completion will set **ISR** CAL bit to 1.
CAL is automatically cleared to 0 when **ISR** CAL bit is set to 1.

VOL **Volume Interrupt Enable**
0 VOL interrupt disabled. Volume gain adjustment completion will not set **ISR** VOL bit to 1.
1 VOL interrupt enabled. Volume gain adjustment completion will set **ISR** VOL bit to 1.
VOL is automatically cleared to 0 when **ISR** VOL bit is set to 1.

AMPCLIP **Amplifier Clipping Interrupt Enable**
0 AMPCLIP interrupt disabled. A clipping event will not set **ISR** AMPCLIP bit to 1.
1 AMPCLIP interrupt enabled. A clipping event will set **ISR** AMPCLIP bit to 1.
AMPCLIP is automatically cleared to 0 when **ISR** AMPCLIP bit is set to 1.

MICL **Microphone Left Channel Level Detection Interrupt Enable**
0 MICL interrupt disabled. A left channel level detection event will not set **ISR** MICL bit to 1.
1 MICL interrupt enabled. A left channel level detection event will set **ISR** MICL bit to 1.
MICL is automatically cleared to 0 when **ISR** MICL bit is set to 1. This bit is equivalent to and its state is always the same as that of the LEN bit in the **LDCTRL** register.

MICR **Microphone Left Channel Level Detection Interrupt Enable**
0 MICR interrupt disabled. A right channel level detection event will not set **ISR** MICR bit to 1.
1 MICR interrupt enabled. A right channel level detection event will set **ISR** MICR bit to 1.
MICR is automatically cleared to 0 when **ISR** MICR bit is set to 1. This bit is equivalent to and its state is always the same as that of the REN bit in the **RDCTRL** register.

5.10 System Control

The Serial Audio Interface, Lineout, Power amplifier and digital/analogue Microphone channels are enabled using the **SYSCTRL** register. The main clock must first be configured as described in section 5.3 and activated using the **COMMAND** register before **SYSCTRL** may be modified.

5.10.1 System Control Registers

SYSCTRL ($32)
System Control (R/W)
Reset Value: $00

7	6	5	4	3	2	1	0
0	ADCSR	SAI	LOUT	PAMP	AMIC	MICL	MICR

ADCSR **ADC Sample Rate (applicable when AMIC=1 for 16/32/48ksps audio sample rates)**
0 2.048Msps for 8/16/32ksps, 3.072Msps for 48ksps.
1 2.048Msps for 8ksps, 4.096Msps for 16/32ksps, 6.144Msps for 48ksps.

SAI **Serial Audio Interface**
0 Serial Audio Interface disabled.
1 Serial Audio Interface enabled.

LOUT **Lineout**
0 Lineout disabled.
1 Lineout enabled.

PAMP	Power Amplifier
0	Power amplifier disabled.
1	Power amplifier enabled. PAMP is automatically cleared to 0 if the **ISR** AMPOC or THERM bits are set to 1.

AMIC	Analogue Microphone Select
0	Digital microphone selected.
1	Analogue microphone selected.

MICL	Microphone Left Channel
0	Microphone left channel disabled.
1	Microphone left channel enabled.

MICR	Microphone Right Channel
0	Microphone right channel disabled.
1	Microphone right channel enabled.

COMMAND ($33)
Command Register (W)
Reset Value: $00

7	6	5	4	3	2	1	0
CMD							

CMD	Command
$00	Clock Stop.
$01	Clock Start.
$02-$FE	Reserved.
$FF	Soft Reset (sets all registers back to their reset value).

This register will always be read back as 0.

5.11 Register Address Map

All device registers are byte addressable. Programmable fields that occupy consecutive byte address locations will be updated with the new written value following a write to the least-significant address byte of the field which resides in the upper address location. Registers which require the main clock to be active are indicated by Yes in the Main Clock column of Table 16 and accesses to these registers should not be attempted if the main clock is inactive.

Table 16 Register Address Map

Address	Register	Description	Reset	R/W	Main Clock
Interrupt and Status					
$00	**ISR**	Interrupt Status Register	$00	R	No
$01	**ISM**	Interrupt Status Mask	$00	R/W	No
$02	**ISE**	Interrupt Status Enable	$00	R/W	Yes
Clock & PLL					
$03	CLKCTRL	Clock Control	$00	R/W	No
$04	**RDIVHI**	R-Divider High Byte	$00	R/W	No
$05	RDIVLO	R-Divider Low Byte	$00	R/W	No
$06	NDIVHI	N-Divider High Byte	$00	R/W	No
$07	NDIVLO	N-Divider Low Byte	$00	R/W	No
$08	PLLCTRL	PLL Control	$00	R/W	No
Serial Audio Interface					
$09	**SAICTRL**	Serial Audio Interface Control	$00	R/W	Yes
$0A	**SAIMUX**	Serial Audio Interface Mux	$00	R/W	Yes
Record					
$0C	**RVF**	Record Voice Filters	$00	R/W	Yes
$0D	**LDCTRL**	Left Channel Detection Control	$00	R/W	Yes
$0E	**RDCTRL**	Right Channel Detection Control	$00	R/W	Yes
$0F	**LEVEL**	Record Level	$00	R/W	Yes
$18	**AGCRANGE**	AGC Range	$00	R/W	Yes

$19	**AGCPRE**	AGC Pre-amplifier Gain	$00	R/W	Yes
$1A	**AGCCTRL**	AGC Control	$00	R/W	Yes
$1B	**AGCTIME**	AGC Time	$00	R/W	Yes
$1C	**NGCTRL**	Noise Gate Control	$00	R/W	Yes
$1D	**NGTIME**	Noise Gate Time	$00	R/W	Yes
$1E	**NGLSTAT**	Noise Gate Left Channel Status	$00	R	Yes
$1F	**NGRSTAT**	Noise Gate Right Channel Status	$00	R	Yes
Playback					
$28	**PVF**	Playback Voice Filters	$00	R/W	Yes
$29	**PREAMP**	Playback Preamp Gain	$00	R/W	Yes
$2A	**VOLUME**	Playback Volume	$00	R/W	Yes
$2B	**ALCCTRL**	ALC Control	$00	R/W	Yes
$2C	**ALCTIME**	ALC Time	$00	R/W	Yes
$2D	**ALCGAIN**	ALC Make-up Gain	$00	R/W	Yes
$2E	**ALCSTAT**	ALC Status	$00	R	Yes
$2F	**DST**	Digital Side Tone Control	$00	R/W	Yes
$30	**CPR**	Click-and-Pop Reduction	$00	R/W	Yes
General System					
$32	**SYSCTRL**	System Control	$00	R/W	Yes
$33	**COMMAND**	Command Register	$00	W	No
Reserved					
$34	**RESERVED**	Not for customer use.	$29	R/W	Yes
$35	**RESERVED**	Not for customer use.	$40	R/W	Yes
$36	**RESERVED**	Not for customer use.	$80	R/W	Yes
$37	**RESERVED**	Not for customer use.	$80	R/W	Yes

Notes:

- All registers will retain data if VDD_AD pin is held high, even if all other power supply pins are disconnected.
- The data interface can run at a lower voltage than the Class D Amplifier section of the device by setting the VDD_AD supply to the required interface voltage, in the range 1.75 V to 3.6 V.
- The CLKCTRL register may only be modified if the main clock is inactive.
- If clock and data lines are shared with other devices VDD_AD must be maintained in its normal operating range otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK, MISO and MOSI pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

6 Application Notes

6.1 Programming Examples

6.1.1 Start-up

- Reset the device by powering-up the VDD_AD and VDD_PA unregulated supplies ensuring that the control port (SPIS pin) is configured as required.

- Configure the main clock and system sample rate and then start the main clock.

R/W	Register	Address	Data	Notes
W	**CLKCTRL**	$03	$20	16ksps, RCLK at 24.576MHz is main clock.
W	**ISM**	$01	$10	IRQN will to go low when the main clock is ready.
W	**COMMAND**	$33	$01	Start the main clock.

- Wait for the IRQN line to go low and then read the **ISR** register to confirm the main clock has gone active. Reading the **ISR** register will clear the CLKRDY bit.

R/W	Register	Address	Data	Notes
R	**ISR**	$00	$10	Expect CLKRDY bit set to 1.

If the CLKRDY **ISM** register bit is not set to 1, the **ISR** register may be polled until the CLKRDY bit is set.

6.1.2 DC-offset Calibration

Following device start-up, perform DC-offset calibration prior to using the analogue microphone interface.

- Enable the left and right analogue microphone record channels.

R/W	Register	Address	Data	Notes
W	**SYSCTRL**	$32	$07	Enable left and right analogue microphone record channels.

Note, after enabling the analogue microphone record channels, a settling period of 150ms should be allowed for the analogue circuits to stabilise before the calibration process is triggered.

- Trigger DC-offset calibration

R/W	Register	Address	Data	Notes
W	**ISM**	$01	$80	IRQN will go low when DC-offset calibration completed.
W	**ISE**	$02	$80	Enable CAL interrupt and trigger DC-offset calibration.

- Wait for the IRQN line to go low and then read the **ISR** register to confirm DC-offset calibration has completed. Reading the **ISR** register will clear the CAL bit.

R/W	Register	Address	Data	Notes
R	**ISR**	$00	$80	Expect CAL bit set to 1.

If the CAL **ISM** register bit is not set to 1, the **ISR** register may be polled until the CAL bit is set. DC-offset calibration takes ~3ms to complete.

Note, once calibration has been triggered by setting the **ISE** register CAL bit to 1, the configuration phase outlined in section 6.1.3 may commence. However, it is recommended to wait for calibration completion prior to enabling the SAI and playback channels as described in section 6.1.4.

6.1.3 Configuration

- Configure the Serial Audio Interface and record and/or playback channels.

R/W	Register	Address	Data	Notes
W	**SAICTRL**	$09	$98	I2S master mode.
W	**SAIMUX**	$0A	$08	Use the mean of left and right input data for playback.
W	**LEVEL**	$0F	$CC	Record level gains set to 0dB.
W	**VOLUME**	$2A	$D5	Playback volume gain set to -6dB with smoothing.
…	…	…	…	Configure audio signal processing blocks as required.

6.1.4 Enable Audio Channels

- Enable the Serial Audio Interface and record and/or playback channels.

R/W	Register	Address	Data	Notes
W	**SYSCTRL**	$32	$2F	Enable SAI, left and right analogue microphone record channels and the Class-D power-amplifier.

6.1.5 Shutdown

- Mute the playback volume if the Class-D amplifier is enabled.

R/W	Register	Address	Data	Notes
W	**VOLUME**	$2A	$80	Playback volume gain set to mute with smoothing.
W	**ISM**	$01	$40	IRQN will go low when volume adjustment completed.
W	**ISE**	$02	$40	Enable volume interrupt generation.

- Wait for the IRQN line to go low and then read the **ISR** register to confirm volume adjustment has completed. Reading the **ISR** register will clear the VOL bit.

R/W	Register	Address	Data	Notes
R	**ISR**	$00	$40	Expect VOL bit set to 1.

If the VOL **ISM** register bit is not set to 1, the **ISR** register may be polled until the VOL bit is set.

- Disable the Serial Audio Interface and record and/or playback channels and stop the main clock.

R/W	Register	Address	Data	Notes
W	**SYSCTRL**	$32	$00	Disable SAI and all record/playback channels.
W	**COMMAND**	$33	$00	Stop the main clock.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (VDD_AD - DGND) or (VDD_PA - VSS_PA)	-0.3	+3.6	V
Voltage on any pin to VSS_PA or DGND	-0.3	V_{max} + 0.3	V
Voltage between VSS_PA pins and DGND	-50	+50	mV
Current into or out of pins, connected to:			
VDD_AD, DGND	-100	+100	mA
VDD_PA, VSS_PA	-800	+800	mA

	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	2290	mW
Storage Temperature	-50	+125	°C
Operating Air Temperature (T_{AMB})	-40	+85	°C
Thermal Resistance R_{JC}		3	°C/W
Maximum Allowable Junction Temperature		125	°C

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. Case temperature refers to the temperature of the exposed paddle on the underside of the package. Careful layout of the PCB is essential for best performance.

7.1.2 Operating Limits

For the following conditions unless otherwise specified:
VSS_PA = DGND = 0V; and T_{AMB} = +25ºC.

	Notes	Min.	Max.	Units
Class-D Amplifier Supply (VDD_PA - VSS_PA)		2.7	3.6	V
Analogue/Digital Supply (VDD_AD - DGND)		1.75[2]	3.6	V

[2] Requires VDD_PA to be unpowered, otherwise 2.7V if VDD_PA is powered.

7.1.3 Operating Characteristics

7.1.3.1 DC Parameters

For the following conditions unless otherwise specified:
VDD_AD = 1.75V to 3.6V; VDD_PA =2.7V to 3.6V; VSS_PA = DGND = 0V; and T_{AMB} = +25ºC.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Standby - main clock enabled and sourced directly from RCLK			60		µA
Standby – main clock enabled and sourced directly from PLL	3		200		µA
Standby – main clock enabled and sourced directly from LPOSC			120		µA
Class-D Power Amplifier @ 1W output	4		1		mA
Class-D Lineout Amplifier @ 0.25mW output	5		0.6		mA
Stereo record channels with digital microphones and main clock sourced directly from RCLK	6		500		µA
Stereo record channels with analogue microphones and main clock sourced directly from RCLK	6		2		mA
Mono record channel with digital microphone and main clock sourced from internal LPOSC	7	-	300		µA
Mono record channel with digital microphone and main clock sourced directly from RCLK			500		µA
Logic ‘1’ Input Level					
VDD_AD = 1.8/2.5/3.3V		1.2/1.7/2.0	-	-	V
Logic ‘0’ Input Level					
VDD_AD = 1.8/2.5/3.3V		-	-	0.6/0.7/0.8	V
Logic ‘1’ Output Level		VDD_AD -0.4	-	-	V
Logic ‘0’ Output Level		-	-	0.4	V
Digital IO Source/Sink Current Limit	8				
VDD_AD = 1.8/2.5/3.3V			1.25/2.0/2.5		mA
SDA Sink Current Limit when SPIS=0 (I_{OL})					
VDD_AD = 1.8/2.5/3.3V			3.75/6.0/7.5		mA
Digital IO pin capacitance			2		pF

[3] PLL reference clock sourced from RCLK.

[4] 4Ω load with VDD_PA at 3.3V

[5] Load impedance of 18kΩ in parallel with 120pF.

[6] Normal operating mode @ 8ksps.

[7] Autonomous low-power listening mode @ 8ksps, Serial Audio Interface disabled.

[8] Applies to all digital pins when SPIS=1; applies to all digital pins except SDA when SPIS=0.

7.1.3.2 AC Parameters

For the following conditions unless otherwise specified:
VDD_AD = 1.75V to 3.6V; VDD_PA =2.7V to 3.6V; VSS_PA = DGND = 0V; and T_{AMB} = +25ºC.

AC Parameters	Notes	Min.	Typ.	Max.	Units
Class-D Power Amplifier					
Speaker Load		4			Ω
Output Power	9		1		W
Overload Current Protection			1.5		A
THD+N @ 48ksps	10,11		1		%
SNR @ 48ksps	10,12		81		dB
Efficiency @ 0.5W output power	10		91		%
Class-D Lineout Amplifier					
Speaker Load	13		18		kΩ
Output Power	13,14		0.25		mW
THD+N @ 48ksps	13,15		0.018		%
SNR @ 48ksps	13,16		76		dB
Microphone Digital Interface					
MICCLK Frequency[17]		2.048		3.072	MHz
MICCLK Duty Cycle			50		%
Microphone Analogue Interface					
PGL1/PGR1 Input Impedance		7.5		30	kΩ
PGL1/PGR1 Gain Range	18	15		28	dB
PGL1/PGR1 Gain Step	18		1		dB
PGL2/PGR2 Input Impedance		275		1375	kΩ
PGL2/PGR2 Gain Range		-6		12	dB
PGL2/PGR2 Gain Step			6		dB
ADC Input Voltage Level			2.1		Vpp
SINAD @ 48ksps	19		86		dB
Peak SNR @ 48ksps	20		90		dB

[9] Average power into 4Ω load, VDD_AD = VDD_PA = 3.3V with max input level.
[10] With 8Ω load, VDD_AD = VDD_PA = 3.3V.
[11] A-weighted, 20Hz–20kHz, 0.5W output power.

[13] Nominal lineout load impedance is 18kΩ in parallel with 120pF.
[14] Average power into nominal load impedance, VDD_AD = VDD_PA = 3.3V with max input level.
[15] A-weighted, 20Hz–20kHz, VDD_AD = VDD_PA = 3.3V, 0.25mW output power.

[17] Not guaranteed for LPOSC.
[18] Figures assume 200Ω source impedance.
[19] ADC sample rate at 3.072Msps. 1kHz input tone
[20] ADC sample rate at 3.072Msps. 1kHz input tone

AC Parameters	Notes	Min.	Typ.	Max.	Units
Automatic Gain Control					
Minimum Gain		9		24	dB
Gain Span		12		27	dB
Threshold Level		-18		-3	dBFS
Threshold Step			1		dB
Hold Time		50		400	ms
Attack Time		0.125		256	ms
Release Time		0.064		8.192	s
Record Level Control					
Gain Range		-12		3	dB
Gain Step			1		dB
Noise Gate					
Gain Range		-31		0	dB
Gain Step			1		dB
Threshold Level		-63		-32	dBFS
Threshold Step			1		dB
Expansion Ratio		1:2		1:4	
Attack Time		1.5		96	ms
Release Time		0.06		7.68	s
Automatic Level Control					
Gain Range		0		12	dB
Gain Step			1		dB
Threshold Level		-31		0	dBFS
Threshold Step			1		dB
Compression Ratio		1:1.5		1:∞	
Attack Time		1.5		96	ms
Release Time		0.06		7.68	s
Playback Volume Control					
Gain Range		-90		0	dB
Gain Step			1		dB
Playback Preamplifier					
Gain Range		0		18	dB
Gain Step			6		dB
Digital Sidetone					
Gain Range		-62		0	dB
Gain Step			2		dB
Phase Delay:	21				ms
8ksps			2.9		
16ksps			1.44		
32ksps			0.74		
48ksps			0.49		
Reference Clock					
RCLK Frequency Range		0.008	-	80	MHz
Duty Cycle		40:60		60:40	
Jitter	22				ps

[21] Microphone input to speaker output with 1kHz tone.

[22] RMS, cycle to cycle.

AC Parameters	Notes	Min.	Typ.	Max.	Units
Record Digital High Pass Filter					
4th Order Butterworth Stopband - 3dB point:					Hz
HPSEL = 1			0.003125 x f_s		
HPSEL = 2			0.01875 x f_s		
HPSEL = 3			0.0375 x f_s		
Record Digital Low Pass Filter					
4th Order Butterworth Passband - 3dB point			0.4375 x f_s		Hz
Record DC Blocking Filter					
DC Attenuation			90		dB
Playback Digital High Pass Filter					
4th Order Butterworth Stopband - 3dB point:					Hz
HPSEL = 1			0.003125 x f_s		
HPSEL = 2			0.01875 x f_s		
HPSEL = 3			0.0375 x f_s		
Playback Digital Low Pass Filter					
4th Order Butterworth Passband - 3dB point			0.4375 x f_s		Hz
Playback DC Blocking Filter					
DC Attenuation			90		dB
PLL					
Start-up Time	23		10		ms
Low Power Oscillator					
Start-up Time	23		2		µs
Oscillator Clock Frequency		TBC	24.576	30	MHz

23 Following the Clock Start command.

7.1.3.3 SPI

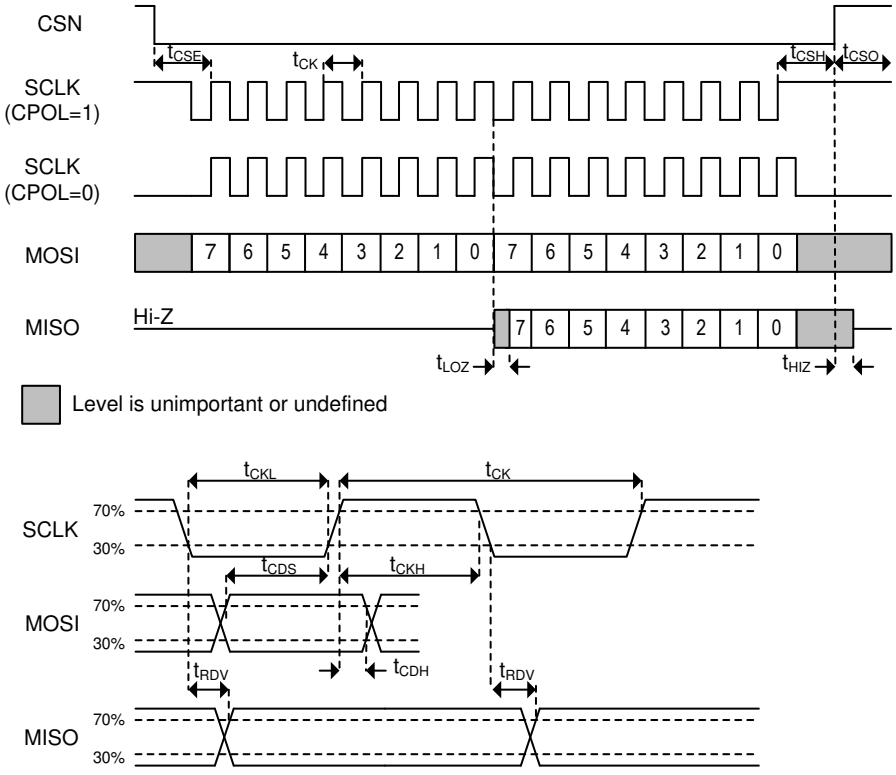


Figure 50 SPI Timing Diagram

Table 17 SPI Timing Parameter Values

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	CSN enable to clock high time	100	-	-	ns
t_{CSH}	Last clock high to CSN high time	100	-	-	ns
t_{LOZ}	Clock low to reply output enable time	0	-	-	ns
t_{HIZ}	CSN high to reply output 3-state time	-	-	25[24]	ns
t_{CSO}	CSN high time between transactions	100	-	-	ns
t_{CK}	Clock cycle time	100	-	-	ns
t_{CKH}	Serial clock high time	50	-	-	ns
t_{CKL}	Serial clock low time	50	-	-	ns
t_{CDS}	Command data set-up time (MOSI)	20	-	-	ns
t_{CDH}	Command data hold time (MOSI)	10	-	-	ns
t_{RDV}	Reply data valid time (MISO)	-	-	25[24]	ns

[24] Maximum figure quoted for 10pF load on MISO.

7.1.3.4 TWI

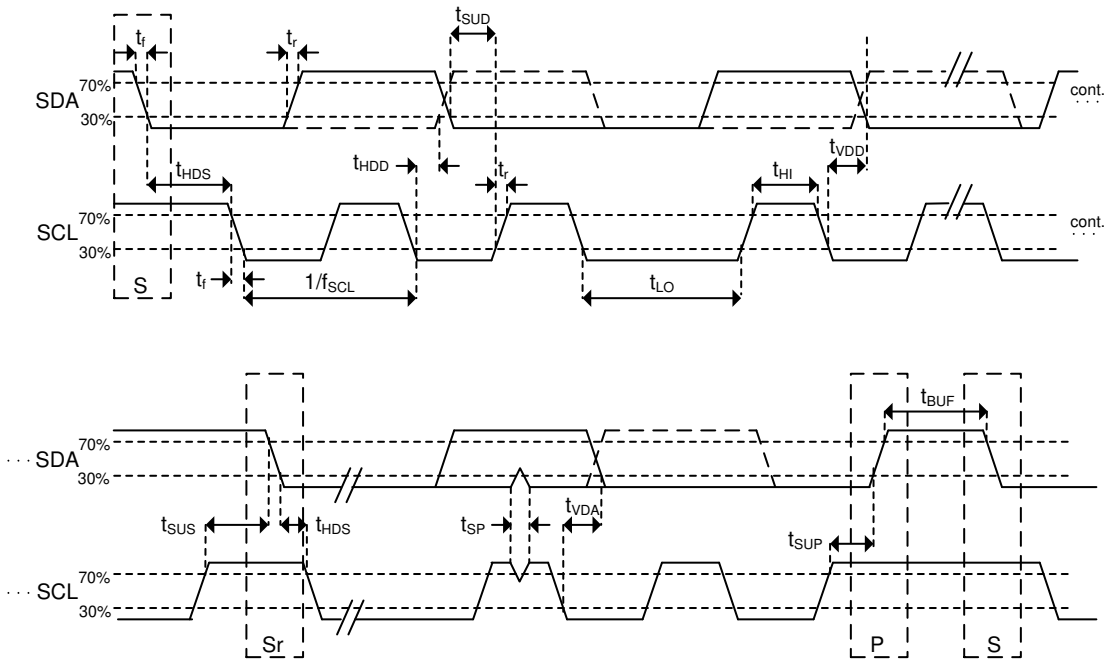


Figure 51 TWI Timing Diagram

Table 18 TWI Standard Mode Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency	0	-	100	kHz
t_{HDS}	Hold time (repeated) START condition	4.9	-	-	µs
t_{LO}	Low period of SCL	4.7	-	-	µs
t_{HI}	High period of SCL	4.0	-	-	µs
t_{SUS}	Set-up time for repeated START condition	4.7	-	-	µs
t_{HDD}	Data hold time measured from falling edge of SCL	0	-	-	µs
t_{SUD}	Data set-up time measured from rising edge of SCL	0.25	-	-	µs
t_r	Rise time of SDA and SCL	-	-	1	µs
t_f	Fall time of SDA and SCL	-	-	0.3	µs
t_{SUP}	Set-up time for STOP condition	4.0	-	-	µs
t_{BUF}	Bus-free time between a STOP and START condition	4.7	-	-	µs
t_{VDD}	Data valid time	-	-	3.45	µs
t_{VDA}	Data valid acknowledge time	-	-	3.45	µs
t_{SP}	Pulse Width of Suppressed Spike	0	-	50	ns

Table 19 TWI Fast Mode Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency	0	-	400	kHz
t_{HDS}	Hold time (repeated) START condition	0.6	-	-	µs
t_{LO}	Low period of SCL	1.3	-	-	µs
t_{HI}	High period of SCL	0.6	-	-	µs
t_{SUS}	Set-up time for (repeated) START condition	0.6	-	-	µs
t_{HDD}	Data hold time measured from falling edge of SCL	0	-	-	µs
t_{SUD}	Data set-up time measured from rising edge of SCL	0.1	-	-	µs
t_r	Rise time of SDA and SCL	-	-	0.3	µs
t_f	Fall time of SDA and SCL	-	-	0.3	µs
t_{SUP}	Set-up time for STOP condition	0.6	-	-	µs
t_{BUF}	Bus-free time between a STOP and START condition	1.3	-	-	µs
t_{VDD}	Data valid time	-	-	0.9	µs
t_{VDA}	Data valid acknowledge time	-	-	0.9	µs
t_{SP}	Pulse Width of Suppressed Spike	0	-	50	ns

Table 20 TWI Pull-up Resistors and Bus Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Units
R_p	Pull-up resistor for each bus line	R_{pmin}	-	R_{pmax}	Ω
C_b	Capacitive load for each bus line	-	-	400	pF

Equation 1 shows the maximum value of the pull-up resistor (R_{pmax}) is a function of the estimated bus capacitance (C_b) and the maximum rise time (t_r) specified in Table 18 and Table 19:

Equation 1 Maximum Pull-up Resistor Value

$$R_{p\max} = \frac{t_r}{0.8473 \times C_b}$$

The CMX655D/CMX655A supply voltage (VDD_AD) and sink current capability (I_{OL}) limit the minimum value of the pull-up resistor (R_{pmin}) as shown in Equation 2:

Equation 2 Minimum Pull-up Resistor Value

$$R_{p\min} = \frac{VDD\_AD}{I_{OL}}$$

The value of I_{OL} is provided in 7.1.3.1.

7.1.3.5 SAI

Figure 52 shows LRCLK/FS, SDO and SDI sampled on the rising edge of BCLK. The timing parameters also apply if the sense of BCLK is inverted.

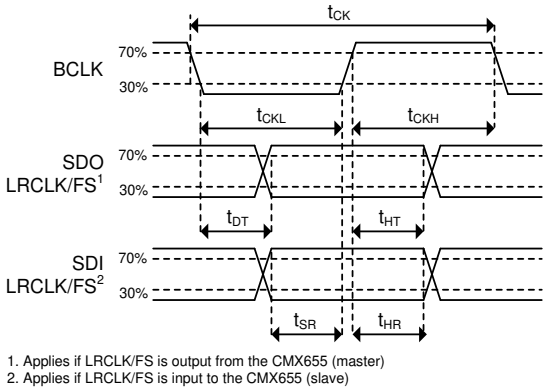


Figure 52 SAI Timing Diagram

Table 21 SAI Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CK}	Clock period.	270	-	-	ns
t_{CKL}	Clock low-time.	135	-	-	ns
t_{CKH}	Clock high-time.	135	-	-	ns
t_{DT}	Transmit data delay time.	-	-	25[25]	ns
t_{HT}	Transmit data hold time.	135	-	-	ns
t_{SR}	Receive data set-up time.	55	-	-	ns
t_{HR}	Receive data hold time.	0	-	-	ns

7.1.3.6 Digital Microphone Interface

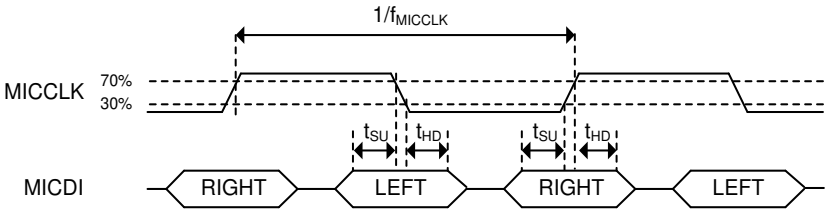


Figure 53 Digital Microphone Timing Diagram

Table 22 Digital Microphone Timing Parameters

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
f_{MICCLK}	MICCLK frequency @ 8/16/32ksps	26	-	2.048	-	MHz
	MICCLK frequency @ 48ksps	27	-	3.072	-	MHz
t_{SU}	MICDI set-up time before rising/falling MICCLK		20	-	-	ns
t_{HD}	MICDI hold time after rising/falling MICCLK		0	-	-	ns

[25] Maximum figure quoted for 10pF load on SDO.

[26] If operating from LPOSC then MICCLK = LPOSC/12 so for 30 MHz maximum LPOSC the maximum MICCLK frequency is 2.5 MHz.

[27] If operating from LPOSC then MICCLK = LPOSC/8 so for 30 MHz maximum LPOSC the maximum MICCLK frequency is 3.75 MHz.

7.2 Typical Performance Characteristics

For the graphs in this section, the following conditions apply:
VDD_PA = VDD_A = 3.3V. T_{AMB} = 25°C

7.2.1 THD+N vs. Level performance

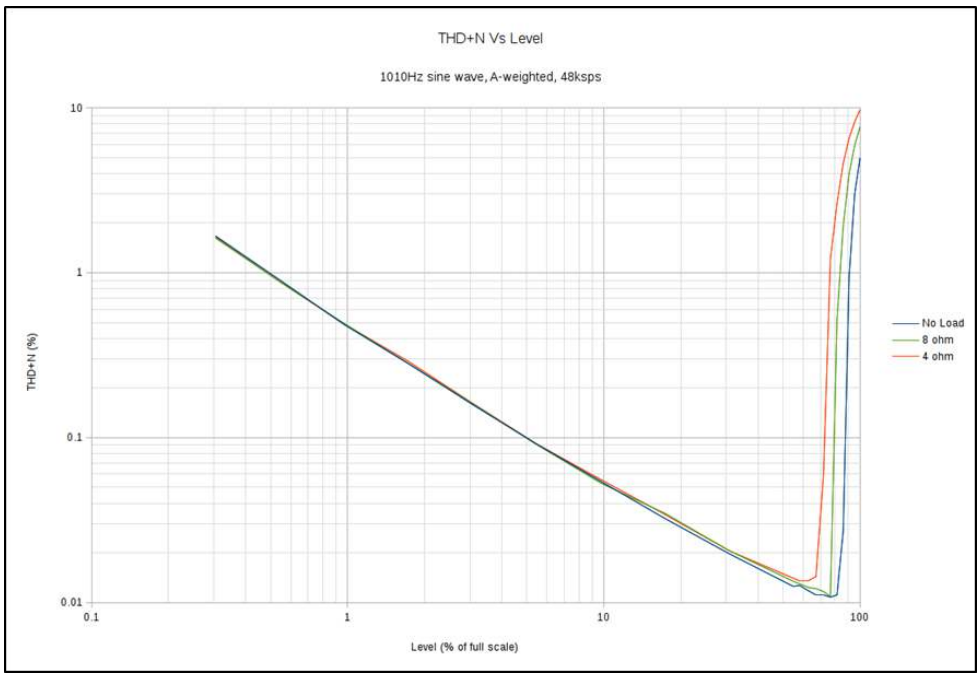


Figure 54 Class D amplifier THD+N vs. Level 48ksps

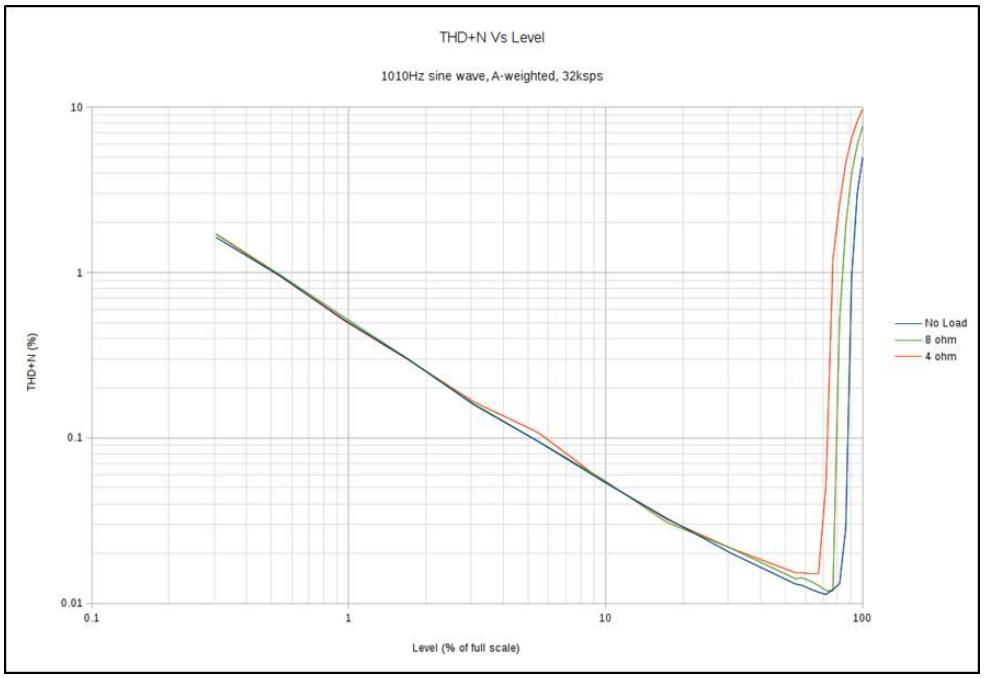


Figure 55 Class D amplifier THD+N vs. Level 32ksps

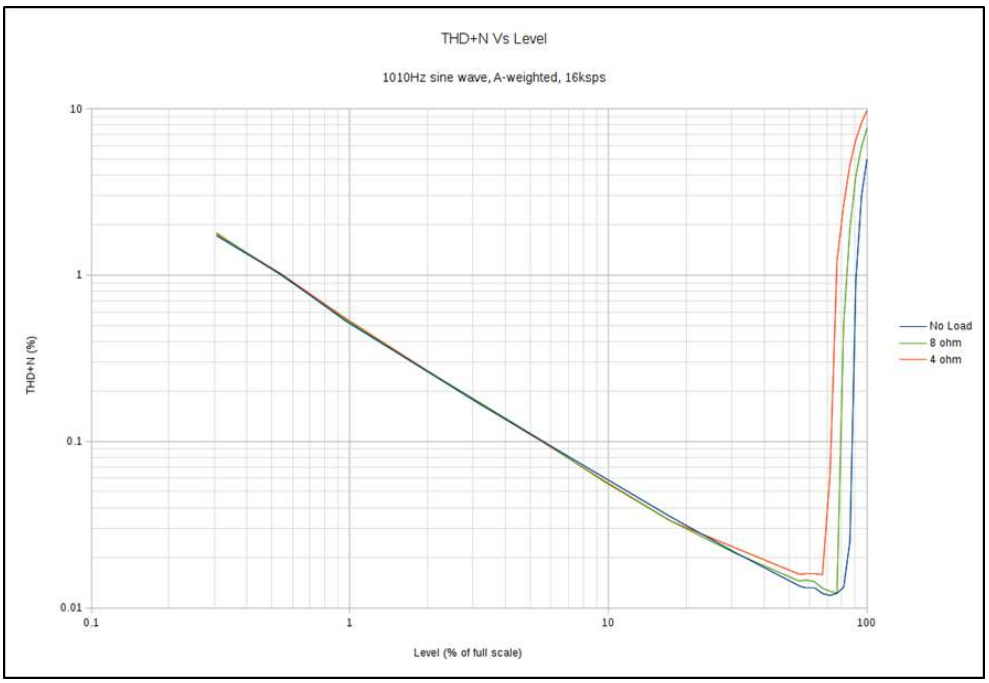


Figure 56 Class D amplifier THD+N vs. Level 16ksps

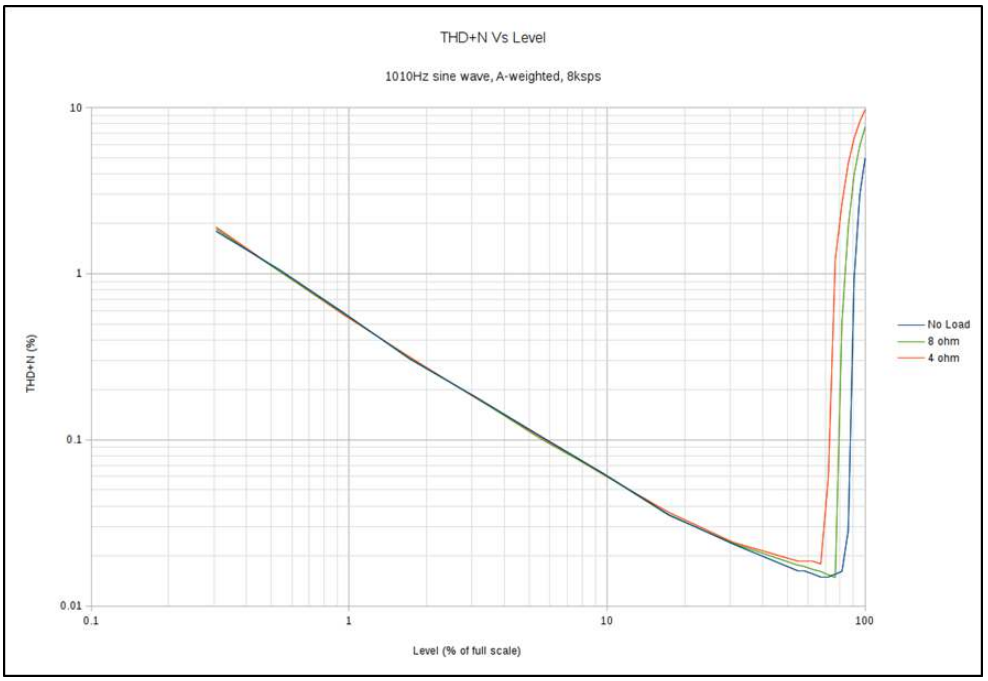


Figure 57 Class D amplifier THD+N vs. Level 8ksps

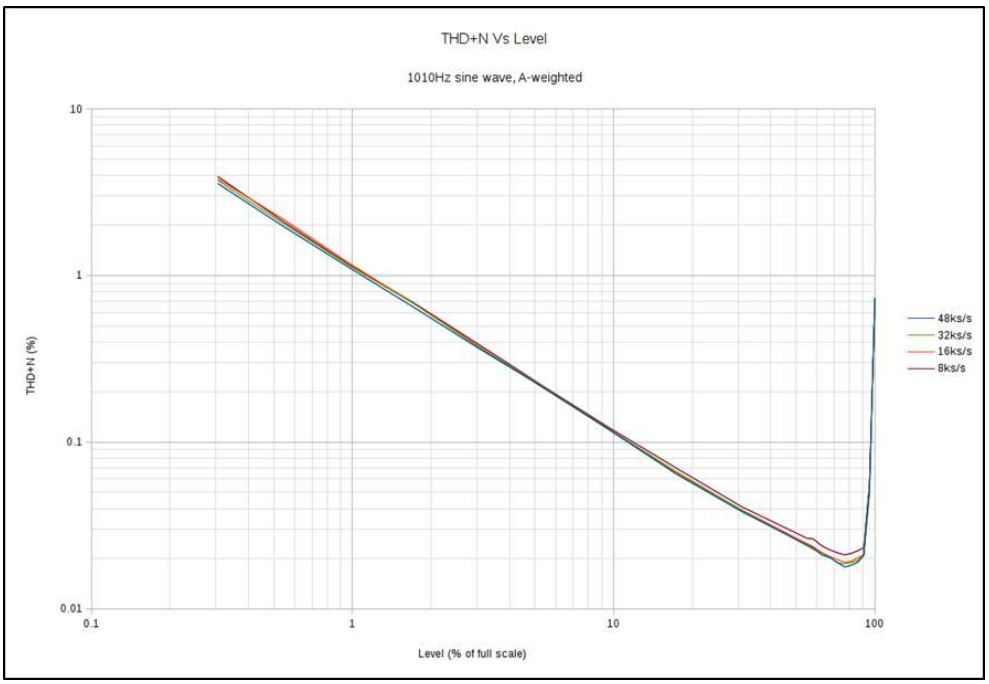


Figure 58 Line out amplifier THD+N vs. Level 48/32/16/8ksps

7.2.2 THD+N vs. Frequency performance

As the A-weighted filter does not produce a flat response across the audio bandwidth the frequency vs THD+N plots have been reported with no filter applied.

The results are also limited to ~6666Hz to ensure the 3rd harmonic was inside the measurement bandwidth of 20kHz

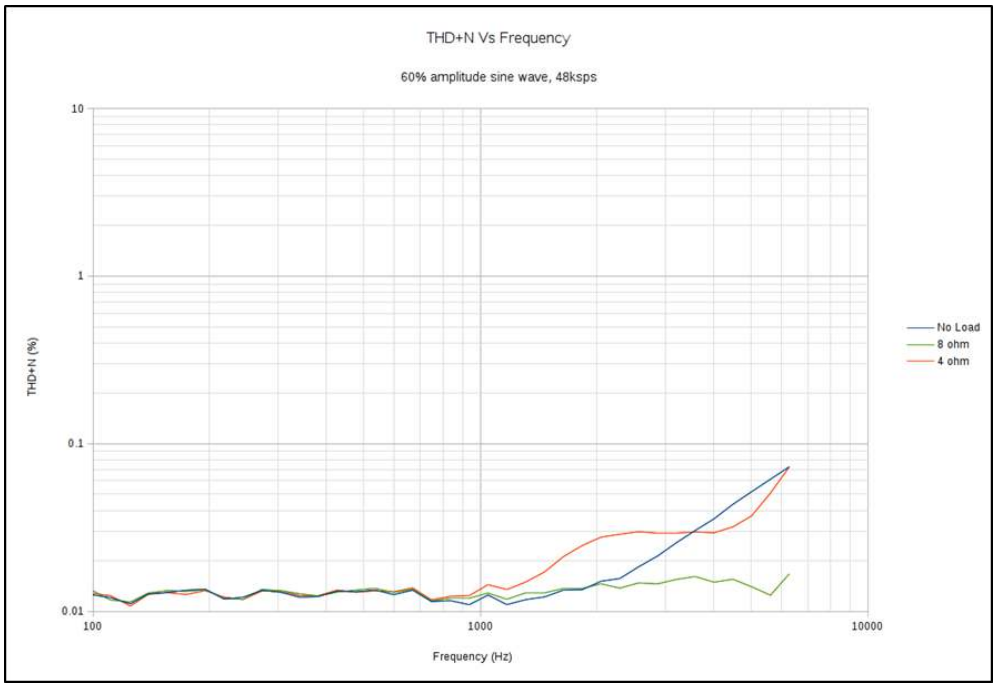


Figure 59 Class D amplifier THD+N vs. Frequency 48ksps

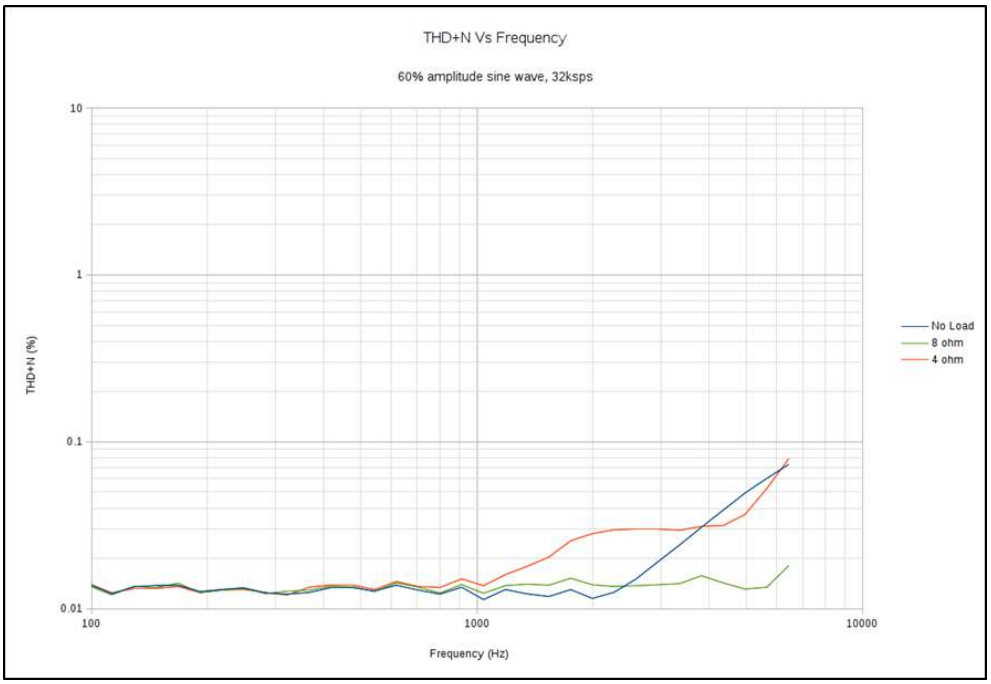


Figure 60 Class D amplifier THD+N vs. Frequency 32ksps

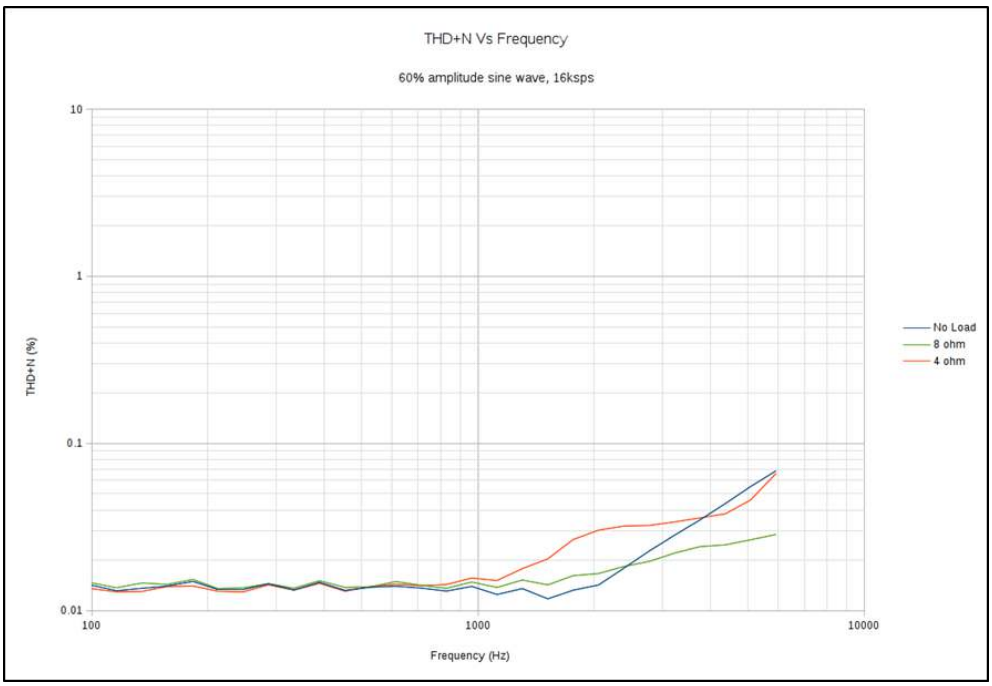


Figure 61 Class D amplifier THD+N vs. Frequency 16ksps

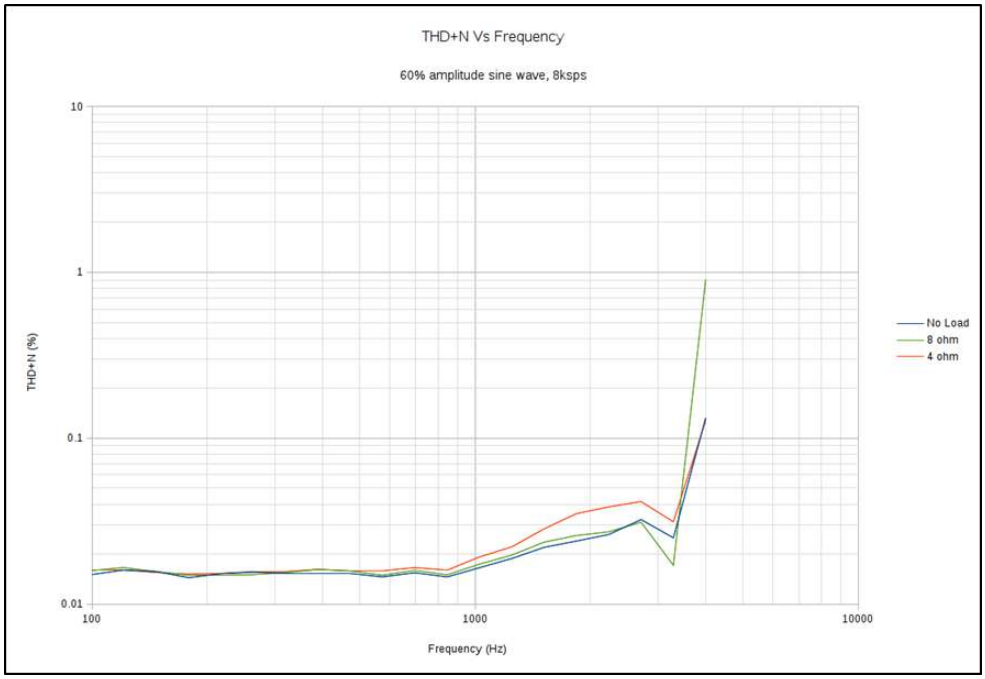


Figure 62 Class D amplifier THD+N vs. Frequency 8ksps

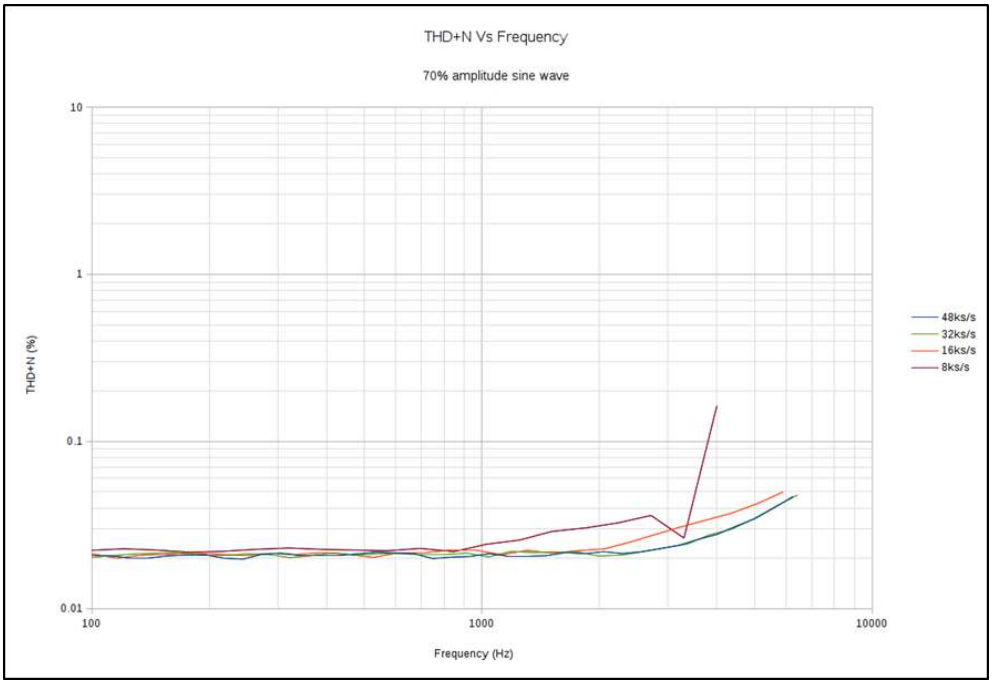


Figure 63 Line out amplifier THD+N vs. Frequency 48/32/16/8ksps

7.2.3 Class D Amplifier Efficiency

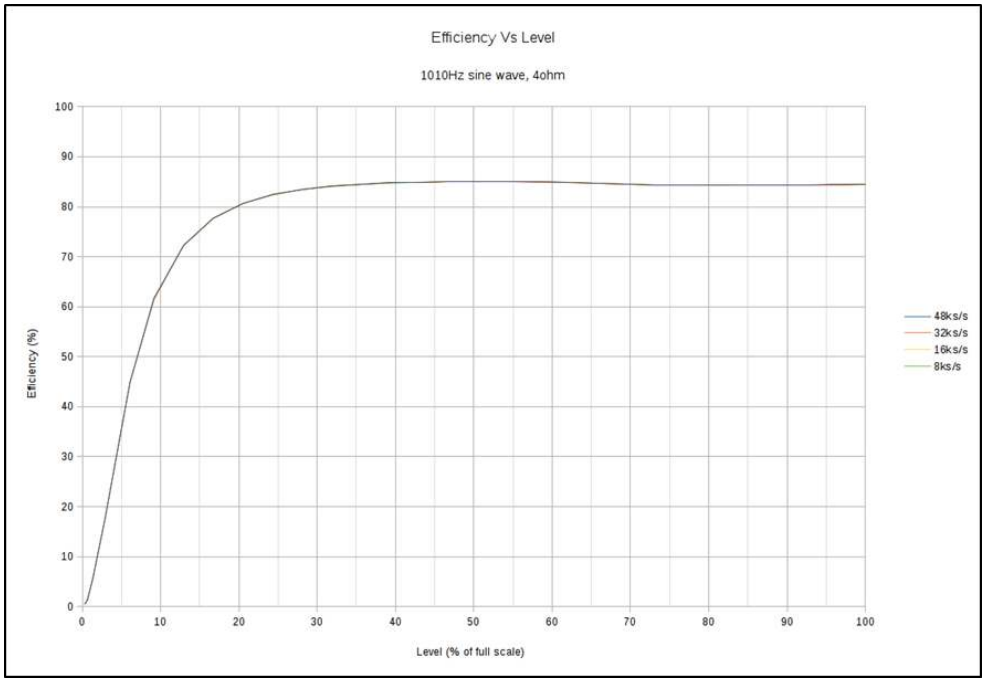


Figure 64 Class D amplifier efficiency 4Ω

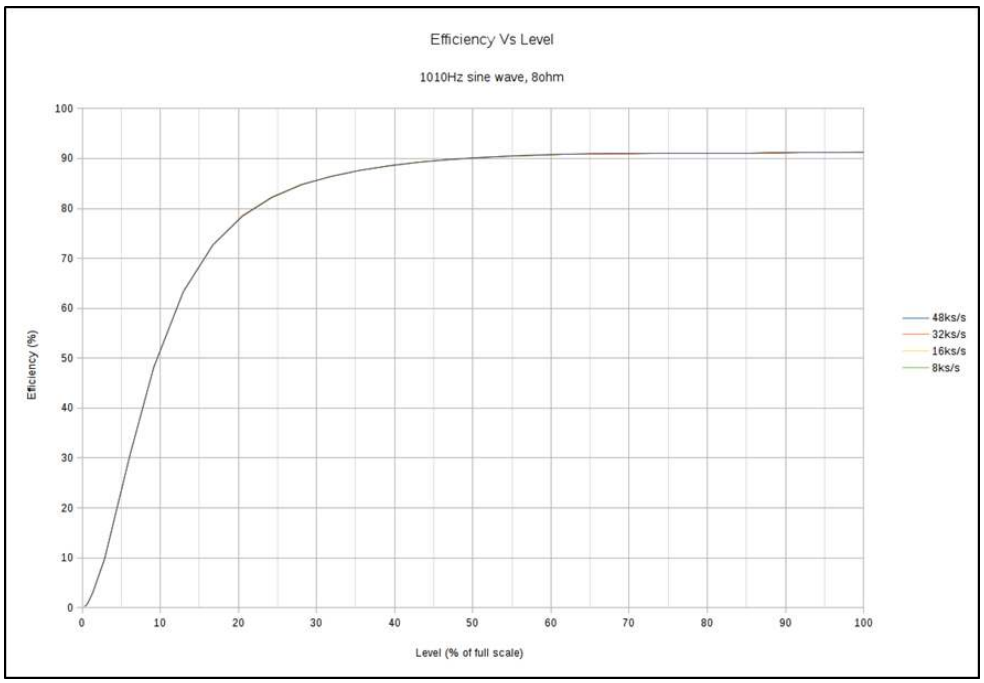


Figure 65 Class D Amplifier Efficiency 8Ω

7.2.4 Filter Performance Speaker Channel

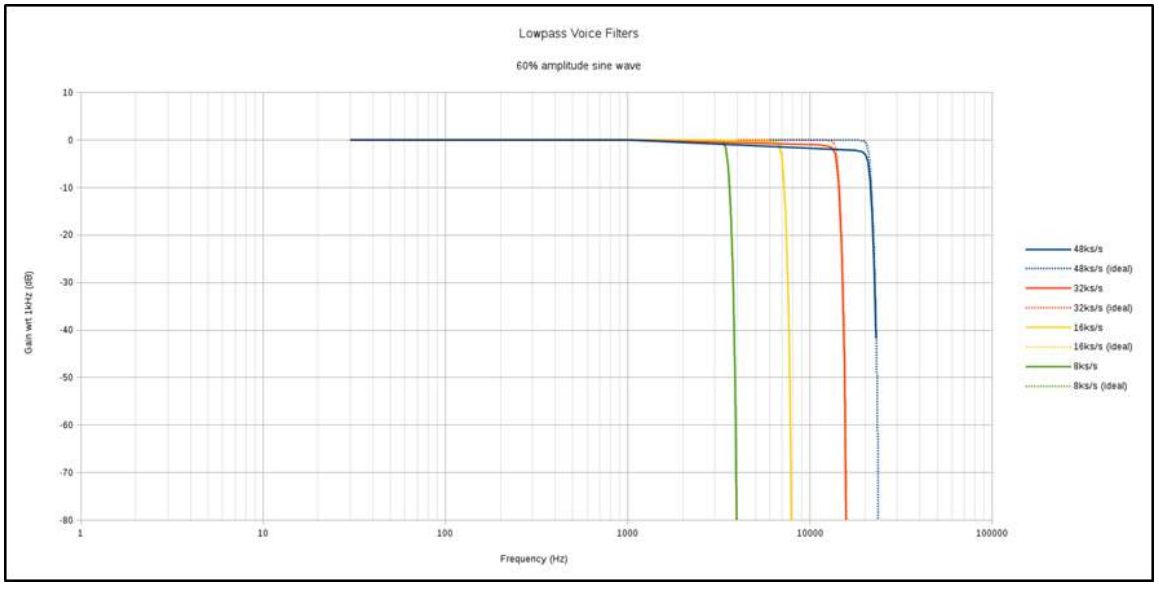


Figure 66 Low Pass Filter Response Speaker Channel

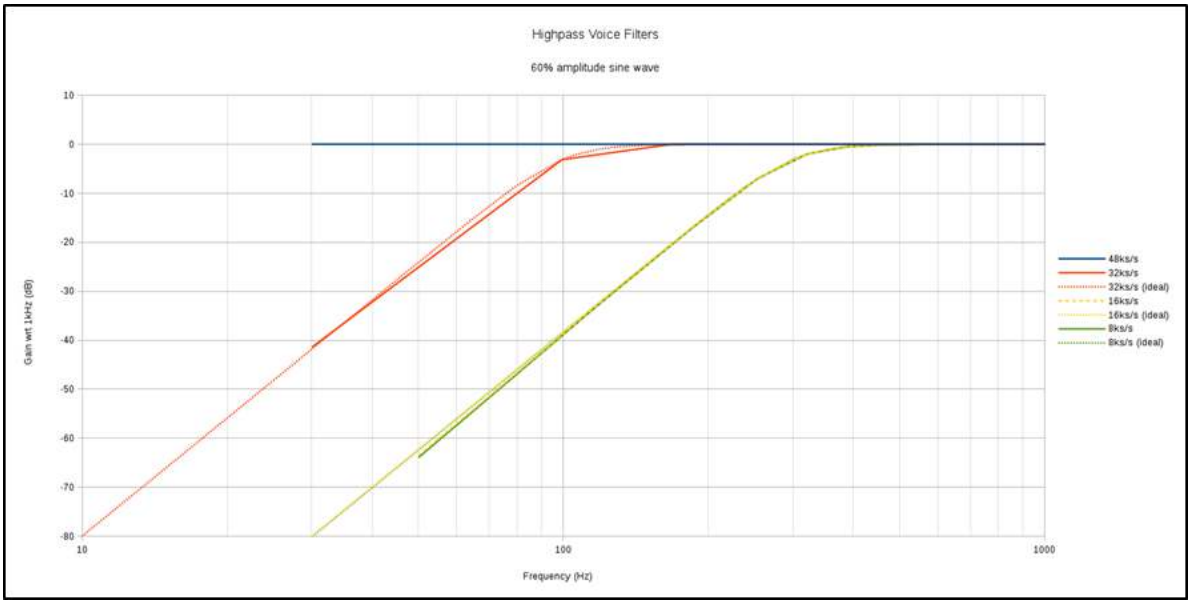
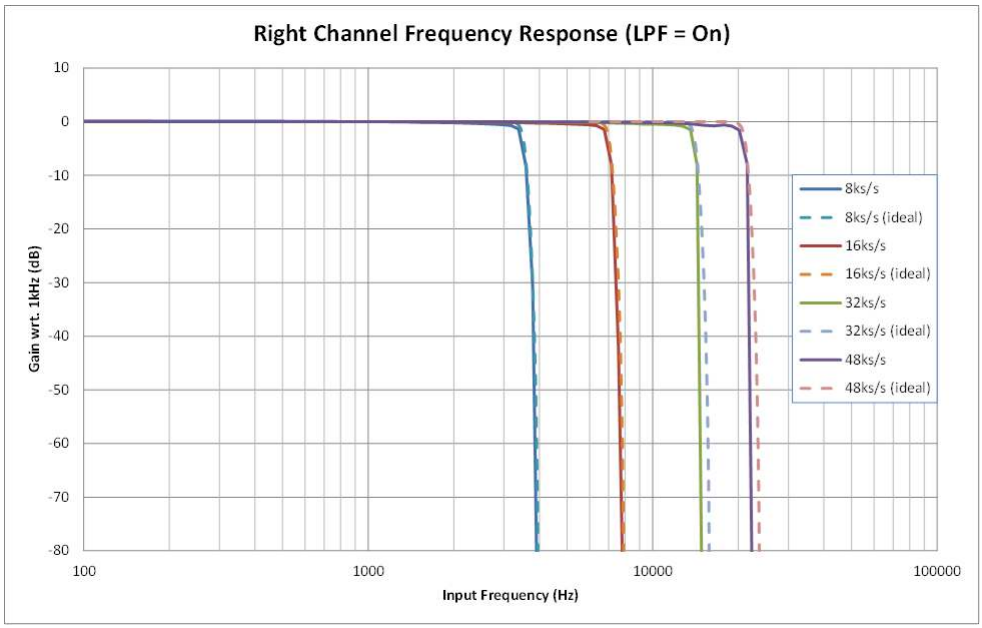


Figure 67 High Pass Filter Response Speaker Channel

7.2.5 Filter Performance Microphone Channel



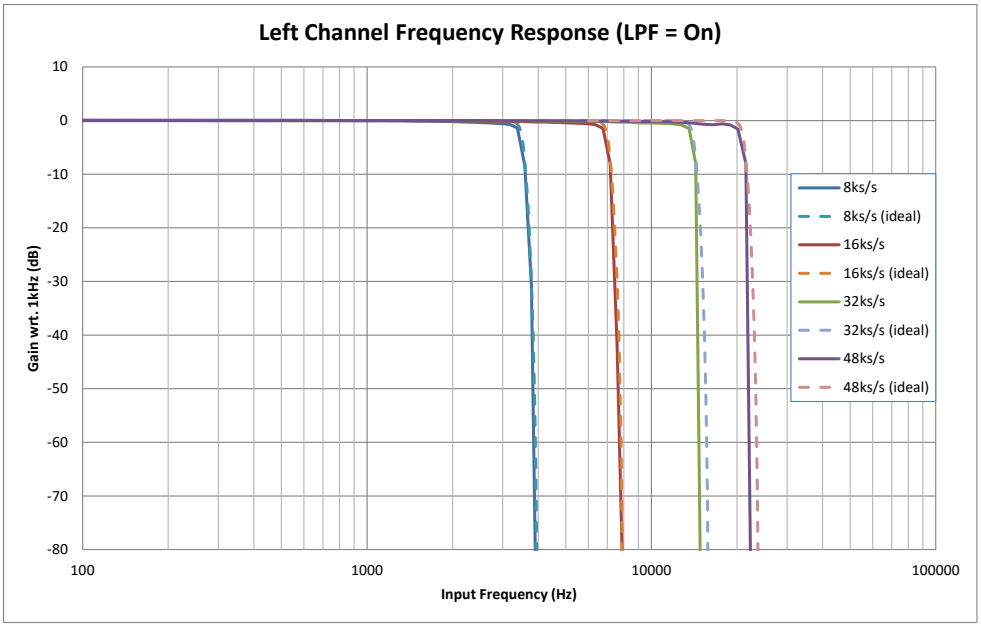
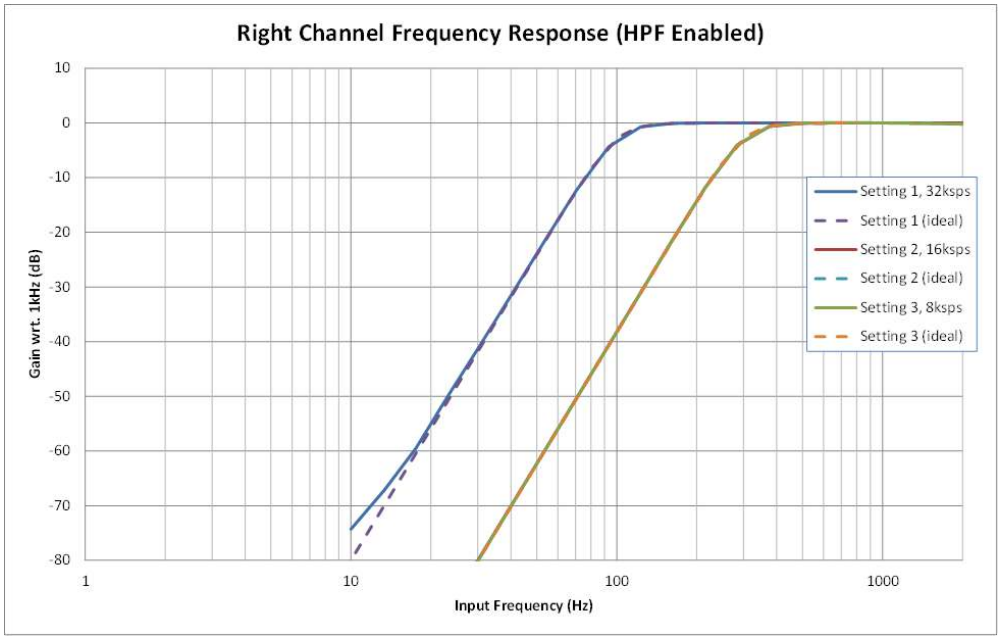


Figure 68 Low Pass Filter response Microphone Channels



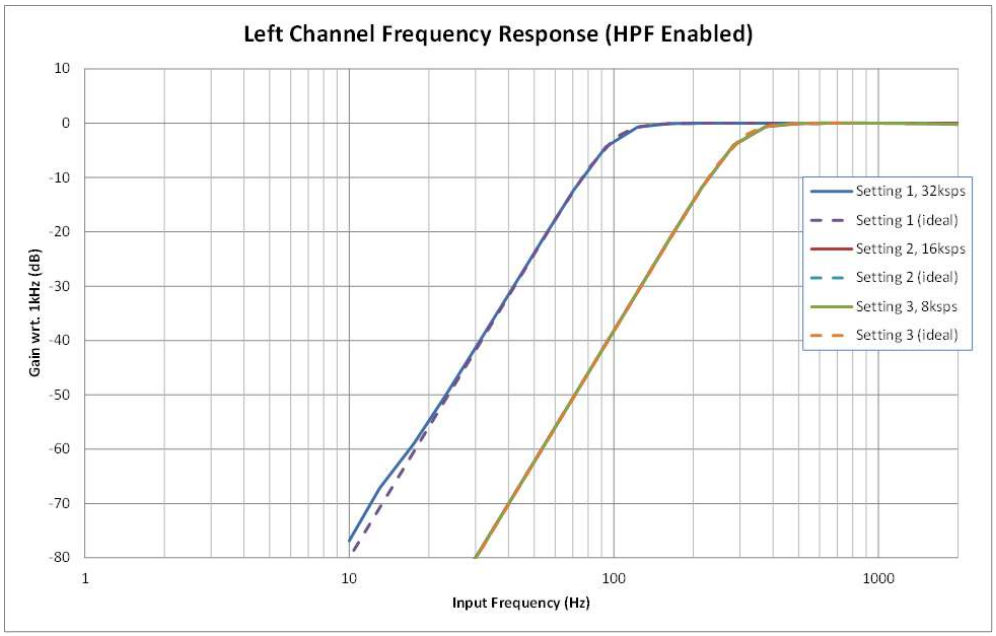
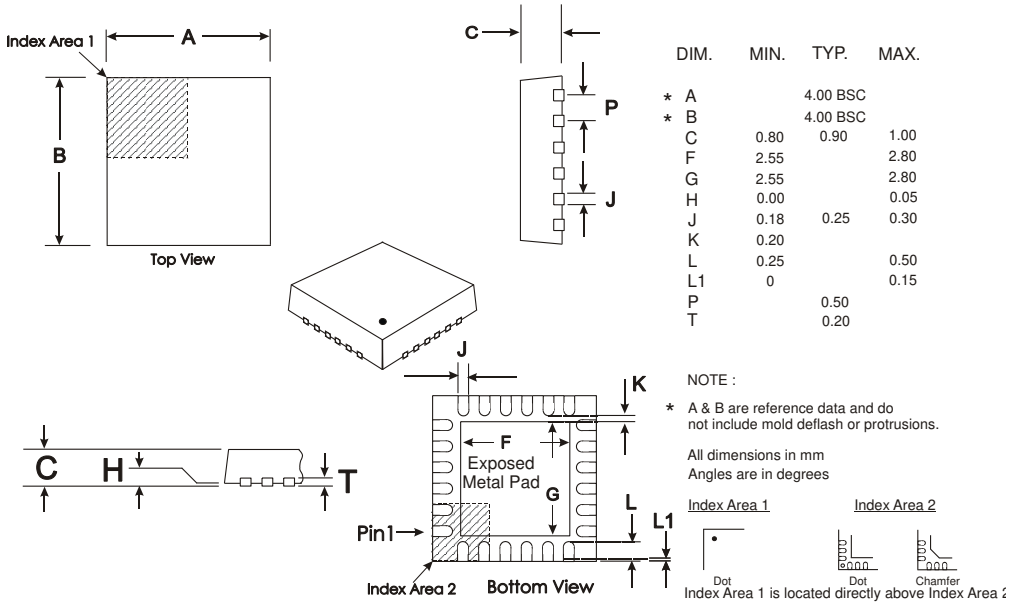


Figure 69 High Pass Filter Response Microphone Channels

7.3 Packaging

7.3.1 CMX655D/CMX655A



DIM.	MIN.	TYP.	MAX.
* A		4.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	2.55		2.80
G	2.55		2.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.25		0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Dot Dot Chamfer

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 70 VQFN-24 Mechanical Outline (Q6)
Order as part number CMX655DQ6 or CMX655AQ6

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