

# LMC6484 CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

## 1 Features

- Rail-to-Rail Input Common-Mode Voltage Range (Specified Over Temperature)
- Rail-to-Rail Output Swing (Within 20 mV of Supply Rail, 100-k $\Omega$  Load)
- Assured 3-V, 5-V and 15-V Performance
- Excellent CMRR and PSRR: 82 dB
- Ultra Low Input Current: 20 fA
- High Voltage Gain ( $R_L = 500\text{ k}\Omega$ ): 130 dB
- Specified for 2-k $\Omega$  and 600- $\Omega$  Loads

## 2 Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-Held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

## 3 Description

The LMC6484 device provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single-supply systems by the rail-to-rail output swing of the LMC6484. The rail-to-rail output swing of the LMC6484 is ensured for loads down to 600  $\Omega$ .

Specified low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

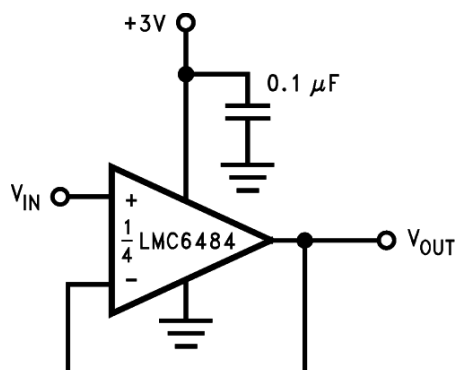
See the LMC6482 ([SNOS674](#)) data sheet for a dual CMOS operational amplifier with these same features.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC6484	SOIC (14)	8.65 mm $\times$ 3.91 mm
	PDIP (14)	19.177 mm $\times$ 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Single-Ended Unity Gain Buffer



## Table of Contents

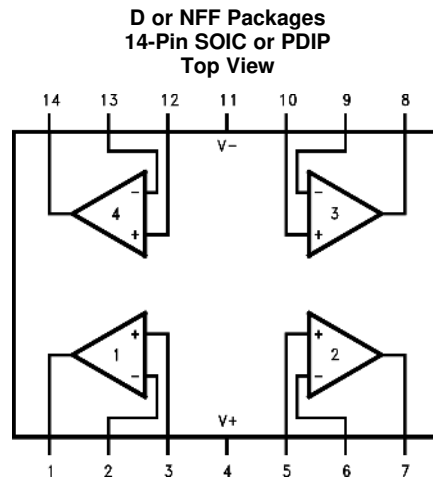
<b>1 Features</b> .....	<b>1</b>	<b>7 Detailed Description</b> .....	<b>23</b>
<b>2 Applications</b> .....	<b>1</b>	7.1 Overview .....	23
<b>3 Description</b> .....	<b>1</b>	7.2 Functional Block Diagram .....	23
<b>4 Revision History</b> .....	<b>2</b>	7.3 Feature Description .....	23
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	7.4 Device Functional Modes .....	24
<b>6 Specifications</b> .....	<b>4</b>	<b>8 Application and Implementation</b> .....	<b>25</b>
6.1 Absolute Maximum Ratings .....	4	8.1 Application Information .....	25
6.2 ESD Ratings .....	4	8.2 Typical Application .....	25
6.3 Recommended Operating Conditions .....	4	8.3 System Examples .....	31
6.4 Thermal Information .....	4	<b>9 Power Supply Recommendations</b> .....	<b>36</b>
6.5 DC Electrical Characteristics for LMC6484AI .....	5	<b>10 Layout</b> .....	<b>36</b>
6.6 DC Electrical Characteristics for LMC6484I .....	7	10.1 Layout Guidelines .....	36
6.7 DC Electrical Characteristics for LMC6484M .....	9	10.2 Layout Example .....	37
6.8 DC Electrical Characteristics for LMC6484AI .....	11	<b>11 Device and Documentation Support</b> .....	<b>38</b>
6.9 DC Electrical Characteristics for LMC6484I .....	11	11.1 Device Support .....	38
6.10 DC Electrical Characteristics for LMC6484M .....	12	11.2 Documentation Support .....	38
6.11 AC Electrical Characteristics for LMC6484A .....	13	11.3 Community Resource .....	38
6.12 AC Electrical Characteristics for LMC6484I .....	13	11.4 Trademarks .....	38
6.13 AC Electrical Characteristics for LMC6484M .....	14	11.5 Electrostatic Discharge Caution .....	38
6.14 AC Electrical Characteristics, $V^+ = 3\text{ V}$ , $V^- = 0\text{ V}$ .....	14	11.6 Glossary .....	38
6.15 Typical Characteristics .....	15	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>38</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2000) to Revision C	Page
<ul style="list-style-type: none"> <li>Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ....</li> </ul>	1

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTPUT1	O	Output for Amplifier 1
2	INVERTING INPUT1	I	Inverting input for Amplifier 1
3	NONINVERTING INPUT1	I	Noninverting input for Amplifier 1
4	V+	P	Positive voltage supply pin
5	NONINVERTING INPUT2	I	Noninverting input for Amplifier 2
6	INVERTING INPUT2	I	Inverting input for Amplifier 2
7	OUTPUT2	O	Output for Amplifier 2
8	OUTPUT3	O	Output for Amplifier 3
9	INVERTING INPUT3	I	Inverting input for Amplifier 3
10	NONINVERTING INPUT3	I	Noninverting input for Amplifier 3
11	V–	P	Negative supply voltage pin
12	NONINVERTING INPUT4	I	Noninverting input for Amplifier 4
13	INVERTING INPUT4	I	Inverting input for Amplifier 4
14	OUTPUT4	O	Output for Amplifier 5

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 See <sup>(1)(2)</sup>

	MIN	MAX	UNIT
Differential input voltage	$\pm$ Supply Voltage		
Voltage at input/output pin	$(V^-) - 0.3$	$(V^+) + 0.3$	V
Supply voltage ( $V^+ - V^-$ )		16	V
Current at input pin <sup>(3)</sup>		$\pm 5$	mA
Current at output pin <sup>(4)(5)</sup>		$\pm 30$	mA
Current at power supply pin		40	mA
Junction temperature <sup>(6)</sup>		150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- (4) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of  $\pm 30$  mA over long term may adversely affect reliability.
- (5) Do not short circuit output to  $V^+$ , when  $V^+$  is greater than 13 V or reliability will be adversely affected.
- (6) The maximum power dissipation is a function of  $T_{J(max)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A)/R_{\theta JA}$ . All numbers apply for packages soldered directly into a PC board.

### 6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)(2)</sup>	$\pm 2000$	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) Human body model, 1.5-k $\Omega$  resistor in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V+		3	15.5	V
Junction temperature, T <sub>J</sub>	LMC6484AM	-55	125	°C
	LMC6484AI, LMC6484I	-40	85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMC6484		UNIT
		D (SOIC)	NFF (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	70	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 DC Electrical Characteristics for LMC6484AI

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input offset voltage				0.11	0.75	mV
		At the temperature extremes				1.35	
$TCV_{OS}$	Input offset voltage average drift				1		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input current <sup>(3)</sup>				0.02		pA
		At the temperature extremes				4	
$I_{OS}$	Input offset current <sup>(3)</sup>				0.01		pA
		At the temperature extremes				2	
$C_{IN}$	Common-mode input capacitance				3		pF
$R_{IN}$	Input resistance				>10		Tera $\Omega$
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{CM} \leq 15\text{ V}$ $V^+ = 15\text{ V}$		70	82		dB
			At the temperature extremes	67			
		$0\text{ V} \leq V_{CM} \leq 5\text{ V}$ $V^+ = 5\text{ V}$		70	82		dB
			At the temperature extremes	67			
+PSRR	Positive power supply rejection ratio	$5\text{ V} \leq V^+ \leq 15\text{ V}$ $V^- = 0\text{ V}$ $V_O = 2.5\text{ V}$		70	82		dB
			At the temperature extremes	67			
-PSRR	Negative power supply rejection ratio	$-5\text{ V} \leq V^- \leq -15\text{ V}$ $V^+ = 0\text{ V}$ $V_O = -2.5\text{ V}$		70	82		dB
			At the temperature extremes	67			
$V_{CM}$	Input common-mode voltage range	$V^+ = 5\text{ V}$ and $15\text{ V}$ For CMRR $\geq 50\text{ dB}$			$V^- - 0.3$	-0.25	V
			At the temperature extremes			0	
				$V^+ + 0.25$	$V^+ + 0.3$		V
			At the temperature extremes	$V^+$			
$A_V$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$ <sup>(4)</sup>	Sourcing		140	666	V/mV
				At the temperature extremes	84		
			Sinking		35	75	V/mV
				At the temperature extremes	20		
		$R_L = 600\ \Omega$ <sup>(3)(4)</sup>	Sourcing		80	300	V/mV
				At the temperature extremes	48		
			Sinking		20	35	V/mV
				At the temperature extremes	13		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

(3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

(4)  $V^+ = 15\text{ V}$ ,  $V_{CM} = 7.5\text{ V}$  and  $R_L$  connected to  $7.5\text{ V}$ . For sourcing tests,  $7.5\text{ V} \leq V_O \leq 11.5\text{ V}$ . For sinking tests,  $3.5\text{ V} \leq V_O \leq 7.5\text{ V}$ .

## DC Electrical Characteristics for LMC6484AI (continued)

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_O$	Output swing	$V^+ = 5\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	4.8	4.9		V
			At the temperature extremes	4.7		
				0.1	0.18	V
		At the temperature extremes			0.24	
		$V^+ = 5\text{ V}$ $R_L = 600\text{ }\Omega$ to $V^+/2$	4.5	4.7		V
			At the temperature extremes	4.24		
				0.3	0.5	V
		At the temperature extremes			0.65	
		$V^+ = 15\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	14.4	14.7		V
			At the temperature extremes	14.2		
				0.16	0.32	V
		At the temperature extremes			0.45	
		$V^+ = 15\text{ V}$ $R_L = 600\text{ }\Omega$ to $V^+/2$	13.4	14.1		V
			At the temperature extremes	13		
				0.5	1	V
		At the temperature extremes			1.3	
$I_{SC}$	Output short circuit current $V^+ = 5\text{ V}$	Sourcing, $V_O = 0\text{ V}$	16	20		mA
			At the temperature extremes	12		
		Sinking, $V_O = 5\text{ V}$	11	15		mA
			At the temperature extremes	9.5		
$I_{SC}$	Output short circuit current $V^+ = 15\text{ V}$	Sourcing, $V_O = 0\text{ V}$	28	30		mA
			At the temperature extremes	22		
		Sinking, $V_O = 12\text{ V}^{(5)}$	30	30		mA
			At the temperature extremes	24		
$I_S$	Supply current	All four amplifiers $V^+ = +5\text{ V}$ , $V_O = V^+/2$		2	2.8	mA
			At the temperature extremes		3.6	
		All four amplifiers $V^+ = +15\text{ V}$ , $V_O = V^+/2$		2.6	3	mA
			At the temperature extremes		3.8	

(5) When  $V^+$  is greater than 13 V, do not short circuit output to  $V^+$  or reliability will be adversely affected.

## 6.6 DC Electrical Characteristics for LMC6484I

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input offset voltage				0.11	3	mV
		At the temperature extremes				3.7	
$TCV_{OS}$	Input offset voltage average drift				1		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input current <sup>(3)</sup>				0.02		pA
		At the temperature extremes				4	
$I_{OS}$	Input offset current <sup>(3)</sup>				0.01		pA
		At the temperature extremes				2	
$C_{IN}$	Common-mode input capacitance				3		pF
$R_{IN}$	Input resistance				>10		Tera $\Omega$
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{CM} \leq 15\text{ V}$ $V^+ = 15\text{ V}$		65	82		dB
			At the temperature extremes	62			
		$0\text{ V} \leq V_{CM} \leq 5\text{ V}$ $V^+ = 5\text{ V}$		65	82		dB
			At the temperature extremes	60			
+PSRR	Positive power supply rejection ratio	$5\text{ V} \leq V^+ \leq 15\text{ V}$ $V^- = 0\text{ V}$ , $V_O = 2.5\text{ V}$		65	82		dB
			At the temperature extremes	62			
-PSRR	Negative power supply rejection ratio	$-5\text{ V} \leq V^- \leq -15\text{ V}$ $V^+ = 0\text{ V}$ , $V_O = -2.5\text{ V}$		65	82		dB
			At the temperature extremes	62			
$V_{CM}$	Input common-mode voltage range	$V^+ = 5\text{ V}$ and $15\text{ V}$ For CMRR $\geq 50\text{ dB}$			$V^- - 0.3$	-0.25	V
			At the temperature extremes			0	
				$V^+ + 0.25$	$V^+ + 0.3$		V
			At the temperature extremes	$V^+$			
$A_V$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$ <sup>(4)</sup>	Sourcing		120	666	V/mV
				At the temperature extremes	72		
			Sinking		35	75	
				At the temperature extremes	20		
		$R_L = 600\ \Omega$ <sup>(3)(4)</sup>	Sourcing		50	300	
				At the temperature extremes	30		
			Sinking		15	35	
				At the temperature extremes	10		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

(3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

(4)  $V^+ = 15\text{ V}$ ,  $V_{CM} = 7.5\text{ V}$  and  $R_L$  connected to  $7.5\text{ V}$ . For sourcing tests,  $7.5\text{ V} \leq V_O \leq 11.5\text{ V}$ . For sinking tests,  $3.5\text{ V} \leq V_O \leq 7.5\text{ V}$ .

**LMC6484**

SNOS675C – AUGUST 2000 – REVISED SEPTEMBER 2015

[www.ti.com](http://www.ti.com)
**DC Electrical Characteristics for LMC6484I (continued)**

 Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}$ .

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_O$ Output swing	$V^+ = 5\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$		4.8	4.9	V
		At the temperature extremes	4.7		
				0.1	V
		At the temperature extremes		0.24	
	$V^+ = 5\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$		4.5	4.7	V
		At the temperature extremes	4.24		
				0.3	V
		At the temperature extremes		0.65	
	$V^+ = 15\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$		14.4	14.7	V
		At the temperature extremes	14.2		
				0.16	V
		At the temperature extremes		0.45	
	$V^+ = 15\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$		13.4	14.1	V
		At the temperature extremes	13		
				0.5	V
		At the temperature extremes		1.3	
$I_{SC}$ Output short circuit current $V^+ = 5\text{ V}$	Sourcing, $V_O = 0\text{ V}$		16	20	mA
		At the temperature extremes	12		
	Sinking, $V_O = 5\text{ V}$		11	15	mA
		At the temperature extremes	9.5		
$I_{SC}$ Output short circuit current $V^+ = 15\text{ V}$	Sourcing, $V_O = 0\text{ V}$		28	30	mA
		At the temperature extremes	22		
	Sinking, $V_O = 12\text{ V}^{(5)}$		30	30	mA
		At the temperature extremes	24		
$I_S$ Supply current	All four amplifiers $V^+ = +5\text{ V}$ $V_O = V^+/2$			2	mA
		At the temperature extremes		3.6	
	All four amplifiers $V^+ = +15\text{ V}$ $V_O = V^+/2$			2.6	mA
		At the temperature extremes		3.8	

 (5) When  $V^+$  is greater than 13 V, do not short circuit output to  $V^+$  or reliability will be adversely affected.

## 6.7 DC Electrical Characteristics for LMC6484M

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input offset voltage				0.11	3	mV
		At the temperature extremes				3.8	
$TCV_{OS}$	Input offset voltage average drift				1		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input current <sup>(3)</sup>				0.02		pA
		At the temperature extremes				100	
$I_{OS}$	Input offset current <sup>(3)</sup>				0.01		pA
		At the temperature extremes				50	
$C_{IN}$	Common-mode input capacitance				3		pF
$R_{IN}$	Input resistance				>10		Tera $\Omega$
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{CM} \leq 15\text{ V}$ $V^+ = 15\text{ V}$		65	82		dB
			At the temperature extremes	60			
		$0\text{ V} \leq V_{CM} \leq 5\text{ V}$ $V^+ = 5\text{ V}$		65	8		dB
			At the temperature extremes	60			
+PSRR	Positive power supply rejection ratio	$5\text{ V} \leq V^+ \leq 15\text{ V}$ $V^- = 0\text{ V}$ , $V_O = 2.5\text{ V}$		65	82		dB
			At the temperature extremes	60			
-PSRR	Negative power supply rejection ratio	$-5\text{ V} \leq V^- \leq -15\text{ V}$ $V^+ = 0\text{ V}$ $V_O = -2.5\text{ V}$		65	82		dB
			At the temperature extremes	60			
$V_{CM}$	Input common-mode voltage range	$V^+ = 5\text{ V}$ and $15\text{ V}$ For CMRR $\geq 50\text{ dB}$			$V^- - 0.3$	-0.25	V
			At the temperature extremes			0	
				$V^+ + 0.25$	$V^+ + 0.3$		V
			At the temperature extremes	$V^+$			
$A_V$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$ <sup>(4)</sup>	Sourcing		120	666	V/mV
				At the temperature extremes	72		
			Sinking		35	75	
				At the temperature extremes	20		
		$R_L = 600\text{ }\Omega$ <sup>(3)(4)</sup>	Sourcing		50	300	
				At the temperature extremes	30		
			Sinking		15	35	
				At the temperature extremes	10		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

(3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

(4)  $V^+ = 15\text{ V}$ ,  $V_{CM} = 7.5\text{ V}$  and  $R_L$  connected to  $7.5\text{ V}$ . For sourcing tests,  $7.5\text{ V} \leq V_O \leq 11.5\text{ V}$ . For sinking tests,  $3.5\text{ V} \leq V_O \leq 7.5\text{ V}$ .

**LMC6484**

SNOS675C – AUGUST 2000 – REVISED SEPTEMBER 2015

[www.ti.com](http://www.ti.com)
**DC Electrical Characteristics for LMC6484M (continued)**

 Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}$ .

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_O$ Output swing	$V^+ = 5\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$		4.8	4.9	V
		At the temperature extremes	4.7		
				0.1	V
		At the temperature extremes		0.24	
	$V^+ = 5\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$		4.5	4.7	V
		At the temperature extremes	4.24		
				0.3	V
		At the temperature extremes		0.65	
	$V^+ = 15\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$		14.4	14.7	V
		At the temperature extremes	14.2		
				0.16	V
		At the temperature extremes		0.45	
	$V^+ = 15\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$		13.4	14.1	V
		At the temperature extremes	13		
				0.5	V
		At the temperature extremes		1.3	
$I_{SC}$ Output short circuit current $V^+ = 5\text{ V}$	Sourcing, $V_O = 0\text{ V}$		16	20	mA
		At the temperature extremes	10		
	Sinking, $V_O = 5\text{ V}$		11	15	mA
		At the temperature extremes	8		
$I_{SC}$ Output short circuit current $V^+ = 15\text{ V}$	Sourcing, $V_O = 0\text{ V}$		28	30	mA
		At the temperature extremes	20		
	Sinking, $V_O = 12\text{ V}^{(5)}$		30	30	mA
		At the temperature extremes	22		
$I_S$ Supply current	All four amplifiers $V^+ = +5\text{ V}$ $V_O = V^+/2$			2	mA
		At the temperature extremes		3.8	
	All four amplifiers $V^+ = +15\text{ V}$ , $V_O = V^+/2$			2.6	mA
		At the temperature extremes		4	

 (5) When  $V^+$  is greater than 13 V, do not short circuit output to  $V^+$  or reliability will be adversely affected.

## 6.8 DC Electrical Characteristics for LMC6484AI

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{ M}$ .

PARAMETER		TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{\text{OS}}$	Input offset voltage				0.9	2	mV
		At the temperature extremes				2.7	
$\text{TCV}_{\text{OS}}$	Input offset voltage average drift				2		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input bias current				0.02		pA
$I_{\text{OS}}$	Input offset current				0.01		pA
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{\text{CM}} \leq 3\text{ V}$		64	74		dB
PSRR	Power supply rejection ratio	$3\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$		68	80		dB
$V_{\text{CM}}$	Input common-mode voltage range	For CMRR $\geq 50\text{ dB}$			$V^- - 0.25$	0	V
				$V^+$	$V^+ + 0.25$		V
$V_O$	Output swing	$R_L = 2\text{ k}\Omega$ to $V^+/2$			2.8		V
					0.2		V
		$R_L = 600\ \Omega$ to $V^+/2$		2.5	2.7		V
					0.37	0.6	V
$I_S$	Supply current	All four amplifiers			1.65	2.5	mA
			At the temperature extremes			3	

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

## 6.9 DC Electrical Characteristics for LMC6484I

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{ M}$ .

PARAMETER		TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{\text{OS}}$	Input offset voltage				0.9	3	mV
		At the temperature extremes				3.7	
$\text{TCV}_{\text{OS}}$	Input offset voltage average drift				2		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input bias current				0.02		pA
$I_{\text{OS}}$	Input offset current				0.01		pA
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{\text{CM}} \leq 3\text{ V}$		60	74		dB
PSRR	Power supply rejection ratio	$3\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$		60	80		dB
$V_{\text{CM}}$	Input common-mode voltage range	For CMRR $\geq 50\text{ dB}$			$V^- - 0.25$	0	V
				$V^+$	$V^+ + 0.25$		V
$V_O$	Output swing	$R_L = 2\text{ k}\Omega$ to $V^+/2$			2.8		V
					0.2		V
		$R_L = 600\ \Omega$ to $V^+/2$		2.5	2.7		V
					0.37	0.6	V
$I_S$	Supply current	All four amplifiers			1.65	2.5	mA
			At the temperature extremes			3	

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

**LMC6484**

SNOS675C – AUGUST 2000 – REVISED SEPTEMBER 2015

[www.ti.com](http://www.ti.com)
**6.10 DC Electrical Characteristics for LMC6484M**

 Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input offset voltage			0.9	3	mV
		At the temperature extremes			3.8	
$TCV_{OS}$	Input offset voltage average drift			2		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input bias current			0.02		pA
$I_{OS}$	Input offset current			0.01		pA
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{CM} \leq 3\text{ V}$	60	74		dB
PSRR	Power supply rejection ratio	$3\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$	60	80		dB
$V_{CM}$	Input common-mode voltage range	For CMRR $\geq 50\text{ dB}$		$V^- - 0.25$	0	V
			$V^+$	$V^+ + 0.25$		V
$V_O$	Output swing	$R_L = 2\text{ k}\Omega$ to $V^+/2$		2.8		V
				0.2		V
		$R_L = 600\ \Omega$ to $V^+/2$	2.5	2.7		V
				0.37	0.6	V
$I_S$	Supply current	All four amplifiers		1.65	2.5	mA
			At the temperature extremes		3.2	

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

## 6.11 AC Electrical Characteristics for LMC6484A

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+ / 2$  and  $R_L > 1\text{ M}$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
SR	Slew rate <sup>(3)</sup>		1	1.3		V/ $\mu\text{s}$
		At the temperature extremes	0.7			
GBW	Gain-bandwidth product	$V^+ = 15\text{ V}$		1.5		MHz
$\Phi_m$	Phase margin			50		Deg
$G_m$	Gain margin			15		dB
	Amplifier-to-amplifier isolation <sup>(4)</sup>			150		dB
$e_n$	Input-referred voltage noise	$f = 1\text{ kHz}$ , $V_{CM} = 1\text{ V}$		37		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-referred current noise	$f = 1\text{ kHz}$		0.03		$\text{pA}/\sqrt{\text{Hz}}$
T.H.D.	Total harmonic distortion	$f = 1\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{PP}$		0.01%		
		$f = 10\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 8.5\text{ V}_{PP}$ , $V^+ = 10\text{ V}$		0.01%		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

(3)  $V^+ = 15\text{ V}$ . Connected as voltage follower with 10-V step input. Number specified is the slower of either the positive or negative slew rates.

(4) Input referred,  $V^+ = 15\text{ V}$  and  $R_L = 100\text{ k}\Omega$  connected to 7.5 V. Each amplifier excited in turn with 1 kHz to produce  $V_O = 12\text{ V}_{PP}$ .

## 6.12 AC Electrical Characteristics for LMC6484I

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+ / 2$  and  $R_L > 1\text{ M}$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
SR	Slew rate <sup>(3)</sup>		0.9	1.3		V/ $\mu\text{s}$
		At the temperature extremes	0.63			
GBW	Gain-bandwidth product	$V^+ = 15\text{ V}$		1.5		MHz
$\Phi_m$	Phase margin			50		Deg
$G_m$	Gain margin			15		dB
	Amplifier-to-amplifier isolation <sup>(4)</sup>			150		dB
$e_n$	Input-referred voltage noise	$f = 1\text{ kHz}$ , $V_{CM} = 1\text{ V}$		37		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-referred current noise	$f = 1\text{ kHz}$		0.03		$\text{pA}/\sqrt{\text{Hz}}$
T.H.D.	Total harmonic distortion	$f = 1\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{PP}$		0.01%		
		$f = 10\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 8.5\text{ V}_{PP}$ , $V^+ = 10\text{ V}$		0.01%		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

(3)  $V^+ = 15\text{ V}$ . Connected as Voltage Follower with 10-V step input. Number specified is the slower of either the positive or negative slew rates.

(4) Input referred,  $V^+ = 15\text{ V}$  and  $R_L = 100\text{ k}\Omega$  connected to 7.5 V. Each amp excited in turn with 1 kHz to produce  $V_O = 12\text{ V}_{PP}$ .

**LMC6484**

SNOS675C – AUGUST 2000 – REVISED SEPTEMBER 2015

[www.ti.com](http://www.ti.com)
**6.13 AC Electrical Characteristics for LMC6484M**

 Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
SR	Slew rate <sup>(3)</sup>		0.9	1.3		V/ $\mu\text{s}$
		At the temperature extremes	0.54			
GBW	Gain-bandwidth product	$V^+ = 15\text{ V}$		1.5		MHz
$\Phi_m$	Phase margin			50		Deg
$G_m$	Gain margin			15		dB
	Amplifier-to-amplifier isolation <sup>(4)</sup>			150		dB
$e_n$	Input-referred voltage noise	$f = 1\text{ kHz}$ , $V_{CM} = 1\text{ V}$		37		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-referred current noise	$f = 1\text{ kHz}$		0.03		$\text{pA}/\sqrt{\text{Hz}}$
T.H.D.	Total harmonic distortion	$f = 1\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{PP}$		0.01%		
		$f = 10\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 8.5\text{ V}_{PP}$ , $V^+ = 10\text{ V}$		0.01%		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

 (3)  $V^+ = 15\text{ V}$ . Connected as Voltage Follower with 10-V step input. Number specified is the slower of either the positive or negative slew rates.

 (4) Input referred,  $V^+ = 15\text{ V}$  and  $R_L = 100\text{ k}\Omega$  connected to 7.5 V. Each amplifier excited in turn with 1 kHz to produce  $V_O = 12\text{ V}_{PP}$ .

**6.14 AC Electrical Characteristics,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$** 

 Unless otherwise specified,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ 

PARAMETER		TEST CONDITIONS	LMC6484AI, LMC6484I, LMC6484M			UNIT
			MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	
SR	Slew rate <sup>(3)</sup>			0.9		V/ $\mu\text{s}$
GBW	Gain-bandwidth product			1		MHz
T.H.D.	Total harmonic distortion	$f = 10\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 2\text{ V}_{PP}$		0.01%		

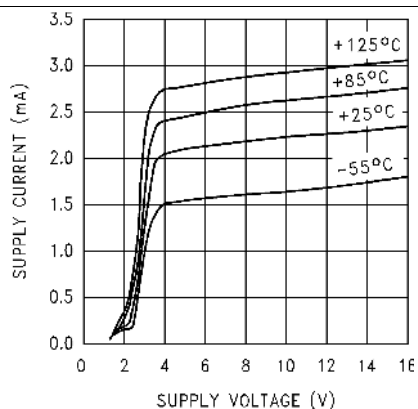
(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric normal.

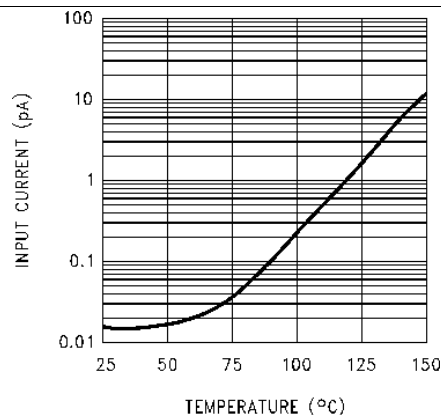
(3) Connected as voltage follower with 2-V step input. Number specified is the slower of either the positive or negative slew rates.

## 6.15 Typical Characteristics

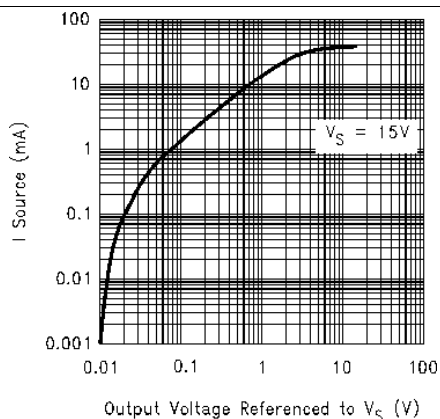
$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)



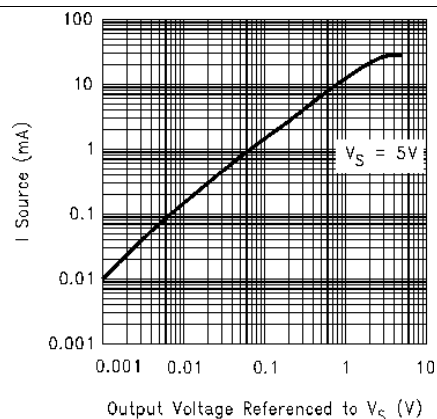
**Figure 1. Supply Current vs Supply Voltage**



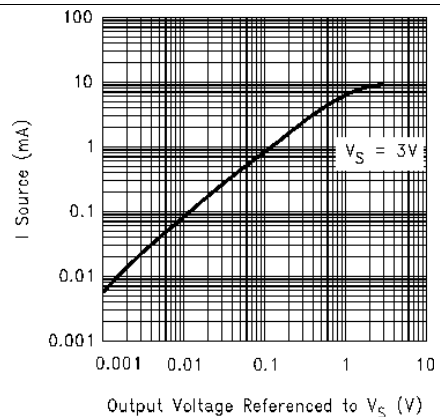
**Figure 2. Input Current vs Temperature**



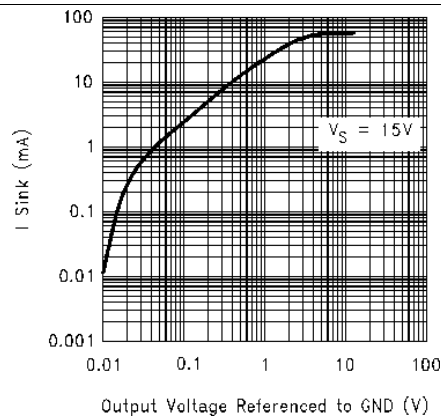
**Figure 3. Sourcing Current vs Output Voltage**



**Figure 4. Sourcing Current vs Output Voltage**

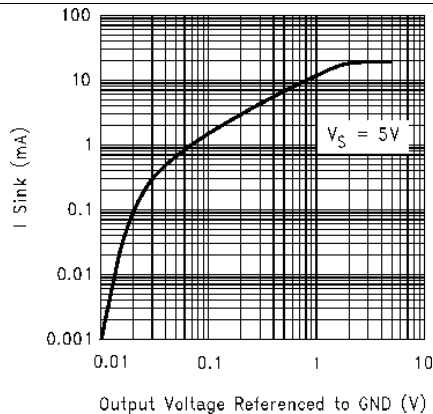
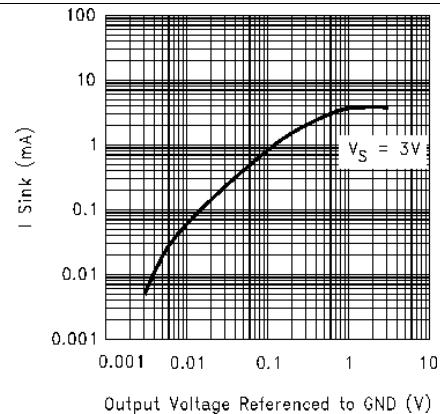
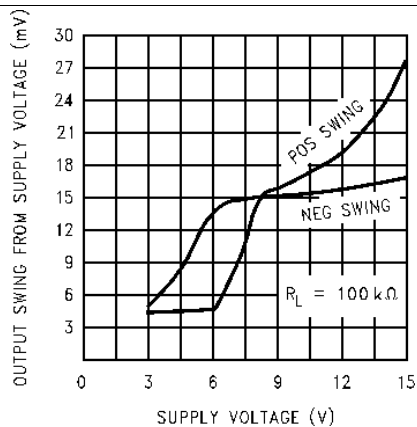
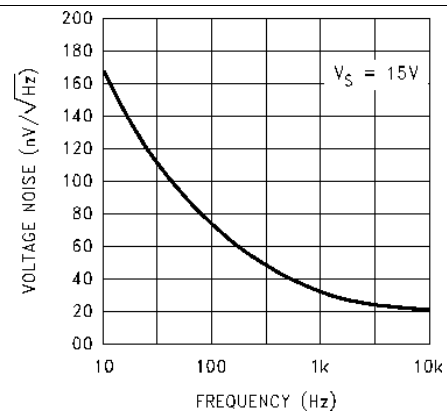
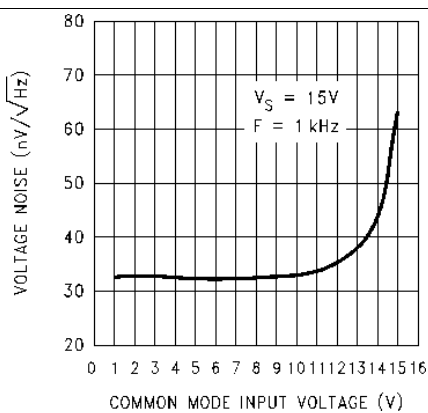
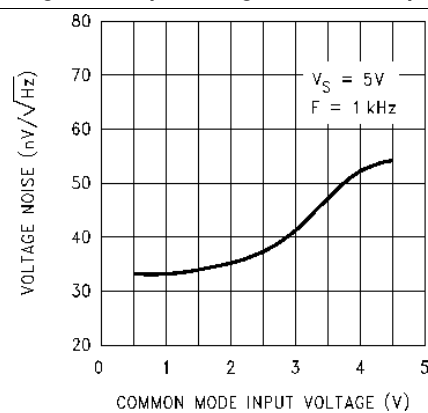


**Figure 5. Sourcing Current vs Output Voltage**



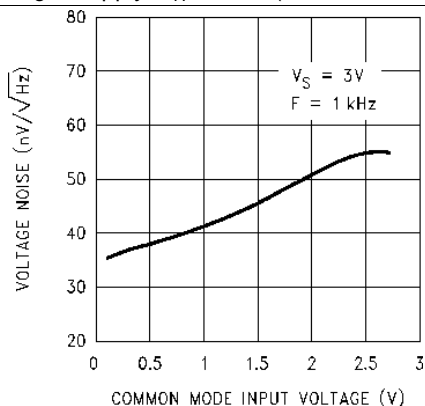
**Figure 6. Sinking Current vs Output Voltage**

## Typical Characteristics (continued)

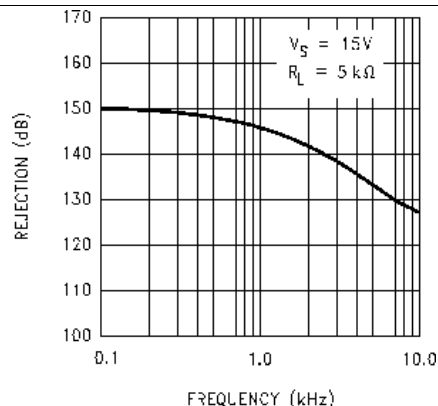
 $V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

**Figure 7. Sinking Current vs Output Voltage**

**Figure 8. Sinking Current vs Output Voltage**

**Figure 9. Output Voltage Swing vs Supply Voltage**

**Figure 10. Input Voltage Noise vs Frequency**

**Figure 11. Input Voltage Noise vs Input Voltage**

**Figure 12. Input Voltage Noise vs Input Voltage**

## Typical Characteristics (continued)

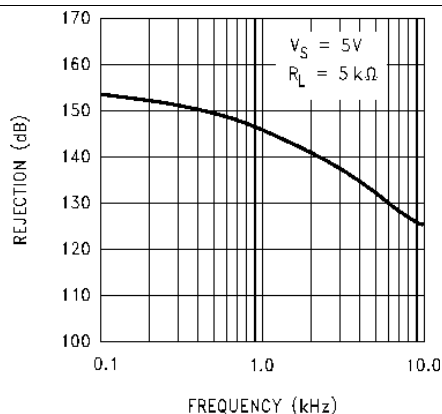
$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)



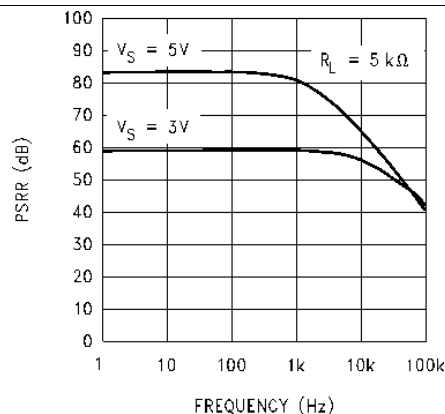
**Figure 13. Input Voltage Noise vs Input Voltage**



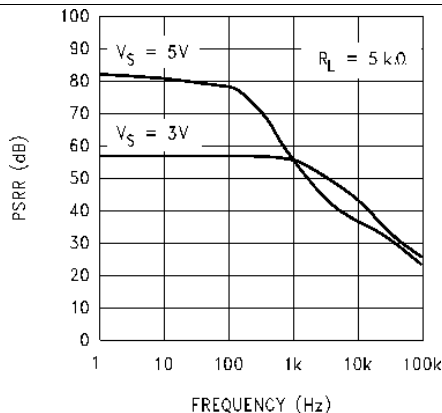
**Figure 14. Crosstalk Rejection vs Frequency**



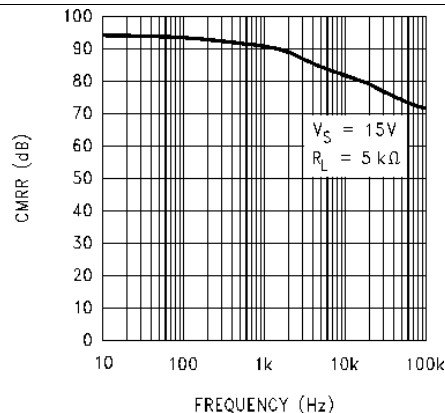
**Figure 15. Crosstalk Rejection vs Frequency**



**Figure 16. Positive PSRR vs Frequency**

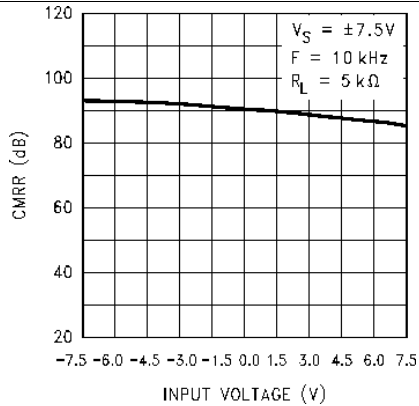
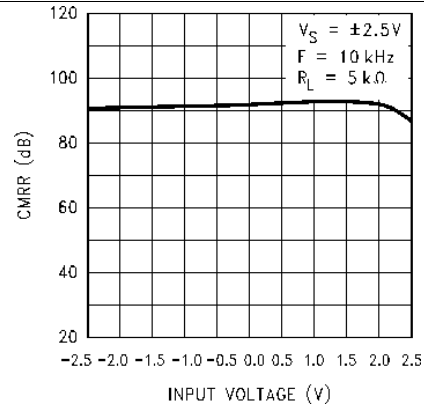
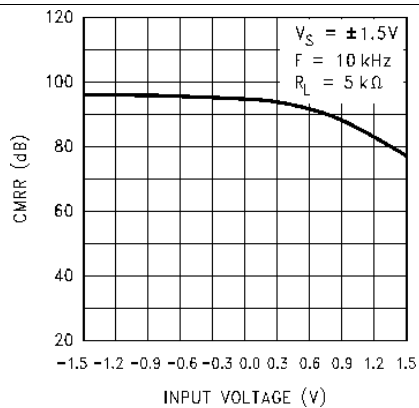
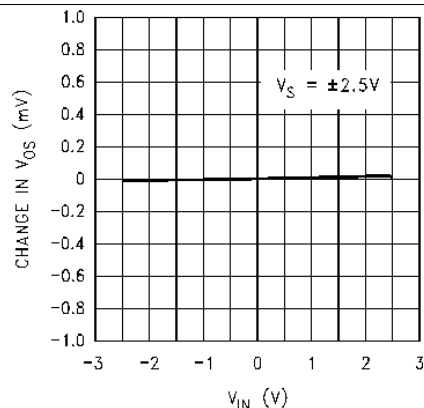
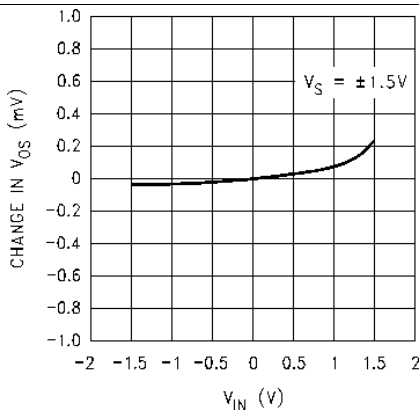
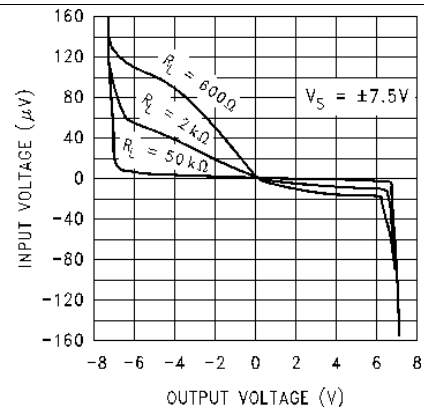


**Figure 17. Negative PSRR vs Frequency**



**Figure 18. CMRR vs Frequency**

## Typical Characteristics (continued)

 $V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

**Figure 19. CMRR vs Input Voltage**

**Figure 20. CMRR vs Input Voltage**

**Figure 21. CMRR vs Input Voltage**

**Figure 22.  $\Delta V_{OS}$  vs CMR**

**Figure 23.  $\Delta V_{OS}$  vs CMR**

**Figure 24. Input Voltage vs Output Voltage**

## Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

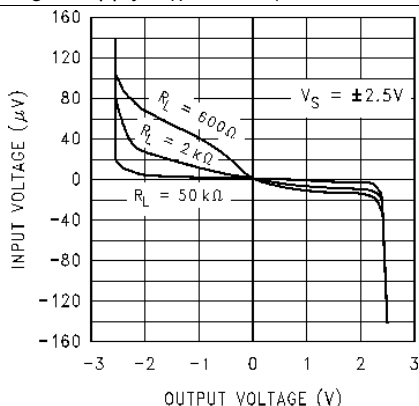


Figure 25. Input Voltage vs Output Voltage

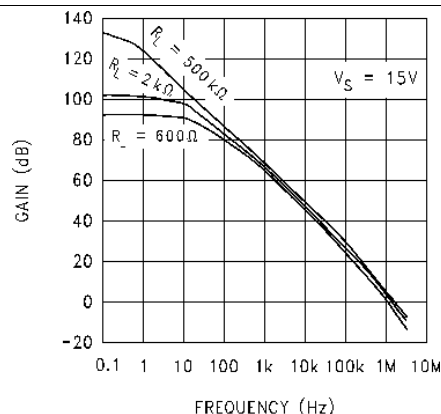


Figure 26. Open Loop Frequency Response

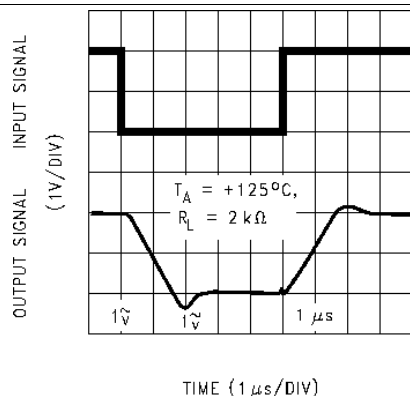


Figure 27. Noninverting Large Signal Pulse Response

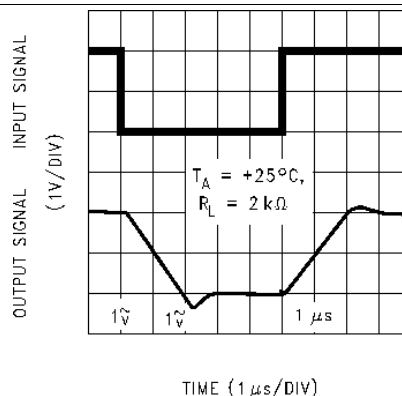


Figure 28. Noninverting Large Signal Pulse Response

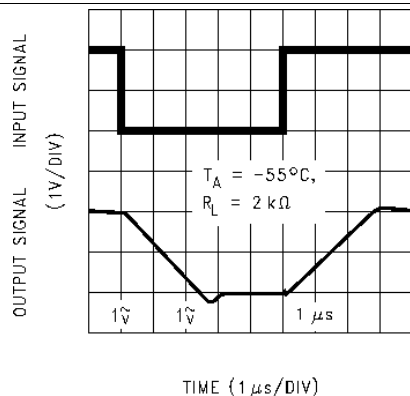


Figure 29. Noninverting Large Signal Pulse Response

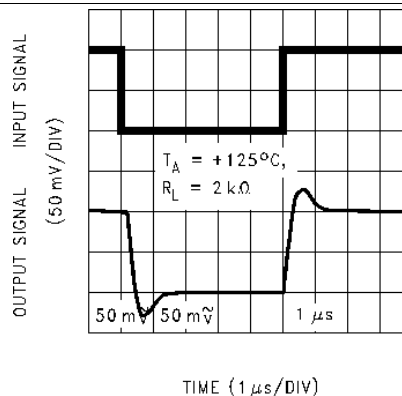
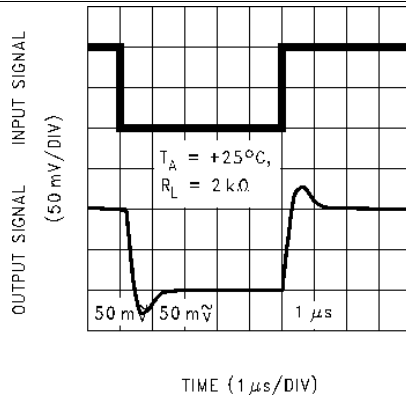


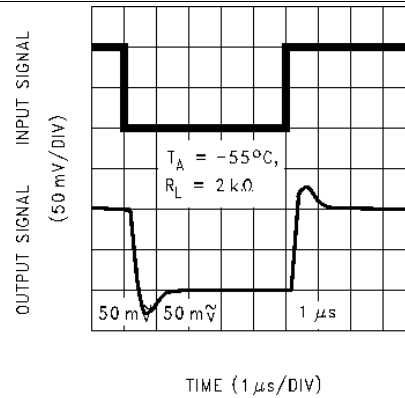
Figure 30. Noninverting Small Signal Pulse Response

## Typical Characteristics (continued)

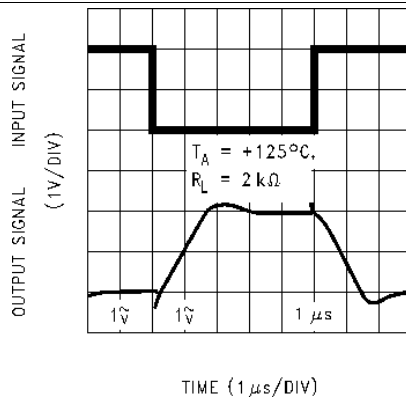
$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)



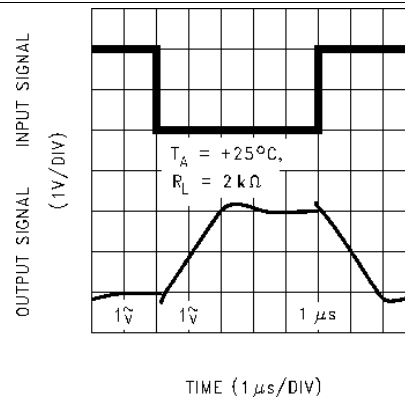
**Figure 31. Noninverting Small Signal Pulse Response**



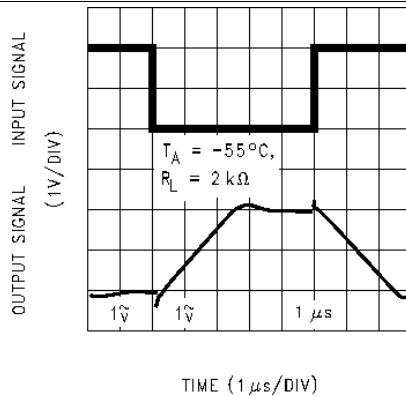
**Figure 32. Noninverting Small Signal Pulse Response**



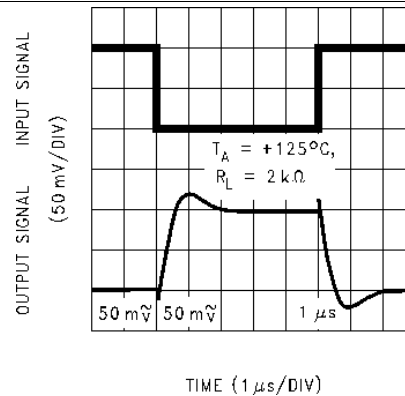
**Figure 33. Inverting Large Signal Pulse Response**



**Figure 34. Inverting Large Signal Pulse Response**



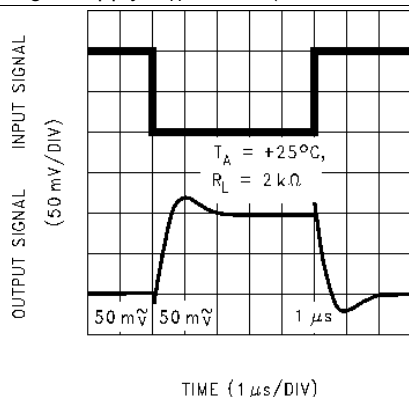
**Figure 35. Inverting Large Signal Pulse Response**



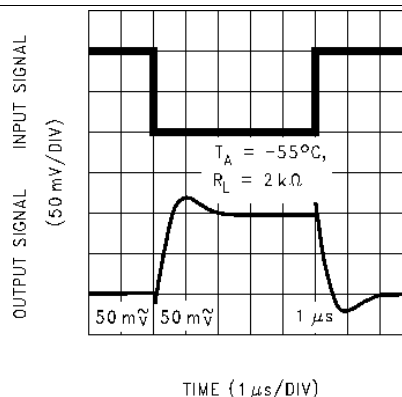
**Figure 36. Inverting Small Signal Pulse Response**

## Typical Characteristics (continued)

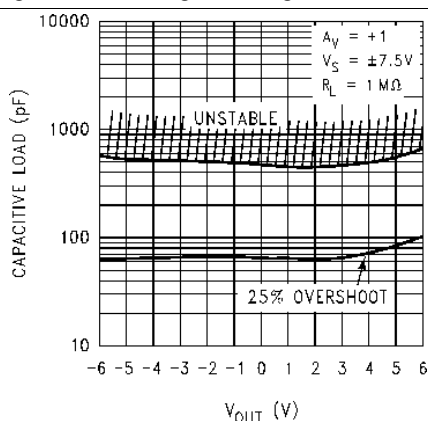
$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)



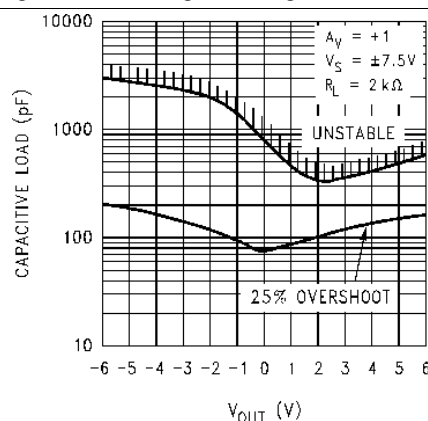
**Figure 37. Inverting Small Signal Pulse Response**



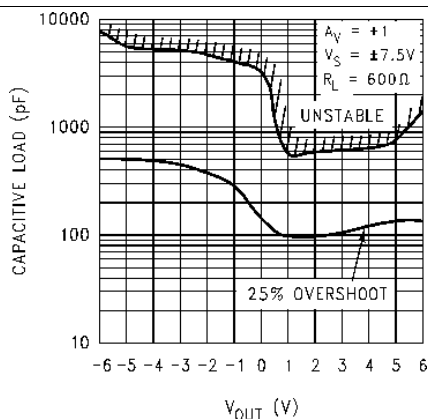
**Figure 38. Inverting Small Signal Pulse Response**



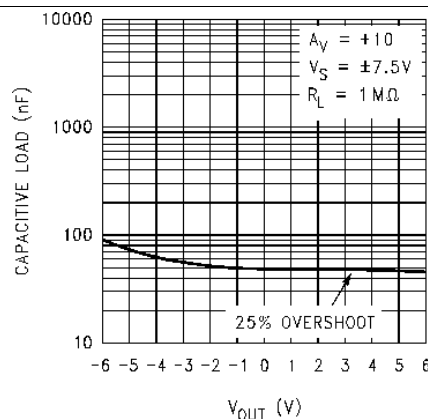
**Figure 39. Stability vs Capacitive Load**



**Figure 40. Stability vs Capacitive Load**



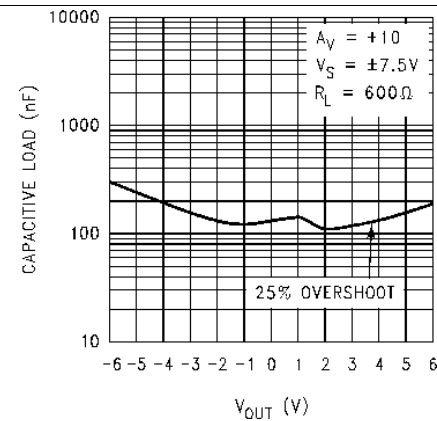
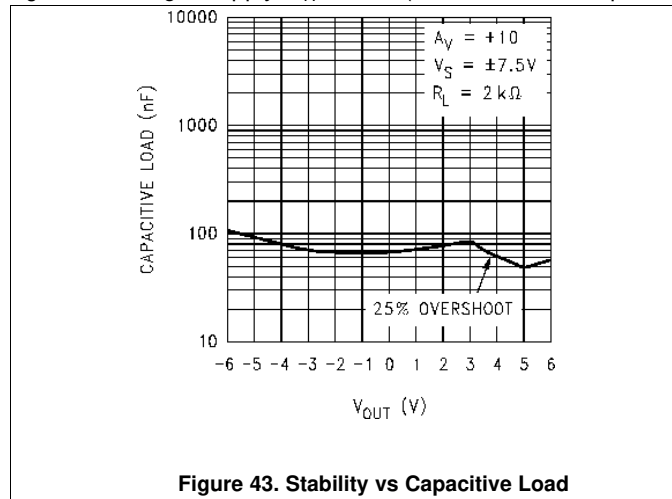
**Figure 41. Stability vs Capacitive Load**



**Figure 42. Stability vs Capacitive Load**

## Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

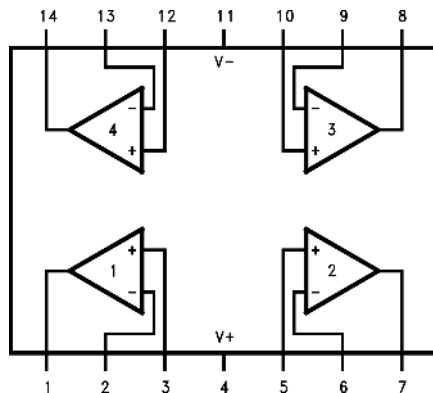


## 7 Detailed Description

### 7.1 Overview

The LMC6484C is a quad operational amplifier that offers a low cost, low power solution for applications requiring multiple operational amplifier stages and rail-to-rail operation. It supports a wide supply range (3 V to 15 V) and excellent amplifier-to-amplifier isolation (150 dB typical). It is ideal for battery-powered signal acquisition systems requiring highly integrated solutions to achieve efficient layout.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

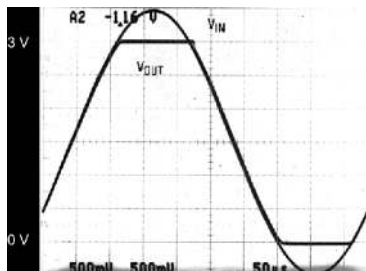
#### 7.3.1 Amplifier Topology

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common-mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, crossover distortion, and open-loop gain variation.

The input stage design of the LMC6484 is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

#### 7.3.2 Input Common-Mode Voltage Range

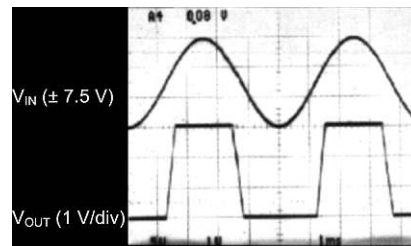
Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 46 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



**Figure 45. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages With No Output Phase Inversion**

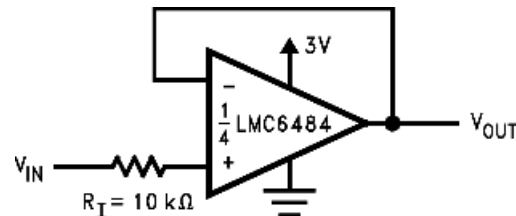
The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 46, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

## Feature Description (continued)



**Figure 46. A  $\pm 7.5\text{V}$  Input Signal Greatly Exceeds the 3-V Supply in [Figure 47](#) Causing No Phase Inversion Due to  $R_I$**

Applications that exceed this rating must externally limit the maximum input current to  $\pm 5\text{ mA}$  with an input resistor as shown in [Figure 47](#).



**Figure 47.  $R_I$  Input Current Protection for Voltages Exceeding the Supply Voltage**

### 7.3.3 Rail-to-Rail Output

The approximated output resistance of the LMC6484 is  $180\text{-}\Omega$  sourcing and  $130\text{-}\Omega$  sinking at  $V_S = 3\text{ V}$  and  $110\text{-}\Omega$  sourcing and  $83\text{-}\Omega$  sinking at  $V_S = 5\text{ V}$ . Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

## 7.4 Device Functional Modes

The LMC6482 may be used in applications where each amplifier channel is used independently, or in applications in which the channels are cascaded. See [Typical Application](#) for more information.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the features of the LMC6484. The key benefit of designing in the LMC6484 is increased linear signal range. Most operational amplifiers have limited input common-mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common-mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common-mode ranges resulting in output phase inversion or severe distortion.

#### 8.1.2 Spice Macromodel

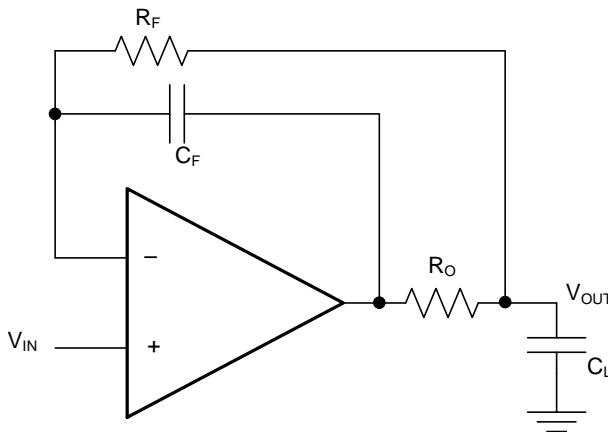
A spice macromodel is available for the LMC6484. This model includes accurate simulation of the following:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

### 8.2 Typical Application



**Figure 48. Unity Gain Buffer for High-Capacitive Loads**

## Typical Application (continued)

### 8.2.1 Design Requirements

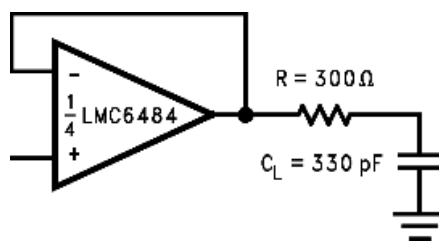
- For best performance, ensure that the input voltage swing is between  $V_+$  and  $V_-$ .
- Ensure that the input does not exceed the common-mode input range.
- To reduce the risk of de-stabilizing the output, use resistive isolation on the output when driving capacitive loads (see [Capacitive Load Compensation](#)).
- When large feedback resistors are used, it may be necessary to compensate for parasitic capacitance on the input (see [Compensating for Input Capacitance](#)).

### 8.2.2 Detailed Design Procedure

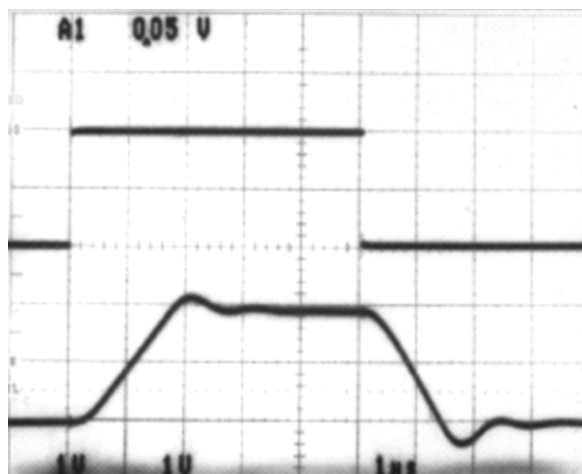
#### 8.2.2.1 Capacitive Load Compensation

The LMC6484 can typically directly drive a 100-pF load with  $V_S = 15\text{ V}$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of operational amplifiers. The combination of the output impedance of the operational amplifier and the capacitive load induces phase lag. This results in either an under-damped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in [Figure 49](#). This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.



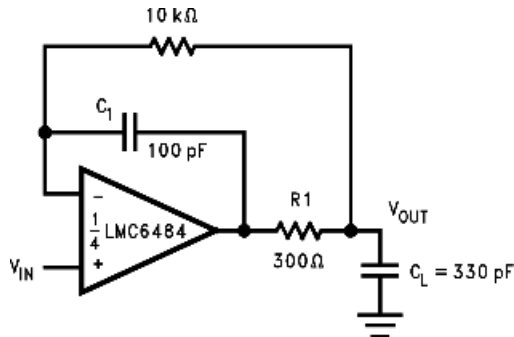
**Figure 49. Resistive Isolation of a 330-pF Capacitive Load**



**Figure 50. Pulse Response of the LMC6484 Circuit in [Figure 49](#)**

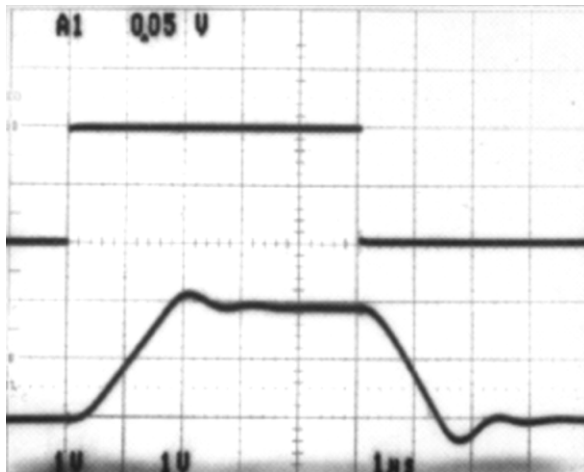
Improved frequency response is achieved by indirectly driving capacitive loads as shown in [Figure 51](#).

## Typical Application (continued)



**Figure 51. LMC6484 Noninverting Amplifier, Compensated to Handle a 330-pF Capacitive Load**

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high-frequency component of the output signal back to the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in [Figure 52](#).

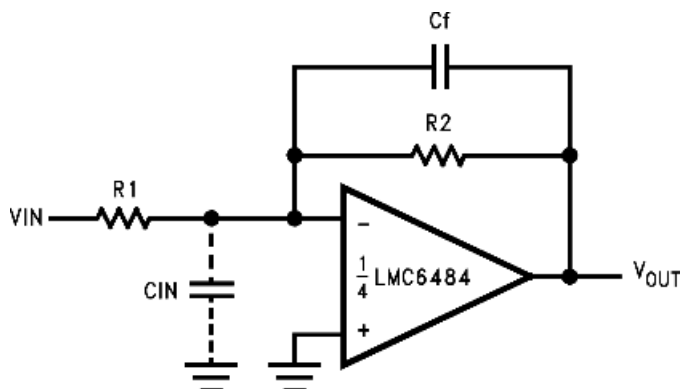


**Figure 52. Pulse Response of LMC6484 Circuit in [Figure 51](#)**

### 8.2.2.2 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

## Typical Application (continued)



**Figure 53. Canceling the Effect of Input Capacitance**

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in [Figure 53](#)),  $C_f$ , is first estimated by [Equation 1](#):

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

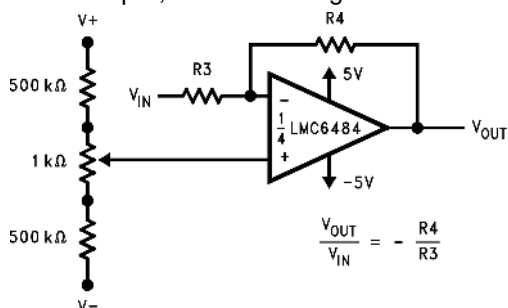
or

$$R_1 C_{IN} \leq R_2 C_f \quad (1)$$

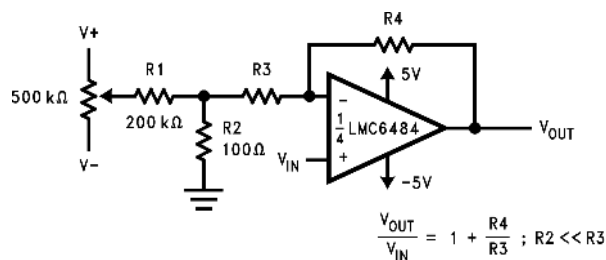
which typically provides significant overcompensation. Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for  $C_f$  may be different. The values of  $C_f$  should be checked on the actual circuit. (Refer to the LMC660 Quad CMOS Amplifier data sheet ([SNOSBZ3](#)) for a more detailed discussion.)

### 8.2.2.3 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in [Figure 54](#) and [Figure 55](#). Large value resistances and potentiometers are used to reduce power consumption while providing typically  $\pm 2.5$  mV of adjustment range, referred to the input, for both configurations with  $V_S = \pm 5$  V.



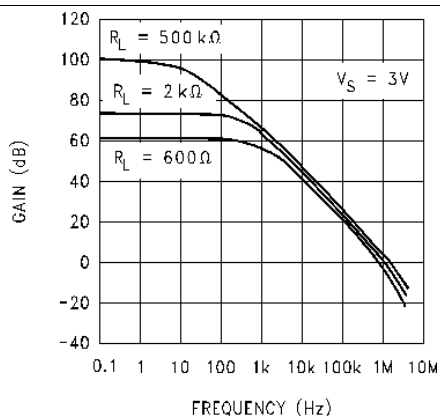
**Figure 54. Inverting Configuration Offset Voltage Adjustment**



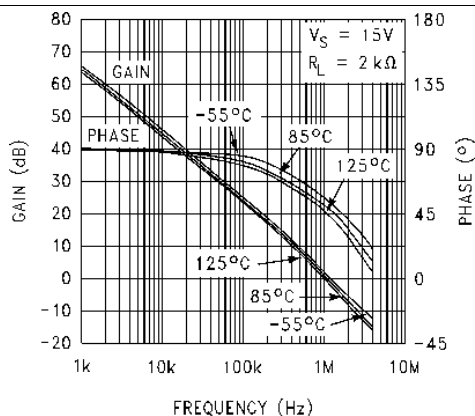
**Figure 55. Noninverting Configuration Offset Voltage Adjustment**

## Typical Application (continued)

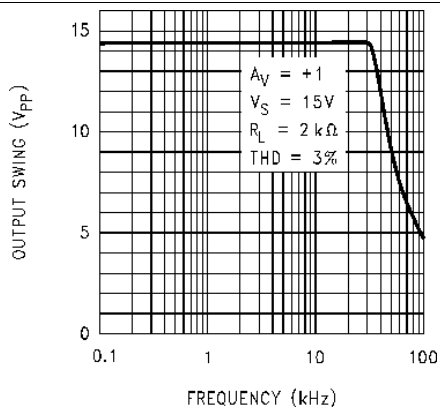
### 8.2.3 Application Curves



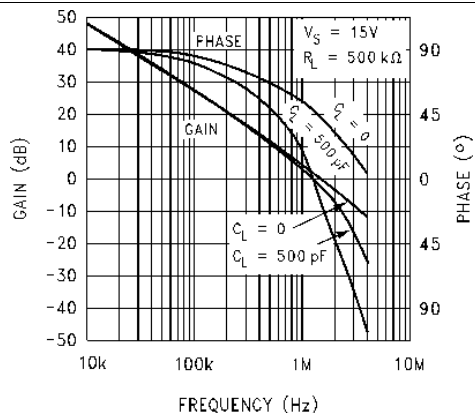
**Figure 56. Open Loop Frequency Response**



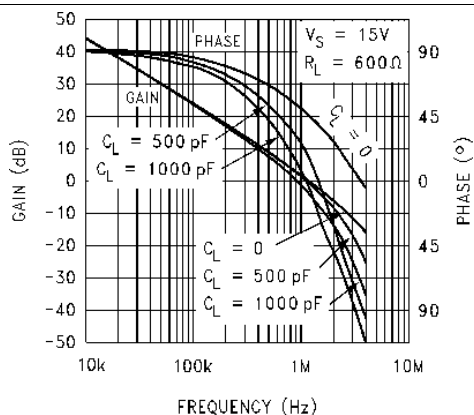
**Figure 57. Open Loop Frequency Response vs Temperature**



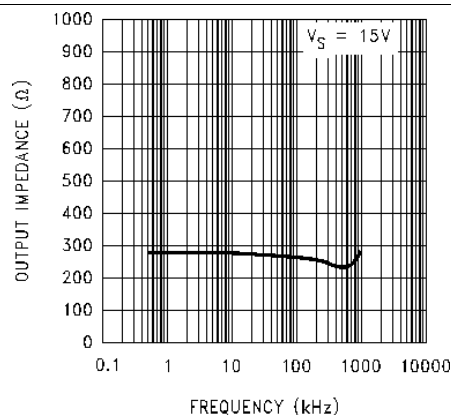
**Figure 58. Maximum Output Swing vs Frequency**



**Figure 59. Gain and Phase vs Capacitive Load**



**Figure 60. Gain and Phase vs Capacitive Load**



**Figure 61. Open Loop Output Impedance vs Frequency**

## LMC6484

SNOS675C – AUGUST 2000 – REVISED SEPTEMBER 2015

[www.ti.com](http://www.ti.com)

### Typical Application (continued)

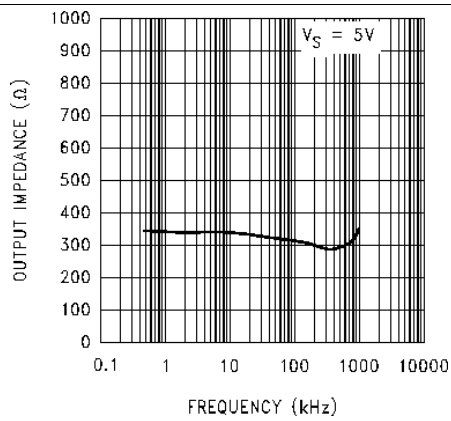


Figure 62. Open Loop Output Impedance vs Frequency

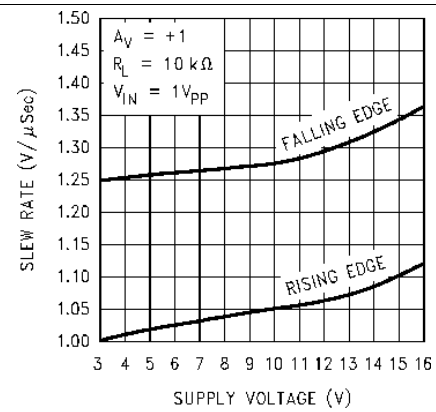


Figure 63. Slew Rate vs Supply Voltage

### 8.3 System Examples

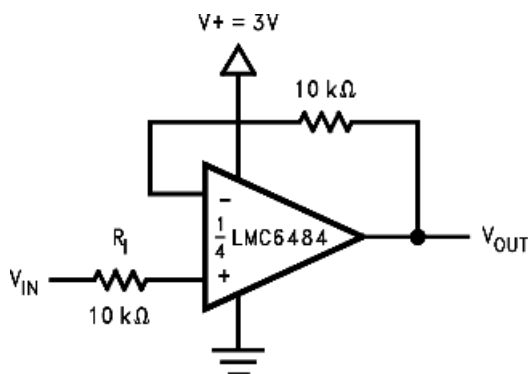


Figure 64. Half-Wave Rectifier with Input Current Protection ( $R_I$ )

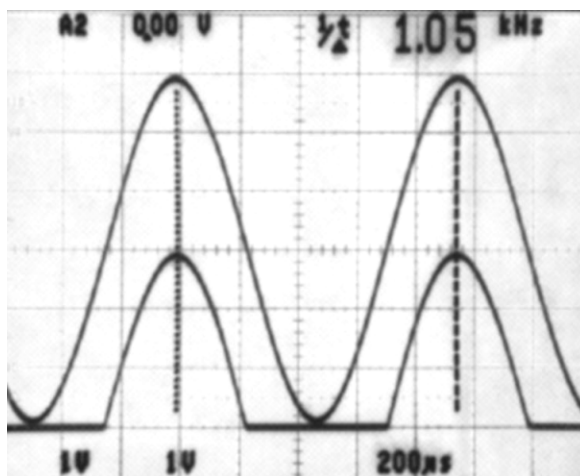


Figure 65. Half-Wave Rectifier Waveform

The circuit in [Figure 64](#) uses a single supply to half wave rectify a sinusoid centered about ground.  $R_I$  limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in [Figure 66](#).

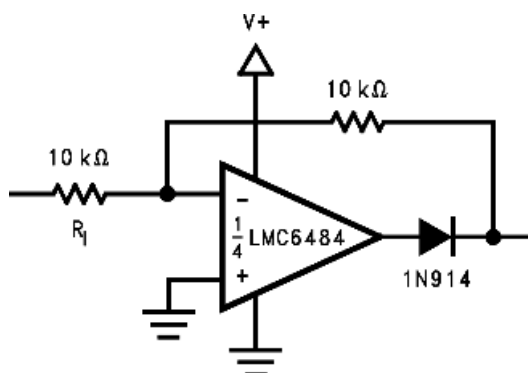
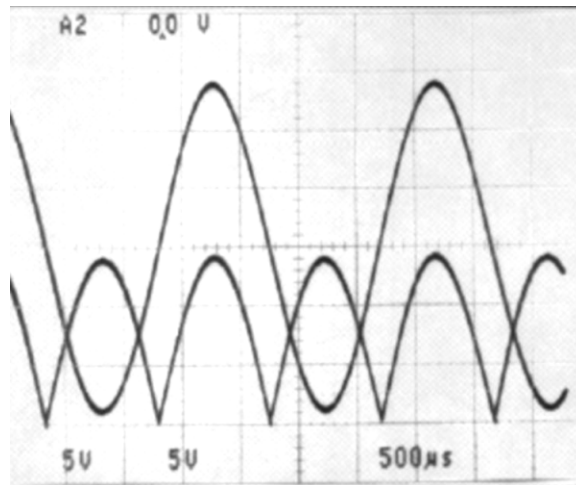
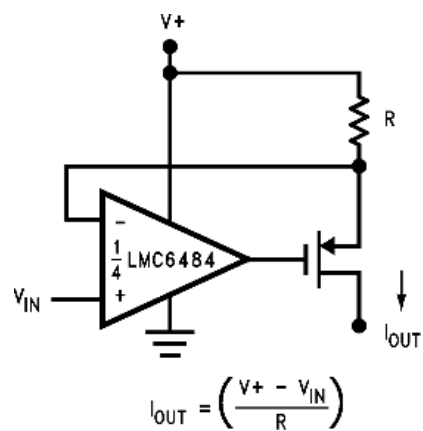


Figure 66. Full Wave Rectifier with Input Current Protection ( $R_I$ )

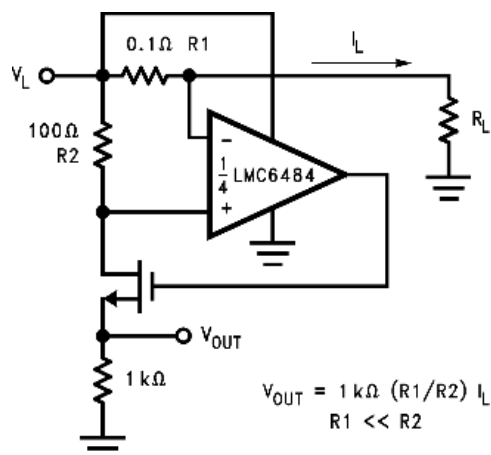
## System Examples (continued)



**Figure 67. Full Wave Rectifier Waveform**

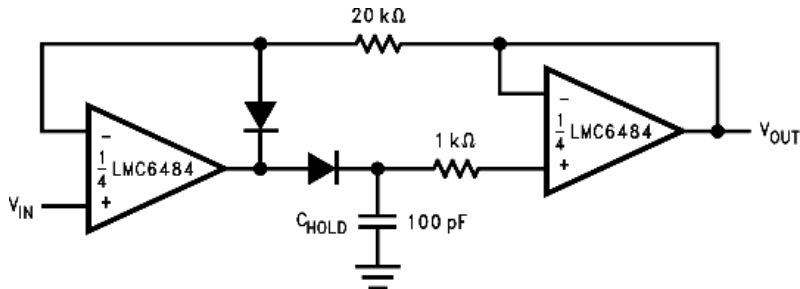


**Figure 68. Large Compliance Range Current Source**



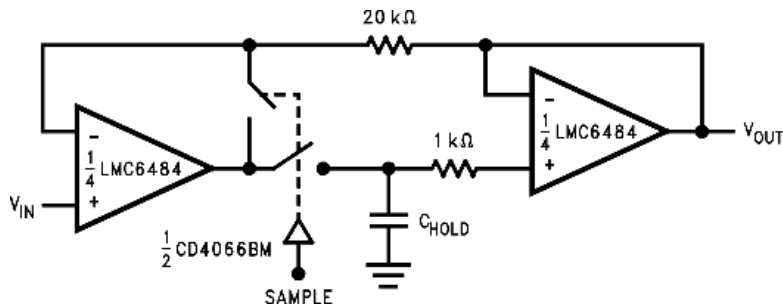
**Figure 69. Positive Supply Current Sense**

## System Examples (continued)



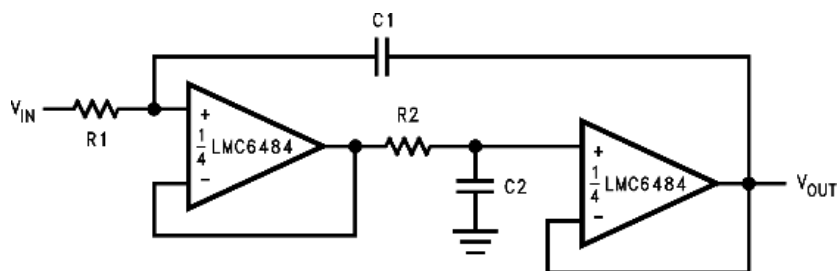
**Figure 70. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range**

In [Figure 70](#) dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of  $C_H$  and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.



**Figure 71. Rail-to-Rail Sample and Hold**

The high CMRR (85 dB) of the LMC6484 allows excellent accuracy throughout the rail-to-rail dynamic capture range of the circuit.



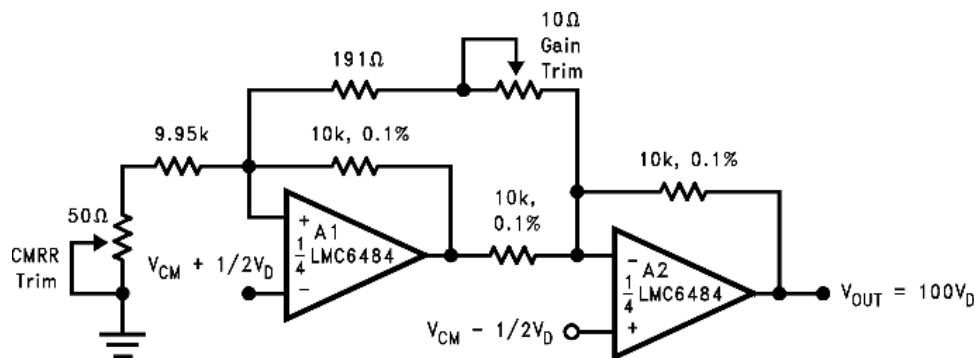
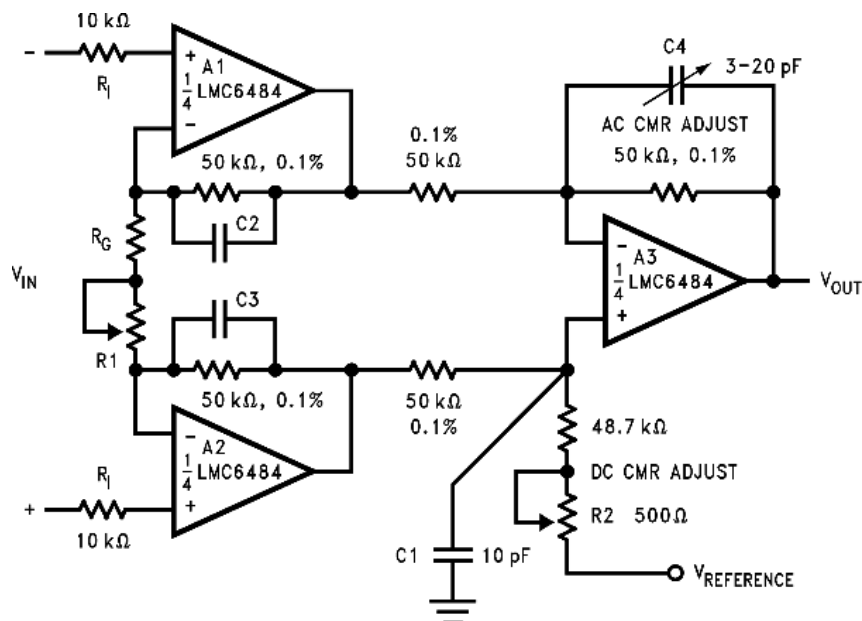
$$R1 = R2, C1 = C2; f = \frac{1}{2\pi R1 C1}; DF = \frac{1}{2} \sqrt{\frac{C2}{C1}} \sqrt{\frac{R2}{R1}}$$

**Figure 72. Rail-to-Rail Single Supply Low Pass Filter**

The low pass filter circuit in [Figure 72](#) can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used, which allows the use of smaller valued capacitors which take less board space and cost less.



### 8.3.2 Instrumentation Circuits



## 9 Power Supply Recommendations

The LMC6482 can be operated over a supply range of 3 V to 15 V. To achieve noise immunity as appropriate to the application, it is important to use good printed circuit board layout practices for power supply rails and planes, as well as using bypass capacitors connected between the power supply pins and ground.

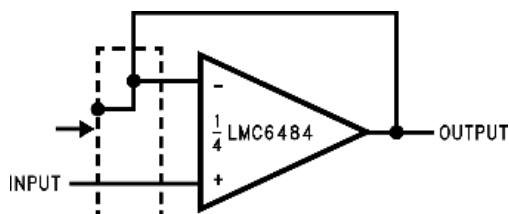
## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Printed-Circuit-Board Layout for High-Impedance Work

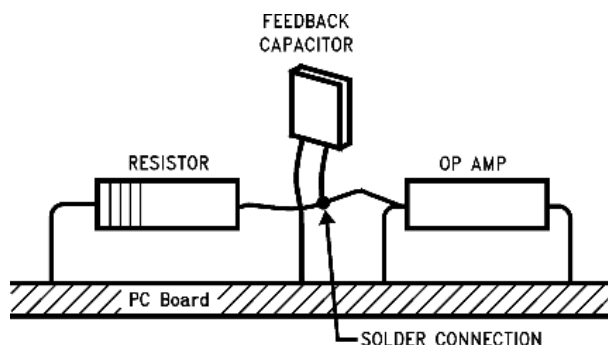
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc., connected to the operational amplifier inputs, as in [Figure 78](#). To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 1012, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input. This would cause a 250 times degradation from the actual performance of the LMC6484. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 1011 would cause only 0.05 pA of leakage current. See [Figure 76](#) for typical connections of guard rings for standard operational amplifier configurations.



**Figure 76. Typical Connections of Guard Rings**

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Do *not* insert the input pin of the amplifier into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 77](#).



Note: (Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

**Figure 77. Air Wiring**

## 10.2 Layout Example

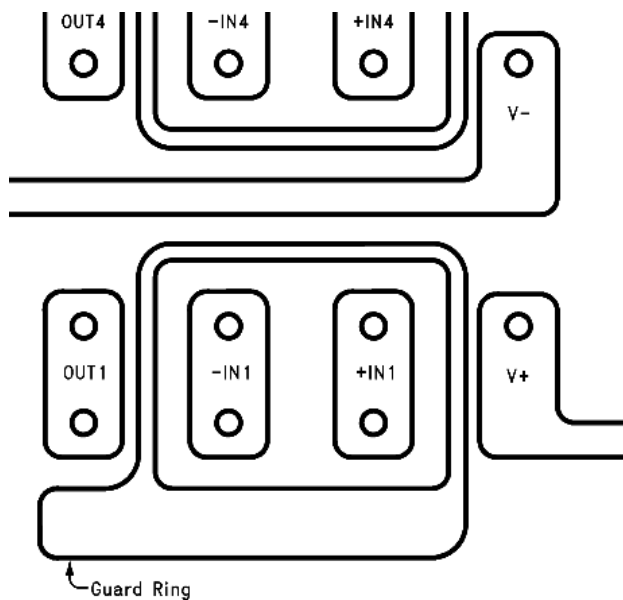


Figure 78. Example of Guard Ring in PCB Layout

## 11 Device and Documentation Support

### 11.1 Device Support

For the LMC6584 PSpice model, see [SNOM165](#).

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- *LMC6482 CMOS Dual Rail-To-Rail Input and Output Operational Amplifier* ([SNOS674](#))
- *LMC660 CMOS Quad Operational Amplifier* ([SNOSBZ3](#))

### 11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6484AIM	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMC6484 AIM	
LMC6484AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6484 AIM	<a href="#">Samples</a>
LMC6484AIMX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC6484 AIM	
LMC6484AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6484 AIM	<a href="#">Samples</a>
LMC6484AIN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6484AIN	<a href="#">Samples</a>
LMC6484IM	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMC6484IM	
LMC6484IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6484IM	<a href="#">Samples</a>
LMC6484IMX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC6484IM	
LMC6484IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6484IM	<a href="#">Samples</a>
LMC6484IN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6484IN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

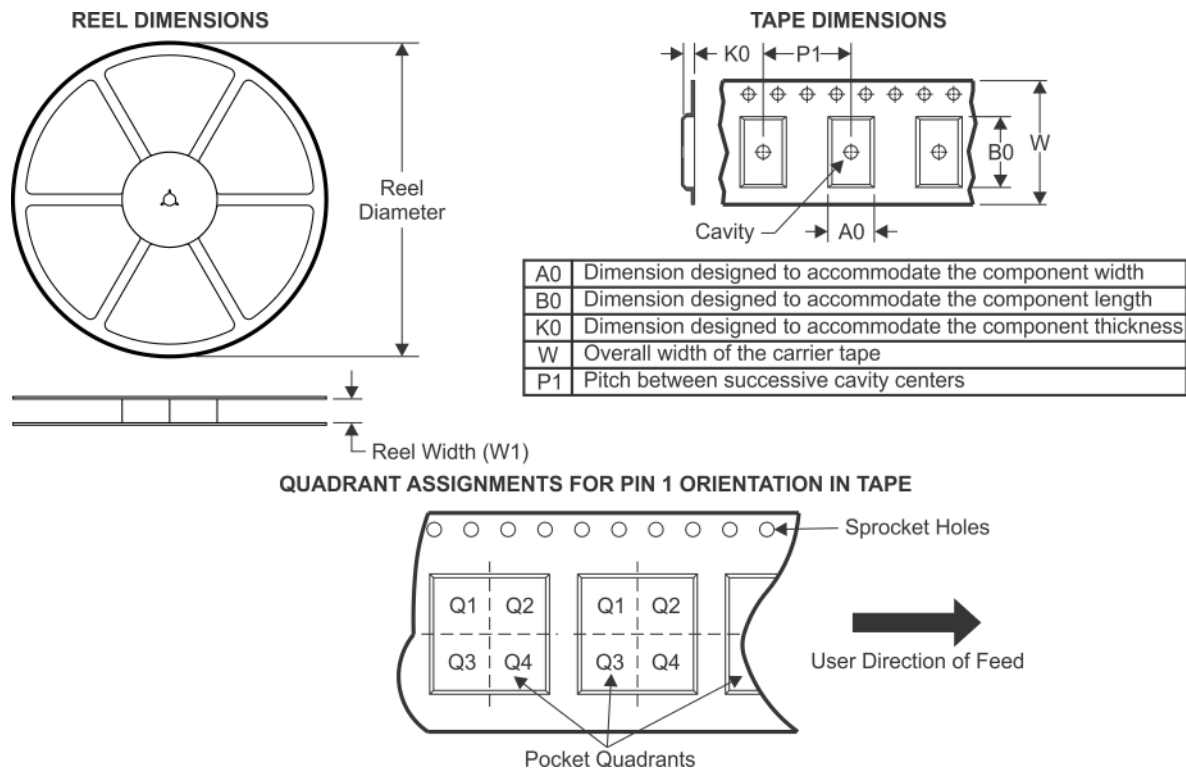
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

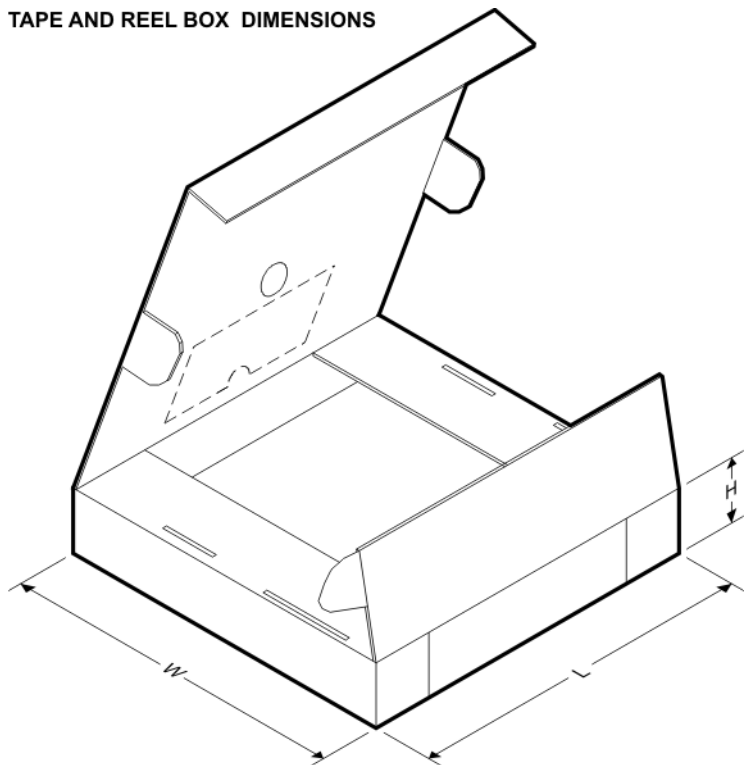
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6484AIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6484AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6484IMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6484IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

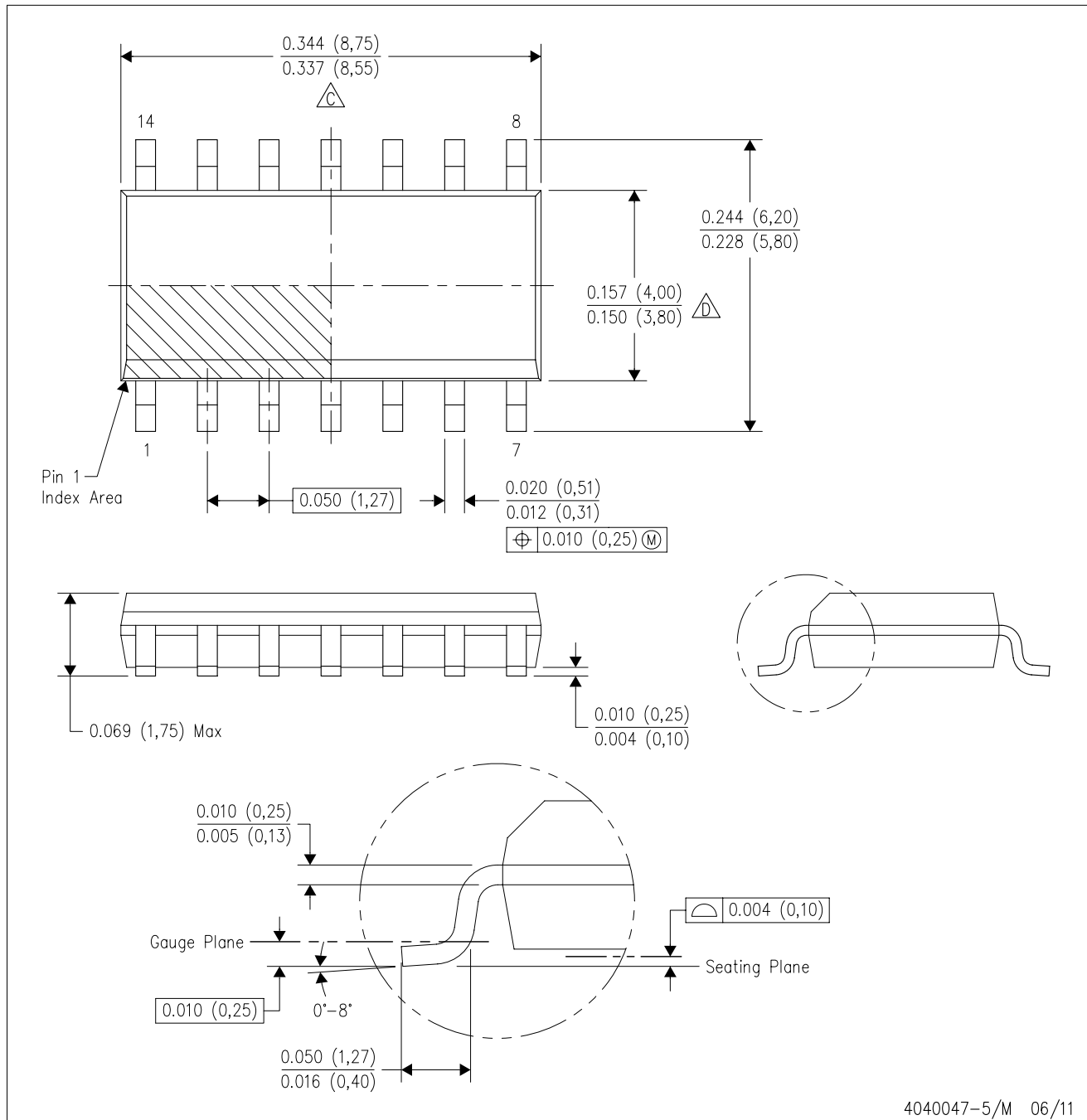


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6484AIMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC6484AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC6484IMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC6484IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

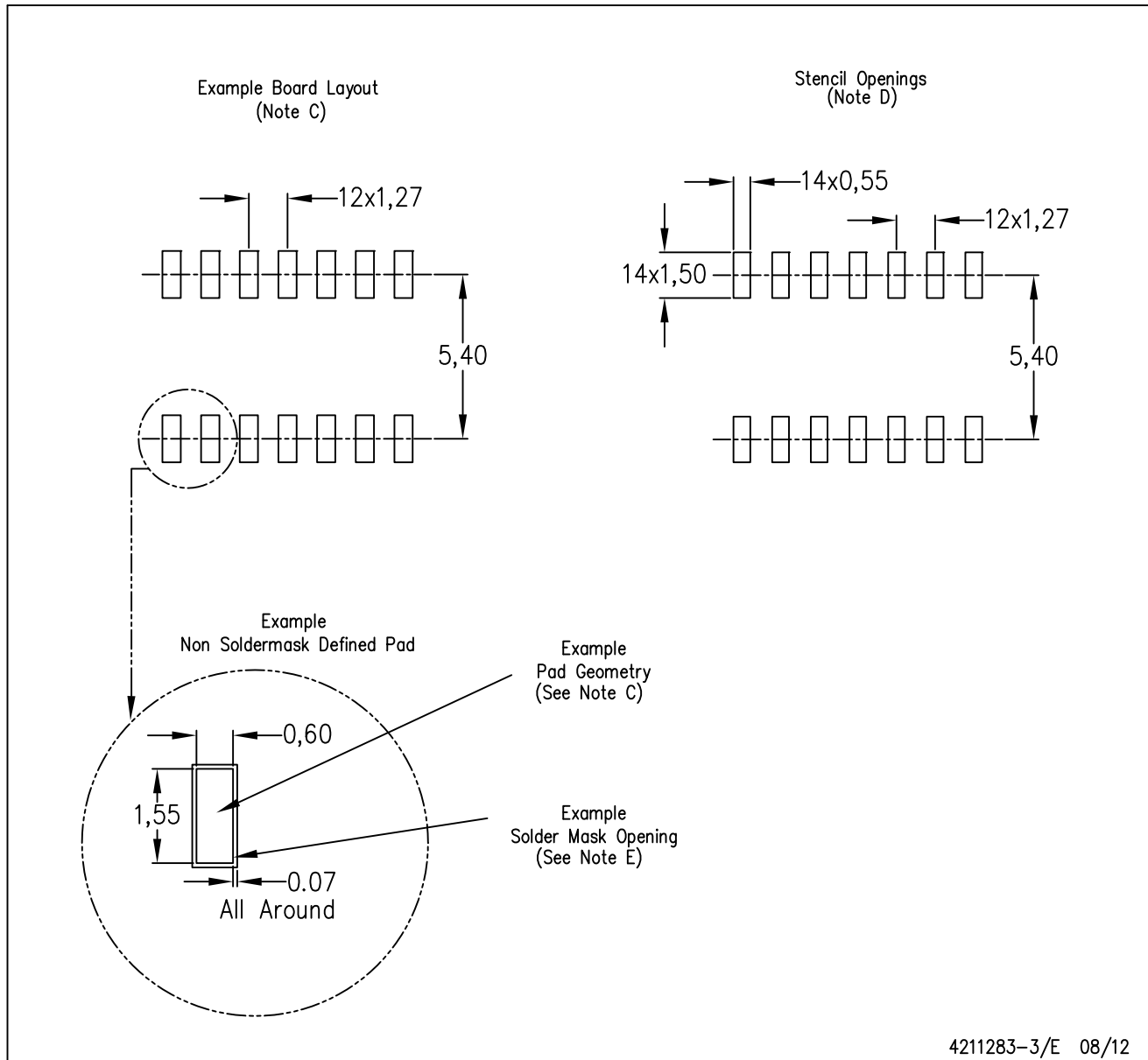


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

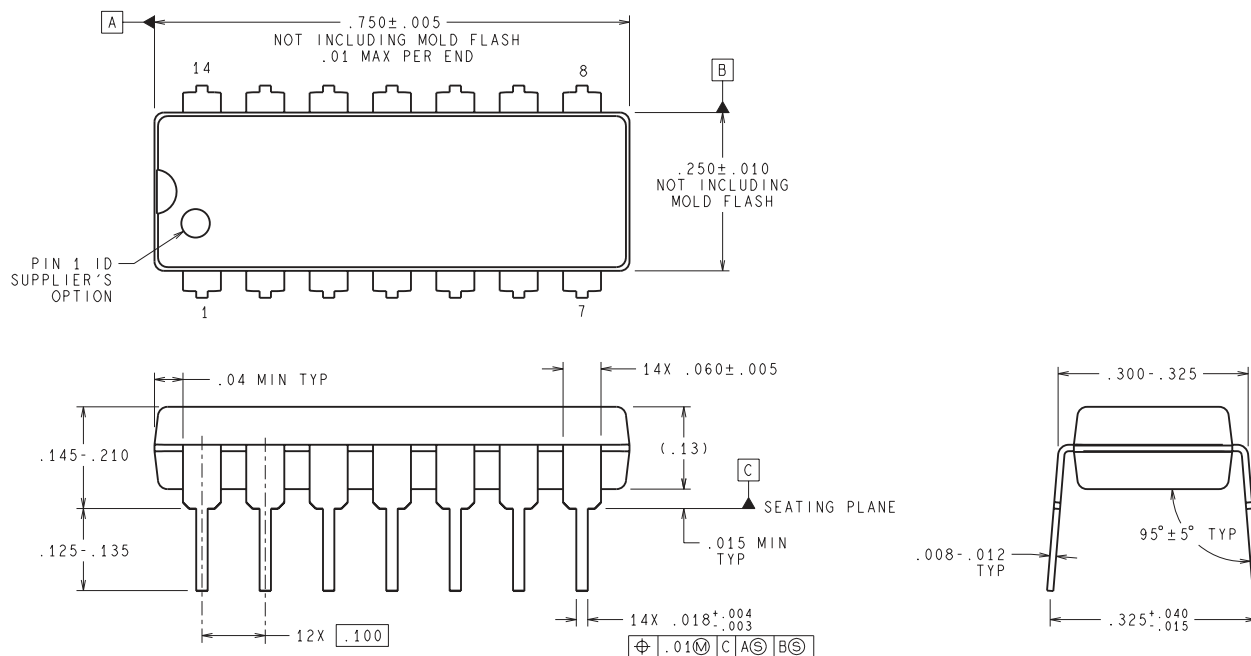
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NFF0014A



**DIMENSIONS ARE IN INCHES**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated