Precision 1-7 Clock Buffer

Features

- High speed: 140 MHz
- Low noise non-inverting 1-7 buffer
- Supports up to three SDRAM DIMMs
- Low skew (<250ps) between any two output clocks
- I^2C Serial Configuration interface
- Multiple V_{dd}, V_{ss} pins for noise reduction
- 3.3V power supply voltage
- 16-pin TSSOP (L) and QSOP (Q) packages

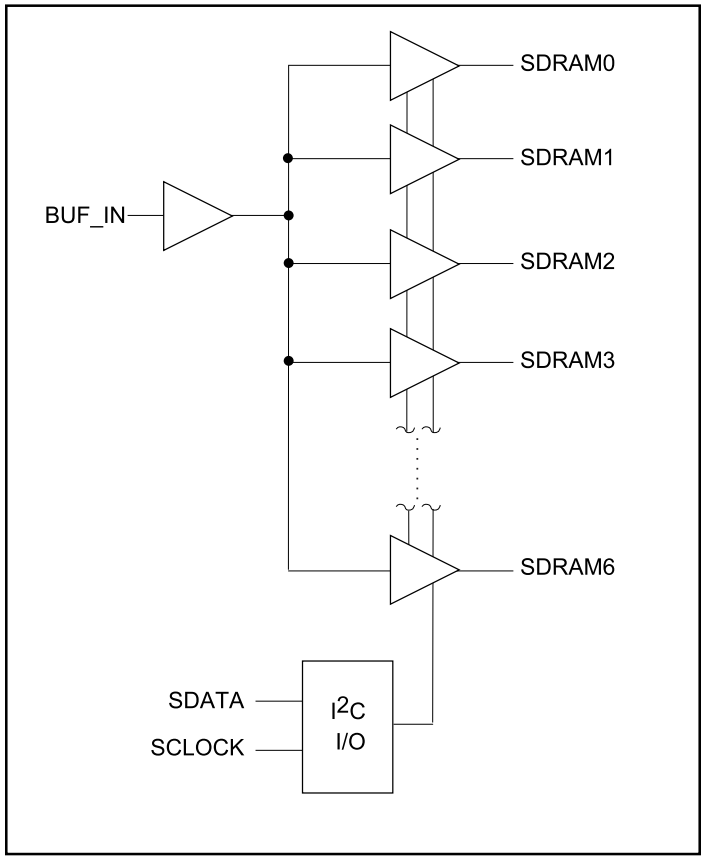
Description

The PI6C185-02B, a high-speed low-noise 1-7 non-inverting buffer, is designed for SDRAM clock buffer applications. It is intended to be used with the PI6C10X clock generator for Intel Architecture-based Mobile systems.

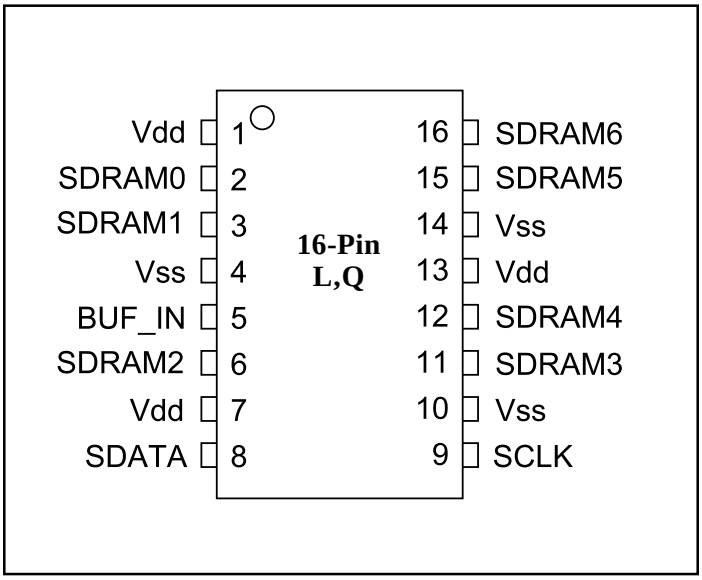
At power up, all SDRAM outputs are enabled and active. The I^2C Serial control may be used to individually activate/deactivate any of the seven output drivers.

Note:
Purchase of I^2C components from Pericom conveys a license to use them in an I^2C system as defined by Philips.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal	Type	Qty.	Description
2,3,6,11,12,15,16	SDRAM [0...6]	I	7	Buffered Clock Outputs
5	BUF_IN	I	1	Clock Buffer Input
8	SDATA	I/O	1	Serial Data for I^2C interface
9	SCLK	I	1	Serial Clock for I^2C interface
1,7,13	V_{DD}	Power	3	3.3V Power Supply
4,10,14	V_{SS}	Ground	3	Ground

PI6C185-02B I^2C Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0

PI6C185-02 Serial Configuration Map

Byte0: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	Description
Bit 7	6	SDRAM2
Bit 6	-	NC (Initialize to 0)
Bit 5	-	NC (Initialize to 0)
Bit 4	-	NC (Initialize to 0)
Bit 3	3	SDRAM1
Bit 2	2	SDRAM0
Bit 1	-	NC (Initialize to 0)
Bit 0	-	NC (Initialize to 0)

Note: Inactive means outputs are held LOWand are disabled from switching

Byte1: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	Description
Bit 7	16	SDRAM6
Bit 6	15	SDRAM5
Bit 5	-	NC (Initialize to 0)
Bit 4	-	NC (Initialize to 0)
Bit 3	12	SDRAM4
Bit 2	11	SDRAM3
Bit 1	-	NC (Initialize to 0)
Bit 0	-	NC (Initialize to 0)

2-Wire I^2C Control

The I^2C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C185-02B, a slave receiver device, cannot be read back. Sub addressing is not supported. To change one of the control bytes, all preceding bytes must be sent.

Every byte put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device.

During normal data transfers, SDATA changes only when SCLK is LOW. Exceptions: A HIGH to LOW transition on SDATA while SCLK is HIGH indicates a "start" condition; a LOW to HIGH transition on SDATA while SCLK is HIGH is a "stop" condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW = write to addressed device). If the device's own address is detected, PI6C185-02B generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (0D2H), two more bytes must be sent:

1. "Command Code" byte &2. "Byte Count" byte.

Although the data bits on these two bytes are "don't care," they must be sent and acknowledged.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied .....–0°C to +70°C
3.3V Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC Input Voltage ..... –0.5V to +4.6V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Supply Current (V_{DD} = +3.465V, Cload = max)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply Current	BUF_IN = 0 MHz			3	mA
I_{DD}	Supply Current	BUF_IN = 66.66 MHz			TBD	
I_{DD}	Supply Current	BUF_IN = 100.0 MHz				

DC Operating Specifications (V_{DD} = +3.3V ±5%, T_A = 0°C –70°C)

Symbol	Parameter	Condition	Min.	Max.	Units
Input Voltage					
V_{IH}	Input High Voltage	V_{DD}	2.0	V_{DD} +0.3	V
V_{IL}	Input Low Voltage		V_{SS} –0.3	0.8	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	µA
V_{DD} = 3.3V ± 5%					
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 1mA		0.4	
C_{IN}	Input Pin Capacitance			5	pF
C_{OUT}	Output pins Capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No Airflow	0	70	°C

SDRAM Clock Buffer Operating Specification

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 2.0V	–40			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			36	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.0V	40			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	
t_{RH}SDRAM	Output rise edge rate SDRAM only	3.3V ±5% @0.4V-2.4V	1.5		4	V/ns
t_{FH}SDRAM	Output fall edge rate SDRAM only	3.3V ±5% @2.4V-0.4V	1.5		4	

AC Timing

Symbol	Parameter	66 MHz		100 MHz		133 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SDKP}	SDRAM CLK period	15.0	15.5	10.0	10.5	7.5	7.8	ns
t_{SDKH}	SDRAM CLK high time	5.6		3.3		1.0		
t_{SDKL}	SDRAM CLK low time	5.3		3.1		1.0		
t_{SDRISE}	SDRAM CLK rise time	1.5	4.0	1.5	4.0	1.5	4.0	V/ns
t_{SDFALL}	SDRAM CLK fall time	1.5	4.0	1.5	4.0	1.5	4.0	
t_{PLH}	SDRAM Buffer LH prop delay	1.0	5.5	1.0	5.5	1.0	5.5	ns
t_{PHL}	SDRAM Buffer HL prop delay	1.0	5.5	1.0	5.5	1.0	5.5	
t_{PZL},t_{PZH}	SDRAM Buffer Enable delay	1.0	8.0	1.0	8.0	1.0	8.0	
t_{PLZ},t_{PHZ}	SDRAM Buffer Disable delay	1.0	8.0	1.0	8.0	1.0	8.0	
Duty Cycle	Measured at 1.5V	45	55	45	55	45	55	%
t_{SDSKW}	SDRAM Output to Output Skew		250		250		250	ps

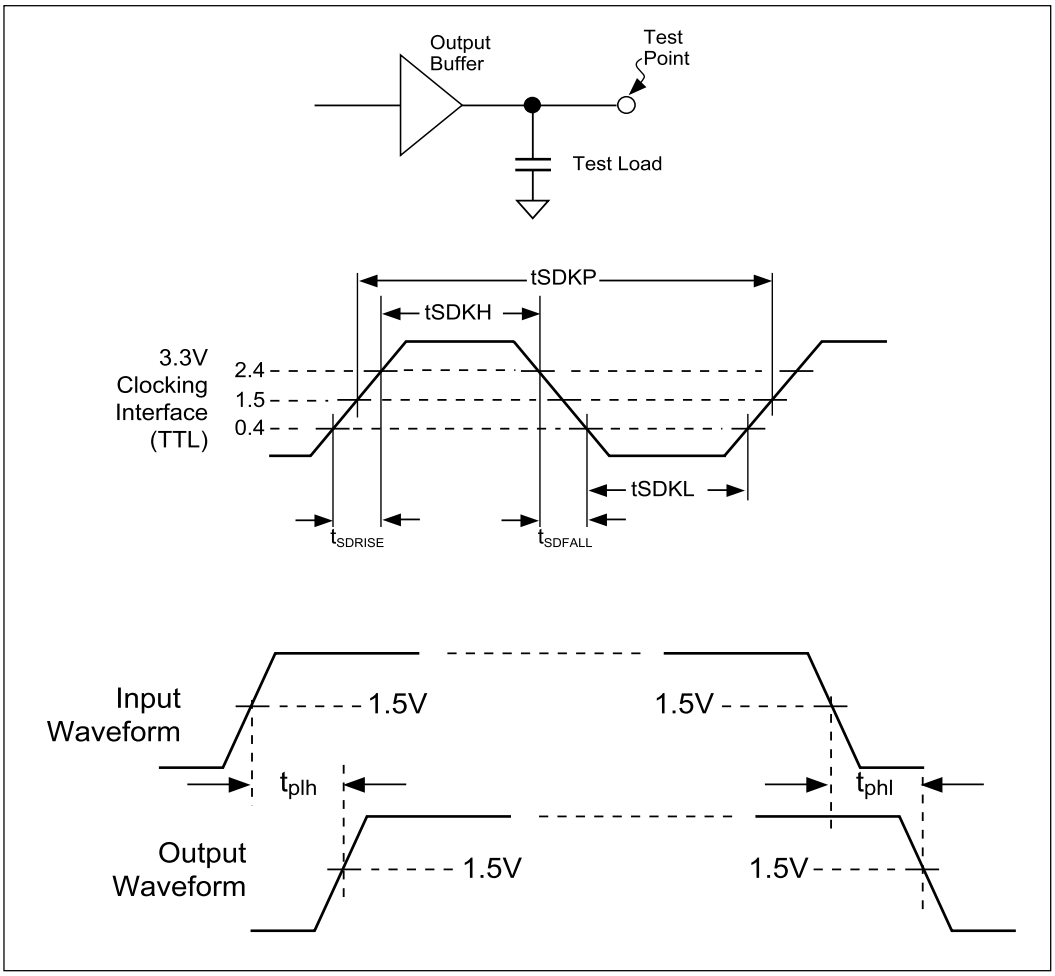


Figure 1. Clock Waveforms

Minimum and Maximum Expected Capacitive Loads

Clock	Min Load	Max Load	Units	Notes
SDRAM	15	20	pF	SDRAM DIMM Specification

Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load.
2. Minimum rise/fall times are guaranteed at minimum specified load.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

1. Place R_S series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. R_S Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.

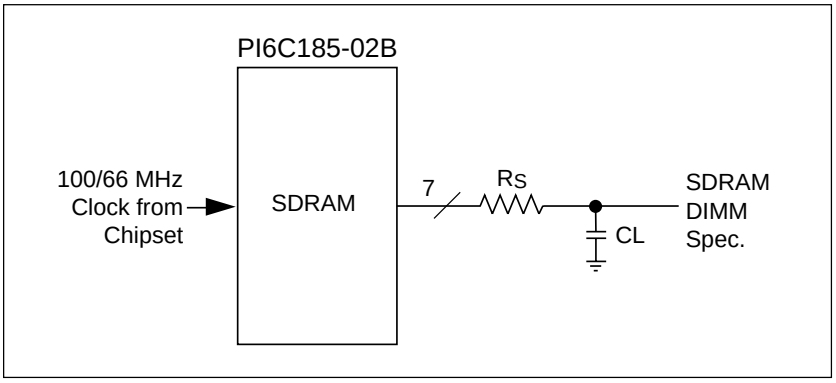
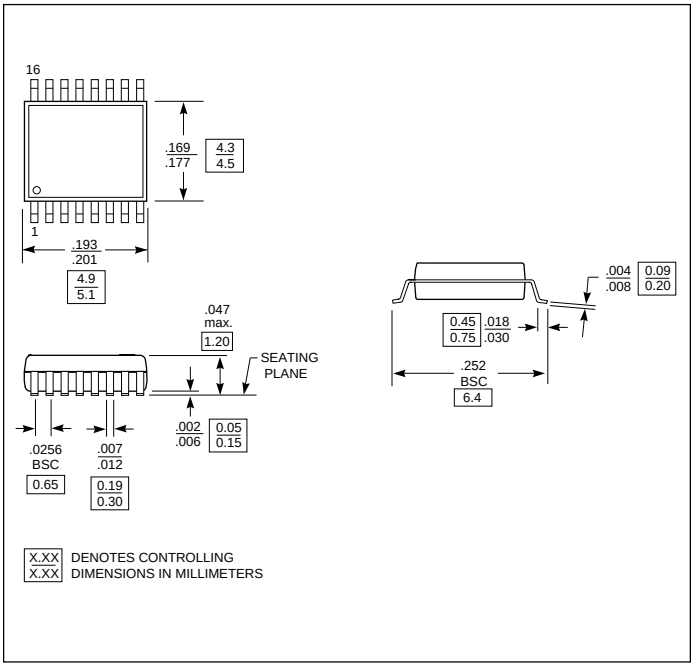
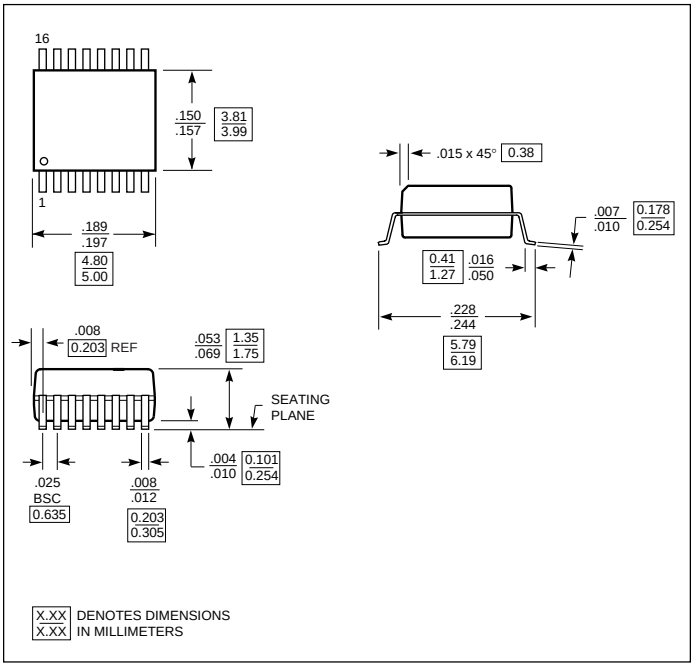


Figure 2. Design Guidelines

16-Pin TSSOP (L) Package



16-Pin QSOP (Q) Package



Ordering Information

P/N	Description
PI6C185-02BL	TSSOP Package
PI6C185-02BQ	QSOP Package