

MC14094B

8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8-stage shift register with a data latch for each stage and a 3-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_5 output data is for use in high-speed cascaded systems. The Q_5 output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by 3-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

Features

- 3-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B
- These are Pb-Free Devices*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|-------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}C$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

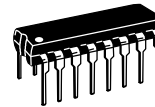
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



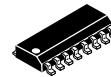
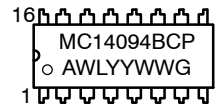
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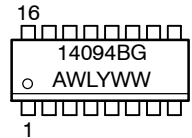
MARKING DIAGRAMS



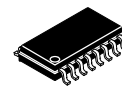
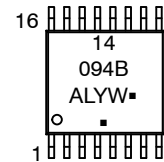
PDIP-16
P SUFFIX
CASE 648



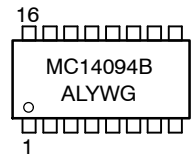
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Indicator

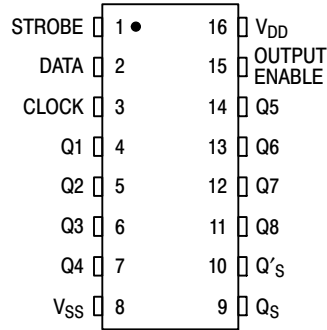
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PIN ASSIGNMENT



TRUTH TABLE

| Clock | Output Enable | Strobe | Data | Parallel Outputs | | Serial Outputs | |
|-------|---------------|--------|------|------------------|------------------|------------------|-----------------|
| | | | | Q ₁ | Q _N | Q _S * | Q' _S |
| | 0 | X | X | Z | Z | Q ₇ | No Chg. |
| | 0 | X | X | Z | Z | No Chg. | Q ₇ |
| | 1 | 0 | X | No Chg. | No Chg. | Q ₇ | No Chg. |
| | 1 | 1 | 0 | 0 | Q _{N-1} | Q ₇ | No Chg. |
| | 1 | 1 | 1 | 1 | Q _{N-1} | Q ₇ | No Chg. |
| | 1 | 1 | 1 | No Chg. | No Chg. | No Chg. | Q ₇ |

Z = High Impedance X = Don't Care

* At the positive clock edge, information in the 7th shift register stage is transferred to Q₈ and Q_S.

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|------------------------|--------------------------|
| MC14094BCPG | PDIP-16 (Pb-Free) | 500 Units / Rail |
| MC14094BDG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC14094BDR2G | SOIC-16 (Pb-Free) | 2500 Units / Tape & Reel |
| MC14094BDTR2G | TSSOP-16* | 2500 Units / Tape & Reel |
| MC14094BFG | SOEIAJ-16 (Pb-Free) | 50 Units / Rail |
| MC14094BFELG | SOEIAJ-16 (Pb-Free) | 2000 Units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | - 55 °C | | 25 °C | | | 125 °C | | Unit | |
|--|---|------------------------|---|-------|-------|--------------------|-------|--------|-------|------|------|
| | | | Min | Max | Min | Typ ⁽²⁾ | Max | Min | Max | | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level V _{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc | |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| | "1" Level V _{in} = 0 or V _{DD} | V _{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | | - |
| | | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | | - |
| | | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | | - |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level V _{IL} | 5.0 | - | 1.5 | - | 2.25 | 1.5 | - | 1.5 | Vdc | |
| | | 10 | - | 3.0 | - | 4.50 | 3.0 | - | 3.0 | | |
| | | 15 | - | 4.0 | - | 6.75 | 4.0 | - | 4.0 | | |
| | "1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IH} | 5.0 | 3.5 | - | 3.5 | 2.75 | - | 3.5 | | - |
| | | | 10 | 7.0 | - | 7.0 | 5.50 | - | 7.0 | | - |
| | | | 15 | 11 | - | 11 | 8.25 | - | 11 | | - |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source I _{OH} | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mAdc | |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | | |
| | Sink I _{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | | mAdc |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | | |
| 15 | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | - | | | |
| Input Current | I _{in} | 15 | - | ± 0.1 | - | ± 0.00001 | ± 0.1 | - | ± 1.0 | μAdc | |
| Input Capacitance (V _{in} = 0) | C _{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF | |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | - | 5.0 | - | 0.005 | 5.0 | - | 150 | μAdc | |
| | | 10 | - | 10 | - | 0.010 | 10 | - | 300 | | |
| | | 15 | - | 20 | - | 0.015 | 20 | - | 600 | | |
| Total Supply Current ^{(3) (4)} (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (4.1 μA/kHz) f + I _{DD} | | | | | | | μAdc | |
| | | 10 | I _T = (14 μA/kHz) f + I _{DD} | | | | | | | | |
| | | 15 | I _T = (140 μA/kHz) f + I _{DD} | | | | | | | | |
| 3-State Output Leakage Current | I _{TL} | 15 | - | ± 0.1 | - | ± 0.0001 | ± 0.1 | - | ± 3.0 | μA | |

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25 °C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

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SWITCHING CHARACTERISTICS ⁽⁵⁾ ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V _{DD} Vdc | Min | Typ ⁽⁶⁾ | Max | Unit |
|--|----------------------------|------------------------|------------------|--------------------|--------------------|---------------|
| Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{TLH} , t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time (Figure 1) Clock to Serial out QS $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 305 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$ Clock to Serial out Q'S $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 350 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 149 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$ Clock to Parallel out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.35 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 122 \text{ ns}$ Strobe to Parallel out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 245 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 127 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ | t_{PLH} , t_{PHL} | 5.0 10 15 | – – – | 350 125 95 | 600 250 190 | ns |
| Output Enable to Output $t_{PHZ}, t_{PZL} = (0.90 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PHZ}, t_{PZL} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHZ}, t_{PZL} = (0.26 \text{ ns/pF}) C_L + 42 \text{ ns}$ | t_{PHZ} , t_{PZL} | 5.0 10 15 | – – – | 140 75 55 | 280 150 110 | |
| $t_{PLZ}, t_{PZH} = (0.90 \text{ ns/pF}) C_L + 180 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.36 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$ | t_{PLZ} , t_{PZH} | 5.0 10 15 | – – – | 225 95 70 | 450 190 140 | |
| Setup Time Data in to Clock | t_{su} | 5.0 10 15 | 125 55 35 | 60 30 20 | – – – | ns |
| Hold Time Clock to Data | t_h | 5.0 10 15 | 0 20 20 | –40 –10 0 | – – – | ns |
| Clock Pulse Width, High | t_{WH} | 5.0 10 15 | 200 100 83 | 100 50 40 | – – – | ns |
| Clock Rise and Fall Time | $t_{r(cl)}$ $t_{f(cl)}$ | 5 10 15 | – – – | – – – | 15 5.0 4.0 | μs |
| Clock Pulse Frequency | f_{cl} | 5.0 10 15 | – – – | 2.5 5.0 6.0 | 1.25 2.5 3.0 | MHz |
| Strobe Pulse Width | t_{WL} | 5.0 10 15 | 200 80 70 | 100 40 35 | – – – | ns |

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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3-STATE TEST CIRCUIT

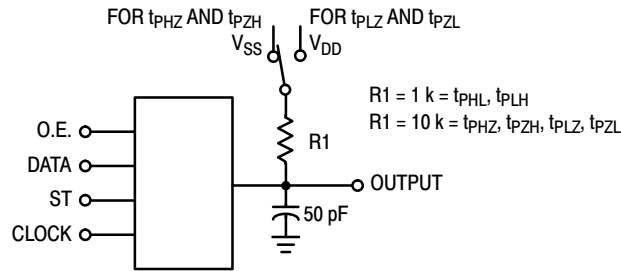
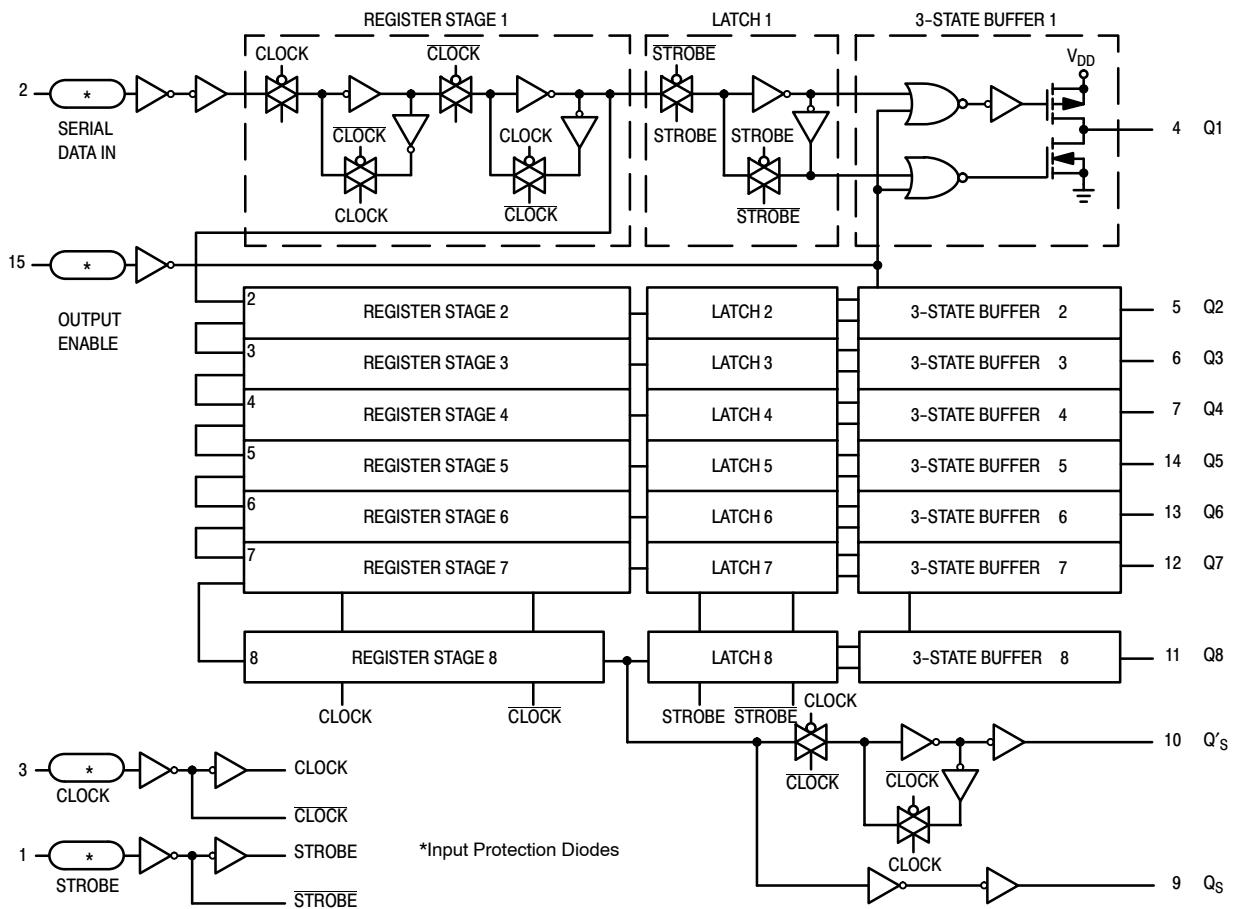


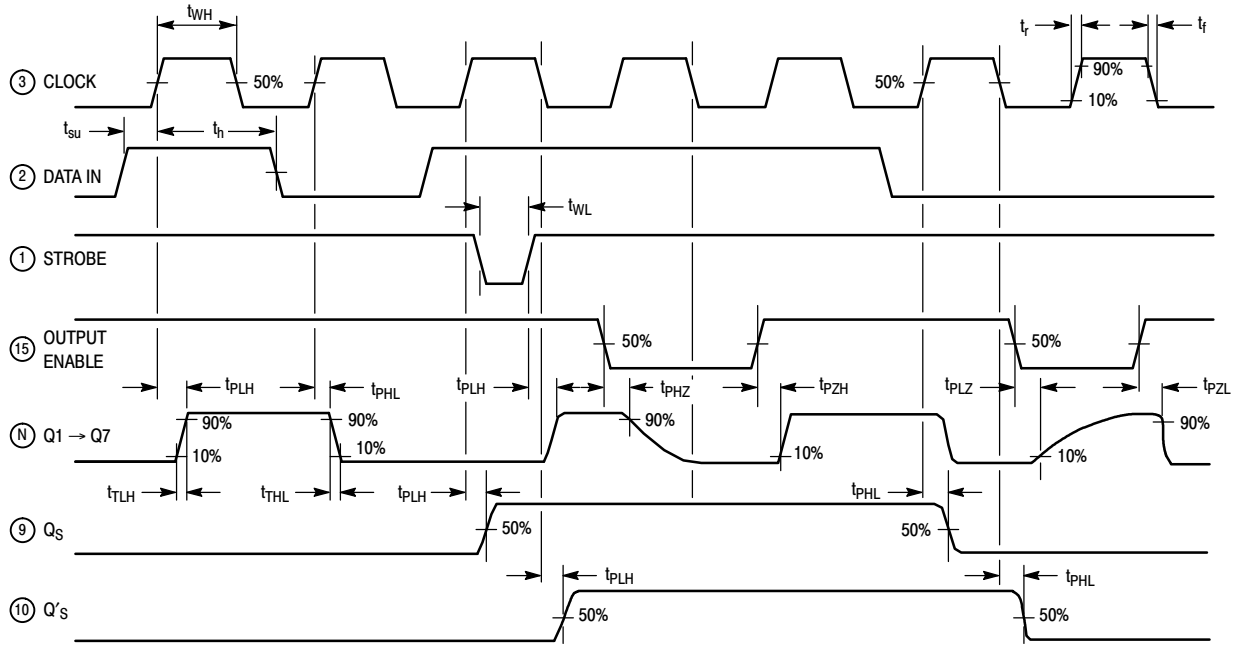
Figure 1.

BLOCK DIAGRAM



MC14094B

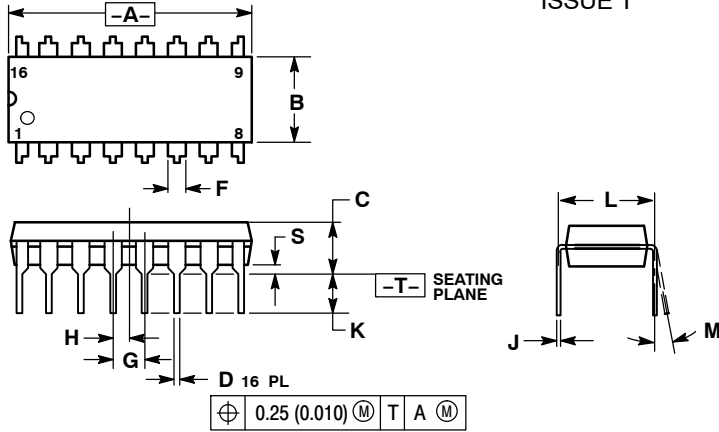
DYNAMIC TIMING DIAGRAM



MC14094B

PACKAGE DIMENSIONS

PDIP-16
P SUFFIX
CASE 648-08
ISSUE T

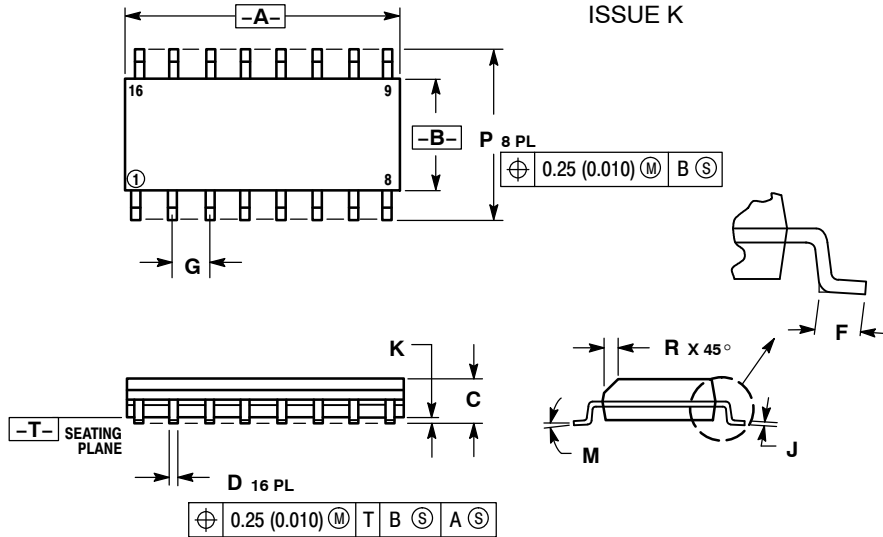


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE K

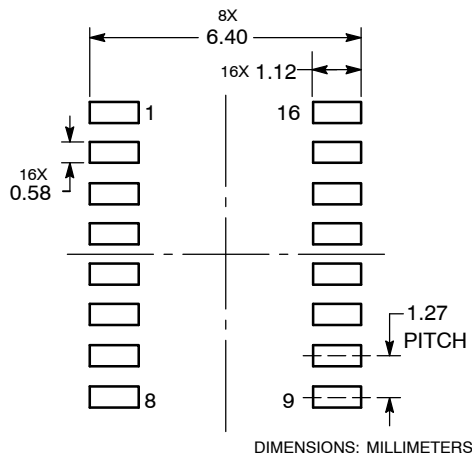


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

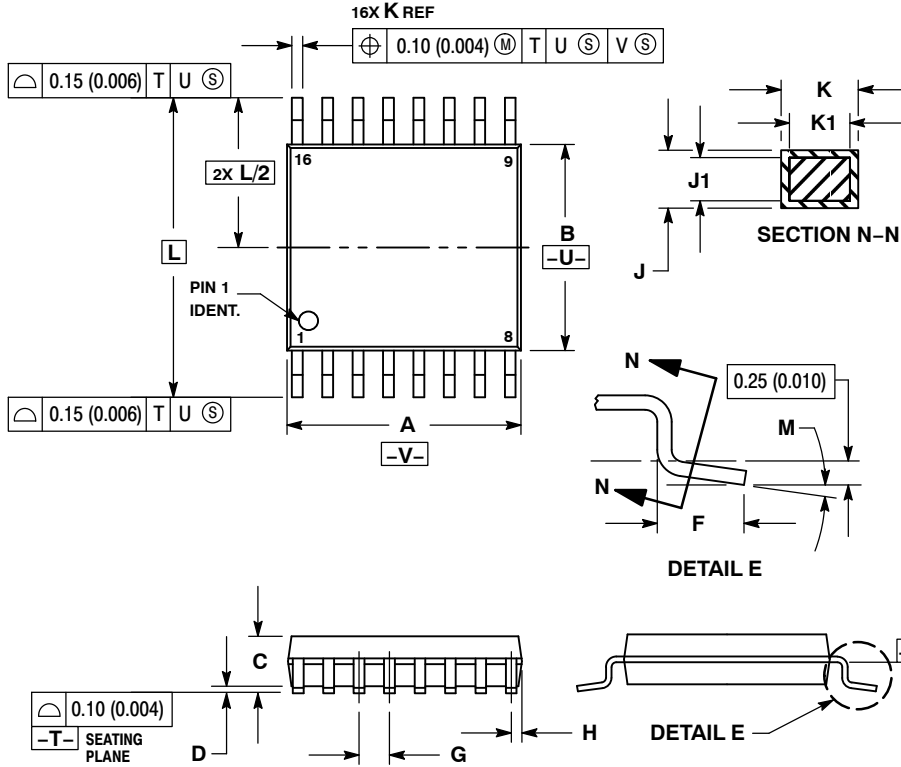
SOLDERING FOOTPRINT



MC14094B

PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B

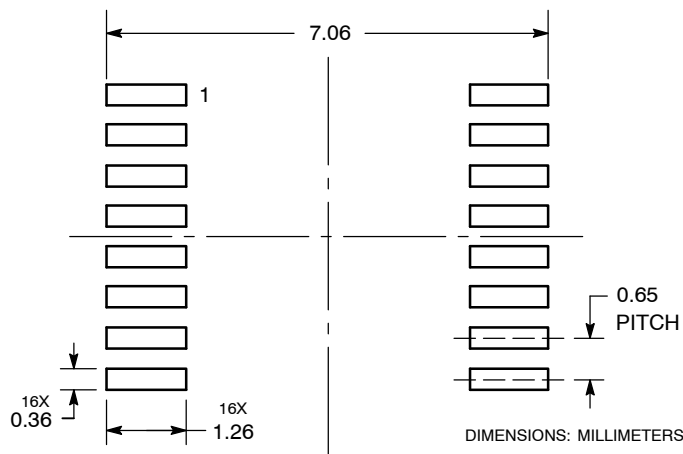


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

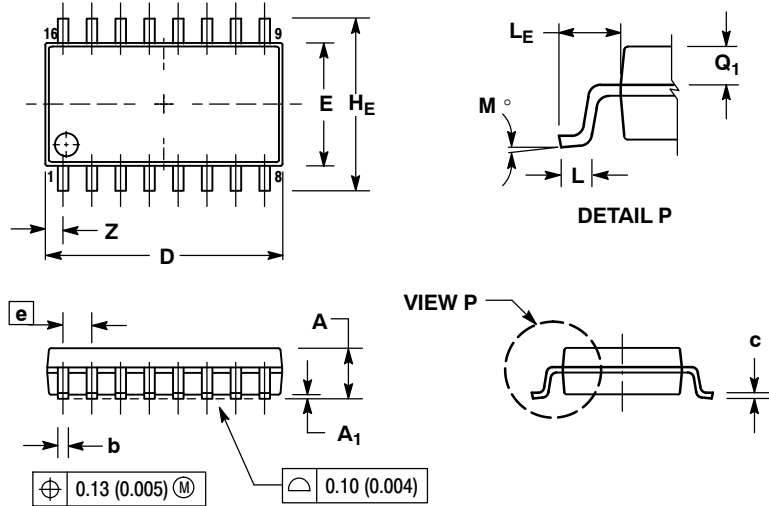
SOLDERING FOOTPRINT



MC14094B

PACKAGE DIMENSIONS

SOEIAJ-16
F SUFFIX
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

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