# MAX5871

# 16-Bit, 5.9Gsps Interpolating and Modulating RF DAC with JESD204B Interface

## General Description

The MAX5871 high-performance interpolating and modulating 16-bit 5.9Gsps RF DAC can directly synthesize up to 600MHz of instantaneous bandwidth from DC to frequencies greater than 2.8GHz. The device enables multi-standard and multi-band transmitters in wireless communications applications. The device meets spectral mask requirements for a broad set of communication standards including multicarrier GSM, UMTS, and LTE.

The device integrates interpolation filters, a digital quadrature modulator, a numerically controlled oscillator (NCO), clock multiplying PLL+VCO and a 14-bit RF DAC core. The user-configurable 5x, 6x, 6.67x, 8x, 10x, 12x, 13.33x, 16x, 20x or 24x, linear phase interpolation filters simplify reconstruction filtering, while enhancing passband dynamic performance, and reduce the input data bandwidth required from an FPGA/ASIC. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis.

The MAX5871 accepts 16-bit input data via a four-lane JESD204B SerDes data input interface that is Subclass-0 and Subclass-1 compliant. The interface can be configured for 1, 2, or 4 lanes and supports data rates up to 10Gbps per lane allowing flexibility to optimize the I/O count and speed.

The MAX5871 clock input has a flexible clock interface and accepts a differential sine-wave, or square-wave input clock signal. A bypassable clock multiplying PLL and VCO can be used to generate a high-frequency sampling clock. The device outputs a divided reference clock to ensure synchronization of the system clock and DAC clock. In addition, multiple devices can be synchronized using JESD204B Subclass-1.

The MAX5871 uses a differential current-steering architecture and can produce a 0dBm full-scale output signal level with a 50Ω load. Operating from 1.8V and 1.0V power supplies, the device consumes 2.5W at 4.9Gsps. The device is offered in a compact 144-pin, 10mm x 10mm, FCCSP package and is specified for the extended industrial temperature range (-40°C to +85°C).

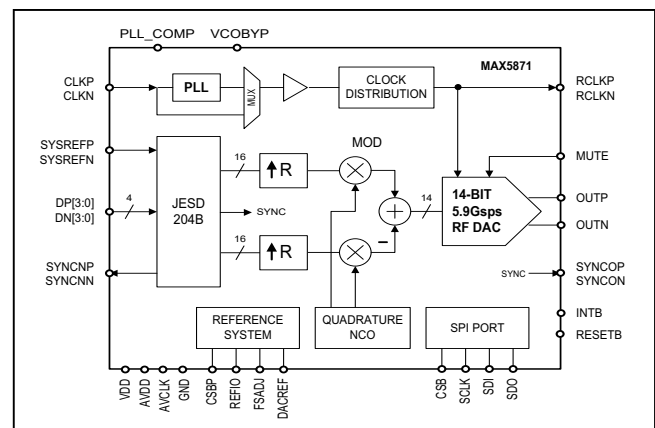*Ordering Information* **appears at end of data sheet.**

## Benefits and Features

- Simplifies RF Design and Enables New Wireless Communication Architectures
  - Eliminates I/Q Imbalance and LO Feedthrough
  - Enables Multi-Band RF Modulation
- Direct RF Synthesis of 600MHz Bandwidth Up to 2.8GHz
  - 5.898Gsps DAC Output Update Rate
  - High-Performance 14-Bit RF DAC Core
  - Digital Quadrature Modulator and NCO with 1Hz/10Hz/100Hz/1kHz/10kHz Resolution
  - 5x/6x/6.67x/8x/10x/12x/13.33x/16x/20x/24x Interpolation
  - Integrated Clock Multiplying PLL+VCO
- Highly Flexible and Configurable
  - 1, 2, or 4-Lane JESD204B Input Data Interface
    - Subclass-0 and Subclass-1 Compliant
    - Up to 10Gbps Per Lane
  - Reference Clock for System Synchronization
  - Multiple DAC Synchronization (Subclass-1)
  - SPI Interface for Device Configuration

## Applications

- Cellular Base-Station Transmitters
  - 2.5G/3G - GSM/TDMA/CDMA/UMTS
  - 4G LTE and WiMAX
- Multi-Standard and Multi-Band Transmitters
- Point-to-Point Microwave Links
- Wireless Backhaul

## Simplified Block Diagram

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VDD2, AVCLK2, AVDD2, AVDD2PLL,
   VDD2PLL.......................................................-0.3V to +2.1V
OUTP, OUTN .................................... -0.3V to ($V_{AVDD2}$ + 0.5V)
MUTE, RESETB, CSB, SCLK, SDO, SDI,
   INTB,TDA .....................-0.3V to ($V_{VDD2}$ + 0.3V, MAX 2.1V)
SYSREFP, SYSREFN, SYNCIP, SYNCIN, SYNCOP, SYNCON,
   RCLKP, RCLKN ............. -0.3V to ($V_{VDD2}$ + 0.3V, MAX 2.1V)
DP0, DN0, DP1, DN1, DP2, DN2, DP3,
   DN3...............................-0.3V to ($V_{VDD2}$ + 0.3V, MAX 2.1V)
JRES, CAPT, SYSREFEN ............................ ($V_{VSSPLL}$ - 0.3V)
   .......................................... to ($V_{VDD2PLL}$ + 0.3V, MAX 2.1V)
VCOBYP..........................-0.3V to ($V_{AVCLK2}$ + 0.3V, MAX 2.1V)

PLL_COMP .................-0.3V to ($V_{AVDD2PLL}$ + 0.3V, MAX 2.1V)
VSSPLL, TDC, DACREF..........($V_{GND}$ - 0.3V) to ($V_{GND}$ + 0.3V)
VDD, AVDD, AVCLK, AVDD1PLL .......................-0.3V to +1.2V
REFIO, FSADJ, CSBP ..... -0.3V to ($V_{AVDD2}$ + 0.3V, MAX 2.1V)
CLKP, CLKN................-0.3V to ($V_{AVDD1PLL}$ + 0.3V, MAX 1.2V)
SDO, INTB Maximum Continuous Current .........................8mA
Continuous Power Dissipation ($T_A$ = +85°C).....................4.0W
Maximum Junction Temperature .....................................+150°C
Storage Temperature Range........................... -60°C to +150°C
Junction Operating Temperature Range ($T_J$)....-40°C to +110°C
Operating Temperature Range ($T_A$)................... -40°C to +85°C
Soldering Temperature (reflow)......................................+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

FCCSP
   Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .......16.2°C/W
   Junction-to-Case Thermal Resistance ($\theta_{JC}$)..............2.5°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$= $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$ = $V_{AVDD2PLL}$ = $V_{VDD2PLL}$ = 1.8V, $P_{CLK}$ = +7dBm, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET}$ = 1.3kΩ between FSADJ and DACREF, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A$ ≥ -40°C and $T_J$ ≤ +110°C (Note 2), unless otherwise noted. Typical values are at $T_J$ = +65.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | |
| Input Data Word Width | N | | | 16 | | Bits |
| DAC Resolution | | | | 14 | | Bits |
| Differential Nonlinearity | DNL | Figure 27 | | ±1.5 | | LSB |
| Integral Nonlinearity | INL | Figure 27 | | ±3 | | LSB |
| Offset Voltage Error | OS | | | 0.003 | | %FS |
| Full-Scale Output Current | $I_{OUTFS}$ | | 10 | | 30 | mA |
| Output Voltage Gain Error | $GE_{FS}$ | $f_{OUT}$ = DC, Figure 27 | | ±3 | | %FS |
| Output Power | $P_{OUT}$ | $f_{OUT}$ = 100MHz | | 0 | | dBm |
| Maximum Output Compliance | | | | $V_{AVDD2}$ + 0.4V | | V |
| Minimum Output Compliance | | | | $V_{AVDD2}$ - 0.4V | | V |
| Output Resistance | $R_{OUT}$ | Differential DAC output resistance | | 50 | | Ω |

## Electrical Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$ = $V_{AVDD2PLL}$ = $V_{VDD2PLL}$ = 1.8V, $P_{CLK}$ = +7dBm, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET}$ = 1.3kΩ between FSADJ and DACREF, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A$ ≥ -40°C and $T_J$ ≤ +110°C (Note 2), unless otherwise noted. Typical values are at $T_J$ = +65.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Maximum DAC Sample Rate | $f_{DAC}$ | Smallest interpolation factor = 5x | | | 3686.4 | | Msps |
| | | Smallest interpolation factor = 6x | | | 4423.68 | | |
| | | Smallest interpolation factor = 6.67x (Note 3) | | | 4915.2 | | |
| | | PLL ON, $f_{CLK}$ = 1474.56MHz, $P_{CLK}$ = -3dBm, smallest interpolation factor or greater = 8x, $f_{SER\_IN}$ = 7372.8Mbps | | | | 5898.24 | |
| Adjusted DAC Update Rate | $AUR_{DAC}$ | (Note 4) | | | | 737.28 | Msps |
| Maximum Input Sample Rate | $f_{S\_IN}$ | For the complex I/Q data set | | | 737.28 | | MHz |
| In-Band SFDR (Notes 5 and 6) | SFDR | CW tone at 1842.5MHz | -15dBFS | | 68 | | dBc |
| | | | -19dBFS | | 82 | | dBFS |
| | | | -33dBFS | | 76 | | |
| HD2, HD3, $f_{DAC}/2$-$f_{OUT}$, Measured in 1st Nyquist Zone | | CW tone at 1842.5MHz | -3dBFS | | -71 | | dBc |
| | | 1.4MHz LTE carrier at 2140MHz; Measured in a 1.4MHz bandwidth around the harmonic/ spur location | -18dBFS | | -65 | | dBc |
| | | | -33dBFS | | -87 | | dBFS |
| Intermodulation Distortion (Note 6) | IMD | Two-tone signal, $f_1$ = 1842MHz and $f_2$ = 1843MHz | Average total power -15dBFS | | -74 | | dBc |
| | | | Average total power -33dBFS | | -80 | | dBFS |
| 3rd Order Intermodulation Distortion (Difference Products Only) | IM3 | Two-Carrier GSM (GMSK) signal, 600kHz spacing, -13dBFS per carrier at DAC input, $f_1$ = 1842.2MHz, $f_2$ = 1842.8MHz, Both carrier and intermodulation products measured with RBW = 30kHz (Note 7) | | -65 | -74 | | dBc |
| Four-Carrier ACLR for WCDMA, Test Model 1 | ACLR | Each a single 5MHz UMTS carrier, $f_1$ = 2131MHz, $f_2$ = 2137MHz, $f_3$ = 2143MHz, $f_4$ = 2149MHz, -15dBFS average total power at DAC input | | | 70 | | dBc |

## Electrical Characteristics (continued)

$(V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDD1PLL} = 1V$, $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{VDD2PLL} = 1.8V$, $P_{CLK} = +7dBm$, $f_{CLK} = 983.04MHz$, $f_{DAC} = 4915.2Msps$, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET} = 1.3k\Omega$ between FSADJ and DACREF, $I_{OUTFS} = 29.5385mA$, output is 50$\Omega$ double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A \geq -40°C$ and $T_J \leq +110°C$ (Note 2), unless otherwise noted. Typical values are at $T_J = +65$.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Power (CW) | | 0dBFS CW tone at DAC input, $f_{OUT} = 2140MHz$ | Excludes loss from cables and matching network at DAC output (Note 8) | | -1.6 | | dBm |
| | | | Excludes loss from cables and matching network at DAC output, includes sin(x)/x roll-off | | -4.5 | | |
| Noise Density | ND | CW tone at 1842.5MHz, -15dBFS, measured at 10MHz offset from carrier in 200kHz bandwidth | | | -160 | | dBm/Hz |
| Output Settling Time for Full-Scale Input Step (Note 9) | | To -0.024% of output full-scale, 5x interpolation, $f_{DAC} = 3686.4Msps$ | | | 20 | | ns |
| Output Bandwidth | | $f_{DAC} = 5898.24Msps$, -1dB bandwidth, Excludes loss from cables and matching network at DAC output (Note 8) | | | 2600 | | MHz |
| **DAC RESPONSE CHARACTERISTIC** | | | | | | | |
| Gain Flatness In-Band (Note 6) | | Over 80MHz bandwidth, $f_{DAC} = 4915.2Msps$, includes 0.2dB sinc(x) roll-off | | | 0.6 | | dB |
| | | Over 300MHz bandwidth, $f_{DAC} = 4915.2Msps$, includes 0.8dB sinc(x) roll-off | | | 2.2 | | |
| **INTERPOLATION FILTERS** | | | | | | | |
| Interpolation Rates (Note 3) | R | | | | 5x, 6x, 6.67x, 8x, 10x, 12x, 13.33x, 16x, 20x, 24x | | |
| Passband Width | | Ripple < 0.01dB | | | 0.407 x $f_{S\_IN}$ | | |
| Stopband Rejection | | 0.593 x $f_{S\_IN}$ | | | 90 | | dB |

## Electrical Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$ = $V_{AVDD2PLL}$ = $V_{VDD2PLL}$ = 1.8V, $P_{CLK}$ = +7dBm, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET}$ = 1.3kΩ between FSADJ and DACREF, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A$ ≥ -40°C and $T_J$ ≤ +110°C (Note 2), unless otherwise noted. Typical values are at $T_J$ = +65.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Latency (Excluding JESD204B Latency) | | 5x interpolation | | 371 | | DAC Update Cycles |
| | | 6x interpolation | | 403 | | |
| | | 6.67x interpolation (Note 3) | | 455 | | |
| | | 8x interpolation | | 438 | | |
| | | 10x interpolation | | 662 | | |
| | | 12x interpolation | | 749 | | |
| | | 13.33x interpolation (Note 3) | | 1260 | | |
| | | 16x interpolation | | 689 | | |
| | | 20x interpolation | | 923 | | |
| | | 24x interpolation | | 1105 | | |
| **NCO** | | | | | | |
| Maximum Frequency | | | | $f_{DAC}$/2 | | Hz |
| Frequency Control Word Resolution | | | | 33 | | Bits |
| SNR | | (Note 10) | | 85.5 | | dB |
| SFDR | | (Note 10) | | 90 | | dBc |
| **REFERENCE** | | | | | | |
| Reference Input Range | | | 1.10 | | 1.30 | V |
| Reference Output Voltage | $V_{REFIO}$ | Internal reference | 1.10 | 1.20 | 1.30 | V |
| Reference Input Resistance | $R_{REFIO}$ | | | 10 | | kΩ |
| Reference Voltage Drift | | | | ±110 | | ppm/°C |
| **CMOS LOGIC INPUTS/OUTPUTS (SCLK, CSB, MUTE, RESETB, SDI, SDO, INTB)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.7 x $V_{DD2}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{DD2}$ | V |
| Input Current | $I_{IN}$ | Excluding RESETB | -1 | ±0.1 | +1 | µA |
| RESETB Input Current | $I_{INRB}$ | | -1 | | 55 | µA |
| Input Capacitance | $C_{IN}$ | | | 3 | | pF |
| Output High Voltage | $V_{OH}$ | $I_{LOAD}$ = 200µA, INTB has a 1kΩ external pullup resistor to $V_{DD2}$ | 0.8 x $V_{DD2}$ | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 200µA, INTB has a 1kΩ external pullup resistor to $V_{DD2}$ | | | 0.2 x $V_{DD2}$ | V |
| Output Leakage Current | | Three-state, SDO pin | -4 | ±2.5 | +4 | µA |

## Electrical Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$= $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$ = $V_{AVDD2PLL}$ = $V_{VDD2PLL}$ = 1.8V, $P_{CLK}$ = +7dBm, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET}$ = 1.3kΩ between FSADJ and DACREF, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A$ ≥ -40°C and $T_J$ ≤ +110°C (Note 2), unless otherwise noted. Typical values are at $T_J$ = +65.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **JESD204B INPUTS (DP3–DP0, DN3–DN0)** | | | | | | |
| Differential Input Return Loss | $R_{LDIFF}$ | | | 8 | | dB |
| Common-Mode Input Return Loss | $R_{LCM}$ | | | 6 | | dB |
| Receiver Differential Impedance | $Z_{RDIFF}$ | At DC | 80 | | 120 | Ω |
| Minimum Differential Input Voltage | $V_{min\_IN}$ | | | 110 | | $mV_{P-P}$ |
| Maximum Differential Input Voltage | $V_{max\_IN}$ | | | 1050 | | $mV_{P-P}$ |
| Discrete Serial Data Rate per Lane | $f_{SER\_IN}$ | Also supports ½ and ¼ fractional data rates | | 9830.4 | | Mbps |
| | | Also supports ½ fractional data rates | | 7372.8 | | |
| | | | | 6144.0 | | |
| **LVDS LOGIC INPUT/OUTPUT (SYNCNP, SYNCNN, SYSREFP, SYSREFN, SYNCIP, SYNCIN, SYNCOP, SYNCON, RCLKP, RCLKN)** | | | | | | |
| Differential Input Logic High | $V_{IH}$ | | 100 | | | mV |
| Differential Input Logic Low | $V_{IL}$ | | | | -100 | mV |
| Input Common-Mode Voltage | $V_{ICM}$ | | 0.675 | | 1.375 | V |
| Differential Input Resistance | $R_{IN}$ | | 87.5 | 100 | 132.5 | Ω |
| Differential Input Capacitance | $C_{INLVDS}$ | | | 1 | | pF |
| Differential Output Logic High | $V_{OH}$ | $R_{LOAD}$ = 100Ω differential | 250 | | 450 | mV |
| Differential Output Logic Low | $V_{OL}$ | $R_{LOAD}$ = 100Ω differential | -450 | | -250 | mV |
| Output Common-Mode Voltage | $V_{OCM}$ | | 1.125 | 1.25 | 1.375 | V |
| Output Maximum Frequency | $f_{RCLK}$ | $R_{LOAD}$ = 100Ω differential, $C_{LOAD}$ = 8pF | | 737.28 | | MHz |
| **CLOCK INPUT (CLKP, CLKN)** | | | | | | |
| Power Level at Differential CLKP/CLKN Clock Input (Note 11) | $P_{CLK}$ | Sine-wave input, PLL OFF, $f_{CLK}$ = 4915.2MHz | | > 0 | | dBm (50Ω) |
| | | Sine-wave input, PLL OFF, $f_{CLK}$ = 5898.24MHz | | > 5 | | |
| | | Sine-wave input, PLL ON | | > –3 | | |
| Common-Mode Voltage | $V_{COM}$ | AC-coupled, internally biased | | 0.5 | | V |
| Differential Input Resistance | $R_{CLK}$ | | | 100 | | Ω |

## Electrical Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$ = $V_{AVDD2PLL}$ = $V_{VDD2PLL}$ = 1.8V, $P_{CLK}$ = +7dBm, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET}$ = 1.3kΩ between FSADJ and DACREF, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A$ ≥ -40°C and $T_J$ ≤ +110°C (Note 2), unless otherwise noted. Typical values are at $T_J$ = +65.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INTERNAL DAC CLOCK PLL** | | | | | | |
| Internal DAC Clock PLL Frequency Range | $f_{PLL}$ | Low-band VCO minimum frequency | | | 4423.68 | MHz |
| | | Low-band VCO maximum frequency | 4915.2 | | | |
| | | High-band VCO minimum frequency | | | 5898.24 | |
| | | High-band VCO maximum frequency | 6144.0 | | | |
| PLL Input Frequencies | $f_{CLK}$ | | | $f_{PLL}$/MLT | | MHz |
| Minimum PLL Input Frequency Multiplier | $MLT_{min}$ | (Note 12) | | 2 | | Hz/Hz |
| Maximum PLL Input Frequency Multiplier | $MLT_{max}$ | (Note 12) | | 60 | | Hz/Hz |
| Phase Noise at 6MHz Offset | | $f_{DAC}$ = 4915.2Msps, measured at PLL output, does not include DAC core phase noise | | -142 | | dBc/Hz |
| Cycle-to-Cycle Jitter | | $f_{DAC}$ = 4915.2Msps, measured at PLL output, does not include DAC core jitter | | 245 | | fs |
| **RESET TIMING** | | | | | | |
| RESET to Ready Delay | $t_{RRDY}$ | | | 350000 | | $f_{CLK}$ Cycles |
| **SERIAL PORT INTERFACE TIMING (Note 7)** | | | | | | |
| SCLK Frequency | $f_{SCLK}$ | 1/$t_{SCLK}$ | | | 25 | MHz |
| SCLK to CSB Setup Time | $t_{CSS}$ | | | 10 | | ns |
| SCLK to CSB Hold Time | $t_{CSH}$ | | | 0 | | ns |
| SDI to SCLK Hold Time | $t_{SDH}$ | Data-write | | 0 | | ns |
| SDI to SCLK Setup Time | $t_{SDS}$ | Data-write | | 5 | | ns |
| Minimum SCLK to SDO Data Delay | $t_{SDD\_MIN}$ | Data-read, 10pF load from SDO to Ground | | 1.5 | | ns |
| | | Data-read, 100pF load from SDO to Ground | | 3.5 | | ns |
| Maximum SCLK to SDO Data Delay | $t_{SDD\_MAX}$ | Data-read, 10pF load from SDO to Ground | | 8 | | ns |
| | | Data-read, 100pF load from SDO to Ground | | 11 | | |
| **POWER SUPPLY** | | | | | | |
| 1.0V Supply Voltage Range | $V_{DD}$, $V_{AVDD}$, $V_{AVDD1PLL}$ | | 0.95 | 1.0 | 1.05 | V |
| | $V_{AVCLK}$ | $f_{DAC}$ sample rate ≤ 4.9152Gsps | 0.95 | 1.0 | 1.05 | |
| | | $f_{DAC}$ sample rate > 4.9152Gsps and ≤ 5.89824Gsps | 1.00 | 1.02 | 1.05 | |

## Electrical Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$ = $V_{AVDD2PLL}$ = $V_{VDD2PLL}$ = 1.8V, $P_{CLK}$ = +7dBm, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4-lanes, 7372.8Mbps per lane, external reference at 1.20V and $R_{SET}$ = 1.3kΩ between FSADJ and DACREF, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A$ ≥ -40°C and $T_J$ ≤ +110°C (Note 2), unless otherwise noted. Typical values are at $T_J$ = +65.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| 1.8V Supply Voltage Range | $V_{DD2}$, $V_{AVCLK2}$, $V_{AVDD2}$, $V_{AVDD2PLL}$, $V_{DD2PLL}$ | | 1.71 | 1.8 | 1.89 | V |
| 1.0V Digital Supply Current | $I_{VDD}$ | $f_{DAC}$ = 4915.2Msps, $f_{OUT}$ = 1842.5MHz, 6.67x interpolation, PLL ON, JESD204B Lanes = 4 | | 530 | 940 | mA |
| 1.8V Digital Supply Current | $I_{VDD2}$ | | | 390 | 445 | mA |
| 1.0V Clock Supply Current | $I_{AVCLK}$ | | | 360 | 510 | mA |
| 1.8V Clock Supply Current | $I_{AVCLK2}$ | | | 57 | 70 | mA |
| 1.0V Analog Supply Current | $I_{AVDD}$ | | | 237 | 345 | mA |
| 1.8V Analog Supply Current | $I_{AVDD2}$ | | | 248 | 292 | mA |
| 1.0V Clock PLL Supply Current | $I_{AVDD1PLL}$ | | | 8 | 15 | mA |
| 1.8V Clock PLL Supply Current | $I_{AVDD2PLL}$ | | | 28 | 34 | mA |
| 1.8V JESD204B PLL Supply Current | $I_{VDD2PLL}$ | | | 30 | 36 | mA |
| Total Power Dissipation | $P_{TOTAL}$ | | | 2490 | 3389 | mW |

**Note 2:** All specifications are guaranteed via test at $T_J$ = +60°C and $T_J$ = +115°C to an accuracy of ±10°C. Specifications at $T_J$ < +60°C are guaranteed by design and characterization. Timing specifications are guaranteed by design and characterization.
**Note 3:** The 6.67x and 13.33x interpolation rates are precisely (20 ÷ 3)x and (40 ÷ 3)x, respectively.
**Note 4:** Adjusted DAC update rate is defined as the maximum DAC update rate divided by the smallest interpolating factor. Note this is a mathematically derived specification.
**Note 5:** SFDR is the minimum ratio in carrier power to the power measured in specified bandwidth (RBW) that is offset from the carrier and swept over a particular band. The carrier power is measured with a 30kHz bandwidth. The spur RBW is 30kHz or 100kHz depending on the frequency distance from the center of the carrier. In the case of multicarrier SFDR, the frequency distance/offset is measured from the center of either edge carrier. The spur RBW is 30kHz for frequency offsets from 0 to 1.8MHz and 100kHz for frequency offsets greater than 1.8MHz.
**Note 6:** In-band is considered to be 1710MHz to 2170MHz, inclusive.
**Note 7:** Specification guaranteed by design and characterization, and functionally tested during production.
**Note 8:** Excludes sin(x)/x roll-off.
**Note 9:** Settling time is dominated by the interpolation filter step response.
**Note 10:** Typical values specified based on worst-case simulation with margin.
**Note 11:** Input power is referenced to a 50Ω load.
**Note 12:** DAC PLL reference input frequency multiplier, MLT, is defined by the ratio of the PLL feedback divide value, M, and the input reference divide value, N.      MLT = M ÷ N
where M can be {16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, or 60} and where N can be {1, 2, 4, or 8}.

## Typical Operating Characteristics

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$ = $V_{AVDD2}$, $V_{AVDD2PLL}$ = $V_{DD2PLL}$ = 1.8V, $P_{CLK}$ = 0dBm, signal power is referred to the DAC core input, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4 lanes, 7.3728Gbps per lane. External reference at 1.2V and $R_{SET}$ = 1.3kΩ, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), and $T_A$ = +25°C, unless otherwise noted.) (Note 6)

**SINGLE-CARRIER GSM (GMSK) NARROW-BAND SPECTRUM**
($f_{OUT}$ = 1.82GHz, $f_{CLK}$ = 1.47456GHz,
INPUT AMPLITUDE = -15dBFS, $T_A$ = +25°C)
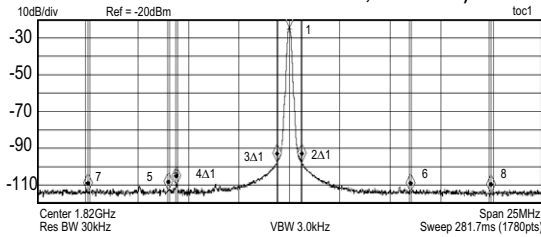
| MKR# | MEASUREMENT TYPE | FREQUENCY | BAND POWER | POWER INTEGRATION BANDWIDTH | UNITS |
|---|---|---|---|---|---|
| 1 | Absolute | 1.82GHz | -24.48 | 30kHz | dBm |
| 2 | Delta to Mkr#1 | +600kHz | -73.36 | 30kHz | dBc |
| 3 | Delta to Mkr#1 | -600kHz | -73.31 | 30kHz | dBc |
| 4 | Delta to Mkr#1 | -5.598MHz | -80.5 | 100kHz | dBc |
| 5 | Absolute | 1.814GHz | -157.84 | 100kHz | dBm/Hz |
| 6 | Absolute | 1.826GHz | -158.57 | 100kHz | dBm/Hz |
| 7 | Absolute | 1.810GHz | -158.56 | 200kHz | dBm/Hz |
| 8 | Absolute | 1.830GHz | -159.48 | 200kHz | dBm/Hz |

**SINGLE-CARRIER GSM (GMSK) NARROW-BAND SPECTRUM**
($f_{OUT}$ = 1.82GHz, $f_{CLK}$ = 1.47456GHz,
INPUT AMPLITUDE = -15dBFS, $T_J$ = 110°C)
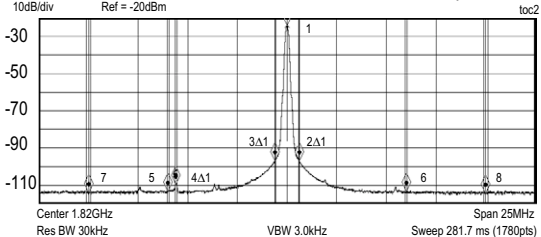
| MKR# | MEASUREMENT TYPE | FREQUENCY | BAND POWER | POWER INTEGRATION BANDWIDTH | UNITS |
|---|---|---|---|---|---|
| 1 | Absolute | 1.82GHz | -24.27 | 30kHz | dBm |
| 2 | Delta to Mkr#1 | +600kHz | -72.89 | 30kHz | dBc |
| 3 | Delta to Mkr#1 | -600kHz | -72.89 | 30kHz | dBc |
| 4 | Delta to Mkr#1 | -5.598MHz | -80.22 | 100kHz | dBc |
| 5 | Absolute | 1.814GHz | -158.29 | 100kHz | dBm/Hz |
| 6 | Absolute | 1.826GHz | -158.44 | 100kHz | dBm/Hz |
| 7 | Absolute | 1.810GHz | -158.94 | 200kHz | dBm/Hz |
| 8 | Absolute | 1.830GHz | -159.48 | 200kHz | dBm/Hz |

**SINGLE-CARRIER GSM (GMSK) NARROW-BAND SPECTRUM**
($f_{OUT}$ = 1.82GHz, $f_{CLK}$ = 1.47456GHz, 8x INTERPOLATION,
INPUT AMPLITUDE = -15dBFS, $T_J$ = +110°C)
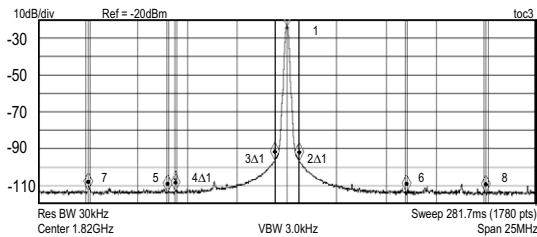
| MKR# | MEASUREMENT TYPE | FREQUENCY | BAND POWER | POWER INTEGRATION BANDWIDTH | UNITS |
|---|---|---|---|---|---|
| 1 | Absolute | 1.82GHz | -23.85 | 30kHz | dBm |
| 2 | Delta to Mkr#1 | +600kHz | -72.85 | 30kHz | dBc |
| 3 | Delta to Mkr#1 | -600kHz | -72.69 | 30kHz | dBc |
| 4 | Delta to Mkr#1 | -5.598MHz | -84.32 | 100kHz | dBc |
| 5 | Absolute | 1.814GHz | -158.81 | 100kHz | dBm/Hz |
| 6 | Absolute | 1.826GHz | -158.56 | 100kHz | dBm/Hz |
| 7 | Absolute | 1.810GHz | -157.62 | 200kHz | dBm/Hz |
| 8 | Absolute | 1.830GHz | -159.48 | 200kHz | dBm/Hz |

## Typical Operating Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2,}$ = $V_{AVDD2}$, $V_{AVDD2PLL}$ = $V_{DD2PLL}$ = 1.8V, $P_{CLK}$ = 0dBm, signal power is referred to the DAC core input, $f_{CLK}$ = 983.04MHz, $f_{DAC}$= 4915.2Msps, 6.67x interpolation, 4 lanes, 7.3728Gbps per lane. External reference at 1.2V and $R_{SET}$ = 1.3kΩ, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), and $T_A$ = +25°C, unless otherwise noted.) (Note 6)

**SIX-CARRIER GSM ($f_{OUT}$ = 1.8425GHz) and
4-CARRIER WCDMA ($f_{OUT}$ = 2.14GHz),
WIDE-BAND SPECTRUM
(INPUT AMPLITUDE = -1dBFS)**
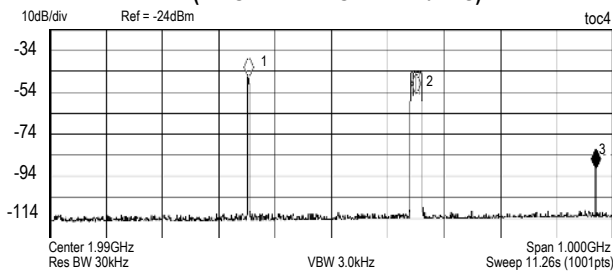
| MKR# | FREQUENCY | POWER |
|------|-----------|-------|
| 1 | 1.841GHz | -47.13dBm |
| 2 | 2.140GHz | -54.87dBm |
| 3 | 2.4576GHz | -90.56dBm |

**SIX-CARRIER GSM ($f_{OUT}$ = 1.8425GHz) and
4-CARRIER WCDMA ($f_{OUT}$ = 2.14GHz),
NARROW-BAND GSM SPECTRUM
(INPUT AMPLITUDE = -1dBFS)**
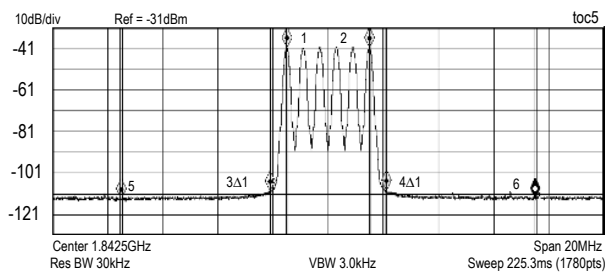
| MKR# | MEASUREMENT TYPE | FREQUENCY | POWER | POWER INTEGRATION BANDWIDTH | UNITS |
|------|------------------|-----------|-------|------------------------------|-------|
| 1 | Absolute | 1.841GHz | -41.17 | 30kHz | dBm |
| 2 | Absolute | 1.844GHz | -40.98 | 30kHz | dBm |
| 3 | Delta to Mkr#1 | -600kHz | -68.83 | 30KHz | dBc |
| 4 | Delta to Mkr#1 | +3.600MHz | -68.38 | 30kHz | dBc |
| 5 | Absolute | 1.835GHz | -158.24 | 100kHz | dBm/Hz |
| 6 | Absolute | 1.850GHz | -158.00 | 100kHz | dBm/Hz |

**SIX-CARRIER GSM ($f_{OUT}$ = 1.8425GHz) and
4-CARRIER WCDMA ($f_{OUT}$ = 2.14GHz),
NARROW-BAND WCDMA SPECTRUM
(INPUT AMPLITUDE = -1dBFS)**
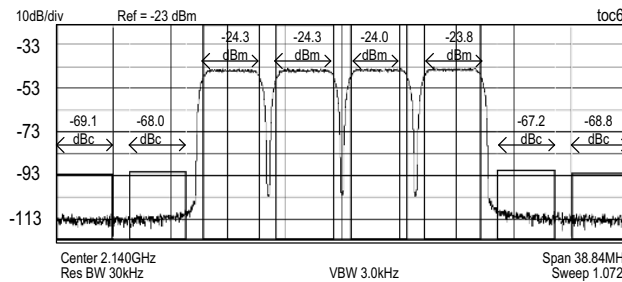
## Typical Operating Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$, = $V_{AVDD2}$, $V_{AVDD2PLL}$ = $V_{DD2PLL}$ = 1.8V, $P_{CLK}$ = 0dBm, signal power is referred to the DAC core input, $f_{CLK}$ = 983.04MHz, $f_{DAC}$= 4915.2Msps, 6.67x interpolation, 4 lanes, 7.3728Gbps per lane. External reference at 1.2V and $R_{SET}$ = 1.3kΩ, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), and $T_A$ = +25°C, unless otherwise noted.) (Note 6)

## Typical Operating Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$, = $V_{AVDD2}$, $V_{AVDD2PLL}$ = $V_{DD2PLL}$ = 1.8V, $P_{CLK}$ = 0dBm, signal power is referred to the DAC core input, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4 lanes, 7.3728Gbps per lane. External reference at 1.2V and $R_{SET}$ = 1.3kΩ, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), and $T_A$ = +25°C, unless otherwise noted.) (Note 6)



IN-BAND SFDR vs. CW FREQUENCY
MEASUREMENT BAND = 1990MHz ±250MHz
OUTPUT FREQUENCY RANGE = 1805MHz to 1880MHz
-1dBFS INPUT AMPLITUDE



IN-BAND SFDR vs. CW FREQUENCY
MEASUREMENT BAND = 1990MHz ±250MHz
OUTPUT FREQUENCY RANGE = 2110MHz to 2170MHz
-1dBFS INPUT AMPLITUDE



IN-BAND SFDR vs. INPUT AMPLITUDE
BAND = 1990MHz ±250MHz



TWO-TONE IM3 vs. CW FREQUENCY
FREQUENCY RANGE = 1805MHz to 1880MHz
$f_{SPACE}$ = 1MHz, -1dBFS INPUT AMPLITUDE

## Typical Operating Characteristics (continued)

($V_{DD}$ = $V_{AVCLK}$ = $V_{AVDD}$ = $V_{AVDD1PLL}$ = 1V, $V_{DD2}$ = $V_{AVCLK2}$, = $V_{AVDD2}$, $V_{AVDD2PLL}$ = $V_{DD2PLL}$ = 1.8V, $P_{CLK}$ = 0dBm, signal power is referred to the DAC core input, $f_{CLK}$ = 983.04MHz, $f_{DAC}$ = 4915.2Msps, 6.67x interpolation, 4 lanes, 7.3728Gbps per lane. External reference at 1.2V and $R_{SET}$ = 1.3kΩ, $I_{OUTFS}$ = 29.5385mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), and $T_A$ = +25°C, unless otherwise noted.) (Note 6)



TWO-TONE IM3 vs. CW FREQUENCY
FREQUENCY RANGE = 2110MHz to 2170MHz
$f_{SPACE}$ = 1MHz, -1dBFS INPUT AMPLITUDE



TWO-TONE IM3 vs. INPUT AMPLITUDE
$f_{SPACE}$ = 1MHz



OUTPUT FREQUENCY RESPONSE
INCLUDING SIN(X)/X ROLL-OFF



9.83Gbps DATA EYE AFTER EQUALIZATION
APPLIED JITTER: 250MUI OF BUJ. 14.53UI (RMS) OF RJ
PATTERN = PRBS7
GCDF: 10G_BASEJITTER_PHY0_VTH1_ECP1

## Pin Configuration

TOP VIEW

| | | | | |
|---|---|---|---|---|
| DIE | GND | SUPPLIES | CRITICAL ANALOG AND RF | RF DATA AND CLOCK |
| ANALOG, DIGITAL IO | NO CONNECT | | | |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | REFIO | CSBP | AVCLK | AVDD2 | AVDD2 | OUTP | OUTN | AVDD2 | AVDD2 | AVCLK | GND | PLL_COMP |
| B | DACREF | FSADJ | GND | AVDD2 | AVDD2 | AVDD2 | AVDD2 | AVDD2 | AVDD2 | GND | VCOBYP | AVCLK2 |
| C | GND | AVDD2 | AVDD2 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| D | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | AVDD2PLL | CLKP |
| E | SCLK | CSB | GND | AVDD | GND | GND | GND | GND | AVDD | GND | AVDD1PLL | CLKN |
| F | SDI | RESETB | GND | GND | VDD | VDD | VDD | VDD | GND | GND | GND | GND |
| G | SDO | INTB | MUTE | VDD2 | VDD | GND | GND | VDD | VDD2 | GND | GND | GND |
| H | SYNCNP | NC | SYNCOP | VDD2 | GND | GND | GND | GND | VDD2 | GND | NC | SYSREFP /SYNCIP |
| J | SYNCNN | NC | SYNCON | VDD2 | GND | GND | GND | GND | VDD2 | GND | NC | SYSREFN /SYNCIN |
| K | GND | GND | GND | GND | GND | RCLKP | RCLKN | GND | GND | GND | TDA | GND |
| L | DP0 | GND | DP1 | GND | SYSREFEN | NC | NC | VDD2PLL | GND | DP2 | GND | DP3 |
| M | DN0 | GND | DN1 | GND | JRES | GND | VSSPLL | CAPT | GND | DN2 | TDC | DN3 |

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| A1 | REFIO | Reference Voltage Input/Output. REFIO outputs an internal 1.2V bandgap reference voltage. REFIO has a 10kΩ series resistance and can be driven using an external 1.2V reference voltage. Connect a 1µF capacitor between REFIO and DACREF. |
| A2 | CSBP | DAC current source bypass. Connect 1.0µF capacitor between CSBP and DACREF. |
| B1 | DACREF | Internal DAC Reference Ground Used for DAC Current Source Bypass Ground. Do not connect to board ground (GND). |
| B2 | FSADJ | Analog Input for DAC Full-Scale Output Current Adjustment. A resistor from FSADJ to DACREF sets the full-scale output current of the DAC. To obtain a 29.5385mA full-scale output current using the internal reference voltage, connect a 1.3kΩ resistor between FSADJ and DACREF ground. |
| A4, A5, A8, A9, B4-B9, C2, C3 | AVDD2 | Analog 1.8V Supply Input |
| A6 | OUTP | Positive Terminal of Differential DAC Output |
| A7 | OUTN | Negative Terminal of Differential DAC Output |
| A11, B3, B10, C1, C4-C12, D1-D10, E3, E5-E8, E10, F3-F4, F9-F12, G6-G7, G10-G12, H5-H8, H10, J5-J8, J10, K1-K5, K8-K10, K12, L2, L4, L9, L11, M2, M4, M6, M9 | GND | Ground |
| A12 | PLL_COMP | Analog I/O for DAC PLL Loop Filter Connection |
| D11 | AVDD2PLL | 1.8V DAC Clock PLL Supply |
| E11 | AVDD1PLL | 1.0V DAC Clock PLL Supply |
| B12 | AVCLK2 | 1.8V Supply Input for Clock |
| D12 | CLKP | Clock Positive Input. Multipurpose pin that generates following internal clocks based on use case: <br> 1) PLL use cases <br>    a) PLL OFF (Bypassed):  Clock for RF DAC core (DACCLK) <br>    b) PLL ON (Enabled):  Reference clock for DAC PLL which in turn generates the DACCLK <br> 2) Device clock (DCLK) for JESD204B interface when frequency is ≤ 1474.56MHz (twice the maximum input sample rate of 737.28MHz) <br> An internal 100Ω termination resistor connects CLKP to CLKN. |
| E12 | CLKN | Clock Negative Input |
| B11 | VCOBYP | Pin for VCO Loop Filter |
| A3, A10 | AVCLK | 1.0V Supply Input for Clock |
| E4, E9 | AVDD | Analog 1.0V Supply Input |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| F5-F8, G5, G8 | VDD | 1.0V Supply Input for Digital Core |
| E1 | SCLK | Digital CMOS Input for Serial Port Interface Clock |
| E2 | CSB | Digital CMOS Input for Serial Port Interface Chip Selection Bar. MAX5871 is selected when CSB = low. |
| F1 | SDI | Digital CMOS Input for Serial Port Interface Data Input in 4-Wire SPI Interface Mode. Serial port data is latched on the rising edge of SCLK. Digital CMOS Input/Output for Serial Port Interface data Input and Output in 3-wire SPI interface mode. Equivalent to SDIO pin in a typical 3-wire SPI interface mode. Serial port data is latched on the rising edge of SCLK. |
| G1 | SDO | Digital CMOS Output for Serial Port Interface Data Output. Serial port data is clocked out from MAX5871 on the falling edge of SCLK. |
| G2 | INTB | Digital CMOS Output for Interrupt, open-drain output. Needs external pullup resistor, 1kΩ recommended. |
| G3 | MUTE | Digital CMOS Input. MUTE = high puts the device into mute mode. MUTE = low puts the device into normal operation mode. |
| F2 | RESETB | Digital CMOS Input with Internal Pulldown to Ground. Device is reset when RESETB = low. Set RESETB low during device startup. RESETB must be set high for normal operation after startup. |
| K11 | TDA | Temperature Sensor Diode Anode. Connect TDC and TDA to ground if not used. |
| M11 | TDC | Temperature Sensor Diode Cathode. Connect TDC and TDA to ground if not used. |
| G4, H4, J4, G9, H9, J9 | VDD2 | 1.8V Supply Input for Digital I/O |
| K6, K7 | RCLKP, RCLKN | LVDS Reference Clock Output for Sample Rate Synchronization to Internal DACCLK at RF DAC Core. Equals DACCLK frequency at RF DAC core divided by DAC interpolation ratio (R). If not used, terminate with a 100Ω resistor differentially. |
| L6, L7, J2, H2, J11, H11 | NC | No Connect |
| H1, J1 | SYNCNP, SYNCNN | LVDS Output. Active low JESD204B error reporting signal (SYNC~) from Rx to Tx. |
| H12, J12 | SYSREFP, SYSREFN | LVDS clock input used for JESD204B Subclass-1 operation (deterministic latency). Signal is synchronous to the device clock (DCLK = CLKP/CLKN) for all transmit and receive devices. Alternate function for multi-purpose pin SYNCIP, SYNCIN. |
| H12, J12 | SYNCIP, SYNCIN | LVDS Input. Required for Multi-DAC Synchronization (Subclass-1). Alternate function for multipurpose pin SYSREFP, SYSREFN. |
| H3, J3 | SYNCOP, SYNCON | LVDS Output used for Multi-DAC Synchronization under JESD204B Subclass-1. Multiple DAC synchronization is not supported in Subclass-0. If not used, terminate with 100Ω resistor differentially. |
| L8 | VDD2PLL | JESD204B PLL 1.8V Power Supply |
| M7 | VSSPLL | Clock Multiplier Unit (CMU) PLL Ground |
| L1, L3, L10, L12 | DP0–DP3 | Analog Input. JESD204B Serial Data Positive Input, Lanes 0-3 |
| M1, M3, M10, M12 | DN0–DN3 | Analog Input. JESD204B Serial Data Negative Input, Lanes 0-3 |
| M5 | JRES | Analog Input. JESD204B Current Biasing. |
| M8 | CAPT | Analog Input. JESD204B PLL Loop Filter Input. |
| L5 | SYSREFEN | Hardwired SYSREF Enable CMOS Input. Use instead of SPI for improved timing control. |

## Functional Diagram
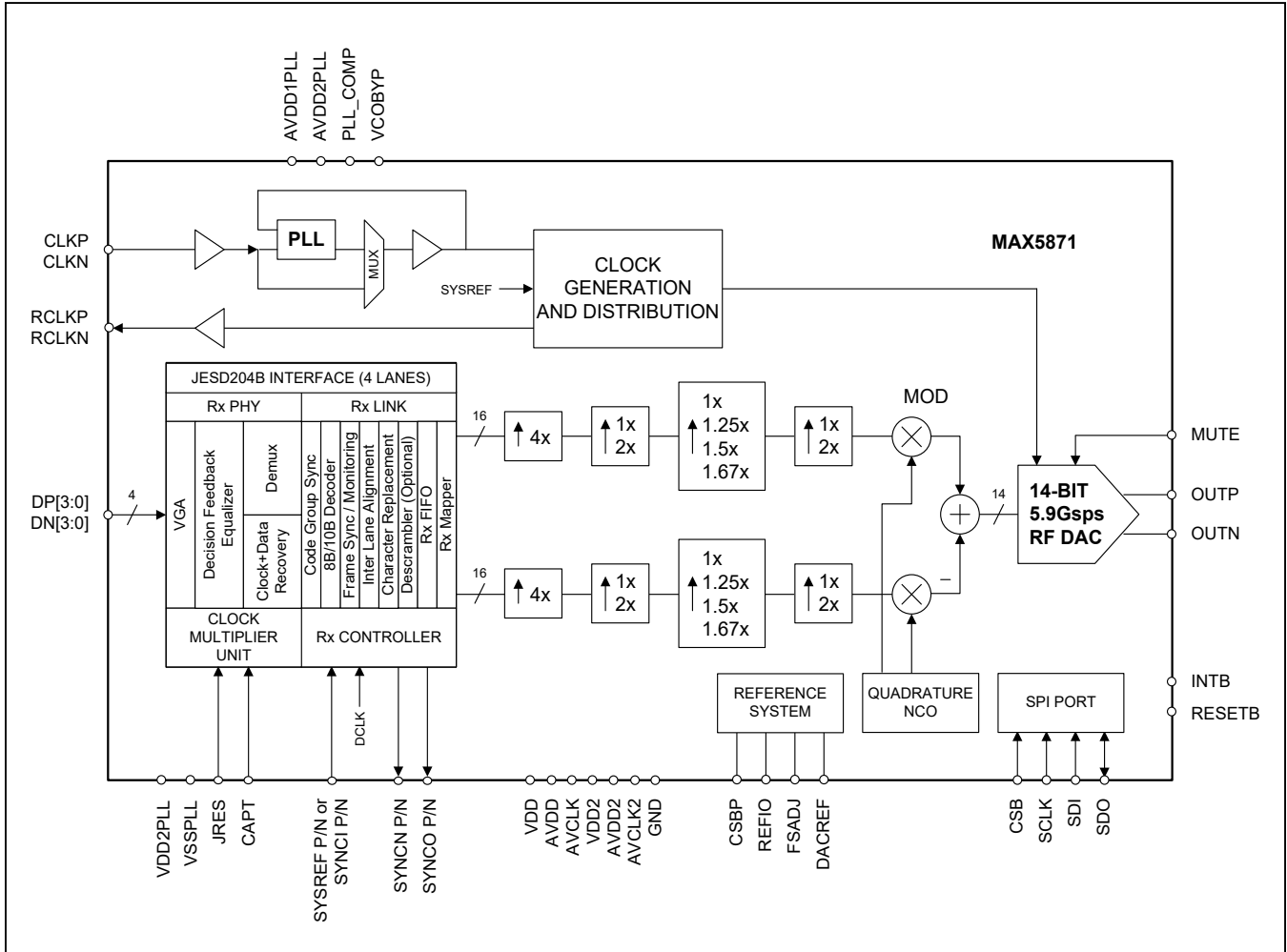
# Detailed Description

The MAX5871 is a high-performance interpolating and modulating 16-bit, 5.9Gsps RF DAC designed for wireless communications applications such as cellular base stations, multistandard and multiband transmitters, and point-to-point microwave links. The device can synthesize up to 600MHz of instantaneous bandwidth at frequencies up to the Nyquist bandwidth ($f_{DAC}/2$) of the DAC. The major functional blocks of the device include a four-lane JESD204B interface which accepts 16-bit input data (I and Q), a cascade of interpolation filters, a digital quadrature modulator and NCO, clock multiplying PLL+VCO and a 14-bit, 5.9Gsps RF DAC core. The supporting functional blocks include the clock distribution system, reference system, and SPI interface. See the detailed *Functional Diagram*.

The 16-bit input data enhances the accuracy of the interpolation and modulation functions and ensures true 14-bit data is presented to the RF DAC core. The 16-bit input baseband data (I and Q) is supplied to the device using up to four lanes of JESD204B (DP[3:0]/DN[3:0]). The JESD204B interface can be configured for Subclass-1 for applications requiring deterministic delay and Subclass-0 for normal operation. The interface can be configured for 1, 2, or 4 lanes and supports serial data rates up to 10Gbps providing flexibility to optimize the I/O count, speed, and power to support the required frequency plan.

The four-lane JESD204B interface has the following major components:

- A high-speed input receiver (Rx) consisting of a physical (PHY) layer for each of the 4 lanes and a common clock multiplier unit (CMU). The PHY layer contains a variable gain amplifier (VGA) which receives the incoming signal and decision feedback equalizer (DFE) to suppress inter-symbol interference. The PHY layer also includes a clock and data recovery (CDR) unit to latch the incoming single-bit data and a Demux to deserialize the data and convert it to a 20-bit parallel data bus.

- A receiver link layer (Rx Link) which takes the 20 bits from the PHY and restores the 16-bit DAC data for I and Q channel each. The Rx link consists of four Rx lanes, four Rx FIFOs, a Rx mapper and a Rx controller. The four Rx lanes perform code group synchronization, 8B/10B decoding, frame synchronization and monitoring, interlane alignment and monitoring, character replacement, and optional descrambling. The four lanes are fed into Rx FIFOs where data is aligned by the Rx controller. Using the Rx mapper, data from each physical channel is mapped to a logical channel.

The DSP path consists of a chain of configurable interpolation filters for I and Q channel each. Interpolation rates of 5x, 6x, 6.67x, 8x, 10x, 12x, 13.33x, 16x, 20x, or 24x can be selected by bypassing one or more of the interpolation filters. Interpolation reduces the required input data rate to the device relaxing the requirements on the FPGA or ASIC. In addition, interpolation increases the separation between the desired signal and its aliased image easing filter design requirements.

After passing through the interpolation stages, the complex signal is modulated using the LO signal generated by the NCO and the digital quadrature modulator. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis with 32 bits of frequency-setting resolution. Placing the modulator at the output of the interpolator chain allows for fully agile placement of the output carrier frequency within the Nyquist bandwidth of the DAC. The quadrature modulator produces a real signal at its output, which is in turn fed into the 14-bit DAC core where it is converted to an analog RF signal. The analog output produces a full-scale current between 10mA and 30mA driving loads up to 50Ω differential.

The clock distribution system provides a low-noise differential input buffer for the external master DAC clock (CLKP/CLKN) and delivers all necessary clocks to all the DAC blocks. The master DAC clock input accepts a differential sine-wave or square-wave signal. An integrated clock multiplying PLL and VCO can be used to generate a high-frequency clock in the range from 4.4GHz to 4.9GHz or at 5.9GHz. The PLL can be bypassed allowing use of an external clock source. The device outputs a divided reference clock (RCLKP/RCLKN) that is equal to the DAC clock frequency divided by the DAC interpolation ratio to ensure synchronization with the system clock. The SYSREF clock input is used for Subclass-1 operation (deterministic latency) and is synchronous to the device clock (DCLK = CLKP/CLKN) for all transmit and receive devices. The SYNCN output is used for error reporting from the receiving device (MAX5871) to the transmitting device (FPGA or ASIC). The SYNCO output is used to synchronize multiple MAX5871 devices.

The reference system delivers the reference current to the DAC current source array and all bias currents necessary for the circuit operation. The reference system also includes a band-gap reference, which can be used as a reference for the DAC full-scale current. The SPI port is a bidirectional interface and is used for configuring the device and reading/writing status and control registers. The device operates from 1.8V and 1.0V power-supply voltages and consumes 2.5W at 4.9Gsps.

## JESD204B Interface

The MAX5871 JESD204B interface consists of four lanes of physical layer (PHY) with a common clock multiplier unit (CMU). Each lane takes a serial 1-bit stream and converts it to a parallel 20 bit bus. The link layer (LINK) takes the 20 bits from the PHY and restores the original 16-bit DAC data for the I and Q channels. See Figure 1.

The MAX5871 JESD204B receiver specifications are compliant with the LV-OIF-6G-SR and LV-OIF-11G-SR specifications from the JESD204B standard.
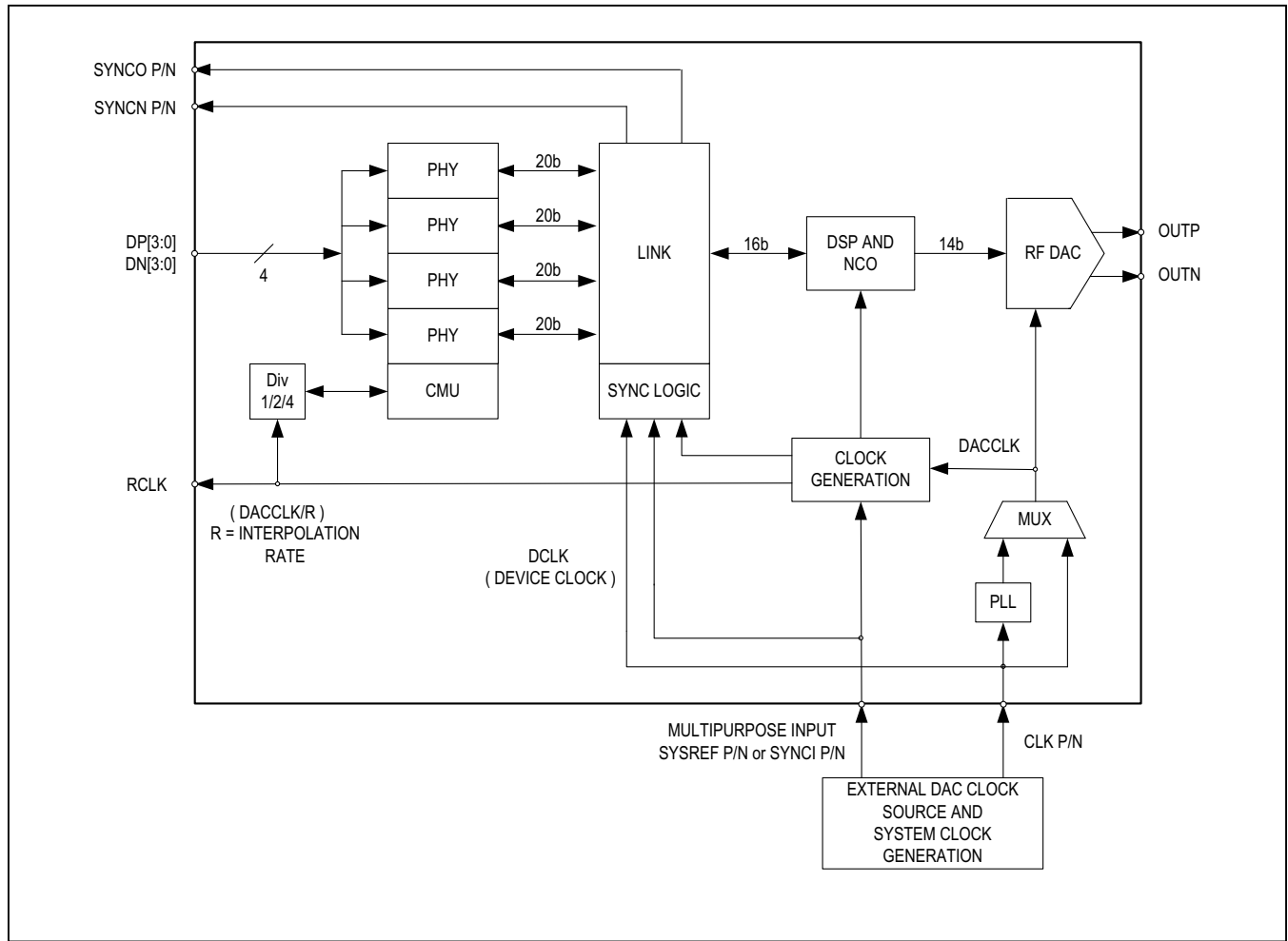


Figure 1. Simplified Diagram of JESD204B Internal to MAX5871

## Table 1. JESD204B Receiver Power Dissipation

| BLOCK | NO. of JESD LANES (7.3728Gbps/LANE) | TOTAL ESTIMATED POWER (PHY+CMU+LINK) (mW) |
|---|---|---|
| LINK RX-1 | 1 | 200 |
| LINK RX-2 | 2 | 322 |
| LINK RX-4 | 4 | 563 |

### JESD204B Data Interface Features

A summary of the MAX5871 SerDes PHY (Rx) and link features are provided below.

### Rx PHY Key Features

- Programmable Gain

- Decision Feedback Equalizer. Fully configurable as to which coefficients to enable/disable.

- Auto adaptation available for all DFE coefficients, gain, boost.

### Link Key Features:

- 8b10b decoding

- Code Group Synchronization

- Inter Lane Alignment (ILA)

- 1 + x14 + x15 Polynomial Scrambling

- Character Replacement

- Dynamic on-the-fly frame/lane realignment if the elastic buffer allows it

- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device

- Subclass-0 and Subclass-1 support

- Number of lanes (L): 1, 2, 4

- Number of data converters or I and Q paths (M): 2

- Number of octets per frame (F): 1, 2, 4

- Number of samples per frame (S): 1, 2

### Other Features:

- Scrambling disable mode

- Elastic buffer depth of 320 serial bit periods

- Detection of following 8b10b control characters: K28.0, K28.3, K28.4, K28.5, K28.7

- Detection of following errors/conditions
  - 8b10b Running Disparity Error
  - 8b10b Not-in-table Error
  - Unexpected Control Character Detection
  - Code Group Synchronization Error
  - Frame Realignment Detection
  - Lane Realignment Detection
  - ILA Failure Detection
  - Link Configuration Error
  - ILA Sequence Error

- Various errors can be enabled to trigger resynchronization through SYNC~ interface

- Continuous /K/ and continuous ILA sequence detection

- Error reporting via the SYNC~ interface

- Data repetition from previous frame/sample on not-in-table error detection

- Sample PRBS data for debug

- SerDes PRBS data for debug

### High-Speed Input Receiver (Rx)

As shown in Figure 2, the high-speed input receiver consists of a variable gain amplifier (VGA), decision feedback equalizer (DFE), clock and data recovery (CDR) unit and deserializer (DEMUX). The VGA and DFE provide **autonomous adaptive** effective equalization to optimize the input receiver filter coefficients to best recover the data dependent jitter introduced by the incoming channel. The initial receiver gain and equalization settings are shadowed by internal registers and may be overridden and driven by the user.
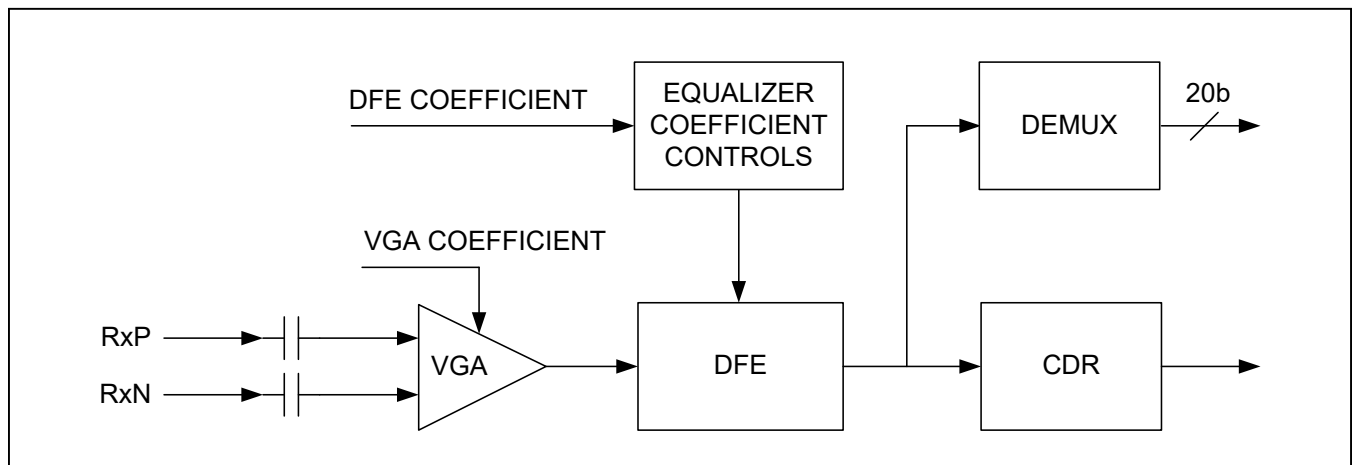


Figure 2. JESD204B Rx Physical Layer Simplified Block Diagram

The VGA is a high-speed input receiver that has high gain, which allows for excellent input sensitivity while still preserving the linearity required for optimal performance of the DFE. The receiver expects the incoming high-speed signal to be differentially driven and AC-coupled to the transmitter. The receiver common-mode voltage is set by a self-biasing network, eliminating the need for any external board circuitry. The receiver provides on-chip termination between the true and complement input signals, RxP and RxN (typically 100Ω differential). The VGA gain settings are set based on the amplitude of the incoming high-speed signal and the optimal setting to the DFE circuitry and the VGA gain range is (±20dB). In addition to the gain function, there is also a boost function in the VGA to compensate for the high-speed frequency loss in the channel as shown in Figure 3.

The PHY receiver provides a sophisticated level of equalization to suppress inter-symbol interference (ISI) caused by a dispersive channel known as decision feedback equalization. The DFE makes use of previously determined data to estimate the current bit. Any trailing ISI caused by a previous bit is reconstructed and then subtracted. This technique allows for the recovery of very lossy backplane and connector channels. The PHY equalizer is designed to meet or exceed the JESD204B standard.

The clock and data recovery unit is responsible for the centering of the incoming data eye for optimal sampling and error-free operation. The PHY clock and data recovery unit has multiple loop bandwidth settings to aid in optimal performance for jitter tolerance.

The recovered clock generated from CDR is used to latch in the single-bit data, then the DEMUX block deserializes the single bit to 20-bit parallel data bus to be used by Rx Link.
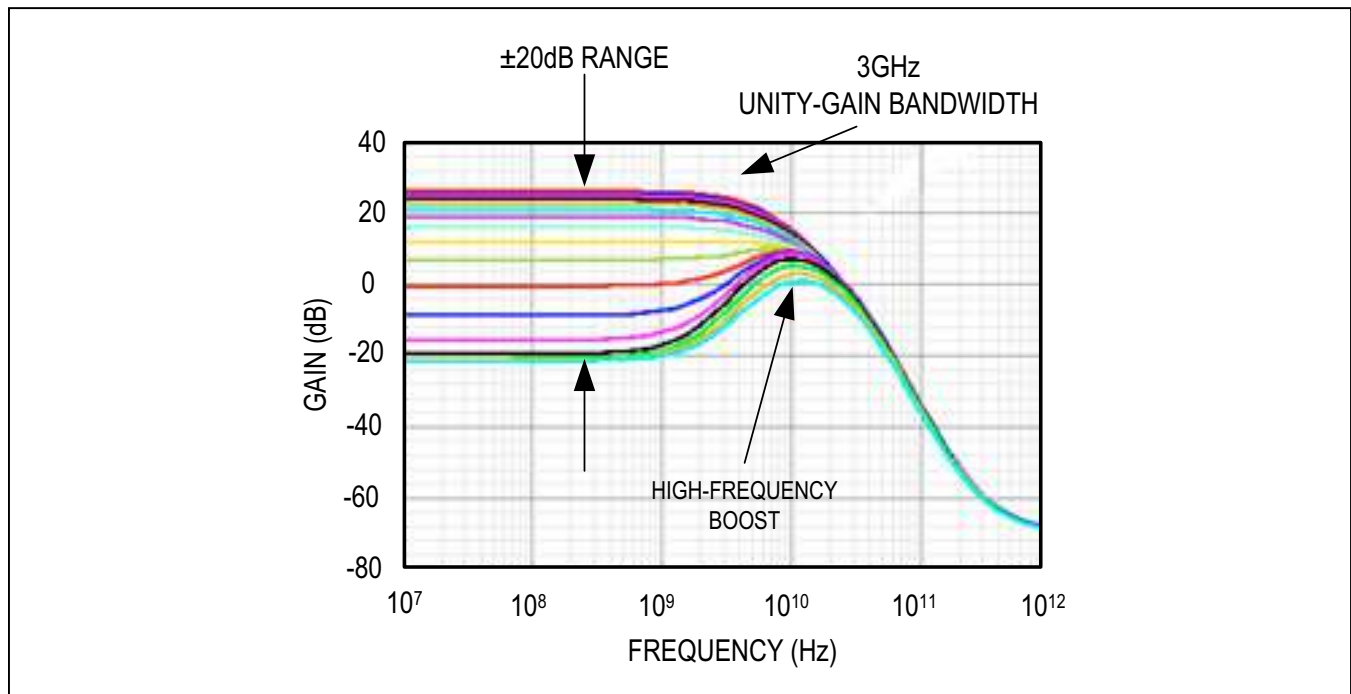


Figure 3. VGA Gain Range

## JESD204B Receiver Equalization

This section demonstrates the JESD204B receiver equal-
ization capability over a long length of cable (30in); how-
ever, use of cables of this length is not recommended.
The MAX5871 is designed for and meets the JESD204B
20cm trace length requirement with a given set of internal
configurations.

Device Configuration

Serial Data Rate: 9.8304Gbps
Xilinx® VC707 FPGA Data Source
Channel: 30in Nelco 4000-13SI plus cables and FMC
connector
30in Nelco Traces = -14.7dB loss at 4.914GHz
Cables and connector ~ 3dB loss at 4.914GHz
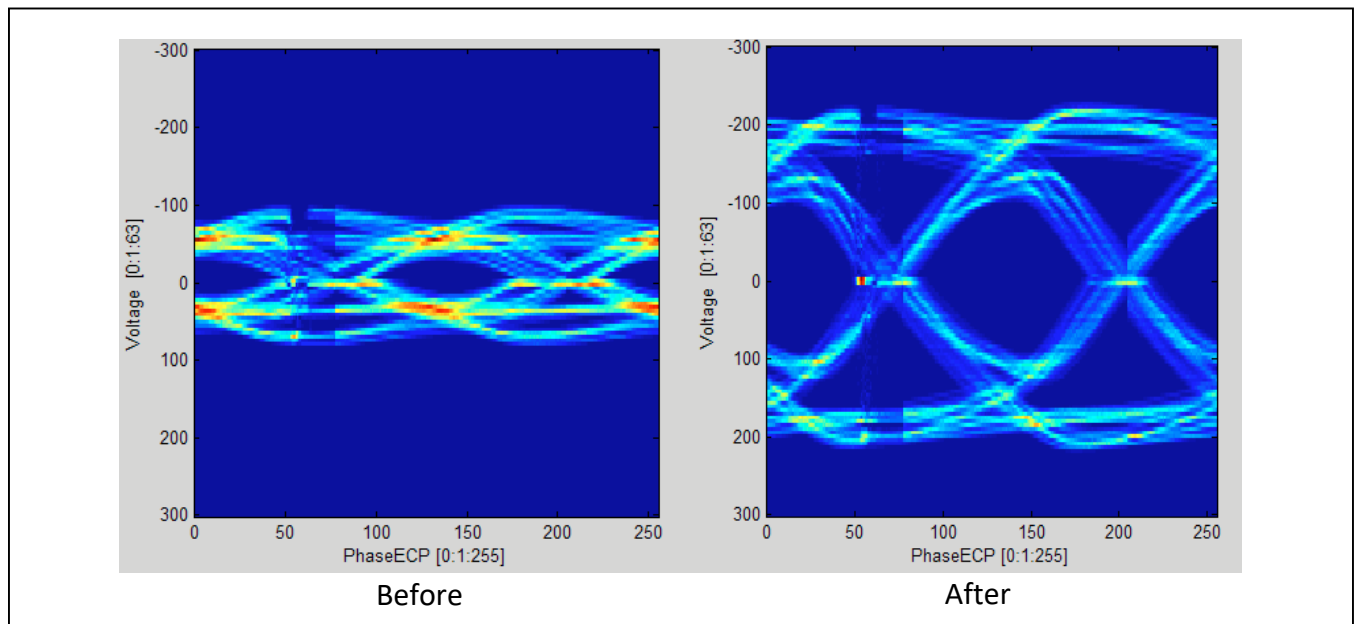
Before

After

Figure 4. Receiver Equalization Eye Diagram Before and After Lane Training (9.8304Gbps, 30in Nelco Trace)
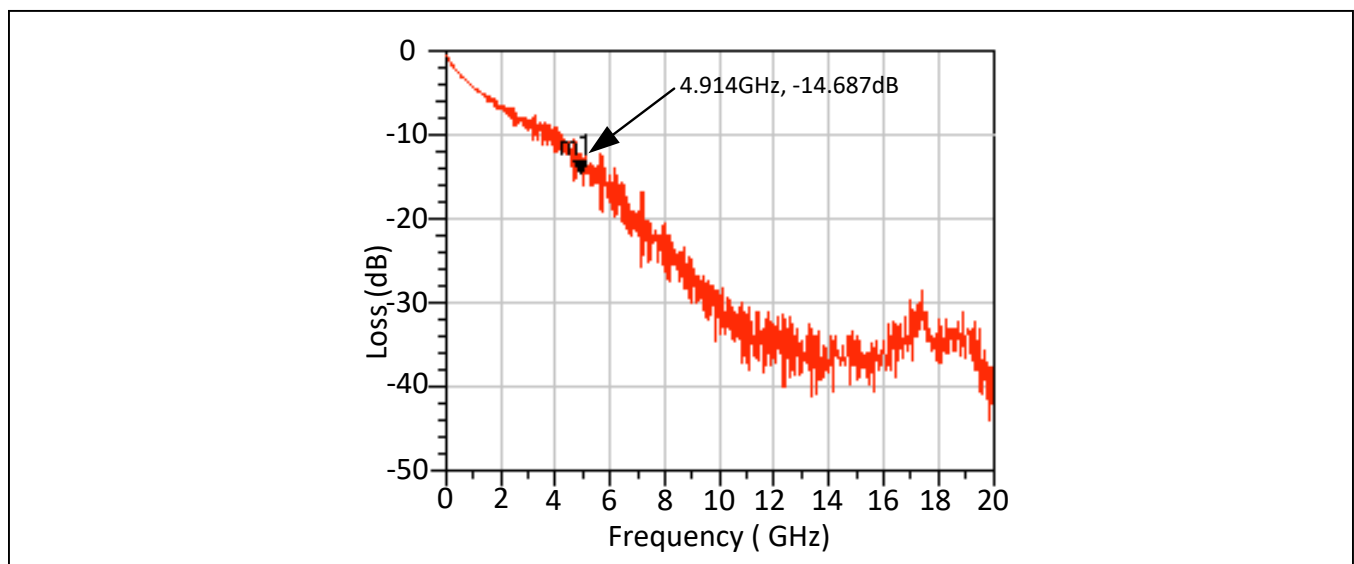
Figure 5. Channel Loss Curve (30in)

## Synchronization with SYSREF

A JESD204B Subclass-1 device achieves deterministic delay through a clock-and-sync interface as specified in the standard. The SYSREF input is synchronous to the device clock (DCLK=CLKP/N) input for all the receive and transmit devices. SYSREF is sampled on the rising edge and then used to reset the phase of the divided clock(s). One of the divided clocks is configured as the sample clock. An extended version of the sampled SYSREF is used to reset the octet and frame counters running on the sample clock. Deterministic delay is achieved by synchronizing the phase of all sample clocks and octet/frame counters and configuring the same point in time for the FIFO read start across all the devices. The transmit logic device (FPGA or ASIC) generates data at the same time for all the receive devices (multiple DACs). After this resynchronization, the data read out of the FIFOs in all the receive devices is triggered at the same time achieving deterministic delay.

The timing diagram (Figure 6) shows the SYSREF signal usage for a JESD204B Subclass-1 device. DCLK is the device clock, SAMCLK is the sample clock, OCNT is the octet counter holding the octet count in a frame and FCNT is the frame counter holding the frame count in a multiframe (as specified in the JESD204B standard). The SYSREF signal essentially sets the phase of the frame and multiframe clocks implemented as octet and frame counters.

The maximum device clock (DCLK) frequency is twice the specified maximum input sample rate of 737.28MHz. This means the SYSREF timing window, for the transmit logic device and the receive device together, is 500ps. This results in tight setup and holds constraints on the DCLK/SYSREF timing, even though it is a source synchronous interface. To enable sufficient margins for sampling of SYSREF on DCLK, a programmable delay on SYSREF needs to be implemented with steps of 10's of ps so that the timing can be adjusted at each of the receive device inputs.
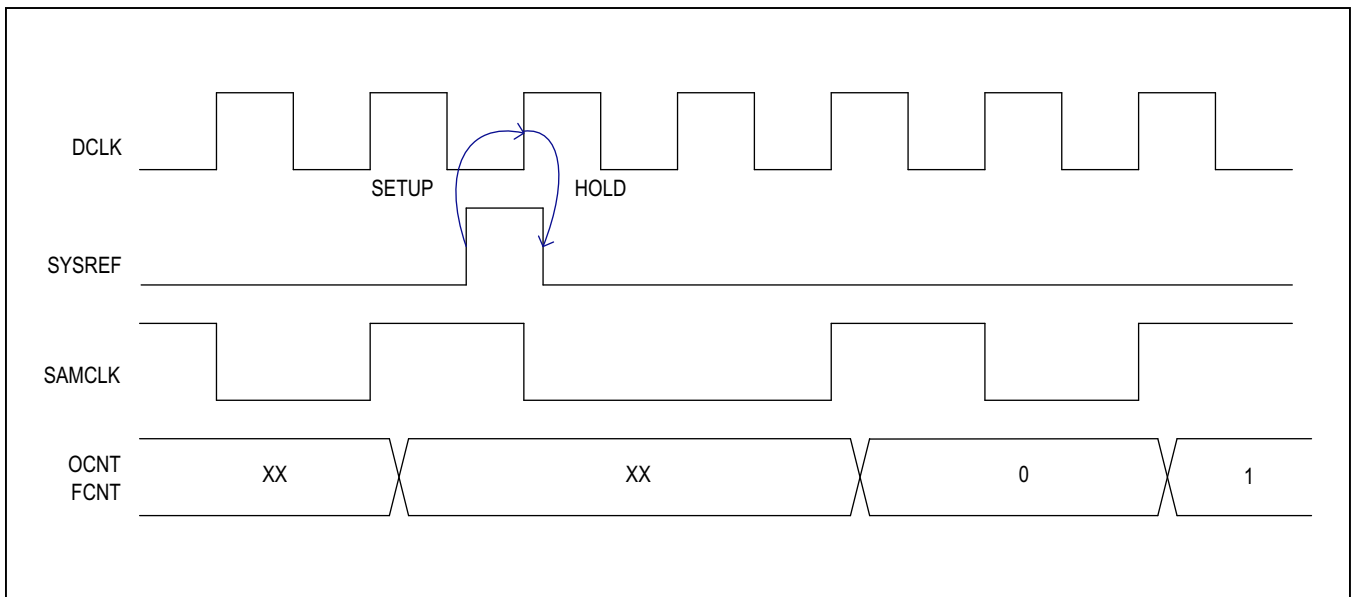


Figure 6. SYSREF Usage for Sample Clock (DLCK/2) Generation and Synchronization

An additional mode to replace the device clock source is to generate the sample clock by dividing down the DACCLK in the DSP section. In this mode, there will not be a device clock and the SYSREF input will be an asynchronous signal. For multi-DAC synchronization, the JESD204B link will not have a deterministic delay but the overall skew within one DAC clock cycle. The SYSREF signal will be passed through to the DSP block where it is used to reset the clock-divider circuit and generate a synchronous signal to RCLK (reference clock at sample rate). This synchronization will occur with one DAC clock uncertainty. The synchronous signal RSYNC is used by the Rx Link block to reset its frame counters. See Figure 7 for the timing diagram for this mode.
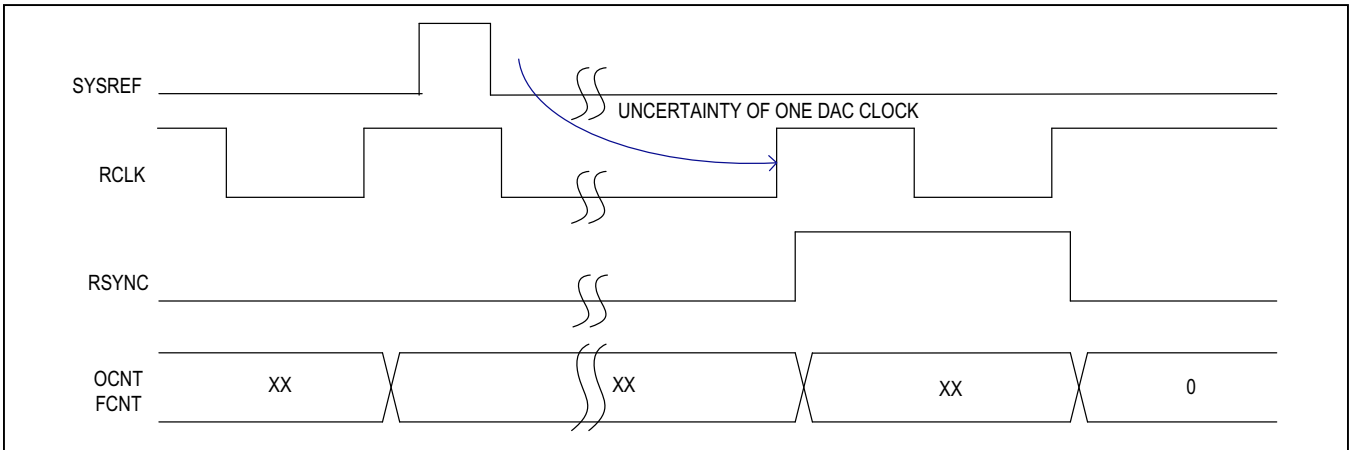


*Figure 7. SYSREF Usage for Sample Clock (From DACCLK) Generation and Synchronization*
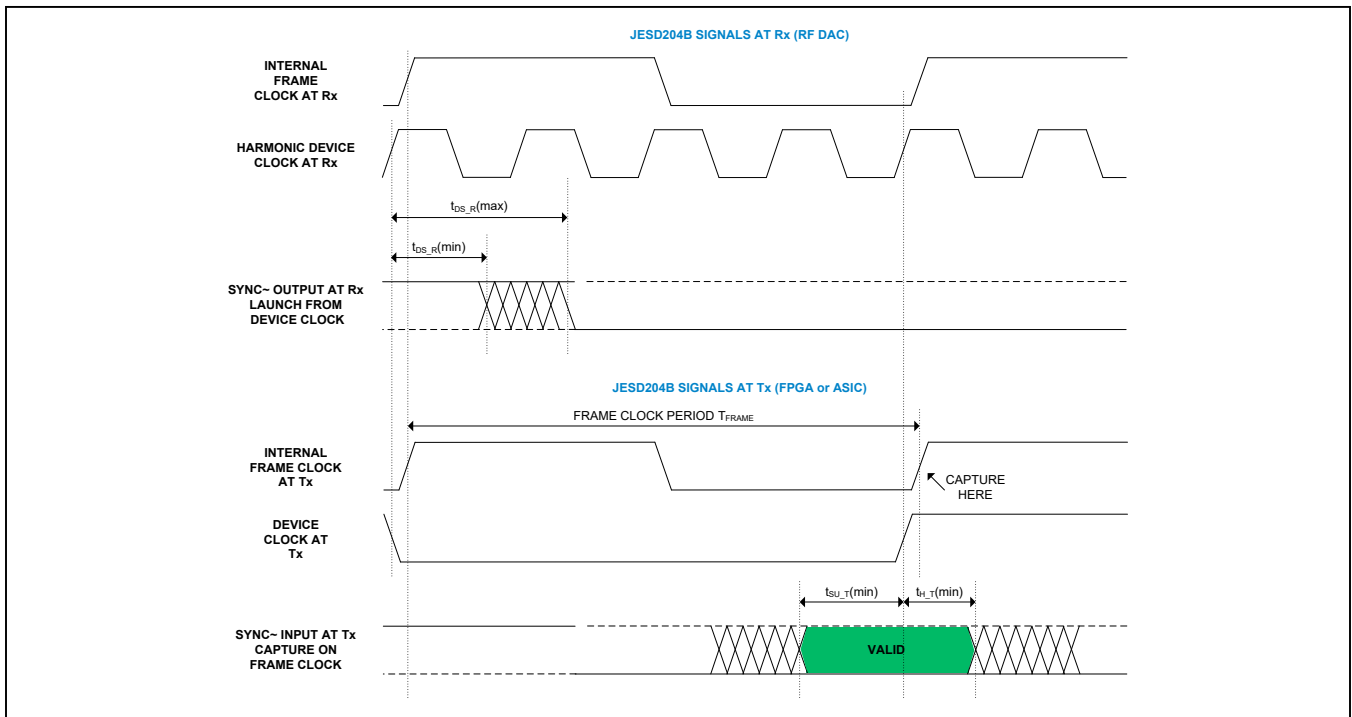


*Figure 8. Interface Timing for Subclass-0 (See JEDEC Standard No. 204B.01, Figure 11)*

### Link Layer (LINK)

The Rx link layer for the MAX5871 consists of 4 lanes interfacing to the 4 PHYs. The data from the 4 lanes is passed through FIFOs controlled by a Rx controller used to align the data on all the configured number of lanes in both JESD204B Subclass-0 and Subclass-1 modes. The Rx controller also handles the Subclass-1 deterministic latency using the input device clock (DCLK=CLKP/N) and SYSREF signals. The Rx controller also generates the SYNCN signal for error reporting as specified by the JESD204B standard. The data from the FIFOs, used to absorb the lane skews, is then mapped into I and Q sample data for the DSP to process.

Each of the 4 lanes in the Rx link operates independently and includes code group synchronization operating on the 20-bit input from the PHY, 8b10b decoding, frame synchronization and monitoring, lane alignment and monitoring, character replacement and optional descrambling. All these functions are specified in the JESD204B standard. In addition to extracting the octets, which are later combined into I and Q samples, the Rx Lane also monitors and acts on various error conditions. Most error conditions can be enabled to trigger a resynchronization request from the transmit logic sevice through the SYNCN signal. See *Link Layer Configuration Registers* for more detail.
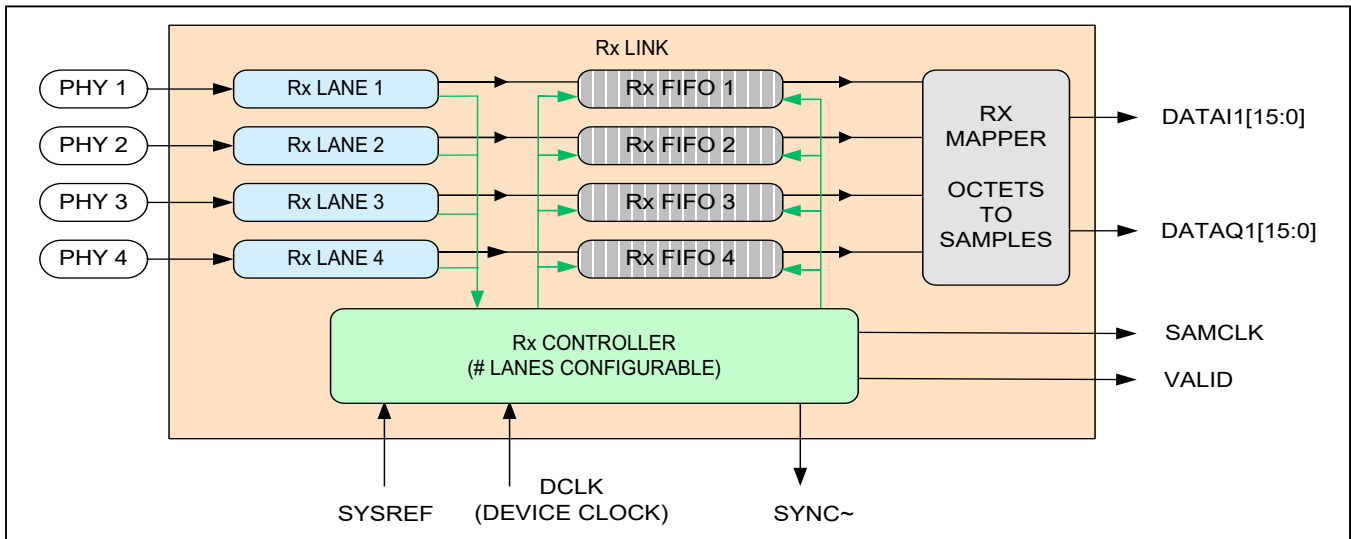


*Figure 9. JESD204B Receive Link Layer Block Diagram*
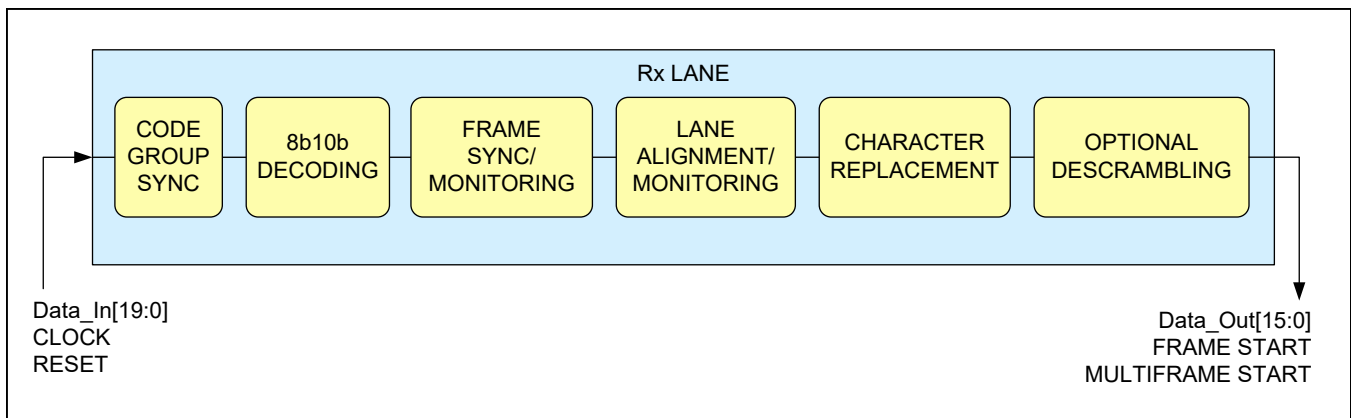


*Figure 10. JESD204B Receive Lane Block Diagram*

*On the input side of the Rx lane are 20-bit data and the clock from the PHY along with a synchronous reset. On the output side are 16-bit data (two octets) and frame/multiframe start signals marking the two bytes of data.*

### Lane Skew Requirement

The skew between the various lanes is absorbed within the FIFOs and through the initial lane alignment process. The FIFO depth determines the amount of lane skew that can be absorbed for a particular Rx Link configuration. A FIFO depth of 32 bytes would account for up to 320 SerDes bit periods of skew between the various lanes. In actuality, the maximum supported skew is smaller than this due to multiple bytes written to and read from the FIFO in a single write/read clock cycle in various modes. The maximum supported skew is also reduced due to the write clock to read clock synchronization uncertainty. A minimum and maximum FIFO depth can be set and the overflow/underflow configured to trigger resynchroniza-tion from the transmit logic device. The configured FIFO range determines the actual lane skew supported by the MAX5871.

### Mapping of Physical to Logical Channels

Each physical channel can be mapped to any logical channel before the octet to sample conversion. The octet to sample conversion for various modes as determined by the number of lanes (L), number of octets per frame (F) per JESD204B, and the number of samples per frame (S) is according to the formats shown below.
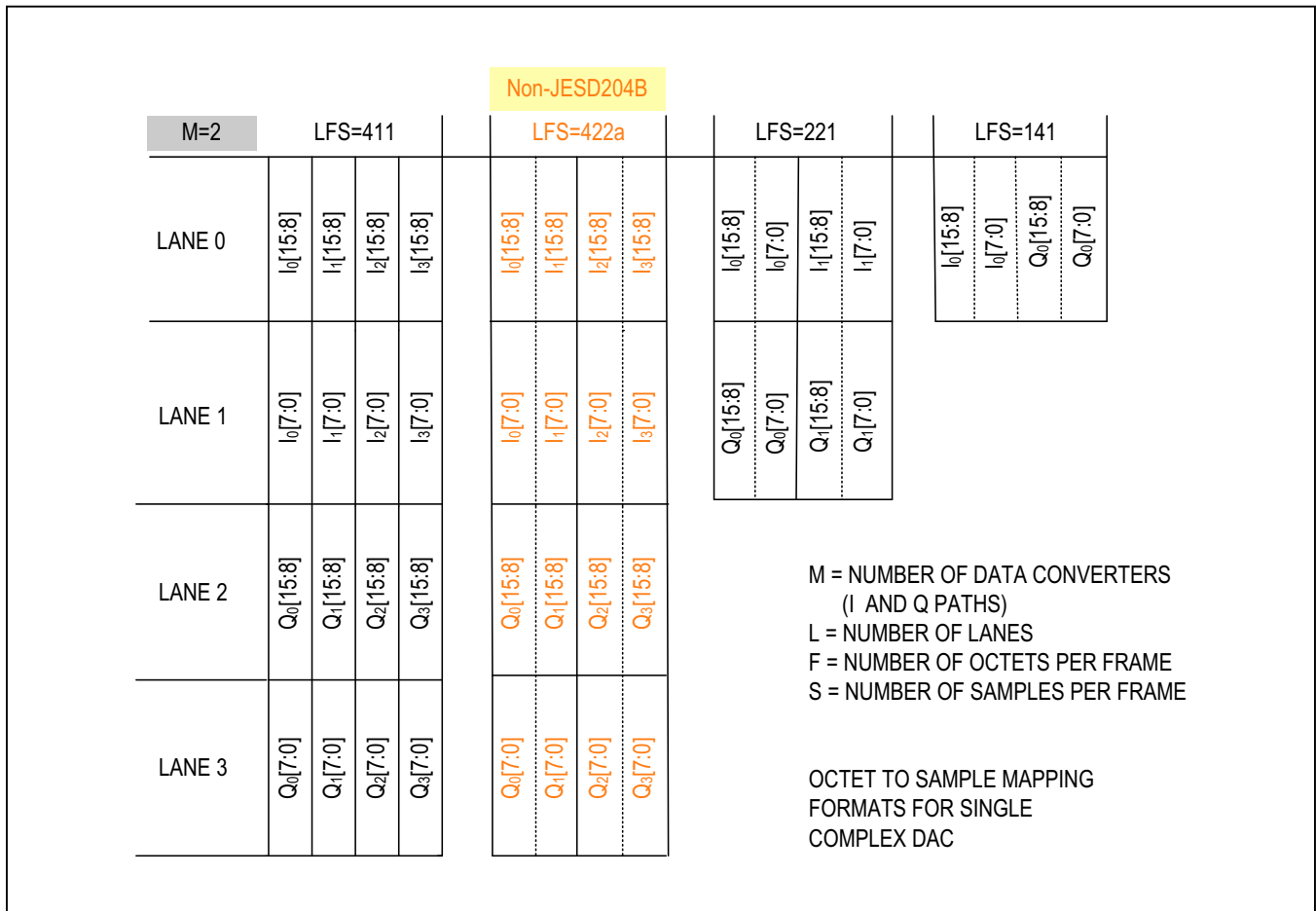


Figure 11. Octet To Sample Conversion vs. Modes and Lanes

## Serial Control Interface

The serial control interface is composed of the CSB, SCLK, SDI, and SDO pins. It supports typical 4-wire SPI interface (CSB, SCLK, SDI, and SDO) where pin SDI is the digital data input, and a typical 3-wire interface (CSB, SCLK, and SDI) where pin SDI is both digital data input and output. In the 3-wire interface mode, the SDI pin is identical to the SDIO pin, as identified in a typical 3-wire interface in some literature.

The MAX5871 is always a slave device with the master controlling CSB, SCLK, and SDI. In 4-wire SPI interface mode, CSB, SCLK, and SDI are CMOS-level digital input pins, with a 1.8V input range. SDO is high impedance except when the MAX5871 is transmitting serial data. SDO is a CMOS output signal with a 1.8V output range. CSB is the chip-select pin. While in the low state, a MAX5871 device is open to communication through the SCLK, SDI, and SDO pins. Each communication cycle is composed of a read/write bit, an address word, and a write data word or a read data word. The serial interface clock, SCLK, latches data into the MAX5871 on the rising edge and clocks data out of the MAX5871 on the falling edge. A one for the R/W bit signifies a read operation and a zero indicates a write operation. A write operation is defined as the controller writing a data word to the MAX5871. A read operation is when the MAX5871 serial interface transmits a data word back to the controller.

Both the R/W bit and the address word are sent to the MAX5871 through the SDI pin. The address word is 15 bits wide and is transmitted MSB to LSB in the default MSB-first mode. In the LSB-first mode, the address word is transmitted LSB to MSB followed by the R/W bit.

For a write operation, a data word is immediately written to the MAX5871 after the last control word (R/W or address word) bit. The data word is 8 bits wide and is transmitted from the external controller, MSB to LSB in the default MSB-first mode. For a read operation, the data word is transmitted from the MAX5871 on the SDO signal line. The transmission starts on the falling edge of SCLK immediately after the last control word bit is latched into the MAX5871. Again the data word from the MAX5871 is transmitted MSB to LSB in the default MSB-first mode. The SDO driver enters a high-impedance state on the next falling SCLK edge immediately after the control word LSB is transmitted. CSB must toggle from low to high and then back down to low before another communication cycle can resume if burst mode is turned off. The SDO and SDI signals can be tied together to achieve an SDIO communication pin.

In the non-default LSB-first mode, the data word is transmitted LSB to MSB both for writes and reads. When burst mode is enabled, a continued assertion of CSB after the data word would auto decrement/increment the address word depending on the configuration for a successive read/write. Every 8 cycles of SCLK would access a successive address for either write or a read based on the R/W bit in the initial control word.
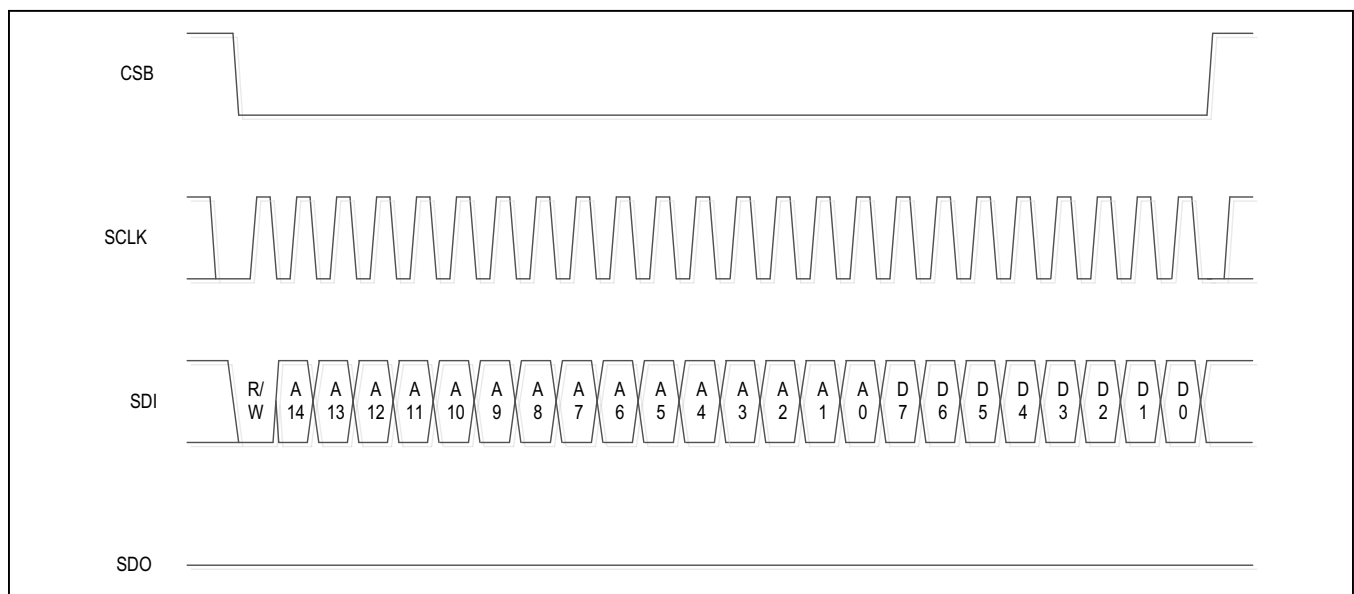


*Figure 12. Single SPI Write Transaction with MSB-First*
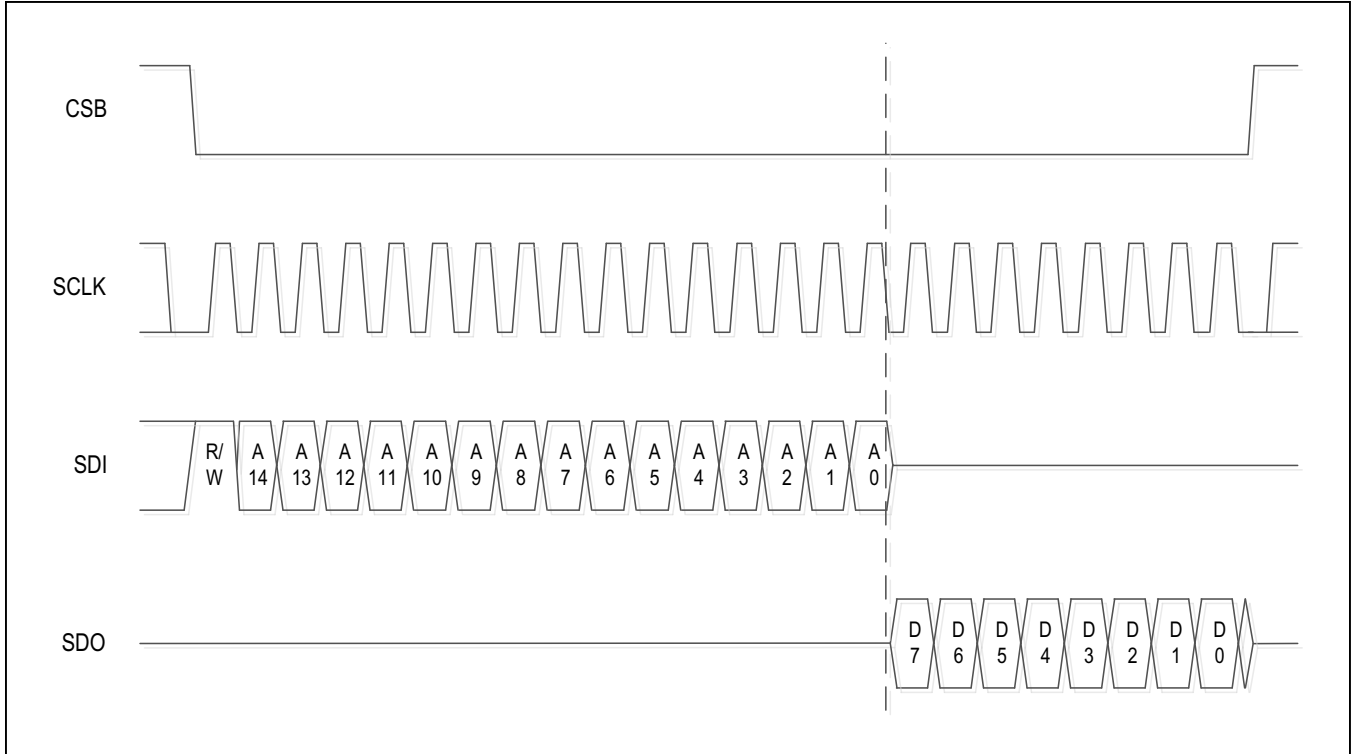
Figure 13. Single SPI Read Transaction with MSB-First
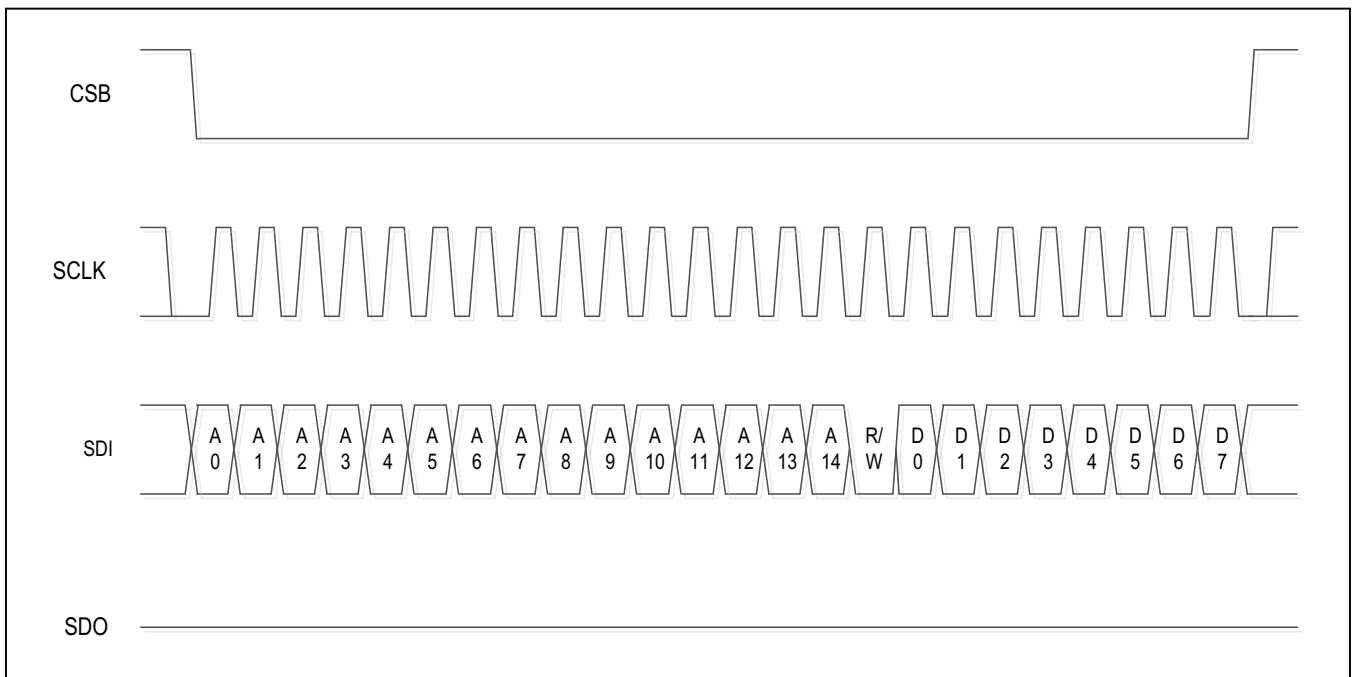


Figure 14. Single SPI Write Transaction with LSB-First
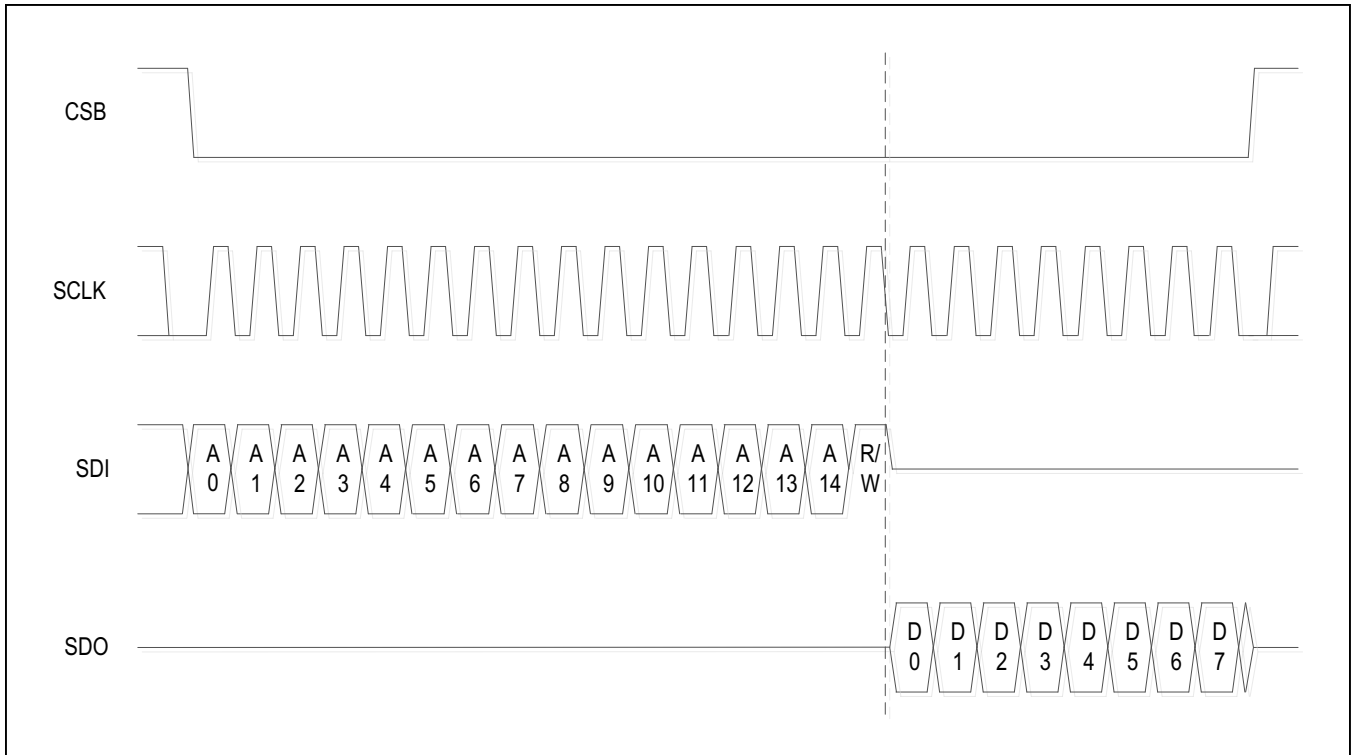
Figure 15. Single SPI Read Transaction with LSB-First
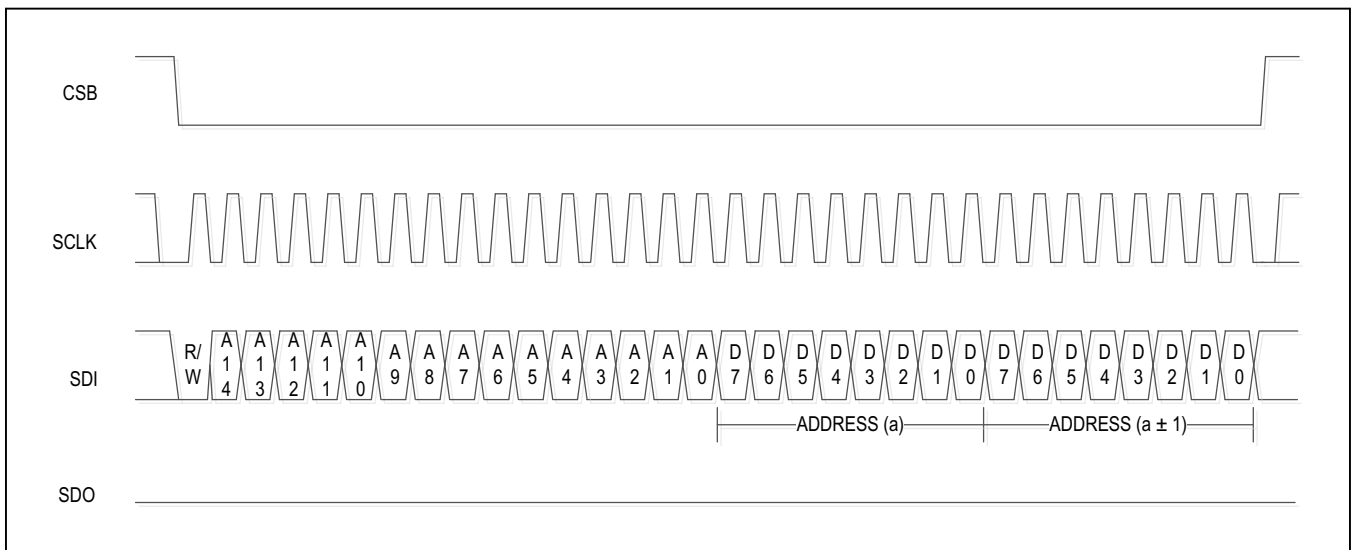


Figure 16. Burst SPI Write Transaction with MSB-First
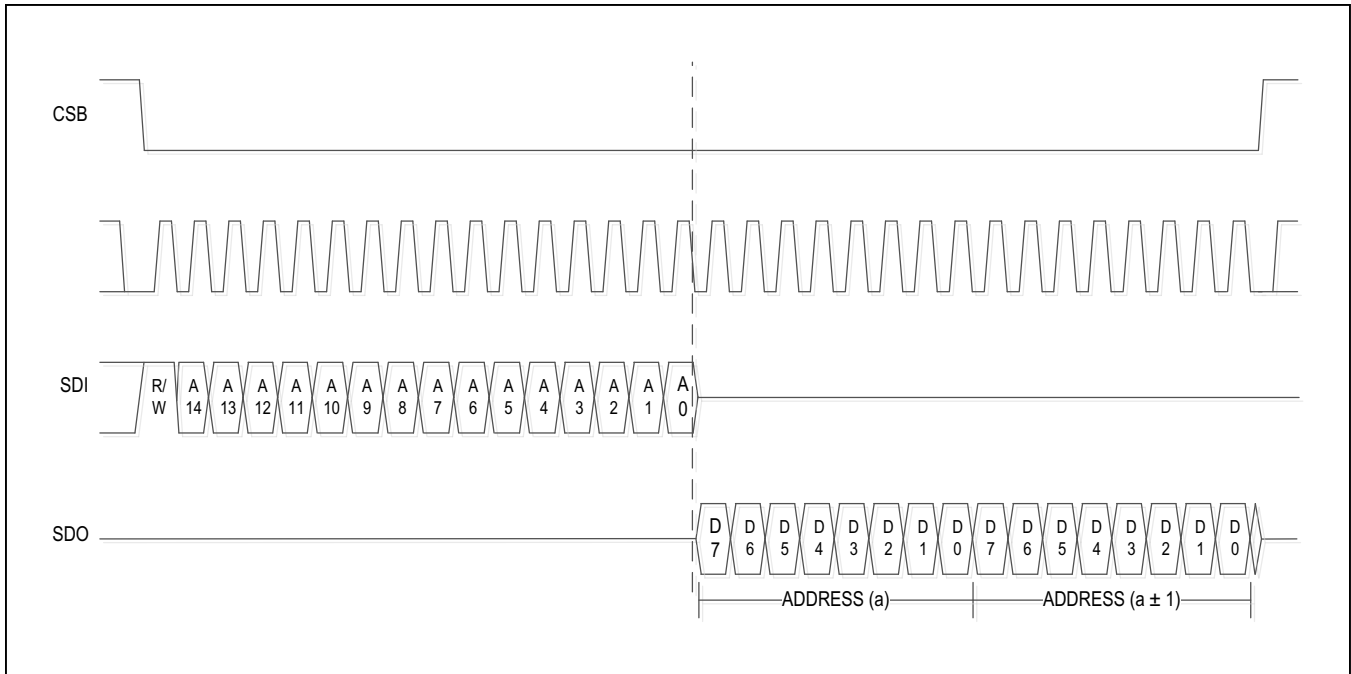
*Figure 17. Burst SPI Read Transaction with MSB-First*
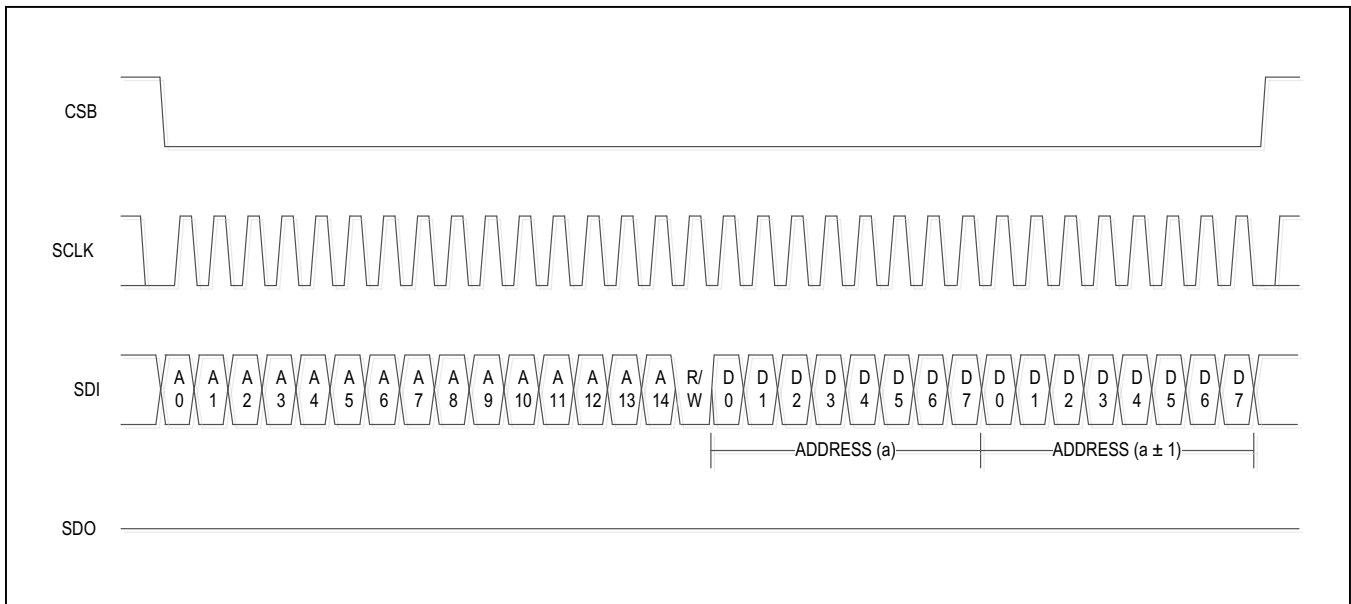


*Figure 18. Burst SPI Write Transaction with LSB-First*
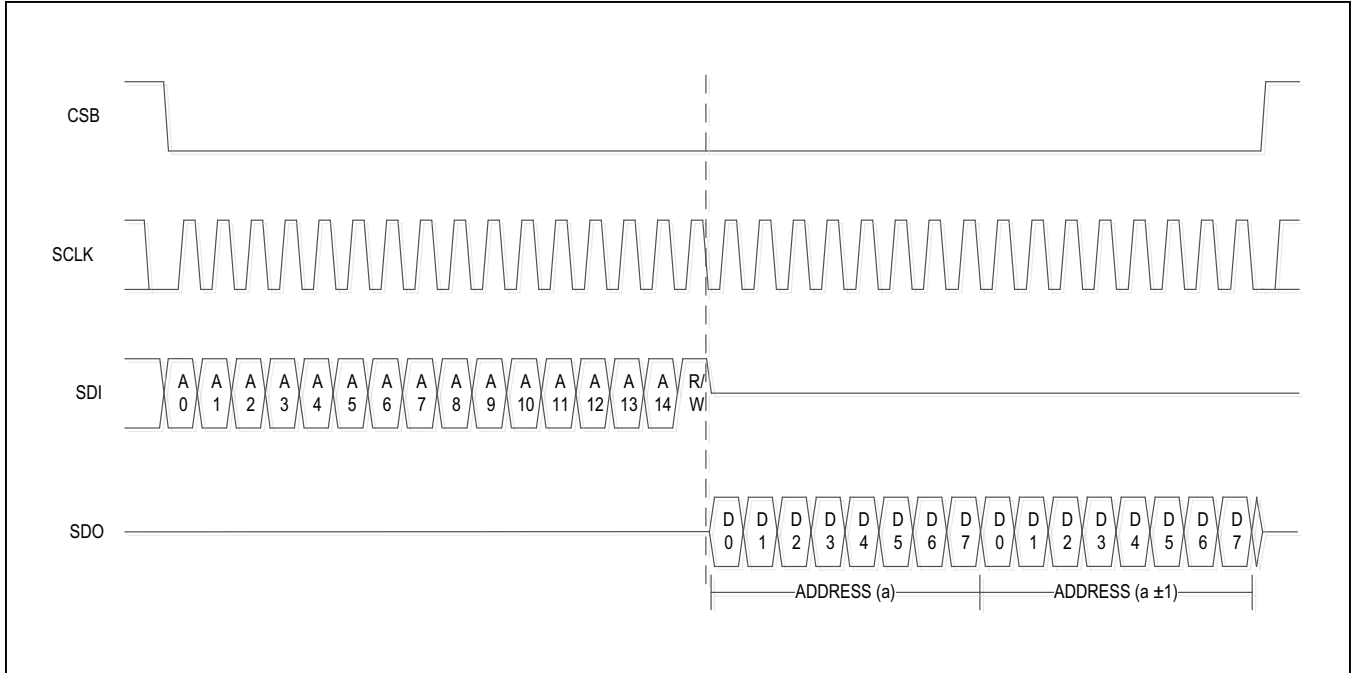
Figure 19. Burst SPI Read Transaction with LSB-First

## Interrupt and Mute

The INTB pin is a CMOS output port that signals an interrupt condition when in the low state. The interrupt system is composed of an interrupt register and an interrupt mask. The interrupt signal is a logic NOR of the bit-wise AND operation of the interrupt register and the interrupt mask. In the MAX5871, 7 interrupt bits are defined: 2 bits for JESD204B mute and interrupt status, 3 bits for a FIFO collision (1-away and 2-away), 1 bit for trim ready, and 1

bit for DAC PLL unlock status. The interrupt tree for the MAX5871 is shown in Figure 20. The JESD204B interface has its own second level of interrupt registers and interrupt mask registers as defined in the register interface. The interrupt mask and register can be modified through the serial interface. Table 2 shows all the status register bits that can be enabled to generate an interrupt.
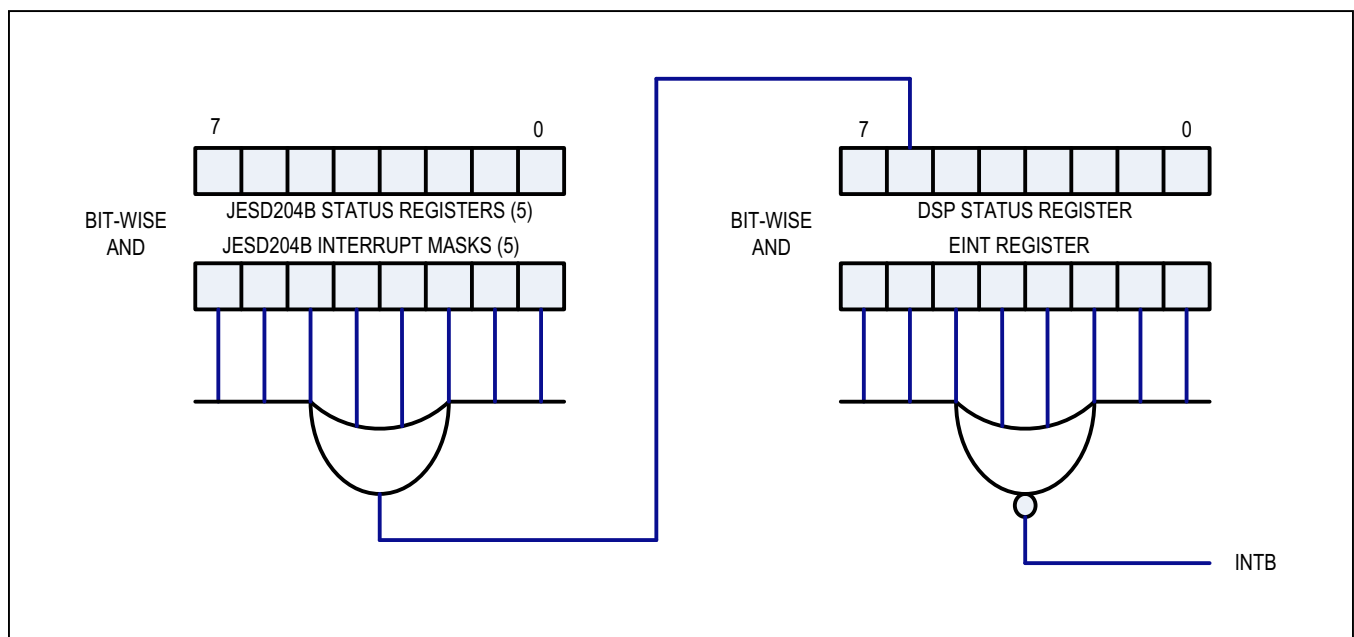


*Figure 20. MAX5871 Interrupt Tree*

## Table 2. MAX5871 Status Register Bits

| DSP STATUS REGISTERS (1ST LEVEL INTERRUPT) | |
|---|---|
| **BANK.REGISTER.BIT** | **FUNCTION** |
| DSP.STATUS.JSDIM | Real-time status indicating DAC mute from JSDI link layer is active |
| DSP.STATUS.JSDII | Real-time status indicating interrupt from JSDI link layer is active |
| DSP.STATUS.FCOL | Latched status set when the input FIFO write and read pointers collide causing FIFO underflow or overflow |
| DSP.STATUS.F1A | Latched status set when the input FIFO write and read pointers are away from each other by one sample |
| DSP.STATUS.F2A | Latched status set when the input FIFO write and read pointers are away from each other by two samples |
| DSP.STATUS.TRDY | Latched status set when trim loading load is complete and the SPI bus is unblocked for external access |
| DSP.STATUS.PLLlck | Latched status set when the DAC PLL is unlocked |

| JESD204B STATUS REGISTERS (2ND LEVEL INTERRUPT) | |
|---|---|
| **BANK.REGISTER.BIT** | **FUNCTION** |
| LNK.StatLane.lnNfnsync | Real-time status indicating the frame synchronization state machine is not in sync on Lane N |
| LNK.StatLane.lnNlnrealgn | Latched status set when a lane realignment occurs on Lane N |
| LNK.StatLane.lnNfrrealgn | Latched status set when a frame realignment occurs on Lane N |
| LNK.StatLane.lnNuk | Latched status set when an unexpected /K/ character is received at an unexpected position while code group synchronization is established on Lane N |
| LNK.StatLane.lnNctrl | Latched status set when an unexpected control character other than /K/ is received when not expected on Lane N |
| LNK.StatLane.lnNdisp | Latched status set when a disparity error is detected on Lane N |
| LNK.StatLane.lnNnit | Latched status set when a NIT error is detected on Lane N |
| LNK.StatLane.lnNcgs | Latched status set when code group synchronization state-machine is out of sync on Lane N |
| LNK.StatFIFO.lnNfafail | Latched status set when dynamic FIFO adjustment fails due to not enough FIFO space on Lane N |
| LNK.StatFIFO.lnNempty | Latched status set when the FIFO goes empty on Lane N |
| LNK.StatFIFO.lnNfull | Latched status set when the FIFO goes full on Lane N |
| LNK.StatILAS.lnNkerr | Latched status set when a /K/ character is received at the current CGS boundary while in frame sync on Lane N |
| LNK.StatILAS.lnNrprbs | Latched status set when the SerDes interface PRBS monitor detected an error on Lane N |
| LNK.StatILAS.lnNkrcv | Latched status set when a non-/K/ character is detected on Lane N |
| LNK.StatILAS.lnNfchkerr | Latched status set when an ILA sequence FCHK error is detected on Lane N |
| LNK.StatILAS.lnNlcfgerr | Latched status set when an ILA sequence lane configuration error is detected on Lane N |
| LNK.StatILAS.lnNilaerr | Latched status set when an ILA sequence decode (/R/, /Q/, /A/ character) error is detected on Lane N |
| LNK.StatILA.nsync | Real-time status indicating ILA synchronization has not been achieved |
| LNK.StatILA.syncn_det | Latched status set on a resync request until a SYSREF pulse is detected |
| LNK.StatILA.sysref_ndet | Real-time SYSREF detection status set until first SYSREF detected |
| LNK.StatILA.fail | Latched status set when ILA failure due to not enough FIFO depth or when ILA is based on lanes that are not ready with data |
| LNK.StatLink.prbs_c2err | Latched status set when Converter 2 (Q-sample) PRBS error is detected |
| LNK.StatLink.prbs_c1err | Latched status set when Converter 1 (I-sample) PRBS error is detected |
| LNK.StatLink.stp_c2err | Latched status set when Converter 2 (Q-sample) short test pattern error is detected |
| LNK.StatLink.stp_c1err | Latched status set when Converter 1 (I-sample) short test pattern error is detected |

## Digital Control Pins

The MAX5871 contains two 1.8V CMOS logic digital control pins, RESETB and MUTE. The device is placed in a reset state when RESETB is low. This control line is level sensitive. On power-up, RESETB should remain low until all supply voltages have stabilized.

The MUTE pin defines when the device enters the mute mode. A high logic level places the device in mute mode while a low state establishes normal operation. In mute mode, the DAC digital input is set to midscale. The main purpose of mute is to eliminate any transmit power during the receive time of a TDMA system. In addition, there is a mute configuration programmed through the serial inter-face that enables the mute mode internally regardless of the state of the MUTE pin. A duplication of the interrupt mask registers as Mute Enable registers generate the internal mute signal. Table 2 shows all the status register bits that can be enabled to generate internal mute. The internal control state of the converter is preserved while the MAX5871 is in the MUTE state.

## Frequency Planning

Using a DAC to generate communications transmit signals requires careful consideration of aliased harmonics and internally generated divided clocks. Figure 22 shows an example of two modulated signals transmitted at 1.8GHz and 2.1GHz. The second harmonic (HD2) and
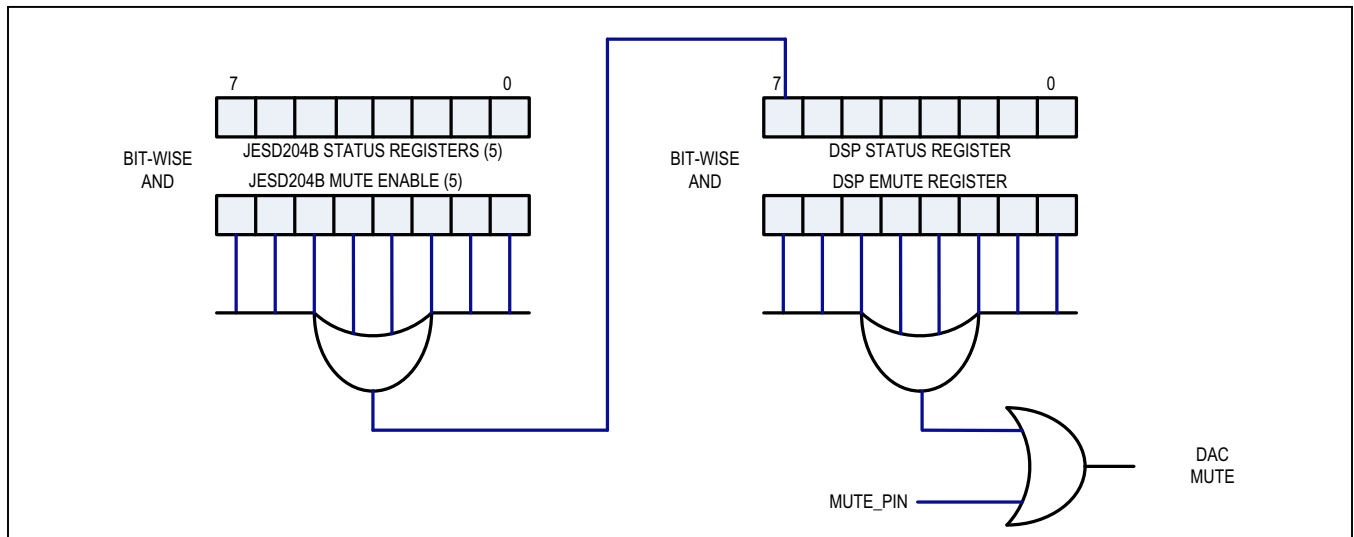


*Figure 21. MAX5871 DAC Mute Generation*
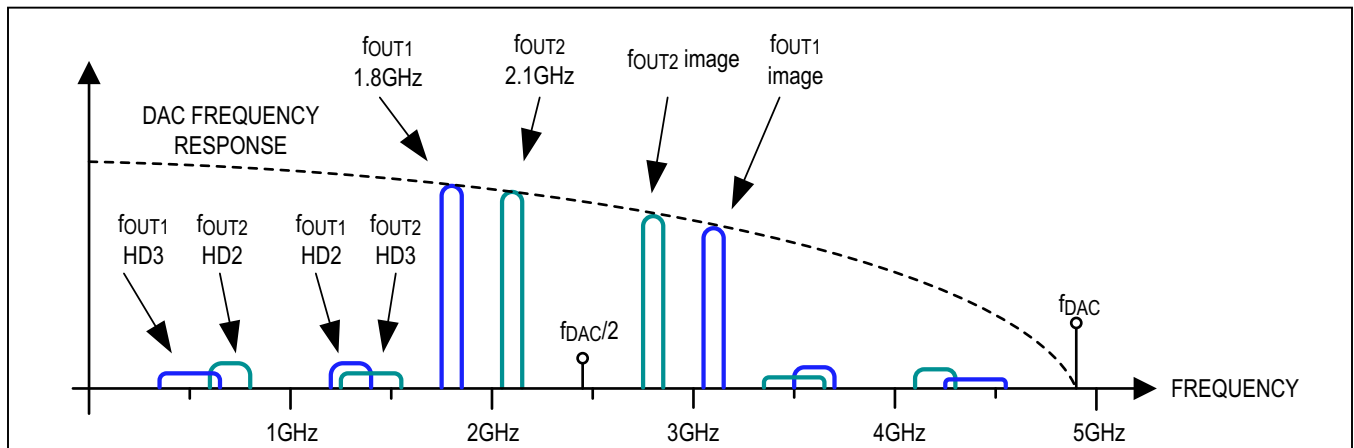


*Figure 22. Example of Multiband Transmission and Dominant Harmonic Locations*

third harmonic (HD3) of the signal are aliased close to the transmitted signal due to the DAC sampling rate.

The MAX5871 features a high-performance DAC core and many of the spurs and harmonics are suppressed. However, care must be taken to select the DAC sample rate such that the location of the dominant harmonics, such has HD2 and HD3, do not fall into the band of interest. If the board is not carefully designed to isolate the digital and analog portions, the input data may cause spurs to appear at the DAC output. The MAX5871 offers many interpolation settings for upconverting the input data such that a proper update rate can be chosen. For frequency planning, determine the input sample (or data) rate for the DAC and choose the DAC update rate such that the dominant harmonics are aliased outside of the band of interest. Next choose an interpolation rate closest to the DAC update rate divided by the input sample rate. Once the interpolation rate is determined, recalculate the exact DAC update rate, thereby determining the frequency of the DAC clock input. For new DAC update rate, reverify that the spur or harmonics are within spurious emission requirements.

## Signal Bandwidth

The MAX5871 can generate a maximum I/Q complex signal bandwidth of 600.15MHz when operating $f_{DAC}$ = 5898.24Msps and 8x interpolation (or $f_{DAC}$ and interpolation setting combinations with the maximum input sample rate of 737.28MHz) for output frequencies ranging from DC to Nyquist.

The actual signal bandwidth is dependent on the input sample rate ($f_{S\_IN}$), or the DAC update rate ($f_{DAC}$) divided by the interpolation setting (R), and the interpolation filter passband width (PBW = 0.407, expressed as a percentage of the input sample rate). The I/Q complex DAC signal bandwidth is calculated as:

DAC Signal Bandwidth = 2 x ($f_{DAC}$/R) x (PBW)

The complex I/Q signals are converted to a real signal using a digital quadrature modulator and quadrature NCO. The real bandwidth is centered around the NCO frequency.

## Complex Modulator and NCO

The device includes a complex modulator comprised of a complex NCO driving two multipliers followed by an adder (Figure 23). The complex modulator produces the result:

I(n) x COS(ωn) - Q(n) x SIN(ωn)

where I and Q are filtered and interpolated versions of the input I-data and Q-data.

The complex NCO employs a 33-bit phase accumulator to provide a programmed signal frequency up to $f_{DAC}$/2. The DAC sample rate, $f_{DAC}$, must be an integer multiple of a 30.72MHz reference frequency. The resolution of the MAX5871 can be programmed at 1Hz/10Hz/100Hz/1kHz/10kHz for a range of DAC clock frequency options. The user needs to program the following three parameters for the NCO, frequency control word (FCW), numerator frequency word (NFW), and denominator frequency word (DFW).

The NCO resolution ($f_{STEP}$) is defined as:

$$f_{STEP} = \frac{f_{DAC}}{M \times 3 \times 2^{10} \times 10^N}$$

where $f_{DAC}$ = M x reference frequency. For example, if the reference frequency is 30.72MHz, use M = 192 for a DAC clock frequency ($f_{DAC}$) of 5898.24Msps. N = 0-4 sets the NCO resolution to 10kHz to 1Hz, respectively. The values of M and N are only used to calculate the FCW, NFW, and DFW that are required to program the required signal frequency.

To program the required output frequency ($f_{OUT}$) of the DAC, the user needs to follow these steps:

1) Convert $f_{OUT}$ into an integer number, mapping it on to the desired frequency resolution scale ($f_r$) that depends on the value of N, using the equation:

$$f_r = f_{sig} \times 10^{n-4}$$

where $f_{OUT}$ is in Hz.

2) The frequency control word parameters can be calculated using the following equation:
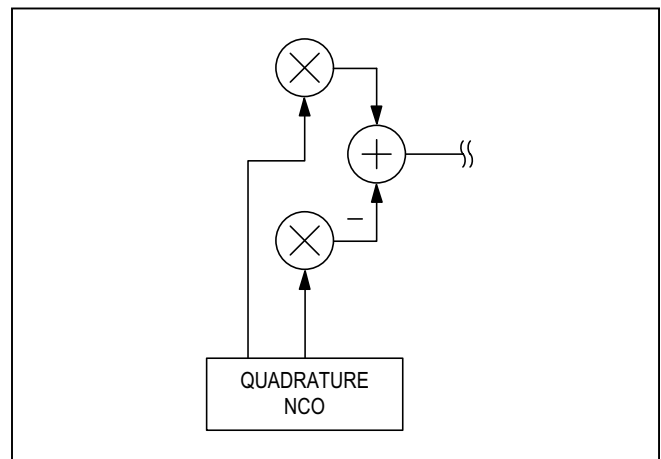


Figure 23. Complex NCO and Modulator

$$FCW = \frac{2^{33} \times f_r}{M \times 3 \times 2^{10} \times 10^N}$$

3) The previous calculation results in a rational value (FCW_full) of the frequency control word. Only the quotient portion is set as the FCW. The remainder fractional value is converted into two integer rational numbers by removing the common integer multiplication factor between them. The numerator of this ratio is set as NFW and the denominator as DFW. Thus:

$$FCW\_full = FCW + \frac{NFW}{DFW}$$

FCW (32-bit), NFW (18-bit), and DFW (19-bit), control words are programmed via the SPI bus. If the above calculation results into an integer number then NFW=DFW=0 should be set:

$$FCW\_full = 2^{33} \times \frac{F_{NCO}}{F_{DAC}} = FCW + \frac{NFW}{DFW}$$

FCW_full = full resolution of rational number to be programmed

FCW = integer part of the FCW_full

NFW = numerator of the fractional part of FCW_full

DFW = denominator of the fractional part of FCW_full

The NCO block diagram is shown in Figure 24.

**When calculating FCW, NFW, and DFW, use long format (more precision) in Matlab code.**

For example, take M = 163 for $f_{DAC}$ = 163 x 30.72MHz = 5007.36MHz.

Case 1 select $f_{NCO}$ = 1796.769375MHz

$$FCW\_full = 2^{33} \times \frac{F_{NCO}}{F_{DAC}} = 2^{33}$$

$$\times \frac{1796.769375MHz}{5007.36MHz} = 3082289152.000000$$

Therefore, FCW = 3082289152, NFW = 0, DFW = 0.

Case 2 select $f_{NCO}$ = 1796.875MHz

$$FCW\_full = 2^{33} \times \frac{F_{NCO}}{F_{DAC}} = 2^{33}$$

$$\times \frac{1796.875MHz}{5007.36MHz} = 3082470347.64826000000$$

Therefore, FCW = 3082470347, NFW/DFW = 317/489 ~ 0.64826000000.
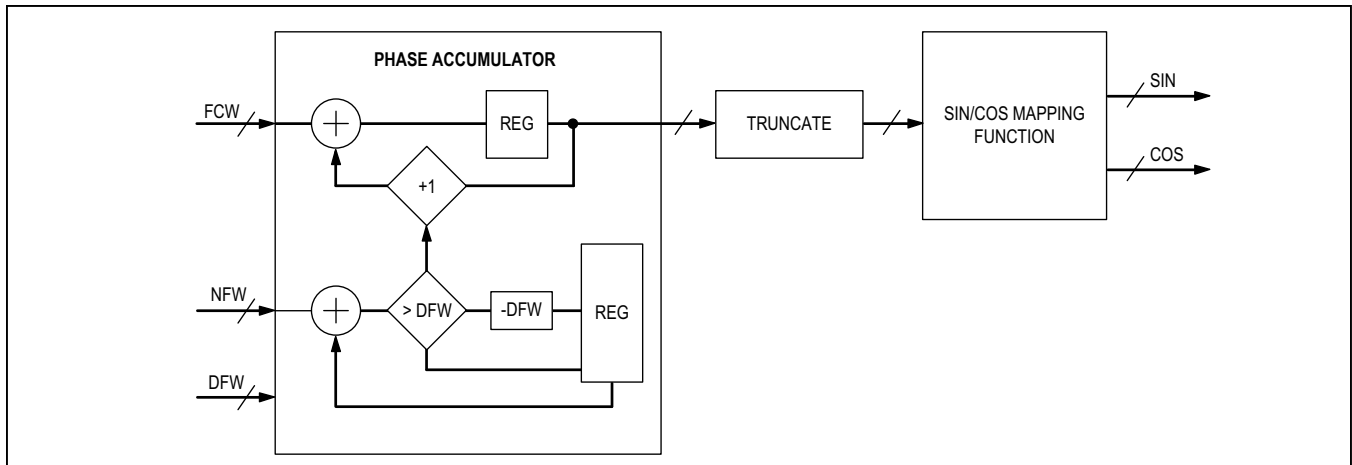


Figure 24. NCO Block Diagram

The following is a simple Matlab code for calculating FCW, NFW, and DFW:

```
% Find out MAX5871 NCO values
format long

% Define DAC clock frequency M=1-200
M = 163

Fdac = 30.72e6*M

% Define desired NCO frequency
Fnco = 1796.769375e6;

FCW_full = 2^33*Fnco/Fdac;

% Calculate FCW, NFW and DFWa
FCW = floor(FCW_full)
rats(FCW_full-FCW)
% END
```

## Analog Interface

### Reference Interface

The device operates with either the on-chip 1.2V bandgap reference or an external reference voltage source as shown in Figures 25a and 25b. REFIO serves as the input for an external, low-impedance reference source, or as the reference output when the internal reference is used. REFIO must be decoupled to DACREF with a 1µF capacitor when using the internal reference. REFIO must be buffered with an external amplifier if heavier loading is required, due to the 10kΩ series resistance.

The reference circuit employs a control amplifier designed to regulate the full-scale, differential output current, $I_{OUTFS}$. The output current is calculated as follows:

$$I_{OUTFS} = 32 \times I_{REF}$$

where $I_{REF}$ is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and $I_{OUTFS}$ is the full-scale output current of the DAC. Using the 1.2V (typical) internal reference and $R_{SET}$ of 1.28kΩ results in a full-scale output current of 30mA. In general, the dynamic performance of the DAC improves with increasing full-scale current.

## Analog Output

The device is a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to AVDD2 providing a 50Ω differential output resistance. In addition to the signal current, a constant current sink ($I_{FIX}$) equal to one half $I_{OUTFS}$ is connected to each differential DAC output. N = 14 and is the number of bits of resolution of the DAC core. Figure 26 shows an equivalent circuit for the internal output structure of the device. The circuit has some resistive, capacitive and inductive elements. These elements have been minimized by design in order to achieve the highest possible output bandwidth (2600MHz typical).

In addition, the device requires a differential external termination (i.e. double termination). This external termination can be accomplished with a differential 50Ω load or a single-ended 50Ω load interfaced through a transformer. RF chokes to the AVDD2 supply should be used with the transformer coupled output. A typical transformer coupled configuration for high-frequency operation is shown in Figure 26.
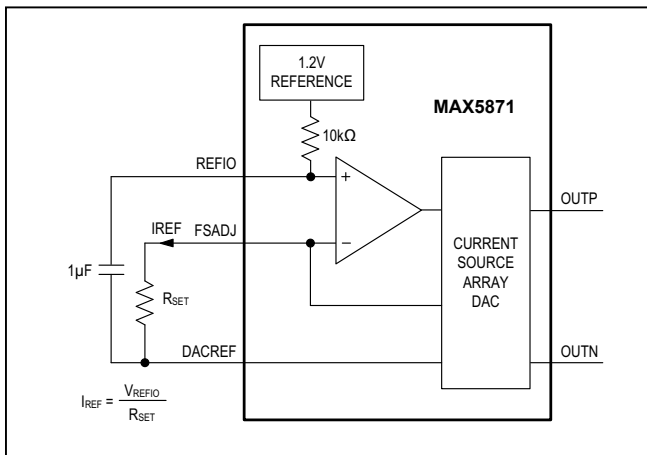


Figure 25a. Reference Architecture, Internal Reference Configuration
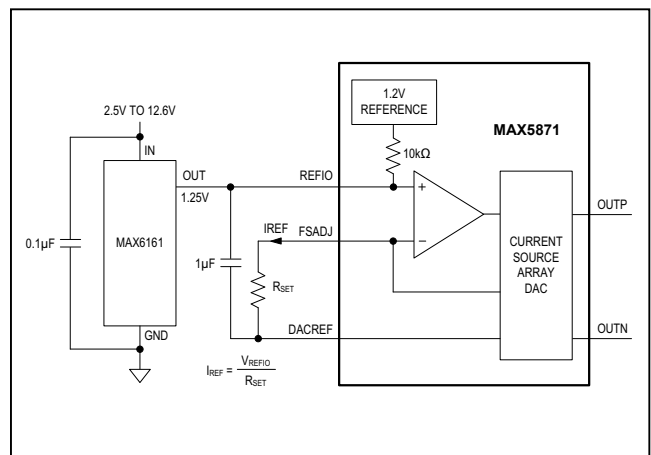


Figure 25b. Reference Architecture, External Reference Configuration

For applications where the DC information is important, the output configuration in Figure 27 can be used. 25Ω resistors to AVDD2 are required for DC coupling. The DC configuration will lower the output common-mode which may reduce performance slightly. The device is not compatible with an unterminated output when using the upper portion of the full-scale current range. Lowering the full-scale current to 20mA or less may allow use of the outputs without external terminations, though performance will be impacted in this configuration.

### Clock Interface

The MAX5871 DAC contains a differential high frequency clock input (CLKP/CLKN) and an optional (bypassable) internal clock multiplying PLL to ease clock distribution. When the PLL is bypassed, the DAC is updated on the rising edge of (CLKP/CLKN) at maximum frequency of 5898.24MHz. See the *DAC Clock PLL* section for operation with PLL enabled.

The high-frequency clock should be a balanced fully differential signal with a 50%, or near 50%, duty cycle. The clock input has internal (on-chip) 100Ω differential termination. The clock inputs requires a minimum of 0dBm input power. The clock inputs must be AC-coupled to the clock source as they are self-biased internally.

### DAC Clock PLL

The MAX5871 differential high frequency clock input (CLKP/CLKN) also accepts an external reference clock signal that can be multiplied internally by a phase-locked-loop (PLL). The PLL includes user-programmable multiplication factors which provide flexibility in the reference clock selection. Figure 28 shows the functional block diagram of the PLL.

The reference input signal is divided by 1, 2, 4, or 8 under user control before being applied to the phase/frequency detector (PFD). The VCO output is divided by a programmable divide by 16/20/24/28 divider and fed back to the PFD. In addition to the programmable reference divider and programmable VCO divider, there is an optional output divide by 2, before the clock signal is supplied to the RF DAC.

Table 3 summarizes frequency multiplication factors between an external reference clock and DACCLK for various PLL settings.
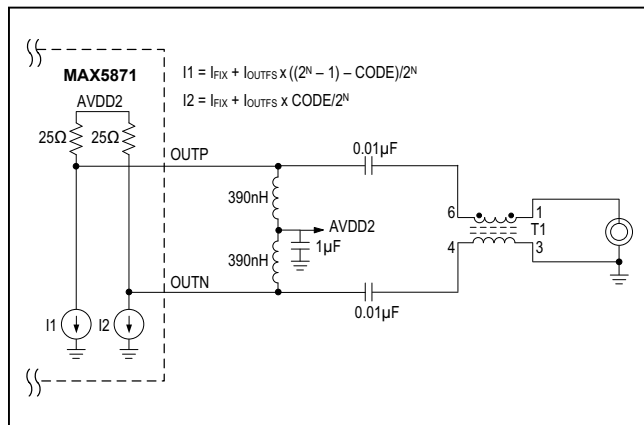


Figure 26. Typical DAC Output Configuration
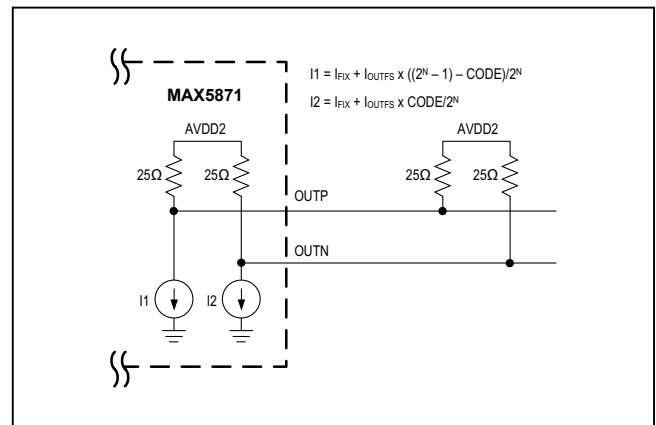


Figure 27. Output Configuration for Low-Frequency Operation

## Table 3. PLL Configuration Settings and Overall Multiplication Factor

| REFERENCE DIVIDE-SETTING (N) | FEEDBACK DIVIDE-SETTING (M) | POST DIVIDE-SETTING | VCO MULTIPLICATION FACTOR | OVERALL FREQUENCY MULTIPLICATION FACTOR |
|:---:|:---:|:---:|:---:|:---:|
| 2 | 16 | 1 | 8 | 8 |
| 2 | 20 | 1 | 10 | 10 |
| 2 | 24 | 1 | 12 | 12 |
| 2 | 28 | 1 | 14 | 14 |
| 2 | 16 | 2 | 8 | 4 |
| 2 | 20 | 2 | 10 | 5 |
| 2 | 24 | 2 | 12 | 6 |
| 2 | 28 | 2 | 14 | 7 |
| 4 | 16 | 1 | 4 | 4 |
| 4 | 20 | 1 | 5 | 5 |
| 4 | 24 | 1 | 6 | 6 |
| 4 | 28 | 1 | 7 | 7 |
| 4 | 16 | 2 | 4 | 2 |
| 4 | 20 | 2 | 5 | 2.5 |
| 4 | 24 | 2 | 6 | 3 |
| 4 | 28 | 2 | 7 | 3.5 |
| 8 | 16 | 1 | 2 | 2 |
| 8 | 20 | 1 | 2.5 | 2.5 |
| 8 | 24 | 1 | 3.0 | 3 |
| 8 | 28 | 1 | 3.5 | 3.5 |
| 8 | 16 | 2 | 2 | 1 |
| 8 | 20 | 2 | 2.5 | 1.25 |
| 8 | 24 | 2 | 3.0 | 1.50 |
| 8 | 28 | 2 | 3.5 | 1.75 |

### VCO Band Select

The VCO has two frequency ranges. The low range is 4.42368GHz to 4.9152GHz and the high range is 5.89824GHz to 6.1440GHz; however, the DAC sample rate is limited to 5.89824Gsps. The combination of reference frequency, reference and feedback divide values, and VCO band select must be chosen to operate the VCO within its allowed frequency range.

### Lock Detect

The DAC clock PLL includes a lock detect indicator which can be read out of the SPI status register (DSP.StatPLL). Bit PLLST3 is set high when the PLL is locked and low when the PLL is unlocked.

### PLL External Components

The DAC clock PLL requires external loop filter components. Figure 29 shows the schematic for the loop filter.

The loop filter components should be placed as close as possible to the MAX5871 to avoid noise coupling into the circuit. In addition to the loop filter, there is a bypass capacitor that must be placed very close to the MAX5871. The C1 nF and C2 pF capacitor values strongly depends on system PCB design and are unique for most designs (see the *Application Guidelines* section).

### Interpolation Filters

The MAX5871 has powerful digital signal process capability with its built-in digital interpolation filters that can be configured with an interpolation ratio of 5x, 6x, 6.67x, 8x, 10x, 12x, 13.33x, 16x, 20x, 24x. Table 4 shows the digital filter coefficients of 8x and 10x interpolation ratios as examples. Figure 30 to Figure 39 show the frequency response of each of the interpolation ratio settings.
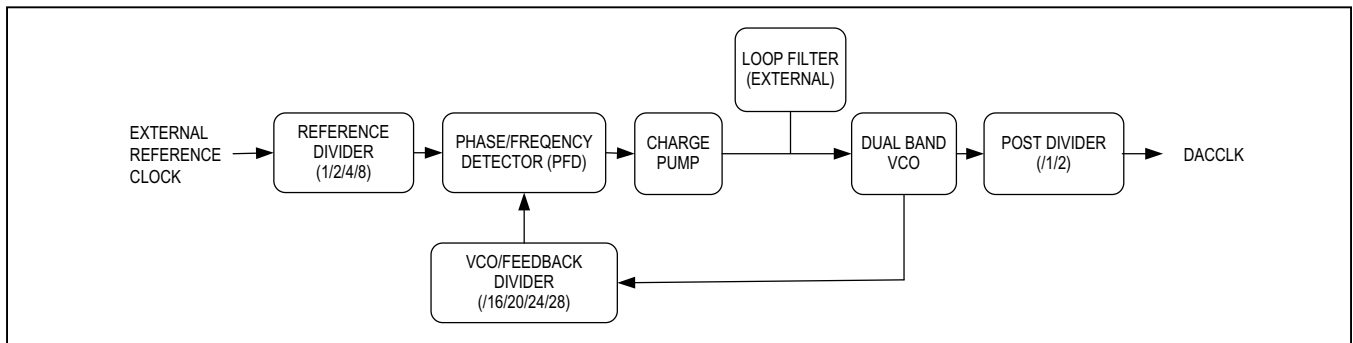


Figure 28. DAC Clock PLL Functional Block Diagram
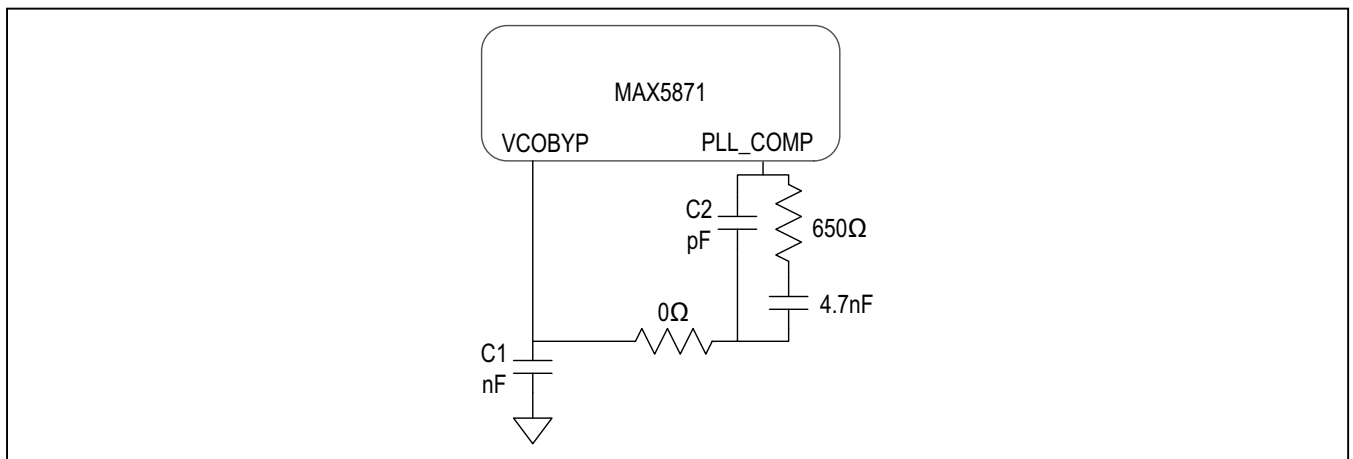


Figure 29. DAC Clock PLL External Components

## Table 4. Digital Filter Coefficients for 8x and 10x Interpolation Ratios

| TAPS | FILTER 8x | FILTER 10x | TAPS | FILTER 8x | FILTER 10x |
|---|---|---|---|---|---|
| 1 | 0.00000000000000000 | 0.00000000000000000 | 171 | 0.04010009765625000 | 0.99548339843750000 |
| 2 | 0.00001525878906250 | 0.00001525878906250 | 172 | 0.05004882812500000 | 0.99548339843750000 |
| 3 | 0.00003051757812500 | 0.00003051757812500 | 173 | 0.05175781250000000 | 0.96273803710937500 |
| 4 | 0.00004577636718750 | 0.00003051757812500 | 174 | 0.04571533203125000 | 0.89920043945312500 |
| 5 | 0.00006103515625000 | 0.00004577636718750 | 175 | 0.03344726562500000 | 0.80863952636718700 |
| 6 | 0.00007629394531250 | 0.00006103515625000 | 176 | 0.01730346679687500 | 0.69641113281250000 |
| 7 | 0.00006103515625000 | 0.00007629394531250 | 177 | 0.00000000000000000 | 0.56901550292968700 |
| 8 | 0.00003051757812500 | 0.00007629394531250 | 178 | -0.01580810546875000 | 0.43365478515625000 |
| 9 | 0.00000000000000000 | 0.00006103515625000 | 179 | -0.02795410156250000 | 0.29772949218750000 |
| 10 | -0.00003051757812500 | 0.00004577636718750 | 180 | -0.03494262695312500 | 0.16838073730468700 |
| 11 | -0.00006103515625000 | 0.00001525878906250 | 181 | -0.03619384765625000 | 0.05197143554687500 |
| 12 | -0.00013732910156250 | 0.00000000000000000 | 182 | -0.03198242187500000 | -0.04637145996093750 |
| 13 | -0.00018310546875000 | -0.00003051757812500 | 183 | -0.02340698242187500 | -0.12295532226562500 |
| 14 | -0.00016784667968750 | -0.00006103515625000 | 184 | -0.01211547851562500 | -0.17572021484375000 |
| 15 | -0.00012207031250000 | -0.00010681152343750 | 185 | 0.00000000000000000 | -0.20431518554687500 |
| 16 | -0.00006103515625000 | -0.00015258789062500 | 186 | 0.01106262207031250 | -0.21008300781250000 |
| 17 | 0.00000000000000000 | -0.00018310546875000 | 187 | 0.01953125000000000 | -0.19575500488281200 |
| 18 | 0.00012207031250000 | -0.00016784667968750 | 188 | 0.02439880371093750 | -0.16522216796875000 |
| 19 | 0.00024414062500000 | -0.00012207031250000 | 189 | 0.02523803710937500 | -0.12316894531250000 |
| 20 | 0.00033569335937500 | -0.00007629394531250 | 190 | 0.02227783203125000 | -0.07461547851562500 |
| 21 | 0.00039672851562500 | -0.00001525878906250 | 191 | 0.01629638671875000 | -0.02461242675781250 |
| 22 | 0.00039672851562500 | 0.00004577636718750 | 192 | 0.00842285156250000 | 0.02224731445312500 |
| 23 | 0.00033569335937500 | 0.00013732910156250 | 193 | 0.00000000000000000 | 0.06210327148437500 |
| 24 | 0.00019836425781250 | 0.00022888183593750 | 194 | -0.00765991210937500 | 0.09211730957031250 |
| 25 | 0.00000000000000000 | 0.00030517578125000 | 195 | -0.01348876953125000 | 0.11053466796875000 |
| 26 | -0.00022888183593750 | 0.00036621093750000 | 196 | -0.01683044433593750 | 0.11682128906250000 |
| 27 | -0.00048828125000000 | 0.00038146972656250 | 197 | -0.01739501953125000 | 0.11148071289062500 |
| 28 | -0.00070190429687500 | 0.00038146972656250 | 198 | -0.01530456542968750 | 0.09611511230468750 |
| 29 | -0.00085449218750000 | 0.00033569335937500 | 199 | -0.01113891601562500 | 0.07298278808593750 |
| 30 | -0.00085449218750000 | 0.00022888183593750 | 200 | -0.00573730468750000 | 0.04495239257812500 |
| 31 | -0.00070190429687500 | 0.00009155273437500 | 201 | 0.00000000000000000 | 0.01504516601562500 |
| 32 | -0.00041198730468750 | -0.00009155273437500 | 202 | 0.00520324707031250 | -0.01383972167968750 |
| 33 | 0.00000000000000000 | -0.00028991699218750 | 203 | 0.00915527343750000 | -0.03907775878906250 |
| 34 | 0.00048828125000000 | -0.00048828125000000 | 204 | 0.01136779785156250 | -0.05859375000000000 |
| 35 | 0.00097656250000000 | -0.00067138671875000 | 205 | 0.01168823242187500 | -0.07099914550781250 |
| 36 | 0.00138854980468750 | -0.00080871582031250 | 206 | 0.01025390625000000 | -0.07569885253906250 |
| 37 | 0.00161743164062500 | -0.00085449218750000 | 207 | 0.00744628906250000 | -0.07284545898437500 |
| 38 | 0.00161743164062500 | -0.00082397460937500 | 208 | 0.00381469726562500 | -0.06326293945312500 |
| 39 | 0.00134277343750000 | -0.00070190429687500 | 209 | 0.00000000000000000 | -0.04837036132812500 |
| 40 | 0.00077819824218750 | -0.00047302246093750 | 210 | -0.00343322753906250 | -0.02996826171875000 |
| 41 | 0.00000000000000000 | -0.00016784667968750 | 211 | -0.00601196289062500 | -0.01005554199218750 |

### Table 4. Digital Filter Coefficients for 8x and 10x Interpolation Ratios (continued)

| TAPS | FILTER 8x | FILTER 10x | TAPS | FILTER 8x | FILTER 10x |
|------|-----------|------------|------|-----------|------------|
| 42 | -0.00090026855468750 | 0.00019836425781250 | 212 | -0.00744628906250000 | 0.00935363769531250 |
| 43 | -0.00177001953125000 | 0.00061035156250000 | 213 | -0.00762939453125000 | 0.02648925781250000 |
| 44 | -0.00247192382812500 | 0.00099182128906250 | 214 | -0.00666809082031250 | 0.03987121582031250 |
| 45 | -0.00286865234375000 | 0.00132751464843750 | 215 | -0.00482177734375000 | 0.04847717285156250 |
| 46 | -0.00283813476562500 | 0.00155639648437500 | 216 | -0.00247192382812500 | 0.05186462402343750 |
| 47 | -0.00231933593750000 | 0.00164794921875000 | 217 | 0.00000000000000000 | 0.05007934570312500 |
| 48 | -0.00134277343750000 | 0.00158691406250000 | 218 | 0.00219726562500000 | 0.04362487792968750 |
| 49 | 0.00000000000000000 | 0.00134277343750000 | 219 | 0.00381469726562500 | 0.03344726562500000 |
| 50 | 0.00152587890625000 | 0.00091552734375000 | 220 | 0.00469970703125000 | 0.02076721191406250 |
| 51 | 0.00299072265625000 | 0.00033569335937500 | 221 | 0.00479125976562500 | 0.00698852539062500 |
| 52 | 0.00415039062500000 | -0.00036621093750000 | 222 | 0.00415039062500000 | -0.00651550292968750 |
| 53 | 0.00479125976562500 | -0.00109863281250000 | 223 | 0.00299072265625000 | -0.01844787597656250 |
| 54 | 0.00469970703125000 | -0.00177001953125000 | 224 | 0.00152587890625000 | -0.02780151367187500 |
| 55 | 0.00381469726562500 | -0.00234985351562500 | 225 | 0.00000000000000000 | -0.03384399414062500 |
| 56 | 0.00219726562500000 | -0.00274658203125000 | 226 | -0.00134277343750000 | -0.03625488281250000 |
| 57 | 0.00000000000000000 | -0.00289916992187500 | 227 | -0.00231933593750000 | -0.03503417968750000 |
| 58 | -0.00247192382812500 | -0.00276184082031250 | 228 | -0.00283813476562500 | -0.03053283691406250 |
| 59 | -0.00482177734375000 | -0.00231933593750000 | 229 | -0.00286865234375000 | -0.02340698242187500 |
| 60 | -0.00666809082031250 | -0.00157165527343750 | 230 | -0.00247192382812500 | -0.01452636718750000 |
| 61 | -0.00762939453125000 | -0.00056457519531250 | 231 | -0.00177001953125000 | -0.00488281250000000 |
| 62 | -0.00744628906250000 | 0.00061035156250000 | 232 | -0.00090026855468750 | 0.00454711914062500 |
| 63 | -0.00601196289062500 | 0.00184631347656250 | 233 | 0.00000000000000000 | 0.01289367675781250 |
| 64 | -0.00343322753906250 | 0.00300598144531250 | 234 | 0.00077819824218750 | 0.01942443847656250 |
| 65 | 0.00000000000000000 | 0.00396728515625000 | 235 | 0.00134277343750000 | 0.02363586425781250 |
| 66 | 0.00381469726562500 | 0.00460815429687500 | 236 | 0.00161743164062500 | 0.02529907226562500 |
| 67 | 0.00744628906250000 | 0.00483703613281250 | 237 | 0.00161743164062500 | 0.02441406250000000 |
| 68 | 0.01025390625000000 | 0.00457763671875000 | 238 | 0.00138854980468750 | 0.02125549316406250 |
| 69 | 0.01168823242187500 | 0.00378417968750000 | 239 | 0.00097656250000000 | 0.01628112792968750 |
| 70 | 0.01136779785156250 | 0.00253295898437500 | 240 | 0.00048828125000000 | 0.01010131835937500 |
| 71 | 0.00915527343750000 | 0.00088500976562500 | 241 | 0.00000000000000000 | 0.00340270996093750 |
| 72 | 0.00520324707031250 | -0.00102233886718750 | 242 | -0.00041198730468750 | -0.00314331054687500 |
| 73 | 0.00000000000000000 | -0.00299072265625000 | 243 | -0.00070190429687500 | -0.00891113281250000 |
| 74 | -0.00573730468750000 | -0.00483703613281250 | 244 | -0.00085449218750000 | -0.01341247558593750 |
| 75 | -0.01113891601562500 | -0.00636291503906250 | 245 | -0.00085449218750000 | -0.01632690429687500 |
| 76 | -0.01530456542968750 | -0.00736999511718750 | 246 | -0.00070190429687500 | -0.01744079589843750 |
| 77 | -0.01739501953125000 | -0.00769042968750000 | 247 | -0.00048828125000000 | -0.01679992675781250 |
| 78 | -0.01683044433593750 | -0.00723266601562500 | 248 | -0.00022888183593750 | -0.01458740234375000 |
| 79 | -0.01348876953125000 | -0.00598144531250000 | 249 | 0.00000000000000000 | -0.01113891601562500 |
| 80 | -0.00765991210937500 | -0.00398254394531250 | 250 | 0.00019836425781250 | -0.00689697265625000 |

16-Bit, 5.9Gsps Interpolating and
Modulating RF DAC with JESD204B Interface

## Table 4. Digital Filter Coefficients for 8x and 10x Interpolation Ratios (continued)

| TAPS | FILTER 8x | FILTER 10x | TAPS | FILTER 8x | FILTER 10x |
|---|---|---|---|---|---|
| 81 | 0.00000000000000000 | -0.00141906738281250 | 251 | 0.00033569335937500 | -0.00231933593750000 |
| 82 | 0.00842285156250000 | 0.00152587890625000 | 252 | 0.00039672851562500 | 0.00215148925781250 |
| 83 | 0.01629638671875000 | 0.00459289550781250 | 253 | 0.00039672851562500 | 0.00607299804687500 |
| 84 | 0.02227783203125000 | 0.00746154785156250 | 254 | 0.00033569335937500 | 0.00909423828125000 |
| 85 | 0.02523803710937500 | 0.00978088378906250 | 255 | 0.00024414062500000 | 0.01103210449218750 |
| 86 | 0.02439880371093750 | 0.01127624511718750 | 256 | 0.00012207031250000 | 0.01174926757812500 |
| 87 | 0.01953125000000000 | 0.01174926757812500 | 257 | 0.00000000000000000 | 0.01127624511718750 |
| 88 | 0.01106262207031250 | 0.01103210449218750 | 258 | -0.00006103515625000 | 0.00976562500000000 |
| 89 | 0.00000000000000000 | 0.00910949707031250 | 259 | -0.00012207031250000 | 0.00744628906250000 |
| 90 | -0.01211547851562500 | 0.00607299804687500 | 260 | -0.00016784667968750 | 0.00460815429687500 |
| 91 | -0.02340698242187500 | 0.00215148925781250 | 261 | -0.00018310546875000 | 0.00154113769531250 |
| 92 | -0.03198242187500000 | -0.00230407714843750 | 262 | -0.00013732910156250 | -0.00141906738281250 |
| 93 | -0.03619384765625000 | -0.00689697265625000 | 263 | -0.00006103515625000 | -0.00399780273437500 |
| 94 | -0.03494262695312500 | -0.01113891601562500 | 264 | -0.00003051757812500 | -0.00596618652343750 |
| 95 | -0.02795410156250000 | -0.01458740234375000 | 265 | 0.00000000000000000 | -0.00720214843750000 |
| 96 | -0.01580810546875000 | -0.01679992675781250 | 266 | 0.00003051757812500 | -0.00765991210937500 |
| 97 | 0.00000000000000000 | -0.01744079589843750 | 267 | 0.00006103515625000 | -0.00733947753906250 |
| 98 | 0.01730346679687500 | -0.01631164550781250 | 268 | 0.00007629394531250 | -0.00634765625000000 |
| 99 | 0.03344726562500000 | -0.01341247558593750 | 269 | 0.00006103515625000 | -0.00482177734375000 |
| 100 | 0.04571533203125000 | -0.00889587402343750 | 270 | 0.00004577636718750 | -0.00297546386718750 |
| 101 | 0.05175781250000000 | -0.00312805175781250 | 271 | 0.00003051757812500 | -0.00100708007812500 |
| 102 | 0.05004882812500000 | 0.00340270996093750 | 272 | 0.00001525878906250 | 0.00090026855468750 |
| 103 | 0.04010009765625000 | 0.01010131835937500 | 273 | 0.00000000000000000 | 0.00254821777343750 |
| 104 | 0.02273559570312500 | 0.01628112792968750 | 274 | | 0.00379943847656250 |
| 105 | 0.00000000000000000 | 0.02127075195312500 | 275 | | 0.00456237792968750 |
| 106 | -0.02496337890625000 | 0.02442932128906250 | 276 | | 0.00482177734375000 |
| 107 | -0.04837036132812500 | 0.02529907226562500 | 277 | | 0.00460815429687500 |
| 108 | -0.06631469726562500 | 0.02363586425781250 | 278 | | 0.00396728515625000 |
| 109 | -0.07537841796875000 | 0.01942443847656250 | 279 | | 0.00300598144531250 |
| 110 | -0.07318115234375000 | 0.01289367675781250 | 280 | | 0.00183105468750000 |
| 111 | -0.05892944335937500 | 0.00454711914062500 | 281 | | 0.00059509277343750 |
| 112 | -0.03358459472656250 | -0.00488281250000000 | 282 | | -0.00056457519531250 |
| 113 | 0.00000000000000000 | -0.01452636718750000 | 283 | | -0.00155639648437500 |
| 114 | 0.03735351562500000 | -0.02339172363281250 | 284 | | -0.00230407714843750 |
| 115 | 0.07293701171875000 | -0.03050231933593750 | 285 | | -0.00274658203125000 |
| 116 | 0.10086059570312500 | -0.03501892089843750 | 286 | | -0.00289916992187500 |
| 117 | 0.11575317382812500 | -0.03625488281250000 | 287 | | -0.00274658203125000 |
| 118 | 0.11360168457031200 | -0.03385925292968750 | 288 | | -0.00234985351562500 |
| 119 | 0.09259033203125000 | -0.02781677246093750 | 289 | | -0.00177001953125000 |

## Table 4. Digital Filter Coefficients for 8x and 10x Interpolation Ratios (continued)

| TAPS | FILTER 8x | FILTER 10x | TAPS | FILTER 8x | FILTER 10x |
|------|-----------|------------|------|-----------|------------|
| 120 | 0.05349731445312500 | -0.01846313476562500 | 290 | | -0.00108337402343750 |
| 121 | 0.00000000000000000 | -0.00651550292968750 | 291 | | -0.00036621093750000 |
| 122 | -0.06158447265625000 | 0.00698852539062500 | 292 | | 0.00032043457031250 |
| 123 | -0.12277221679687500 | 0.02076721191406250 | 293 | | 0.00091552734375000 |
| 124 | -0.17385864257812500 | 0.03343200683593750 | 294 | | 0.00134277343750000 |
| 125 | -0.20507812500000000 | 0.04360961914062500 | 295 | | 0.00158691406250000 |
| 126 | -0.20782470703125000 | 0.05007934570312500 | 296 | | 0.00164794921875000 |
| 127 | -0.17584228515625000 | 0.05187988281250000 | 297 | | 0.00154113769531250 |
| 128 | -0.10620117187500000 | 0.04849243164062500 | 298 | | 0.00131225585937500 |
| 129 | 0.00000000000000000 | 0.03987121582031250 | 299 | | 0.00097656250000000 |
| 130 | 0.13760375976562500 | 0.02648925781250000 | 300 | | 0.00059509277343750 |
| 131 | 0.29754638671875000 | 0.00936889648437500 | 301 | | 0.00018310546875000 |
| 132 | 0.46774291992187500 | -0.01005554199218750 | 302 | | -0.00018310546875000 |
| 133 | 0.63421630859375000 | -0.02996826171875000 | 303 | | -0.00048828125000000 |
| 134 | 0.78253173828125000 | -0.04838562011718750 | 304 | | -0.00070190429687500 |
| 135 | 0.89944458007812500 | -0.06327819824218750 | 305 | | -0.00082397460937500 |
| 136 | 0.97422790527343700 | -0.07286071777343750 | 306 | | -0.00086975097656250 |
| 137 | 0.99996948242187500 | -0.07571411132812500 | 307 | | -0.00079345703125000 |
| 138 | 0.97422790527343700 | -0.07101440429687500 | 308 | | -0.00067138671875000 |
| 139 | 0.89944458007812500 | -0.05859375000000000 | 309 | | -0.00048828125000000 |
| 140 | 0.78253173828125000 | -0.03907775878906250 | 310 | | -0.00028991699218750 |
| 141 | 0.63421630859375000 | -0.01385498046875000 | 311 | | -0.00009155273437500 |
| 142 | 0.46774291992187500 | 0.01502990722656250 | 312 | | 0.00009155273437500 |
| 143 | 0.29754638671875000 | 0.04498291015625000 | 313 | | 0.00022888183593750 |
| 144 | 0.13760375976562500 | 0.07301330566406250 | 314 | | 0.00032043457031250 |
| 145 | 0.00000000000000000 | 0.09613037109375000 | 315 | | 0.00038146972656250 |
| 146 | -0.10620117187500000 | 0.11149597167968700 | 316 | | 0.00039672851562500 |
| 147 | -0.17584228515625000 | 0.11682128906250000 | 317 | | 0.00038146972656250 |
| 148 | -0.20782470703125000 | 0.11056518554687500 | 318 | | 0.00032043457031250 |
| 149 | -0.20507812500000000 | 0.09213256835937500 | 319 | | 0.00024414062500000 |
| 150 | -0.17385864257812500 | 0.06210327148437500 | 320 | | 0.00015258789062500 |
| 151 | -0.12277221679687500 | 0.02223205566406250 | 321 | | 0.00006103515625000 |
| 152 | -0.06158447265625000 | -0.02462768554687500 | 322 | | -0.00001525878906250 |
| 153 | 0.00000000000000000 | -0.07464599609375000 | 323 | | -0.00009155273437500 |
| 154 | 0.05349731445312500 | -0.12318420410156200 | 324 | | -0.00013732910156250 |
| 155 | 0.09259033203125000 | -0.16522216796875000 | 325 | | -0.00016784667968750 |
| 156 | 0.11360168457031200 | -0.19572448730468700 | 326 | | -0.00016784667968750 |
| 157 | 0.11575317382812500 | -0.21005249023437500 | 327 | | -0.00015258789062500 |
| 158 | 0.10086059570312500 | -0.20428466796875000 | 328 | | -0.00012207031250000 |

## Table 4. Digital Filter Coefficients for 8x and 10x Interpolation Ratios (continued)

| TAPS | FILTER 8x | FILTER 10x | TAPS | FILTER 8x | FILTER 10x |
|------|-----------|------------|------|-----------|------------|
| 159 | 0.07293701171875000 | -0.17565917968750000 | 329 | | -0.00007629394531250 |
| 160 | 0.03735351562500000 | -0.12292480468750000 | 330 | | -0.00003051757812500 |
| 161 | 0.00000000000000000 | -0.04637145996093750 | 331 | | 0.00000000000000000 |
| 162 | -0.03358459472656250 | 0.05195617675781250 | 332 | | 0.00001525878906250 |
| 163 | -0.05892944335937500 | 0.16836547851562500 | 333 | | 0.00003051757812500 |
| 164 | -0.07318115234375000 | 0.29769897460937500 | 334 | | 0.00004577636718750 |
| 165 | -0.07537841796875000 | 0.43363952636718700 | 335 | | 0.00006103515625000 |
| 166 | -0.06631469726562500 | 0.56903076171875000 | 336 | | 0.00006103515625000 |
| 167 | -0.04837036132812500 | 0.69642639160156200 | 337 | | 0.00006103515625000 |
| 168 | -0.02496337890625000 | 0.80863952636718700 | 338 | | 0.00004577636718750 |
| 169 | 0.00000000000000000 | 0.89920043945312500 | 339 | | 0.00003051757812500 |
| 170 | 0.02273559570312500 | 0.96275329589843700 | 340 | | 0.00001525878906250 |
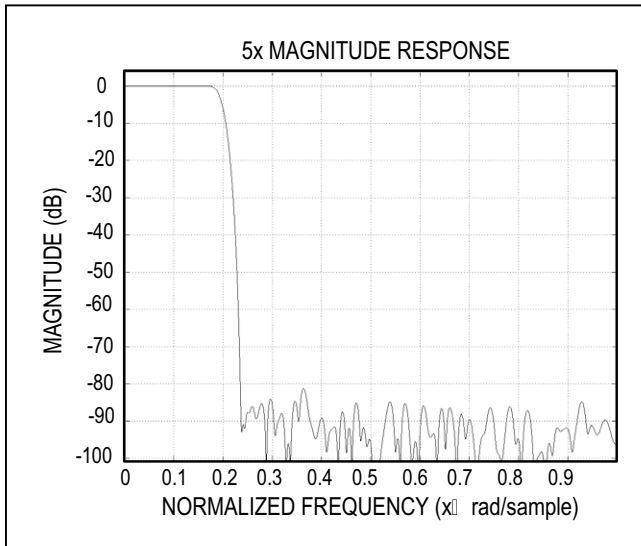


Figure 30. 5x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
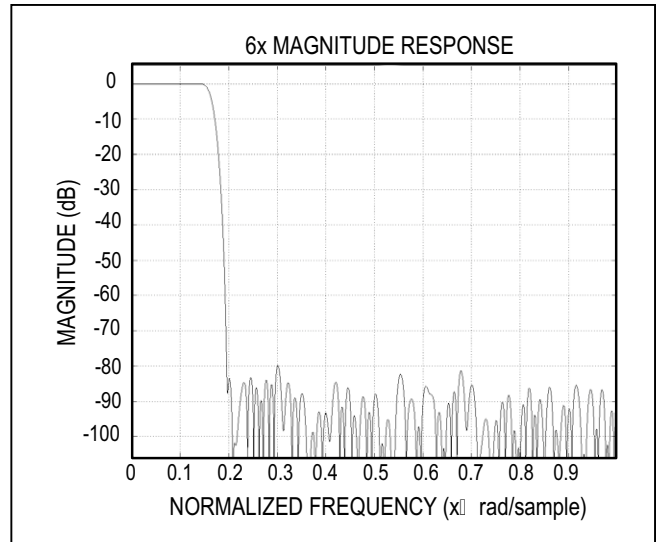


Figure 31. 6x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
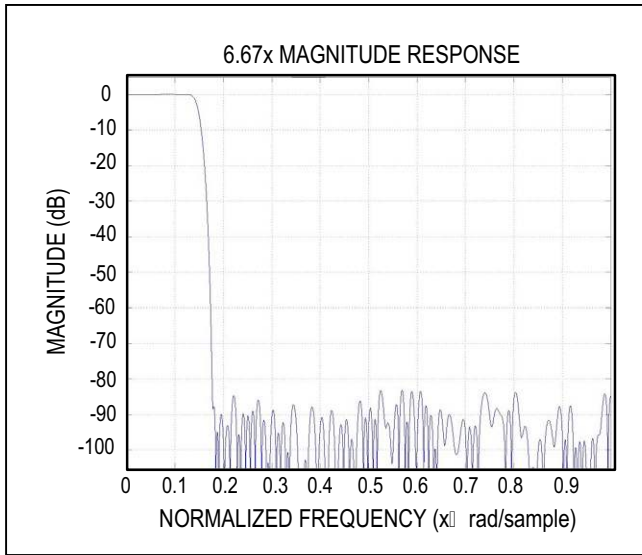
Figure 32. 6.67x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
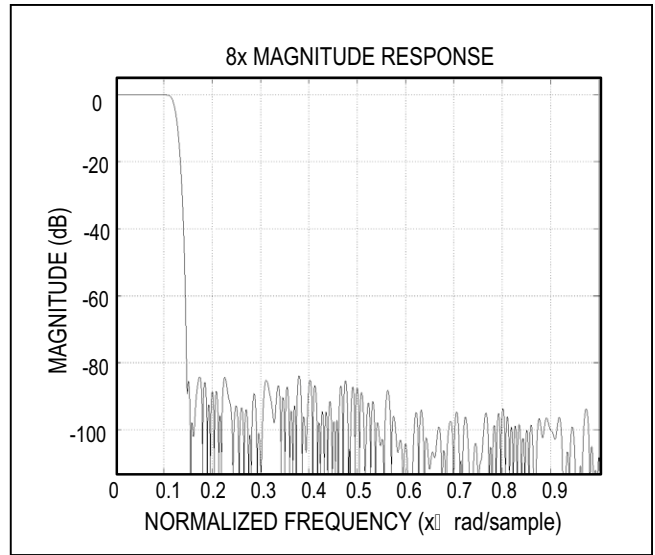


Figure 33. 8x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
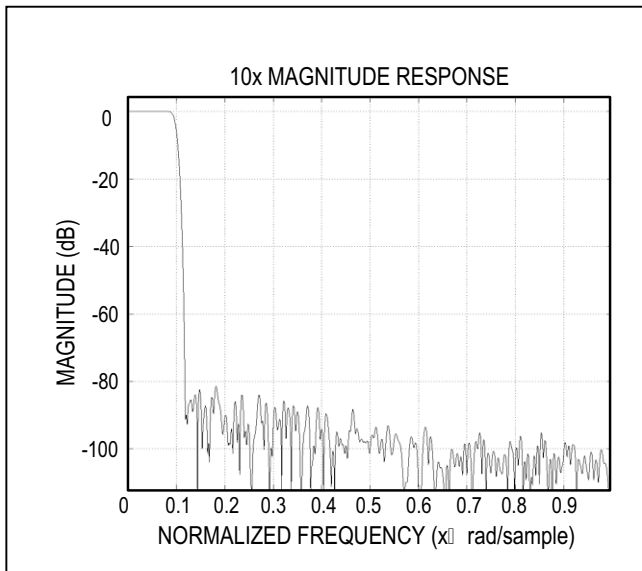


Figure 34. 10x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
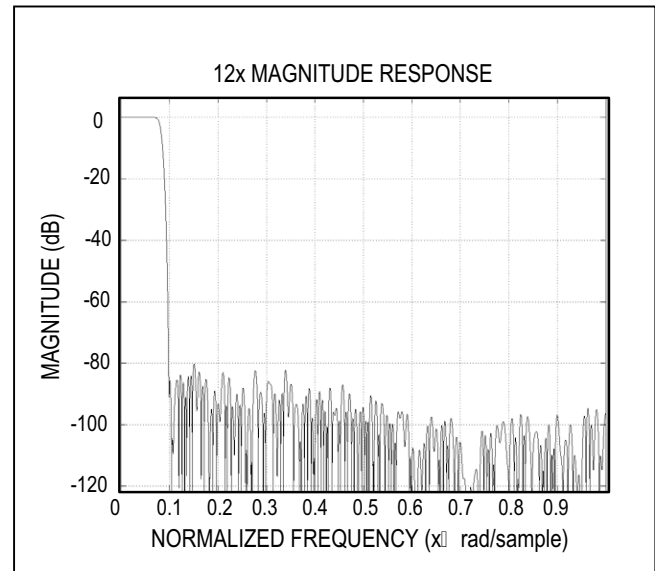


Figure 35. 12x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
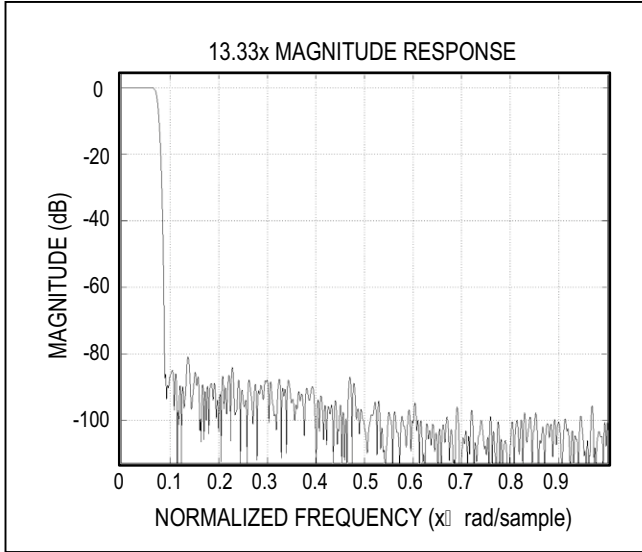
Figure 36. 13.33x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
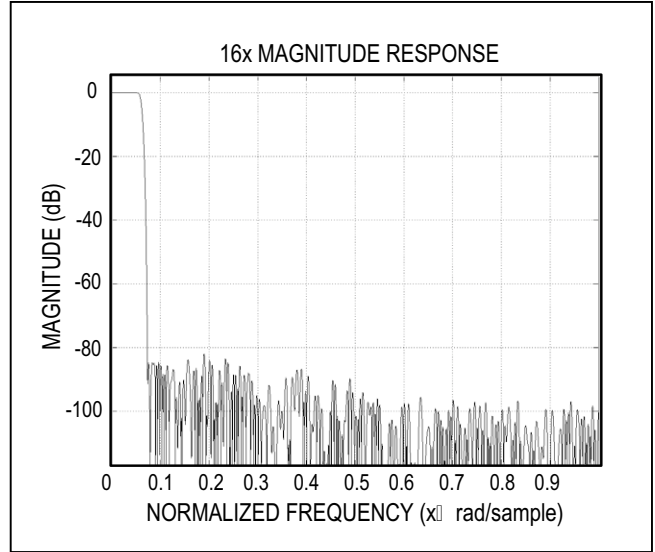


Figure 37. 16x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
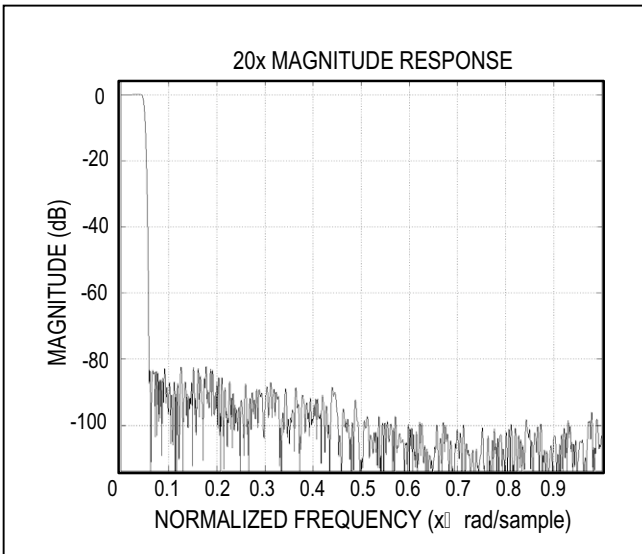


Figure 38. 20x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate
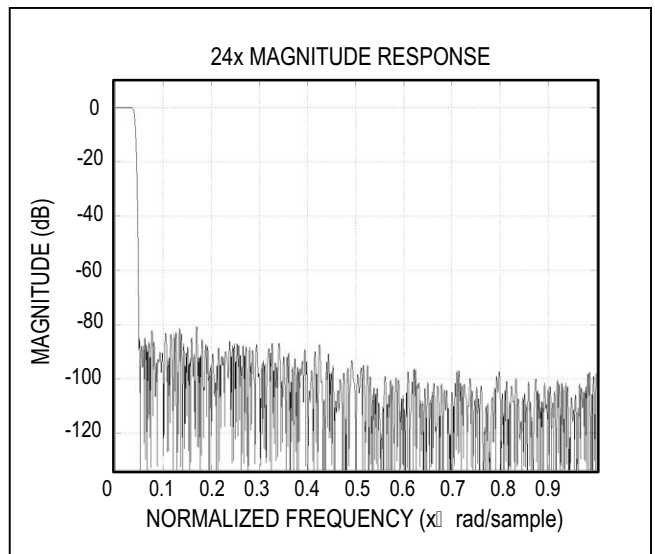


Figure 39. 24x Filter Baseband Frequency Response
Normalized to DAC Output Update Rate

## Register Definition and Description

There are four banks of configuration registers in the MAX5871, which can be configured through SPI serial control interface.

### Configuration Register Banks

#### 1) Global Configuration Registers – GLB

This register bank configures SPI serial control interface, device information.

#### 2) DSP and DAC Configuration Registers – DSP

This register bank configures the MAX5871 chip operation, DSP engine, NCO, DAC operation, interruption and status, DAC PLL operation.

#### 3) Link Layer Configuration Registers for JESD204B – LNK

This register bank configures the JESD204B link layer on the serial data interface lanes, operation, and synchronization.

#### 4) SerDes Configuration Registers for JESD204B – SER

This register bank configures the JESD204B SerDes physical layer on the serial data interface lanes, operation, and synchronization.

### Register Bank Name, Bytes, Type, Address and Description

(**Note:** Do not write to registers with addresses not listed in the table below. Register addresses not listed are reserved for factory use.)

| REGISTER NAME | BYTES | TYPE | ADDRESS DECIMAL | DESCRIPTION |
|---|---|---|---|---|
| **Global Configuration Registers–GLB** | | | | |
| CfgIFA | 1 | RW | 0 | Configure Interface A |
| CfgIFB | 1 | RW | 1 | Configure Interface B |
| CfgDev | 1 | RW | 2 | Device Configuration |
| ChipType | 1 | R | 3 | Chip Type Status |
| VendorID | 2 | R | 12 | Vendor ID |
| CfgIFC | 1 | RW | 15 | Configure Interface C |
| CfgDACrate | 1 | RW | 16 | Configure DAC Update Rate |
| CfgCLKrate | 1 | RW | 17 | Configure CLKP/N Input Rate |
| CfgREGS | 1 | RW | 18 | Configure Register Options |
| **DSP and DAC Configuration Registers–DSP** | | | | |
| CfgChipOM | 1 | RW | 256 | Configure Chip Operation Mode |
| CfgDSP | 1 | RW | 257 | Configure DSP Engine |
| CfgNCOF | 4 | RW | 258 | Configure NCO Frequency Control Word for DAC DSP |
| CfgNCON | 3 | RW | 262 | Configure NCO Frequency Control Word Numerator Word for DAC DSP |
| CfgNCOD | 3 | RW | 265 | Configure NCO Frequency Control Word Denominator Word for DAC DSP |
| CfgNCOU | 1 | RW | 268 | Configure NCO Update for DAC DSP |
| CfgNCOUS | 3 | RW | 269 | Configure NCO Step Size for DAC DSP |
| CfgPM | 1 | RW | 272 | Configure Power Monitor for DAC DSP |
| CfgPMT | 1 | RW | 273 | Configure Power Monitor Threshold for DAC DSP |
| CfgPMIC | 6 | RW | 274 | Configure Power Monitor Init Count 6x8=48 Bits for DAC DSP |

| REGISTER NAME | BYTES | TYPE | ADDRESS DECIMAL | DESCRIPTION |
|---|---|---|---|---|
| StatPM | 2 | R | 280 | Power Monitor Status for DAC DSP |
| CfgSync | 1 | RW | 346 | Configure Multi-DAC Synchronization for DAC DSP |
| CfgFIFO | 1 | RW | 347 | Configure Input FIFO for DAC |
| EMUTE | 1 | RW | 354 | Mute Enable Mask for DAC |
| EINT | 1 | RW | 355 | Interrupt Enable Mask for DAC DSP |
| STATUS | 1 | R | 356 | Status Register for DAC DSP |
| iFIFOLevel | 1 | R | 357 | Input FIFO Level for DAC |
| DieSN | 3 | R | 358 | MAX5871 RF DAC Serial Number. Total 8x3 = 24 Bits |
| CfgPLL | 3 | RW | 384 | Configure DAC PLL |
| StatPLL | 2 | R | 387 | DAC PLL Status |
| **Link Layer Configuration Registers for JESD204B–LNK** | | | | |
| CfgSRst | 1 | RW | 1024 | Configure Soft Reset |
| CfgLnRst | 1 | RW | 1025 | Configure Lane Reset |
| CfgLinkSet | 1 | RW | 1026 | Configure Link Settings |
| CfgSYSREF | 1 | RW | 1027 | Configure SYSREF Signal |
| CfgSTHRSH | 1 | RW | 1028 | Configure SYSREF Threshold |
| CfgSIGN | 1 | RW | 1029 | Configure SYSREF Ignore Count |
| CfgSVLD | 1 | RW | 1030 | Configure SYSREF Valid Count |
| CfgSYNCN | 1 | RW | 1031 | Configure SYNCN pin options |
| CfgSAC | 1 | RW | 1032 | Configure SYNCN assert frame count |
| CfgSDC | 1 | RW | 1033 | Configure SYNCN deassert frame count |
| CfgLinkMLFS | 1 | RW | 1034 | Configure Link for M, L, F and S |
| CfgLinkK | 1 | RW | 1035 | Configure Link Multiframe Length |
| CfgBID | 1 | RW | 1036 | Configure Bank ID |
| CfgDID | 1 | RW | 1037 | Configure Device ID |
| CfgLID | 4 | RW | 1038 | Configure Lane N ID |
| CfgLinkSrc | 1 | RW | 1042 | Configure Link Signal Source |
| CfgClkInv | 1 | RW | 1043 | Configure Lane Clock Inversion |
| CfgLinkCtl | 1 | RW | 1044 | Configure Link Control |
| CfgBOff | 2 | RW | 1045 | Configure Manual Code Group Synch Bit Offsets |
| CfgRstCnt | 1 | RW | 1047 | Configure SYSREF Reset Counts |
| CfgILALck | 1 | RW | 1048 | Configure ILA Lock Configuration |
| CfgILAC | 1 | RW | 1049 | Configure ILA Control |
| CfgILAD | 1 | RW | 1050 | Configure ILA Delay Control |
| CfgILAM | 4 | RW | 1051 | Configure Lane N Manual ILA Delay |
| CfgILAmfs | 2 | RW | 1055 | Configure ILA Multiframe start |
| CfgILAsn | 2 | RW | 1057 | Configure ILA Sequence Number |
| CfgLerrM | 2 | RW | 1059 | Configure Error Mask for Reporting on SYNCN |
| CfgSerrM | 2 | RW | 1061 | Configure Error Mask for Resync Request on SYNCN |
| CfgMDS | 2 | RW | 1063 | Configure Multi-DAC Synchronization |

| REGISTER NAME | BYTES | TYPE | ADDRESS DECIMAL | DESCRIPTION |
|---|---|---|---|---|
| CfgINV | 1 | RW | 1065 | Configure Data Inversion |
| CfgLnSrc | 2 | RW | 1066 | Configure Lane Source |
| CfgLnEn | 1 | RW | 1068 | Configure Lane Enable |
| CfgFIFO | 2 | RW | 1069 | Configure FIFO Depths |
| CfgRepl | 1 | RW | 1071 | Configure Sample Replacement on NIT Error |
| CfgSamTest | 1 | RW | 1072 | Configure Sample Interface Test |
| CfgSTPc1s1 | 2 | RW | 1073 | Configure Short Test Pattern for Converter 1, Sample 1 |
| CfgSTPc1s2 | 2 | RW | 1075 | Configure Short Test Pattern for Converter 1, Sample 2 |
| CfgSTPc2s1 | 2 | RW | 1077 | Configure Short Test Pattern for Converter 2, Sample 1 |
| CfgSTPc2s2 | 2 | RW | 1079 | Configure Short Test Pattern for Converter 2, Sample 2 |
| CfgCnt | 1 | RW | 1280 | Configure Counter Settings |
| CfgCntSel | 1 | RW | 1281 | Configure Counter Selects |
| EIntLane | 4 | RW | 1283 | Lane N Interrupt Enable |
| EIntFIFO | 4 | RW | 1287 | Lane N FIFO Interrupt Enable |
| EIntILAS | 4 | RW | 1291 | Lane N ILA Sequence Interrupt Enable |
| EIntILA | 1 | RW | 1295 | Initial Lane Alignment Interrupt Enable |
| EIntLink | 1 | RW | 1296 | Link Interrupt Enable |
| EMuteLane | 4 | RW | 1297 | Lane N Mute Enable |
| EMuteFIFO | 4 | RW | 1301 | Lane N FIFO Mute Enable |
| EMuteILAS | 4 | RW | 1305 | Lane N ILA Sequence Mute Enable |
| EMuteILA | 1 | RW | 1309 | Initial Lane Alignment Mute Enable |
| EMuteLink | 1 | RW | 1310 | Link Mute Enable |
| StatLane | 4 | R | 1408 | Lane N Status |
| StatFIFO | 4 | R | 1412 | Lane N FIFO Status |
| StatILAS | 4 | R | 1416 | Lane N ILA Sequence Status |
| StatILA | 1 | R | 1420 | Initial Lane Alignment Status |
| StatLink | 1 | R | 1421 | Link Status |
| CntInvld | 2 | R | 1422 | Counter for Invalid Errors |
| CntDbg | 2 | R | 1424 | Counter for Lane Debug |
| **SERDES Configuration Registers for JESD204B–SER** | | | | |
| CfgRst | 1 | RW | 1536 | Configure Reset for All Lanes |
| CfgRate | 1 | RW | 1542 | Configure Rate for All Lanes |
| CfgTrainLnN | 4 | RW | 1543 | Configure Training for Lane N |
| CfgMisc | 1 | RW | 1547 | Configure Miscellaneous for All Lanes |
| EIntLnN | 4 | RW | 1600 | SerDes Phy Logic Interrupt Enable for Lane N |
| EMuteLnN | 4 | RW | 1604 | SerDes Phy Logic DAC Mute Enable for Lane N |
| StatusLnN | 4 | R | 1608 | SerDes Phy Logic Status for Lane N |
| CfgCMU | 8 | RW | 1792 | Configure CMU |

**Note:** In the following *Register Definition and Description* sections, register and register bit marked with asterisk "*" indicates that it needs GLB.CfgIFC.Xfer writing a 1 to transfer the register content into active registers to take effect, when GLB.CfgREGS.ActSel = 1.

## Global Configuration Registers Definition and Description

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0000 | 1 | CfgIFA | Configure Interface A | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | SftRst | LSBF | AddIncr | 4Wire | 4Wire | AddIncr | LSBF | SftRst |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | SftRst Writing a 1 to this bit resets all of the digital logic except address 0x0000, 0x0001, and SPI interface. This bit is self-clearing. | | | | | | | |
| | | | | LSBF<br>0 = MSB first for SPI interface input control/data and output data<br>1 = LSB first for SPI interface input control/data and output data | | | | | | | |
| | | | | AddIncr<br>0 = Decrement address for SPI streaming mode<br>1 = Increment address for SPI streaming mode | | | | | | | |
| | | | | 4Wire<br>0 = 3-Wire SPI mode, SDIO used for both input and output<br>1 = 4-Wire SPI mode, SDIO is input and SDO is output | | | | | | | |
| | | | Note | Bits[3:0] are mirrored in Bits[4:7], both low and high bits need to be written to the same value | | | | | | | |
| | | | | | | | | | | | |
| 0x0001 | 1 | CfgIFB | Configure Interface B | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | StrmDis | Res | RdReg | Res | Reserved | X | X | Res |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | StrmDis<br>0 = SPI streaming mode is enabled<br>1 = SPI streaming mode is disabled and continued CSB assertion forces instruction-data format | | | | | | | |
| | | | | RdReg<br>0 = Register read back from active registers<br>1 = Register read back from buffer registers<br>For fields that are not implemented with active/buffer registers, this bit has no effect. | | | | | | | |
| | | | | | | | | | | | |
| 0x0002 | 1 | CfgDev | Device Configuration | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | Res | Res | Res | Res | Res | CDrst* | PDM1 | PDM0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | PDM[1:0]<br>00 = Normal operation mode<br>01 = Reserved<br>10 = Reserved<br>11 = Sleep mode with lowest power dissipation with chip inactivity except SPI interfaceCDrst<br> 0 = Clock Divider is not reset<br> 1 = Clock Divider is reset | | | | | | | |

## Global Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0003 | 1 | ChipType | Chip Type Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | Type3 | Type2 | Type1 | Type0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | Definition | Type[3:0]<br>Read-only field indicating high-speed DAC | | | | | | | |
| 0x000C | 2 | VendorID | Maxim Integrated ID | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | VID15 | VID14 | VID13 | VID12 | VID11 | VID10 | VID9 | VID8 |
| | | | Default | 16'h0B6A | | | | | | | |
| | | | Definition | Read-only Maxim Integrated ID | | | | | | | |
| 0x000F | 1 | CfgIFC | Configure Interface C | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | X | X | Xfer |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | Xfer<br>Writing a 1 transfers the buffer registers to active registers. This bit is self-clearing.<br>**Note:** After the internal configuration is complete, DSP.STATUS.TRDY status is set | | | | | | | |
| 0x0010 | 1 | CfgDACrate | Configure DAC Update Rate | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | Drate3 | Drate2 | Drate1 | Drate0 |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| | | | Definition | Drate[3:0]    DAC rate<br>0000 = 2211.8MHz      0111 = 4096.0MHz<br>0001 = 2457.6MHz      1000 = 4423.7MHz<br>0010 = 2949.1MHz      1001 = 4915.2MHz<br>0011 = 3072.0MHz      1010 = 5898.2MHz<br>0100 = 3276.8MHz      1011 = 6144.0MHz<br>0101 = 3686.4MHz      1100–1111 = Reserved<br>0110 = 3932.2MHz | | | | | | | |

## Global Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0011 | 1 | CfgCLKrate | Configure CLKP/N Input Rate | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | Crate3 | Crate2 | Crate1 | Crate0 |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | | | Definition | Crate[3:0]    CLKP/N rate<br><br>0000 = 2211.8MHz          1000 = 4423.7MHz<br>0001 = 2457.6MHz          1001 = 4915.2MHz<br>0010 = 2949.1MHz          1010 = 5898.2MHz<br>0011 = 3072.0MHz          1011 = 6144.0MHz<br>0100 = 3276.8MHz          1100 = 983.04MHz<br>0101 = 3686.4MHz          1101 = 1228.8MHz<br>0110 = 3932.2MHz          1110 = 1474.56MHz<br>0111 = 4096.0MHz          1111 = Reserved | | | | | | | |
| 0x0012 | 1 | CfgREGS | Configure Register options | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | X | ActSel | IntCfg |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ActSel<br>0 = Buffer register output is used<br>1 = Active register output is used for registers that are updated with CfgIFC.Xfer bitIntCfg<br>0 = Internal register configuration is disabled<br>1 = When CfgIFC.Xfer bit is set, some JESD204B registers are configured internally.<br>(After internal configuration is complete, the DSP.STATUS.TRDY latched status is set.)<br>Contact the chip manufacturer for more details if this function is needed. | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0100 | 1 | CfgChipOM | Configure Chip Operation Mode | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | Reserved2 | RclkM1 | RclkM0 | INVQ* | Reserved1 | Mute | Reserved0 | DFMT* |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | Definition | Reserved2<br>Reserved – Do not write | | | | | | | |
| | | | | RclkM[1:0]<br>00 = RCLK output is DAC clock divided by (interpolation ratio x 1)<br>01 = RCLK output is DAC clock divided by (interpolation ratio x 2)<br>10 = RCLK output is DAC clock divided by (interpolation ratio x 4)<br>11 = Reserved | | | | | | | |
| | | | | INVQ<br>0 = Disable DAC I-Q data Q being inverted to make I-Q (default)<br>1 = Enable DAC I-Q data Q being inverted to make I+Q | | | | | | | |
| | | | | Reserved1<br>Reserved – Do not write | | | | | | | |
| | | | | Mute<br>0 = DAC in normal mode<br>1 = Enable DAC mute | | | | | | | |
| | | | | Reserved0<br>Reserved – Do not write | | | | | | | |
| | | | | DFMT<br>0 = DAC Input data in two's complement format<br>1 = DAC Input data in offset binary format | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0101 | 1 | CfgDSP | Configure DSP Engine | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | R3* | R2* | R1* | R0* | RstDSP | RstFIFO | NCOE* | NCOLD |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | R[3:0]<br>1001 = DSP interpolation mode is 5x<br>1010 = DSP interpolation mode is 6x<br>1011 = DSP interpolation mode is 8x<br>0000 = DSP interpolation mode is 10x<br>1100 = DSP interpolation mode is 12x<br><br>1101 = DSP interpolation mode is 16x<br>1110 = DSP interpolation mode is 20x<br>1111 = DSP interpolation mode is 24x<br>0010 = DSP interpolation mode is 20/3x<br>0011 = DSP interpolation mode is 40/3x<br>0001, 0100 - 1000 = Reserved | | | | | | | |
| | | | RstDSP<br>0 = No reset<br>1 = Reset DSP (Input FIFO, interpolation filters, complex modulator and NCO) | | | | | | | |
| | | | RstFIFO<br>0 = No reset<br>1 = Reset input data FIFO | | | | | | | |
| | | | NCOE<br>0 = Disable Extended NCO mode for DAC<br>1 = Enable Extended NCO mode using the fractional NCO control words in CfgNCON and CfgNCOD | | | | | | | |
| | | | NCOLD<br>Writing a 1 loads NCO frequency control words to the DSP, this bit is self-clearing<br>The NCO frequency control words are also loaded when GLBL.CfgIFC.Xfer bit is set to 1 | | | | | | | |
| 0x0102 | 4 | CfgNCOF* | Configure NCO Frequency Control Word for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | FCW7 | FCW6 | FCW5 | FCW4 | FCW3 | FCW2 | FCW1 | FCW0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | FCW15 | FCW14 | FCW13 | FCW12 | FCW11 | FCW10 | FCW9 | FCW8 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | FCW23 | FCW22 | FCW21 | FCW20 | FCW19 | FCW18 | FCW17 | FCW16 |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | FCW31 | FCW30 | FCW29 | FCW28 | FCW27 | FCW26 | FCW25 | FCW24 |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | FCW[31:0]<br>NCO Frequency Control Word | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0106 | 3 | CfgNCON* | Configure NCO Frequency Control Word Numerator Word for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | NFW7 | NFW6 | NFW5 | NFW4 | NFW3 | NFW2 | NFW1 | NFW0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | NFW15 | NFW14 | NFW13 | NFW12 | NFW11 | NFW10 | NFW9 | NFW8 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | X | X | X | NFW17 | NFW16 |
| | | | Default | 0x000000 | | | | | | | |
| | | | Definition | NFW[17:0]<br>Numerator word of the Extended NCO Frequency Control Word | | | | | | | |
| 0x0109 | 3 | CfgNCOD* | Configure NCO Frequency Control Word Denominator Word for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | DFW7 | DFW6 | DFW5 | DFW4 | DFW3 | DFW2 | DFW1 | DFW0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | DFW15 | DFW14 | DFW13 | DFW12 | DFW11 | DFW10 | DFW9 | DFW8 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | X | X | DFW18 | DFW17 | DFW16 |
| | | | Default | 0x000000 | | | | | | | |
| | | | Definition | DFW[18:0]<br>Denominator word of the Extended NCO Frequency Control Word | | | | | | | |
| 0x010C | 1 | CfgNCOU | Configure NCO Update for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | Reserved | Reserved | Reserved | Reserved | RLM1 | Reserved |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | RLM1<br>0 = Load immediately with no glitch control<br>1 = Use step increment/decrement mode for a slow change in NCO phase towards the new frequency | | | | | | | |
| 0x010D | 3 | CfgNCOUS | Configure NCO Step Size for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | TIM7 | TIM6 | TIM5 | TIM4 | TIM3 | TIM2 | TIM1 | TIM0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | TIM15 | TIM14 | TIM13 | TIM12 | TIM11 | TIM10 | TIM9 | TIM8 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | TIM23 | TIM22 | TIM21 | TIM20 | TIM19 | TIM18 | TIM17 | TIM16 |
| | | | Default | 0x000000 | | | | | | | |
| | | | Definition | TIM[23:0]<br>NCO Step Size in DAC Clock /8 clock cycles when CfgNCOU.RLM1=1 | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0110 | 1 | CfgPM | Configure Power Monitor for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | Start | Mode | Reset |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | Start<br>0 = Power Monitor Stop<br>1 = Power Monitor Start | | | | | | | |
| | | | | Mode<br>0 = Count samples below the threshold<br>1 = Count samples above the threshold | | | | | | | |
| | | | | Reset<br>Writing a 1 resets the power monitor count, this bit is self-clearing | | | | | | | |
| 0x0111 | 1 | CfgPMT | Configure Power Monitor Threshold for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | PMT7 | PMT6 | PMT5 | PMT4 | PMT3 | PMT2 | PMT1 | PMT0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | PMT[7:0]<br>Power Monitor Threshold | | | | | | | |
| 0x0112 | 6 | CfgPMIC | Configure Power Monitor Initial Count for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | PMIC7 | PMIC6 | PMIC5 | PMIC4 | PMIC3 | PMIC2 | PMIC1 | PMIC0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | PMIC15 | PMIC14 | PMIC13 | PMIC12 | PMIC11 | PMIC10 | PMIC9 | PMIC8 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | PMIC23 | PMIC22 | PMIC21 | PMIC20 | PMIC19 | PMIC18 | PMIC17 | PMIC16 |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | PMIC31 | PMIC30 | PMIC29 | PMIC28 | PMIC27 | PMIC26 | PMIC25 | PMIC24 |
| | | | Bit | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| | | | Name | PMIC39 | PMIC38 | PMIC37 | PMIC36 | PMIC35 | PMIC34 | PMIC33 | PMIC32 |
| | | | Bit | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 |
| | | | Name | PMIC47 | PMIC46 | PMIC45 | PMIC44 | PMIC43 | PMIC42 | PMIC41 | PMIC40 |
| | | | Default | 0x000000000000 | | | | | | | |
| | | | Definition | PMIC[47:0]<br>Power Monitor initial count | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0118 | 2 | StatPM | Power Monitor Status for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | PMST7 | PMST6 | PMST5 | PMST4 | PMST3 | PMST2 | PMST1 | PMST0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | PMDONE | X | X | X | PMST11 | PMST10 | PMST9 | PMST8 |
| | | | Default | 12'h000 | | | | | | | |
| | | | Definition | PMST[11:0]<br>Power Monitor Status indicating the threshold crossing count<br>PMDONE<br>1 = Power Monitor Status update done<br>0 = Power Monitor Status update in progress | | | | | | | |
| 0x015A | 1 | CfgSYNC | Configure multiple-DAC synchronization for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | DSP_ASync* | ClkDiv_Sync* | iFIFO_Sync* | NCO_Sync* | X | Reserved | OIF_dinc | OIF_ddec |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | DSP_ASync<br>0 = Disable Asynchronous SYSREF reset to the DSP<br>1 = Enable Asynchronous SYSREF reset to the DSP when there is no device cock to the JESD204B Link | | | | | | | |
| | | | | ClkDiv_Sync<br>When DSP_ASync = 0<br>0 = Disable synchronous SYSREF reset to the clock-divider block<br>1 = Enable synchronous SYSREF reset to the clock-divider block<br>When DSP_ASync = 1<br>0 = Enable first asynchronous SYSREF reset to the clock-divider block<br>1 = Enable continuous asynchronous SYSREF reset to the clock-divider block | | | | | | | |
| | | | | iFIFO_Sync<br>0 = Disable synchronous SYSREF reset to the input FIFO<br>1 = Enable synchronous SYSREF reset to the input FIFO | | | | | | | |
| | | | | NCO_Sync<br>0 = Disable synchronous SYSREF reset to the NCO<br>1 = Enable synchronous SYSREF reset to the NCO | | | | | | | |
| | | | | OIF_dinc<br>Writing a 1 increases the DSP latency by one DAC clock cycle, this bit is self-clearing | | | | | | | |
| | | | | OIF_ddec<br>Writing a 1 decreases the DSP latency by one DAC clock cycle, this bit is self-clearing | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x015B | 1 | CfgFIFO | Configure Input FIFO for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | RdPtrAdj3 | RdPtrAdj2 | RdP-trAdj1 | RdP-trAdj0 | Off | Dupl* | SwapIQ* | RevBi-tOrd* |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | RdPtrAdj[3:0]<br>0Adjust read pointer by adding this value to the free running read pointer | | | | | | | |
| | | | | Off<br>0 = Input FIFO is not bypassed<br>1 = Input FIFO is bypassed | | | | | | | |
| | | | | Dupl<br>0 = Do not duplicate I<br>1 = Duplicate I for Q | | | | | | | |
| | | | | SwapIQ<br>0 = Normal I/Q Order<br>1 = Reverse I/Q Order | | | | | | | |
| | | | | RevBitOrd<br>0 = Normal LSB/MSB Order<br>1 = Reverse LSB/MSB Order | | | | | | | |
| 0x0162 | 1 | EMUTE | Mute Enable Register for DAC | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | EM7 | EM6 | EM5 | EM4 | EM3 | EM2 | EM1 | EM0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | EM[7:0]<br>0 = DAC Mute not enabled when the corresponding bit in STATUS register is set<br>1 = Enable DAC Mute when the corresponding bit in STATUS register is set | | | | | | | |
| 0x0163 | 1 | EINT | Interrupt Enable Register for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | EINT7 | EINT6 | EINT5 | EINT4 | EINT3 | EINT2 | EINT1 | EINT0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | Definition | EINT[7:0]<br>0 = Interrupt not enabled when the corresponding bit in STATUS register is set<br>1 = Enable Interrupt when the corresponding bit in STATUS register is set | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0164 | 1 | STATUS | Status Register for DAC DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | JSDIM | JSDII | FCOL | F1A | F2A | TRDY | Reserved | PLLlck |
| | | | Default | 0xXX | | | | | | | |
| | | | Definition | **JSDIM**<br>0 = JSDI Link layer Mute is not active<br>1 = JSDI Link layer Mute is active | | | | | | | |
| | | | | **JSDII**<br>0 = JSDI Link layer Interrupt is not active<br>1 = JSDI Link layer Interrupt is active | | | | | | | |
| | | | | **FCOL**<br>0 = Input FIFO Rd/Wr pointers are not in collision<br>1 = Input FIFO Rd/Wr pointers are in collision indicating FIFO underflow/overflow.<br>This is a latched state. | | | | | | | |
| | | | | **F1A**<br>0 = Input FIFO Rd/Wr pointers are not away by 1<br>1 = Input FIFO Rd/Wr pointers are away by 1.<br>This is a latched state. | | | | | | | |
| | | | | **F2A**<br>0 = Input FIFO Rd/Wr pointers are not away by 2<br>1 = Input FIFO Rd/Wr pointers are away by 2. This is a latched state. | | | | | | | |
| | | | | **TRDY**<br>0 = SPI interface access is unavailable out of reset through RESETB.<br>1 = SPI interface access is available after a reset through RESETB. It indicates that trim loading complete after RESETB deassertion, latched status and internal configuration complete after setting GLB.CfgIFC.Xfer, latched status | | | | | | | |
| | | | | **PLLlck**<br>DAC PLL loss-of-lock, latched status. Writing 0 to clear this bit for status" 0 = locked, 1 = loss-of-lock. | | | | | | | |
| | | | Note | Writing 0 clears these bits and writing 1 has no effect, except for JSDII and JSDIM which are second-level statuses and cannot be cleared | | | | | | | |
| 0x0165 | 1 | iFIFOLevel | Input FIFO Level for DSP | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | iFL7 | iFL6 | iFL5 | iFL4 | iFL3 | iFL2 | iFL1 | iFL0 |
| | | | Default | 0xXX | | | | | | | |
| | | | Definition | iFL[7:0]<br>Input FIFO Level thermometer code, number of 1's indicating the FIFO depth | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0166 | 3 | DieSN | MAX5871 RF DAC Serial Number | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | SN7 | SN6 | SN5 | SN4 | SN3 | SN2 | SN1 | SN0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | SN15 | SN14 | SN13 | SN12 | SN11 | SN10 | SN9 | SN8 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | SN23 | SN22 | SN21 | SN20 | SN19 | SN18 | SN17 | SN16 |
| | | | Default | 0xXXXXXX | | | | | | | |
| | | | Definition | SN[23:0]<br>Serial Number of the MAX5871 RF DAC die | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0180 | 3 | CfgPLL | Configure DAC PLL | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | PLL7 | PLL6 | PLL5 | PLL4 | PLL3 | PLL2 | PLL1 | PLL0 |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | PLL15 | PLL14 | PLL13 | PLL12 | PLL11 | PLL10 | PLL9 | PLL8 |
| | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | Name | PLL23 | PLL22 | PLL21 | PLL20 | PLL19 | PLL18 | PLL17 | PLL16 |
| | | Default | 0x004000 | | | | | | | |
| | | Definition | PLL[23:21]<br>Reserved - do not write | | | | | | | |
| | | | PLL[20:19]  (DVAL[3:2])<br>See decode below | | | | | | | |
| | | | PLL16<br>0 = Selects the lowband VCO<br>1 = Selects the highband VCO | | | | | | | |
| | | | PLL17, PLL15<br>Reserved – do not write | | | | | | | |
| | | | PLL14<br>0 = DAC PLL is not bypassed<br>1 = DAC PLL is bypassed | | | | | | | |
| | | | PLL[13:12]  (DVAL[1:0])<br>0100 = Feedback divider set to div-by-16<br>0101 = Feedback divider set to div-by-20<br>0110 = Feedback divider set to div-by-24<br>1000 = Feedback divider set to div-by-32<br>1001 = Feedback divider set to div-by-36<br>1010 = Feedback divider set to div-by-40<br>1100 = Feedback divider set to div-by-48 | | | | | | | |
| | | | PLL11 (PVAL)<br>0 = Output divider set to div-by-2<br>1 = Output divider set to div-by-1 | | | | | | | |
| | | | PLL18, PLL10 (RVAL)<br>00 = Reference divider control set to div-by-8<br>01 = Reference divider control set to div-by-4<br>10 = Reference divider control set to div-by-2<br>11 = Reference divider control set to div-by-1 | | | | | | | |
| | | | PLL[9:2]<br>Reserved – Do not writ | | | | | | | |
| | | | PLL1<br>Reserved – Do not write | | | | | | | |
| | | | PLL0<br>Force restart PLL digital tuning by toggling from 1 to 0 and back to 1 | | | | | | | |

## DSP and DAC Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0183 | 2 | StatPLL | DAC PLL Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | PLLST7 | PLLST6 | PLLST5 | PLLST4 | PLLST3 | PLLST2 | PLLST1 | PLLST0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | PLLST15 | PLLST14 | PLLST13 | PLLST12 | PLLST11 | PLLST10 | PLLST9 | PLLST8 |
| | | | Default | 0xXXXX | | | | | | | |
| | | | Definition | PLLST[15:4] Reserved | | | | | | | |
| | | | | PLLST3 0 = PLL not locked 1 = PLL locked | | | | | | | |
| | | | | PLLST[2:0] Reserved | | | | | | | |

## Link Layer Configuration Registers Definition and Description

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0400 | 1 | CfgSRst | Configure Soft Reset | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | X | srl | ila |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | srl Soft reset to clear all the latched statuses | | | | | | | |
| | | | | ila Soft reset for ILA engine | | | | | | | |
| | | | | | | | | | | | |
| 0x0401 | 1 | CfgLnRst | Configure Lane Reset | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | ln4 | ln3 | ln2 | ln1 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ln[4:1] Soft reset for Lane N | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0402 | 1 | CfgLinkSet | Configure Link Settings | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | idisp | scrmd* | X | X | ddiv1* | ddiv0* | sclass1* | sclass0* |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | Definition | idisp<br>0 = Do not ignore running disparity errors for data processing<br>1 = Ignore running disparity errors for data processing<br><br>scrmd<br>0 = Descrambler is enabled<br>1 = Descrambler is disabled<br><br>ddiv[1:0]<br>00 = Device clock to sample clock frequency ratio is 1<br>01 = Device clock to sample clock frequency ratio is 2<br>10 = Device clock to sample clock frequency ratio is 4<br>11 = Device clock to sample clock frequency ratio is 8<br><br>sclass[1:0]<br>JESD204B Subclass (0, 1 or 2), only 00 and 01 are valid values | | | | | | | |
| 0x0403 | 1 | CfgSYSREF | Configure SYSREF Signal | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | valid_det | senext | rsync | smode1 | smode0 | ignore_en | thrsh_en |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | valid_det<br>0 = SYSREF validity is not checked<br>1 = SYSREF validity is checked to be a number of symbol clocks as configured in CfgSVLD.<br>valid[7:0]<br><br>senext<br>0 = SYSREF_EN pin is ignored<br>1 = SYSREF enable is controlled by SYSREF_EN pin for better timing than through SPI writes<br><br>rsync0 = A re-sync request is not output on SYNCN on a new SYSREF multiframe boundary<br>1 = A re-sync request is output on SYNCN on a new SYSREF multiframe boundary<br><br>smode[1:0]<br>00 = SYSREF is ignored<br>01 = The first SYSREF pulse is enabled when smode0 is toggled from 0 to 1<br>10 = All SYSREF pulses are enabled<br>11 = ReservedThese bits are only used for synchronous SYSREF mode<br><br>ignore_en<br>0 = No SYSREF pulses are dropped before smode[1:0] takes effect<br>1 = SYSREF pulses are dropped as configured in CfgSIGN.ign[7:0] before smode[1:0] takes effect<br><br>thrsh_en<br>0 = LMFC is reset irrespective of the new SYSREF offset<br>1 = LMFC is reset only if the new SYSREF offset exceeds the threshold from CfgSTHRSH.<br>thrsh[3:0] | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0404 | 1 | Cfg-STHRSH | Configure SYSREF Threshold | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | dfath3 | dfath2 | dfath1 | dfath0 | thrsh3 | thrsh2 | thrsh1 | thrsh0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | dfath[3:0]<br>0 = No threshold for Dynamic FIFO adjustment<br>1-15 = Dynamic FIFO adjustment is suppressed when the new frame/lane boundary is offset by more than the decimal value of this field in sample clock cycles | | | | | | | |
| | | | | thrsh[3:0]<br>SYSREF offset threshold in sample clock cycles when enabled by CfgSYSREF.thrsh_en | | | | | | | |
| | | | | | | | | | | | |
| 0x0405 | 1 | CfgSIGN | Configure SYSREF Ignore Count | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ign7 | ign6 | ign5 | ign4 | ign3 | ign2 | ign1 | ign0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ign[7:0]<br>SYSREF number of pulses ignored count when enabled by CfgSYSREF.ignore_en | | | | | | | |
| | | | | | | | | | | | |
| 0x0406 | 1 | CfgSVLD | Configure SYSREF Valid Count | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | valid7 | valid6 | valid5 | valid4 | valid3 | valid2 | valid1 | valid0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | valid[7:0]<br>SYSREF validity check count of device clock cycles when enabled by CfgSYSREF.valid_det | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0407 | 1 | CfgSYNCN | Configure SYNCN pin options | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | X | ret | Reserved2 | cset | Reserved1 | Reserved0 | init | pol |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Definition | ret<br>0 = SYNCN is output synchronous to the internal sample clock1 = SYNCN is retimed to device clock, useful for Subclass0 at lower frequencies<br>This bit should be cleared when the device clock is not present (CfgLinkSrc.rclk = 1) | | | | | | | |
| | | | Reserved2Reserved–Do not write | | | | | | | |
| | | | cset0 = Disable manual control of assert/deassert frame cycle of SYNCN error reporting<br>1 = Enable manual control of assert/deassert frame cycle of SYNCN error reporting through Cfg-SAC and CfgSDC | | | | | | | |
| | | | Reserved1-0<br>Reserved–Do not write | | | | | | | |
| | | | init<br>0 = Out-of-reset value for SYNCN output is 0<br>1 = Out-of-reset value for SYNCN output is 1 | | | | | | | |
| | | | pol<br>0 = SYNCN polarity is active low according to the JESD204B standard<br>1 = SYNCN polarity is active-high | | | | | | | |
| | | | | | | | | | | |
| 0x0408 | 1 | CfgSAC | Configure SYNCN assert frame count | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | X | X | X | acnt4 | acnt3 | acnt2 | acnt1 | acnt0 |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Definition | acnt[4:0]<br>When CfgSYNCN.cset is set, this value determines the SYNCN error reporting assertion frame count | | | | | | | |
| | | | | | | | | | | |
| 0x0409 | 1 | CfgSDC | Configure SYNCN deassert frame count | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | X | X | X | dcnt4 | dcnt3 | dcnt2 | dcnt1 | dcnt0 |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Definition | dcnt[4:0]<br>When CfgSYNCN.cset is set, this value determines the SYNCN error reporting deassertion frame count | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x040A | 1 | CfgLink-MLFS | Configure Link for M, L, F and S | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | S | F1 | F0 | X | L1 | L0 | X | M |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | | Definition | S<br>Number of samples per frame cycle is (S1), restricted to allowed combinations of L/F/S | | | | | | | |
| | | | | F[1:0]<br>Number of octets per frame cycle per lane is (F1), restricted to allowed combinations of L/F/S | | | | | | | |
| | | | | L[1:0]<br>Number of active lanes in the Link is (L1), restricted to allowed combinations of L/F/S | | | | | | | |
| | | | | M<br>Number of converters in the Link is (M1), should always be set to 1 | | | | | | | |
| | | | | | | | | | | | |
| 0x040B | 1 | CfgLinkK | Configure Link multiframe length | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | K4 | K3 | K2 | K1 | K0 |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | | | Definition | K[4:0]<br>Number of frames per multiframe is (K1) | | | | | | | |
| | | | | | | | | | | | |
| 0x040C | 1 | CfgBID | Configure Bank ID | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | bid3 | bid2 | bid1 | bid0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | bid[3:0]<br>Bank ID used for ILA sequence checking | | | | | | | |
| | | | | | | | | | | | |
| 0x040D | 1 | CfgDID | Configure Device ID | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | did7-0 | did6 | did5 | did4 | did3 | did2 | did1 | did0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | did[7:0]<br>Device ID used for ILA sequence checking | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x040E | 4 | CfgLID | Configure Lane N ID | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | lid1_4 | lid1_3 | lid1_2 | lid1_1 | lid1_0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | lid2_4 | lid2_3 | lid2_2 | lid2_1 | lid2_0 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | lid3_4 | lid3_3 | lid3_2 | lid3_1 | lid3_0 |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | X | X | lid4_4 | lid4_3 | lid4_2 | lid4_1 | lid4_0 |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | lidN_[4:0]<br>Lane ID for Lane N used for ILA sequence checking | | | | | | | |
| 0x0412 | 1 | CfgLinkSrc | Configure Link signal source | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | X | async_avl | rclk |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | Definition | async_avl<br>0 = Frame synchronization supports re-initialization over the data interface, monitoring the reception of /K/ characters<br>1 = SYNCN signals from all receivers are available and frame synchronization state machine does not support re-initialization over the data interface (no FS_CHECK state) | | | | | | | |
| | | | | rclk<br>0 = Sample Clock is derived from Device Clock (CLKP/N) with a divide down set by CfgLinkSet. ddiv[1:0]<br>1 = Sample Clock is sourced from the DSP through the DAC Clock divided by interpolation ratio | | | | | | | |
| 0x0413 | 1 | CfgClkInv | Configure Lane Clock Inversion | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | ln4 | ln3 | ln2 | ln1 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | lnN<br>When set, invert Rx clock from SerDes | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0414 | 1 | CfgLinkCtl | Configure Link control | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | cgsmen | serrc | altm | dynfadj | lcoren | fcoren | bswap | afdeti |
| | | | Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | | | Definition | cgsmen<br>When set, enable Manual Code Group Synchronization through CfgBOff<br>serrc<br>When set, enable SYNCN error reporting assertion/deassertion on any frame–JESD204A<br>altm<br>When set, enable alternate sample data mapping for MLFS=2422<br>dynfadj<br>When set, enable dynamic FIFO pointer adjustment on a frame/lane synchronization change<br>lcoren<br>When set, enable Lane Synchronization auto-correction<br>fcoren<br>When set, enable Frame Synchronization auto-correction<br>bswap<br>When set, enable Bit Swap MSB<->LSB in an octet on all lanes<br>afdeti<br>When set, enable detection of invalid (Running Disparity) /A/ and /F/ characters | | | | | | | |
| 0x0415 | 2 | CfgBOff | Configure Manual Code Group Synch Bit Offsets | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ln2_3 | ln2_2 | ln2_1 | ln2_0 | ln1_3 | ln1_2 | ln1_1 | ln1_0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | ln4_3 | ln4_2 | ln4_1 | ln4_0 | ln3_3 | ln3_2 | ln3_1 | ln3_0 |
| | | | Default | 0x0000 | | | | | | | |
| | | | Definition | ln[4:1]_[3:0]<br>Lane N manual Code Group Synchronization boundary enabled by CfgLinkCtl.cgsmen | | | | | | | |
| 0x0417 | 1 | CfgRstCnt | Configure SYSREF reset counts | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | oi | fi4 | fi3 | fi2 | fi1 | fi0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | oi<br>Initial value of octet count in the frame cycle from SYSREF sampling | | | | | | | |
| | | | | fi[4:0]<br>Initial value of frame count in the multiframe cycle from SYSREF sampling<br>This value along with CfgRstCnt.oi is useful for setting the LMFC boundary relative to SYSREF | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0418 | 1 | CfgILALck | Configure ILA Lock configuration | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | lksel4 | lksel3 | lksel2 | lksel1 |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | | | Definition | lkselN<br>ILA Lock Select mask for Lane N based on FIFO write start, 1 indicating the lane is included<br>This field is typically set to the same value as CfgLnEn.ln[3:0] but if the lksel bit is set to 0 when the lane is enabled, that particular lane will not be included in the ILA process. | | | | | | | |
| 0x0419 | 1 | CfgILAC | Configure ILA Control | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | lsdis | ilasd1 | ilasd0 | dfsync |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | lsdis<br>0 = Lane synchronization enabled<br>1 = Lane synchronization disabled | | | | | | | |
| | | | | ilasd[1:0]<br>00 = ILA sequence detection is enabled<br>01 = ILA sequence detection is disabled for the first CfgILAsn.snum frames<br>10 = ILA sequence detection is disabled<br>11 = Reserved | | | | | | | |
| | | | | dfsync<br>0 = Enable ILA restart on frame resynchronization<br>1 = Disable ILA restart on frame resynchronization | | | | | | | |
| 0x041A | 1 | CfgILAD | Configure ILA Delay Control | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ilam | X | idly5 | idly4 | idly3 | idly2 | idly1 | idly0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ilam<br>0 = Manual ILA control is disabled<br>1 = Manual ILA control is enabled | | | | | | | |
| | | | | idly[5:0]<br>ILA Delay sample clock count from the LMFC boundary for FIFO read start<br>This field is useful to set the FIFO depths based on the link delay | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x041B | 4 | CfgILAM | Configure Lane N Manual ILA Delay | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | ln1imd5 | ln1imd4 | ln1imd3 | ln1imd2 | ln1imd1 | ln1imd0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | ln2imd5 | ln2imd4 | ln2imd3 | ln2imd2 | ln2imd1 | ln2imd0 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | ln3imd5 | ln3imd4 | ln3imd3 | ln3imd2 | ln3imd1 | ln3imd0 |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | X | ln4imd5 | ln4imd4 | ln4imd3 | ln4imd2 | ln4imd1 | ln4imd0 |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | ln[4:1]imd[5:0]<br>Manual ILA Delay sample clock count for FIFO read start for Lane N when enabled by CfgILAD.ilam | | | | | | | |
| | | | | | | | | | | | |
| 0x041F | 2 | CfgILAmfs | Configure ILA Multiframe start | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | mfsel7 | mfsel6 | mfsel5 | mfsel4 | mfsel3 | mfsel2 | mfsel1 | mfsel0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | X | X | X | X | Re-served0 |
| | | | Default | 0x0004 | | | | | | | |
| | | | Definition | mfsel[7:0]<br>ILA multiframe count for FIFO write start | | | | | | | |
| | | | | Reserved0<br>Reserved–do not write | | | | | | | |
| | | | | | | | | | | | |
| 0x0421 | 2 | CfgILAsn | Configure ILA sequence number | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | snum7 | snum6 | snum5 | snum4 | snum3 | snum2 | snum1 | snum0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | X | X | X | X | Re-served0 |
| | | | Default | 0x0003 | | | | | | | |
| | | | Definition | snum[7:0]<br>Number of multiframes used for ILA sequence checking | | | | | | | |
| | | | | Reserved0<br>Reserved–do not write | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0423 | 2 | CfgLerrM* | Configure Mask for error reporting on SYNCN | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | lerrm7 | lerrm6 | lerrm5 | lerrm4 | lerrm3 | lerrm2 | lerrm1 | lerrm0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | lerrm14 | lerrm13 | lerrm12 | lerrm11 | lerrm10 | lerrm9 | lerrm8 |
| | | | Default | 0x0000 | | | | | | | |
| | | | Definition | lerrm14<br>When set, ILA Fail error is enabled | | | | | | | |
| | | | | lerrm13<br>Reserved | | | | | | | |
| | | | | lerrm12<br>When set, FIFO empty error is enabled | | | | | | | |
| | | | | lerrm11<br>When set, FIFO full error is enabled | | | | | | | |
| | | | | lerrm10<br>When set, Lane Configuration in ILA sequence FCS check error is enabled | | | | | | | |
| | | | | lerrm9<br>When set, Lane Configuration in ILA sequence mismatch error is enabled | | | | | | | |
| | | | | lerrm8<br>When set, ILA sequence control character error is enabled | | | | | | | |
| | | | | lerrm7<br>When set, Dynamic FIFO adjustment failure is enabled | | | | | | | |
| | | | | lerrm6<br>When set, Lane realignment event is enabled | | | | | | | |
| | | | | lerrm5<br>When set, Frame realignment event is enabled | | | | | | | |
| | | | | lerrm4<br>When set, 8b10b /K/ character at unexpected alignment error is enabled | | | | | | | |
| | | | | lerrm3<br>When set, unexpected 8b10b control character other than /K/ error is enabled | | | | | | | |
| | | | | lerrm2<br>When set, 8b10b Running Disparity error is enabled | | | | | | | |
| | | | | lerrm1<br>When set, 8b10b Not-in-table error is enabled | | | | | | | |
| | | | | lerrm0<br>Reserved | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0425 | 2 | CfgSerrM* | Configure Mask for re-sync request on SYNCN | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | serrm7 | serrm6 | serrm5 | 0 | 0 | serrm2 | serrm1 | 0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | serrm14 | serrm13 | serrm12 | serrm11 | serrm10 | serrm9 | serrm8 |
| | | | Default | 0x0000 | | | | | | | |
| | | | Definition | serrm14<br>When set, ILA Fail error is enabled | | | | | | | |
| | | | | serrm13<br>Reserved | | | | | | | |
| | | | | serrm12<br>When set, FIFO empty error is enabled | | | | | | | |
| | | | | serrm11<br>When set, FIFO full error is enabled | | | | | | | |
| | | | | serrm10<br>When set, Lane Configuration in ILA sequence FCS check error is enabled | | | | | | | |
| | | | | serrm9<br>When set, Lane Configuration in ILA sequence mismatch error is enabled | | | | | | | |
| | | | | serrm8<br>When set, ILA sequence control character error is enabled | | | | | | | |
| | | | | serrm7<br>When set, Dynamic FIFO adjustment failure is enabled | | | | | | | |
| | | | | serrm6<br>When set, Lane realignment event is enabled | | | | | | | |
| | | | | serrm5<br>When set, Frame realignment event is enabled | | | | | | | |
| | | | | serrm4<br>Reserved = 0 only | | | | | | | |
| | | | | serrm3<br>Reserved = 0 only | | | | | | | |
| | | | | serrm2<br>When set, 8b10b Running Disparity error is enabled | | | | | | | |
| | | | | serrm1<br>When set, 8b10b Not-in-table error is enabled | | | | | | | |
| | | | | serrm0<br>Reserved = 0 only | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0427 | 2 | CfgMDS | Configure Multi-DAC Synchronization | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | rclk | Re-served3 | Re-served2 | Re-served1 | Re-served0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | Re-served8 | Re-served7 | Re-served6 | Re-served5 | Re-served4 |
| | | | Default | 0x0000 | | | | | | | |
| | | | Definition | rclk<br>When set, RSYNC from DSP replaces SYSREF<br>This bit should be set to 1 when SYSREF is used for multi-DAC synchronization and no Device Clock is available to sample SYSREF on | | | | | | | |
| | | | | Reserved8-0<br>Reserved–do not write | | | | | | | |
| 0x0429 | 1 | CfgINV | Configure data inversion | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | ln4 | ln3 | ln2 | ln1 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ln[4:1]<br>0 = Lane N octet data inversion is disabled<br>1 = Lane N octet data inversion is enable | | | | | | | |
| 0x042A | 2 | CfgLnSrc | Configure Lane Source | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | ln2_1 | ln2_0 | X | X | ln1_1 | ln1_0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | ln4_1 | ln4_0 | X | X | ln3_1 | ln3_0 |
| | | | Default | 0x3210 | | | | | | | |
| | | | Definition | ln[4:1]_[1:0]<br>Physical Lane number source for Logical Lane N at octet-to-sample mapping | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x042C | 1 | CfgLnEn | Configure Lane Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | ln4 | ln3 | ln2 | ln1 |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | | | Definition | ln[4:1]<br>Lane N enable | | | | | | | |
| 0x042D | 2 | CfgFIFO | Configure FIFO depths | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | minfd4 | minfd3 | minfd2 | minfd1 | minfd0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | maxfd4 | maxfd3 | maxfd2 | maxfd1 | maxfd0 |
| | | | Default | 0x1A06 | | | | | | | |
| | | | Definition | maxfd[4:0]<br>Maximum FIFO depth for dynamic adjustment and full/empty status | | | | | | | |
| | | | | minfd[4:0]<br>Minimum FIFO depth for dynamic adjustment and full/empty status | | | | | | | |
| | | | | | | | | | | | |
| 0x042F | 1 | CfgRepl | Configure Sample Replacement on NIT error | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | ac | frm | sam |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ac<br>When set, replace sample/frame for all converters with previous good sample/frame | | | | | | | |
| | | | | frm<br>When set, replace frame with previous good frame | | | | | | | |
| | | | | sam<br>When set, replace sample with previous good sample | | | | | | | |
| | | | | | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0430 | 1 | CfgSamTest | Configure SerDes/Sample Interface Test | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | prbst1 | prbst0 | tprbs | rprbs | X | X | sprbs2 | sprbs1 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | prbst[1:0]<br>00 = PRBS7 for SerDes Interface<br>01 = PRBS23 for SerDes Interface<br>10 = PRBS31 for SerDes Interface<br>11 = Reserved | | | | | | | |
| | | | | tprbs<br>Enable PRBS on transmit SerDes interface, pattern based on prbst1-0 | | | | | | | |
| | | | | rprbs<br>Enable PRBS checking on receive SerDes interface, pattern based on prbst1-0<br>This bit should be toggled from 0 to 1 for restarting the PRBS check | | | | | | | |
| | | | | sprbsN<br>Enable PRBS15 checker for converter N samples<br>This bit should be toggled from 0 to 1 for restarting the PRBS check | | | | | | | |
| 0x0431 | 2 | CfgST-Pc1s1 | Configure Short Test Pattern for Converter 1, Sample 1 | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | pat7 | pat6 | pat5 | pat4 | pat3 | pat2 | pat1 | pat0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | pat15 | pat14 | pat13 | pat12 | pat11 | pat10 | pat9 | pat8 |
| | | | Default | 0x0000 | | | | | | | |
| | | | Definition | pat[15:0]<br>Converter 1, Sample 1 short test pattern (alternating sample test pattern) | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0433 | 2 | CfgST-Pc1s2 | Configure Short Test Pattern for Converter 1, Sample 2 | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | pat7 | pat6 | pat5 | pat4 | pat3 | pat2 | pat1 | pat0 |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | pat15 | pat14 | pat13 | pat12 | pat11 | pat10 | pat9 | pat8 |
| | | Default | 0x0000 | | | | | | | |
| | | Definition | pat[15:0]<br>Converter 1, Sample 2 short test pattern (alternating sample test pattern) | | | | | | | |
| 0x0435 | 2 | CfgST-Pc2s1 | Configure Short Test Pattern for Converter 2, Sample 1 | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | pat7 | pat6 | pat5 | pat4 | pat3 | pat2 | pat1 | pat0 |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | pat15 | pat14 | pat13 | pat12 | pat11 | pat10 | pat9 | pat8 |
| | | Default | 0x0000 | | | | | | | |
| | | Definition | pat[15:0]<br>Converter 2, Sample 1 short test pattern (alternating sample test pattern) | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0437 | 2 | CfgST-Pc2s2 | Configure Short Test Pattern for Converter 2, Sample 2 | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | pat7 | pat6 | pat5 | pat4 | pat3 | pat2 | pat1 | pat0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | pat15 | pat14 | pat13 | pat12 | pat11 | pat10 | pat9 | pat8 |
| | | | Default | 0x0000 | | | | | | | |
| | | | Definition | pat[15:0]<br>Converter 2, Sample 2 short test pattern (alternating sample test pattern) | | | | | | | |
| | | | | | | | | | | | |
| 0x0500 | 1 | CfgCnt | Configure Counter Settings | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | samld | rxld | cdcor |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | samld<br>Load signal for sample clock domain Lane FIFO depth update, this bit is self-clearing | | | | | | | |
| | | | | rxld<br>Load signal for Rx SerDes clock domain counter update, this bit is self-clearing | | | | | | | |
| | | | | cdcor<br>Counter data clear-on-read enable | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0501 | 1 | CfgCntSel | Configure Counter Selects | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ctsel3 | ctsel2 | ctsel1 | ctsel0 | X | X | rxcsel1 | rxcsel0 |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | ctsel[3:0]<br>Lane debug counter error type select for CntDbg register<br>0000 = No counts<br>0001 = NIT errors<br>0010 = Disparity errors<br>0011 = /K/ detect<br>0100 = /R/ detect<br>0101 = /Q/ detect<br>0110 = /A/ detect<br>0111 = /F/ detect<br>1000 = Unexpected control character error<br>1001 = ILA sequence control character error<br>1010-1111 = No counts | | | | | | | |
| | | | | rxcsel[1:0]<br>00 = Lane 1 counts enabled for CntDbg register<br>01 = Lane 2 counts enabled for CntDbg register<br>10 = Lane 3 counts enabled for CntDbg register<br>11 = Lane 4 counts enabled for CntDbg register | | | | | | | |
| | | | | | | | | | | | |
| 0x0503 | 4 | EIntLane | Lane N Interrupt Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ln1fnsync | ln1lnrealgn | ln1frrealgn | ln1uk | ln1ctrl | ln1disp | ln1nit | ln1cgs |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | ln2fnsync | ln2lnrealgn | ln2frrealgn | ln2uk | ln2ctrl | ln2disp | ln2nit | ln2cgs |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | ln3fnsync | ln3lnrealgn | ln3frrealgn | ln3uk | ln3ctrl | ln3disp | ln3nit | ln3cgs |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | ln4fnsync | ln4lnrealgn | ln4frrealgn | ln4uk | ln4ctrl | ln4disp | ln4nit | ln4cgs |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | Interrupt enable for the corresponding bit in StatLane register | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0507 | 4 | EIntFIFO | Lane N FIFO Interrupt Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ln1fafail | ln1empty | ln1full | X | X | X | X | X |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | ln2fafail | ln2empty | ln2full | X | X | X | X | X |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | ln3fafail | ln3empty | ln3full | X | X | X | X | X |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | ln4fafail | ln4empty | ln4full | X | X | X | X | X |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | Interrupt enable for the corresponding bit in StatFIFO register | | | | | | | |
| | | | | | | | | | | | |
| 0x050B | 4 | EIntILAS | Lane N ILA Sequence Interrupt Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | ln1drcv | ln1kerr | ln1rprbs | ln1krcv | ln1fchkerr | ln1lcfgerr | ln1ilaerr |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | ln2drcv | ln2kerr | ln2rprbs | ln2krcv | ln2fchkerr | ln2lcfgerr | ln2ilaerr |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | ln3drcv | ln3kerr | ln3rprbs | ln3krcv | ln3fchkerr | ln3lcfgerr | ln3ilaerr |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | ln4drcv | ln4kerr | ln4rprbs | ln4krcv | ln4fchkerr | ln4lcfgerr | ln4ilaerr |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | Interrupt enable for the corresponding bit in StatILAS register | | | | | | | |
| | | | | | | | | | | | |
| 0x050F | 1 | EIntILA | Initial Lane Alignment Interrupt Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | sysref_nvld | nsync | Re-served0 | sysref_ndet | fail |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | Definition | Interrupt enable for the corresponding bit in StatILA register | | | | | | | |
| | | | | | | | | | | | |
| 0x0510 | 1 | EIntLink | Link Interrupt Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | prbs_c2err | prbs_c1err | X | X | stp_c2err | stp_c1err |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | Interrupt enable for the corresponding bit in StatLink register | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0511 | 4 | EMuteLane | Lane N Mute Enable | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | ln1fnsync | ln1lnrealgn | ln1frrealgn | ln1uk | ln1ctrl | ln1disp | ln1nit | ln1cgs |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | ln2fnsync | ln2lnrealgn | ln2frrealgn | ln2uk | ln2ctrl | ln2disp | ln2nit | ln2cgs |
| | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | Name | ln3fnsync | ln3lnrealgn | ln3frrealgn | ln3uk | ln3ctrl | ln3disp | ln3nit | ln3cgs |
| | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | Name | ln4fnsync | ln4lnrealgn | ln4frrealgn | ln4uk | ln4ctrl | ln4disp | ln4nit | ln4cgs |
| | | Default | 0x00000000 | | | | | | | |
| | | Definition | Enable DAC Mute for the corresponding bit in StatLane register | | | | | | | |
| | | | | | | | | | | |
| 0x0515 | 4 | EMuteFIFO | Lane N FIFO Mute Enable | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | ln1fafail | ln1empty | ln1full | X | X | X | X | X |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | ln2fafail | ln2empty | ln2full | X | X | X | X | X |
| | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | Name | ln3fafail | ln3empty | ln3full | X | X | X | X | X |
| | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | Name | ln4fafail | ln4empty | ln4full | X | X | X | X | X |
| | | Default | 0x00000000 | | | | | | | |
| | | Definition | Enable DAC Mute for the corresponding bit in StatFIFO register | | | | | | | |
| | | | | | | | | | | |
| 0x0519 | 4 | EMuteILAS | Lane N ILA Sequence Mute Enable | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | X | ln1drcv | ln1kerr | ln1rprbs | ln1krcv | ln1fchkerr | ln1lcfgerr | ln1ilaerr |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | X | ln2drcv | ln2kerr | ln2rprbs | ln2krcv | ln2fchkerr | ln2lcfgerr | ln2ilaerr |
| | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | Name | X | ln3drcv | ln3kerr | ln3rprbs | ln3krcv | ln3fchkerr | ln3lcfgerr | ln3ilaerr |
| | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | Name | X | ln4drcv | ln4kerr | ln4rprbs | ln4krcv | ln4fchkerr | ln4lcfgerr | ln4ilaerr |
| | | Default | 0x00000000 | | | | | | | |
| | | Definition | Enable DAC Mute for the corresponding bit in StatILAS register | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x051D | 1 | EMuteILA | Initial Lane Alignment Mute Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | sysref_ nvld | nsync | Reserved | sysref_ ndet | fail |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | Definition | Enable DAC Mute for the corresponding bit in StatILA register | | | | | | | |
| | | | | | | | | | | | |
| 0x051E | 1 | EMuteLink | Link Mute Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | prbs_c2err | prbs_c1err | X | X | stp_c2err | stp_c1err |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Definition | Enable DAC Mute for the corresponding bit in StatLink register | | | | | | | |
| | | | | | | | | | | | |
| 0x0580 | 4 | StatLane | Lane N Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ln1fnsync | ln1lnrealgn | ln1frrealgn | ln1uk | ln1ctrl | ln1disp | ln1nit | ln1cgs |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | ln2fnsync | ln2lnrealgn | ln2frrealgn | ln2uk | ln2ctrl | ln2disp | ln2nit | ln2cgs |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | ln3fnsync | ln3lnrealgn | ln3frrealgn | ln3uk | ln3ctrl | ln3disp | ln3nit | ln3cgs |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | ln4fnsync | ln4lnrealgn | ln4frrealgn | ln4uk | ln4ctrl | ln4disp | ln4nit | ln4cgs |
| | | | Default | 0xXXXXXXXX | | | | | | | |
| | | | Definition | lnNfnsync<br>Frame synchronization state machine not in Sync real-time | | | | | | | |
| | | | | lnNlnrealgnLane realignment occurred latched | | | | | | | |
| | | | | lnNfrrealgn<br>Frame realignment occurred latched | | | | | | | |
| | | | | lnNuk<br>Lane N unexpected /K/ character latched. When set, this bit is not necessarily indicating an error since /K/ can occur across the character boundaries. | | | | | | | |
| | | | | lnNctrl<br>Lane N unexpected control character latched | | | | | | | |
| | | | | lnNdisp<br>Lane N Disparity error latched | | | | | | | |
| | | | | lnNnit<br>Lane N NIT error latched | | | | | | | |
| | | | | lnNcgs<br>Lane N Code Group Synchronization out of Sync latched | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0584 | 4 | StatFIFO | Lane N FIFO Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | ln1fafail | ln1empty | ln1full | ln1fd4 | ln1fd3 | ln1fd2 | ln1fd1 | ln1fd0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | ln2fafail | ln2empty | ln2full | ln2fd4 | ln2fd3 | ln2fd2 | ln2fd1 | ln2fd0 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | ln3fafail | ln3empty | ln3full | ln3fd4 | ln3fd3 | ln3fd2 | ln3fd1 | ln3fd0 |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | ln4fafail | ln4empty | ln4full | ln4fd4 | ln4fd3 | ln4fd2 | ln4fd1 | ln4fd0 |
| | | | Default | 0xXXXXXXXX | | | | | | | |
| | | | Definition | lnNfafail<br>Lane N dynamic FIFO adjustment failure latched | | | | | | | |
| | | | | lnNempty<br>Lane N FIFO empty status latched | | | | | | | |
| | | | | lnNfull<br>Lane N FIFO full status latched | | | | | | | |
| | | | | lnNfd[4:0]<br>Lane N FIFO depth real-time loaded when CfgCnt.samld is set to 1 | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0588 | 4 | StatILAS | Lane N ILA Sequence Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | ln1drcv | ln1kerr | ln1rprbs | ln1krcv | ln1fchkerr | ln1lcfgerr | ln1ilaerr |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | ln2drcv | ln2kerr | ln2rprbs | ln2krcv | ln2fchkerr | ln2lcfgerr | ln2ilaerr |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | ln3drcv | ln3kerr | ln3rprbs | ln3krcv | ln3fchkerr | ln3lcfgerr | ln3ilaerr |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | ln4drcv | ln4kerr | ln4rprbs | ln4krcv | ln4fchkerr | ln4lcfgerr | ln4ilaerr |
| | | | Default | 0xXXXXXXXX | | | | | | | |
| | | | Definition | lnNdrcv<br>Lane N continuous D21.5 not-detect latched | | | | | | | |
| | | | | lnNkerr<br>Lane N /K/ character while in frame sync latched | | | | | | | |
| | | | | lnNrprbs<br>Lane N SerDes interface PRBS error latched | | | | | | | |
| | | | | lnNkrcv<br>Lane N continuous /K/ not-detect latched | | | | | | | |
| | | | | lnNfchkerr<br>Lane N ILA sequence FCHK error latched | | | | | | | |
| | | | | lnNlcfgerr<br>Lane N ILA sequence lane configuration error latched | | | | | | | |
| | | | | lnNilaerr<br>Lane N ILA sequence decode error latched | | | | | | | |
| 0x058C | 1 | StatILA | Initial Lane Alignment Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | sysref_nvld | nsync | Re-served0 | sysref_ndet | fail |
| | | | Default | 0xXX | | | | | | | |
| | | | Definition | sysref_nvld<br>SYSREF validity detection error status latched | | | | | | | |
| | | | | nsync<br>ILA synchronization not achieved real-time | | | | | | | |
| | | | | Reserved0 | | | | | | | |
| | | | | sysref_ndet<br>SYSREF detection status set until a SYSREF pulse is detected and used for LMFC reset | | | | | | | |
| | | | | fail<br>ILA failure latched<br>This status is set when a lane FIFO is empty or full when the read starts | | | | | | | |

## Link Layer Configuration Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x058D | 1 | StatLink | Link Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | prbs_c2err | prbs_c1err | X | X | stp_c2err | stp_c1err |
| | | | Default | 0xXX | | | | | | | |
| | | | Definition | prbs_cNerr Converter N PRBS error latched | | | | | | | |
| | | | | stp_cNerr Converter N short test pattern error latched | | | | | | | |
| | | | | | | | | | | | |
| 0x058E | 2 | CntInvld | Counter for Invalid Errors | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | cnt7 | cnt6 | cnt5 | cnt4 | cnt3 | cnt2 | cnt1 | cnt0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | cnt15 | cnt14 | cnt13 | cnt12 | cnt11 | cnt10 | cnt9 | cnt8 |
| | | | Default | 0xXXXX | | | | | | | |
| | | | Definition | cnt1[5:0] Invalid character count for lane # controlled by CfgCntSel.rxcsel1-0 This counter should be loaded by setting CfgCnt.rxld to 1 | | | | | | | |
| | | | | | | | | | | | |
| 0x0590 | 2 | CntDbg | Counter for Lane Debug | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | cnt7 | cnt6 | cnt5 | cnt4 | cnt3 | cnt2 | cnt1 | cnt0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | cnt15 | cnt14 | cnt13 | cnt12 | cnt11 | cnt10 | cnt9 | cnt8 |
| | | | Default | 0xXXXX | | | | | | | |
| | | | Definition | cnt1[5:0] Debug count type controlled by CfgCntSel.ctsel3-0 for lane # controlled by CfgCntSel.rxcsel1-0 This counter should be loaded by setting CfgCnt.rxld to 1 | | | | | | | |

*SYNCN behavior per the JESD204B standard is to be asserted while the Rx Link is out of Code Group Synchronization (CGS). The MAX5871 asserts SYNCN (drive low) as long as any of the active lanes are out of CGS.

LNK.CfgLerrM register can be used for error reporting on SYNCN which asserts SYNCN for 2 frame clock cycles at the end of the multiframe on an error that is enabled through this register.

LNK.CfgSerrM register can be used for resynchronization request on SYNCN which asserts SYNCN for the minimum required period of "5 frames + 9 octets" on an error that is enabled through this register.

If LNK.CfgSerrM.serrm0 is set, it would interfere with the required behavior of SYNCN per the JESD204B standard and asserts SYNCN only for the minimum required period and not as long as CGS error persists.

## SERDES Common Registers Definition and Description

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0600 | 1 | CfgRst | Configure Reset for all Lanes | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | PhyKill | RstTx | Rst |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | Definition | PhyKill<br>Reserved – do not write | | | | | | | |
| | | | | RstTx<br>Reserved – do not write | | | | | | | |
| | | | | Rst<br>0 = SerDes PHY Logic is not in reset<br>1 = SerDes PHY Logic is in reset | | | | | | | |
| | | | | | | | | | | | |
| 0x0606 | 1 | CfgRate | Configure Rate for all lanes | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | TxRate1 | TxRate0 | RxRate1 | RxRate0 |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | | | Definition | TxRate[1:0]<br>Reserved – do not write | | | | | | | |
| | | | | RxRate[1:0]<br>00 = Reserved<br>01 = Serial Rate for Rx SerDes is CMU clock rate divide-by-4<br>10 = Serial Rate for Rx SerDes is CMU clock rate divide-by-2<br>11 = Serial Rate for Rx SerDes is CMU clock rate | | | | | | | |

## SERDES Common Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0607 | 4 | CfgTrain-Ln | Configure Training for Lane | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | Ln1DnGate | Ln1IdleGate | Ln1Force1 | Ln1Force0 |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | X | Ln2DnGate | Ln2IdleGate | Ln2Force1 | Ln2Force0 |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | X | Ln3DnGate | Ln3IdleGate | Ln3Force1 | Ln3Force0 |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | X | X | X | Ln4DnGate | Ln4IdleGate | Ln4Force1 | Ln4Force0 |
| | | | Default | 0x0D for each lane | | | | | | | |
| | | | Definition | Ln[4:1]DnGate<br>0 = Do not gate data off to Link layer when SerDes Training done status is low for lane N<br>1 = Gate data off to Link layer when SerDes Training done status is low for lane N | | | | | | | |
| | | | | Ln[4:1]IdleGate<br>0 = Do not gate data off to Link layer when SerDes Idle detect is high for lane N<br>1 = Gate data off to Link layer when SerDes Idle detect is high for lane N | | | | | | | |
| | | | | Ln[4:1]Force[1:0]<br>00, 11 = Reserved<br>01 = Deactivate training for Lane N<br>10 = Activate training for Lane N | | | | | | | |
| 0x060B | 1 | CfgMisc | Configure Miscellaneous for all Lanes | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | PhyWMde1 | PhyWMde0 | X | BCast | Reserved | Reserved |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | Definition | PhyWMde[1:0]<br>00 = Buffer upper 3 bytes and transfer all 4 bytes on a write to LSB for the 32-bit interface on the PHY<br>01 = Buffer lower 3 bytes and transfer all 4 bytes on a write to MSB for the 32-bit interface on the PHY<br>10 = Enable individual byte writes to the SerDes PHY<br>11 = Reserved | | | | | | | |
| | | | | BCast<br>0 = SPI writes to one SerDes PHY are not broadcasted to all lanes<br>1 = SPI writes to one SerDes PHY are broadcasted to all lanes | | | | | | | |

## SERDES Common Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0640 | 4 | EIntLn | SerDes Phy Logic Interrupt Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | Ln1SigDet | Ln1TrainDn | Ln1Phy |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | X | X | Ln2SigDet | Ln2TrainDn | Ln2Phy |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | X | X | Ln3SigDet | Ln3TrainDn | Ln3Phy |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | X | X | X | X | Ln4SigDet | Ln4TrainDn | Ln4Phy |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | Interrupt enable for the corresponding bit in StatusLn register | | | | | | | |
| | | | | | | | | | | | |
| 0x0644 | 4 | EMuteLn | SerDes Phy Logic DAC Mute Enable | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | Ln1SigDet | Ln1TrainDn | Ln1Phy |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | X | X | Ln2SigDet | Ln2TrainDn | Ln2Phy |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | X | X | Ln3SigDet | Ln3TrainDn | Ln3Phy |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | X | X | X | X | Ln4SigDet | Ln4TrainDn | Ln4Phy |
| | | | Default | 0x00000000 | | | | | | | |
| | | | Definition | DAC Mute enable enable for the corresponding bit in StatusLn register | | | | | | | |

## SERDES Common Registers Definition and Description (continued)

| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---------|------|---------------|-------------|---|---|---|---|---|---|---|
| 0x0648 | 4 | StatusLn | SerDes Phy Logic Status | | | | | | | |
| | | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | Name | X | X | X | X | X | Ln1SigDet | Ln1TrainDn | Ln1Phy |
| | | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | Name | X | X | X | X | X | Ln2SigDet | Ln2TrainDn | Ln2Phy |
| | | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | Name | X | X | X | X | X | Ln3SigDet | Ln3TrainDn | Ln3Phy |
| | | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | Name | X | X | X | X | X | Ln4SigDet | Ln4TrainDn | Ln4Phy |
| | | | Default | 0xXXXXXXXX | | | | | | | |
| | | | Definition | Ln[4:1]SigDet<br>0 = SerDes Idle not Detected on Lane N<br>1 = SerDes Idle Detected on Lane N | | | | | | | |
| | | | | Ln[4:1]TrainDn<br>0 = SerDes Training Not Done on Lane N<br>1 = SerDes Training Done on Lane N | | | | | | | |
| | | | | Ln[4:1]Phy<br>0 = PHY interrupt for Lane N is not set<br>1 = PHY interrupt for Lane N is set | | | | | | | |

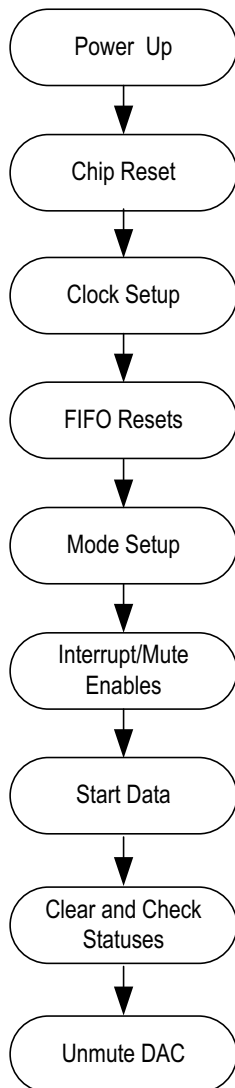| ADDRESS | BYTE | REGISTER NAME | DESCRIPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0700 | 8 | CfgCMU | Serdes CMU Configuration Register – to configure the different JESD204B rate | | | | | | | |
| | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Name | Reserved | | | | | | | |
| | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Name | Reserved | | | | | | | |
| | | Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | Name | Reserved | | | | | | | |
| | | Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | Name | Reserved | | | | | | | |
| | | Bit | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| | | Name | Reserved | | FBDIV<1:0> | | VCOSEL<1:0> | | Reserved | |
| | | Bit | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 |
| | | Name | Reserved | | | | | | | |
| | | Bit | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 |
| | | Name | Cref_divsel1p0<1:0> | | Reserved | | | | | |
| | | Bit | 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 |
| | | Name | Reserved | | | | | cd_tune1p0<2:0> | | |
| | | Default | 64'h0000000000000000 | | | | | | | |
| | | Definition | cd_tune1p0<2:0><br>3'b000 – 10G Mode<br>3'b100 – 7G Mode<br>3'b111 – 6G Mode | | | | | | | |
| | | | Cref_divsel1p0<1:0><br>2'b00 – JESD204B internal reference div-1<br>2'b01 – JESD204B internal reference div-2<br>2'b10 – JESD204B internal reference div-4<br>2'b11 – JESD204B internal reference div-8 | | | | | | | |
| | | | FBDIV<1:0><br>2'b00 – divide by 40 default<br>2'b01 – divide by 80<br>2'b10 – Reserved<br>2'b 11 – divide by 20 | | | | | | | |
| | | | VCOSEL<1:0><br>2'b00 – 10G Mode<br>2'b10 – 7G Mode<br>2'b11 – 6G Mode | | | | | | | |

# Applications Information

### Typical Configuration

The overall configuration of the MAX5871 includes setting up the clocking as described in the following sections and setting all other configurations before or after that. Configuration registers other than the clocking includes the DSP, JESD204B Clock Multiplier Unit (CMU), SerDes, and Rx Link registers.

### MAX5871 Flow Chart

The following is the overall flowchart from power-up to DAC output enable. Some of the intermediate steps are mode specific and described below.

Power Up

↓

Chip Reset

↓

Clock Setup

↓

FIFO Resets

↓

Mode Setup

↓

Interrupt/Mute Enables

↓

Start Data

↓

Clear and Check Statuses

↓

Unmute DAC

**Power Up**

Ramp up power for all supplies and this does not require any particular order.
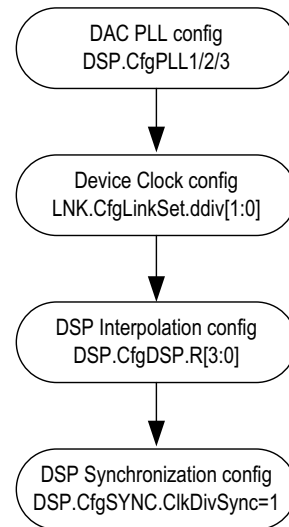
**Chip Reset**

Assert chip reset RESETB for 1µs. After reset release, either monitor the INTB pin to go low or poll the DSP.STATUS.TRDY bit to go high. This indicates that device trimming is complete and is ready for configuration.
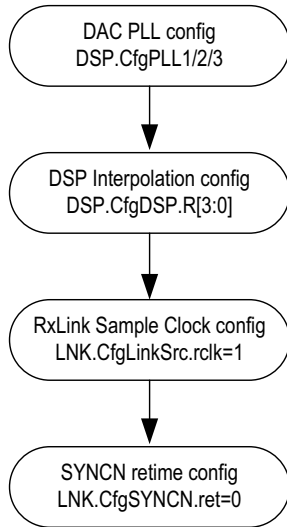
**Clock Setup**

Clock setup includes configuring the clock sources for the DAC, DSP, and JESD204B functions. The clocking depends on the required setup including the following. This also includes the JESD204B subclass mode since it determines how the FIFOs come up centered in a known state.

1) DAC PLL usage

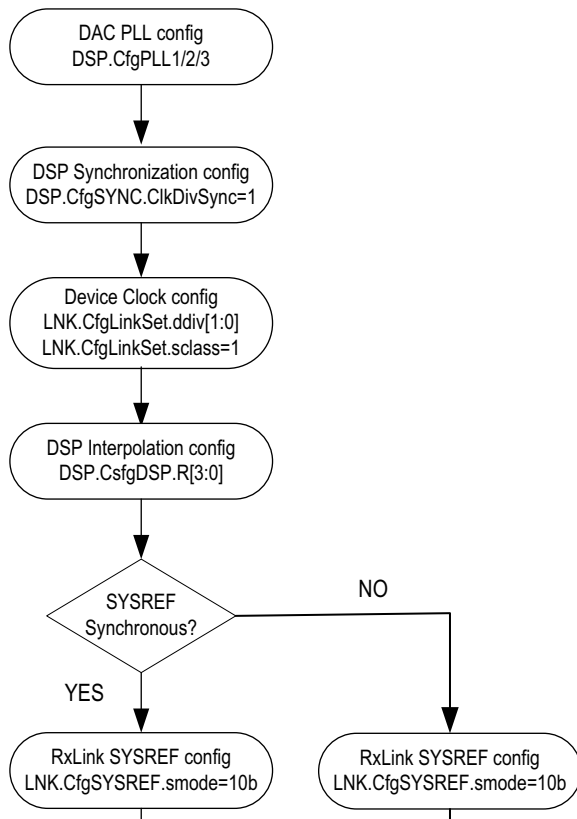2) Device Clock availability for JESD204B function

3) DSP interpolation rate

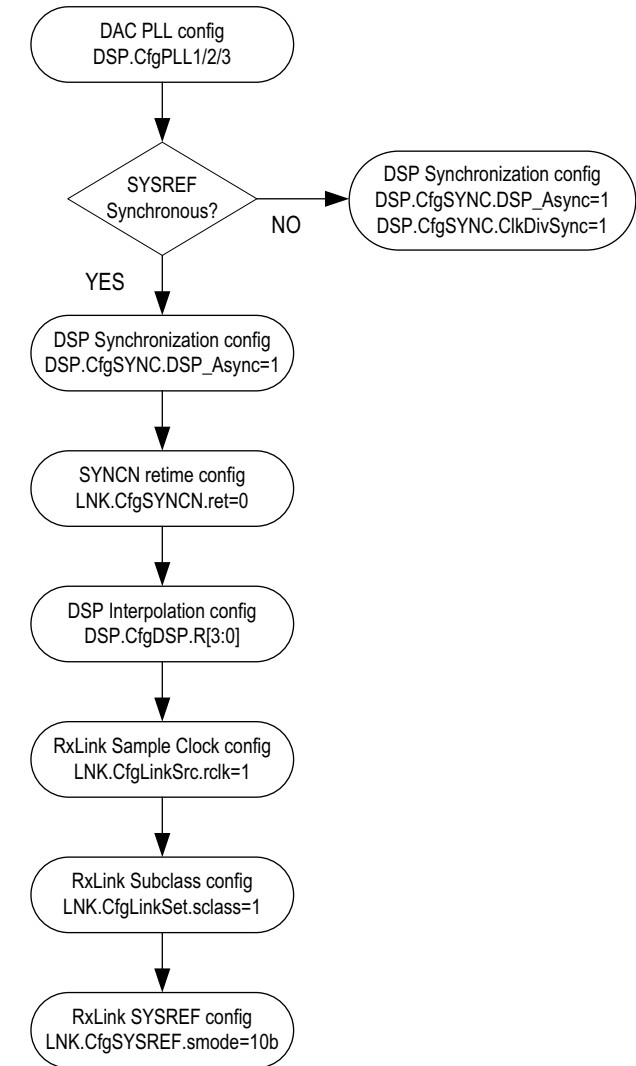For JESD204B Subclass-0 with device clock used for generating the sample clock, the following clock setup is required

DAC PLL config
DSP.CfgPLL1/2/3

↓

Device Clock config
LNK.CfgLinkSet.ddiv[1:0]

↓

DSP Interpolation config
DSP.CfgDSP.R[3:0]

↓

DSP Synchronization config
DSP.CfgSYNC.ClkDivSync=1

For JESD204B Subclass-0 with DSP used for generating the sample clock, the following clock setup is required.

```
      DAC PLL config
     DSP.CfgPLL1/2/3
            │
            ▼
   DSP Interpolation config
     DSP.CfgDSP.R[3:0]
            │
            ▼
  RxLink Sample Clock config
    LNK.CfgLinkSrc.rclk=1
            │
            ▼
    SYNCN retime config
    LNK.CfgSYNCN.ret=0
```

For JESD204B Subclass-1 with device clock used for generating the sample clock and a synchronous SYSREF to device clock, the following clock setup is required.

```
      DAC PLL config
     DSP.CfgPLL1/2/3
            │
            ▼
  DSP Synchronization config
   DSP.CfgSYNC.ClkDivSync=1
            │
            ▼
    Device Clock config
   LNK.CfgLinkSet.ddiv[1:0]
   LNK.CfgLinkSet.sclass=1
            │
            ▼
   DSP Interpolation config
    DSP.CsfgDSP.R[3:0]
            │
            ▼
        SYSREF         ──NO──┐
      Synchronous?           │
            │                │
          YES                │
            ▼                ▼
  RxLink SYSREF config   RxLink SYSREF config
 LNK.CfgSYSREF.smode=10b LNK.CfgSYSREF.smode=10b
```

For JESD204B Subclass-1 with DSP used for generating the sample clock and an asynchronous SYSREF, the following clock setup is required.

```
      DAC PLL config
     DSP.CfgPLL1/2/3
            │
            ▼
        SYSREF         ──NO──→  DSP Synchronization config
      Synchronous?             DSP.CfgSYNC.DSP_Async=1
            │                  DSP.CfgSYNC.ClkDivSync=1
          YES
            ▼
  DSP Synchronization config
   DSP.CfgSYNC.DSP_Async=1
            │
            ▼
    SYNCN retime config
    LNK.CfgSYNCN.ret=0
            │
            ▼
   DSP Interpolation config
     DSP.CfgDSP.R[3:0]
            │
            ▼
  RxLink Sample Clock config
    LNK.CfgLinkSrc.rclk=1
            │
            ▼
    RxLink Subclass config
   LNK.CfgLinkSet.sclass=1
            │
            ▼
    RxLink SYSREF config
  LNK.CfgSYSREF.smode=10b
```
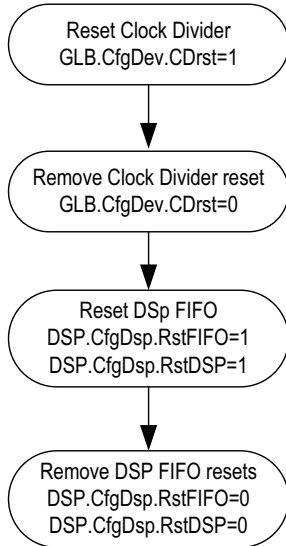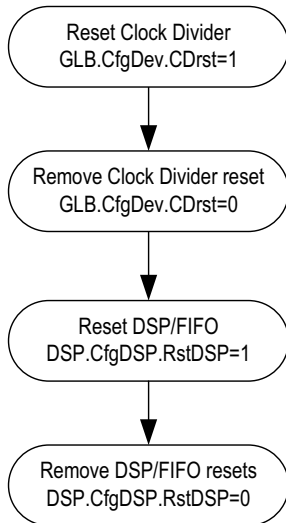
**FIFO Resets**

After the clock modes are setup and after a sufficient wait time for the DAC PLL to lock, the DSP clock divider needs to be reset and then the Rx Link and DSP FIFOs need to be centered through configuration in Subclass-0 mode or SYSREF in Subclass-1 mode.

Subclass-0 with Device Clock

```
┌──────────────────────────┐
│    Reset Clock Divider    │
│    GLB.CfgDev.CDrst=1     │
└──────────────────────────┘
             │
             ▼
┌──────────────────────────┐
│  Remove Clock Divider reset │
│    GLB.CfgDev.CDrst=0     │
└──────────────────────────┘
             │
             ▼
┌──────────────────────────┐
│      Reset DSp FIFO       │
│  DSP.CfgDsp.RstFIFO=1     │
│  DSP.CfgDsp.RstDSP=1      │
└──────────────────────────┘
             │
             ▼
┌──────────────────────────┐
│   Remove DSP FIFO resets  │
│  DSP.CfgDsp.RstFIFO=0     │
│  DSP.CfgDsp.RstDSP=0      │
└──────────────────────────┘
```

Subclass-0 without Device Clock

```
┌──────────────────────────┐
│    Reset Clock Divider    │
│    GLB.CfgDev.CDrst=1     │
└──────────────────────────┘
             │
             ▼
┌──────────────────────────┐
│  Remove Clock Divider reset │
│    GLB.CfgDev.CDrst=0     │
└──────────────────────────┘
             │
             ▼
┌──────────────────────────┐
│      Reset DSP/FIFO       │
│   DSP.CfgDSP.RstDSP=1     │
└──────────────────────────┘
             │
             ▼
┌──────────────────────────┐
│   Remove DSP/FIFO resets  │
│   DSP.CfgDSP.RstDSP=0     │
└──────────────────────────┘
```

Subclass-1 with Device Clock (and Synchronous SYSREF)

Or

Subclass-1 without Device Clock (and Asynchronous SYSREF)

```
┌──────────────────────────┐
│       Pulse SYSREF        │
└──────────────────────────┘
```

```
┌──────────────────────────┐
│        Mode Setup         │
└──────────────────────────┘
```

Setup device modes other than DAC PLL, clocking, synchronization, and resets.

```
┌──────────────────────────┐
│     Interrupt/Mute        │
│        Enables            │
└──────────────────────────┘
```

Enable internal DAC mute and interrupt enables in the JESD204B RxLink and DSP registers.

```
┌──────────────────────────┐
│        Start Data         │
└──────────────────────────┘
```

Start JESD204B link data carrying the signal.

```
┌──────────────────────────┐
│     Clear and Check       │
│        Statuses           │
└──────────────────────────┘
```

Clear all the latched statuses enabled for internal DAC mute and interrupt.

```
┌──────────────────────────┐
│        Unmute DAC         │
└──────────────────────────┘
```

Reset DAC mute register bit (DSP.CfgChipOM.Mute) to enable the DAC output.

## JESD204B Rx Link and DSP Clocking
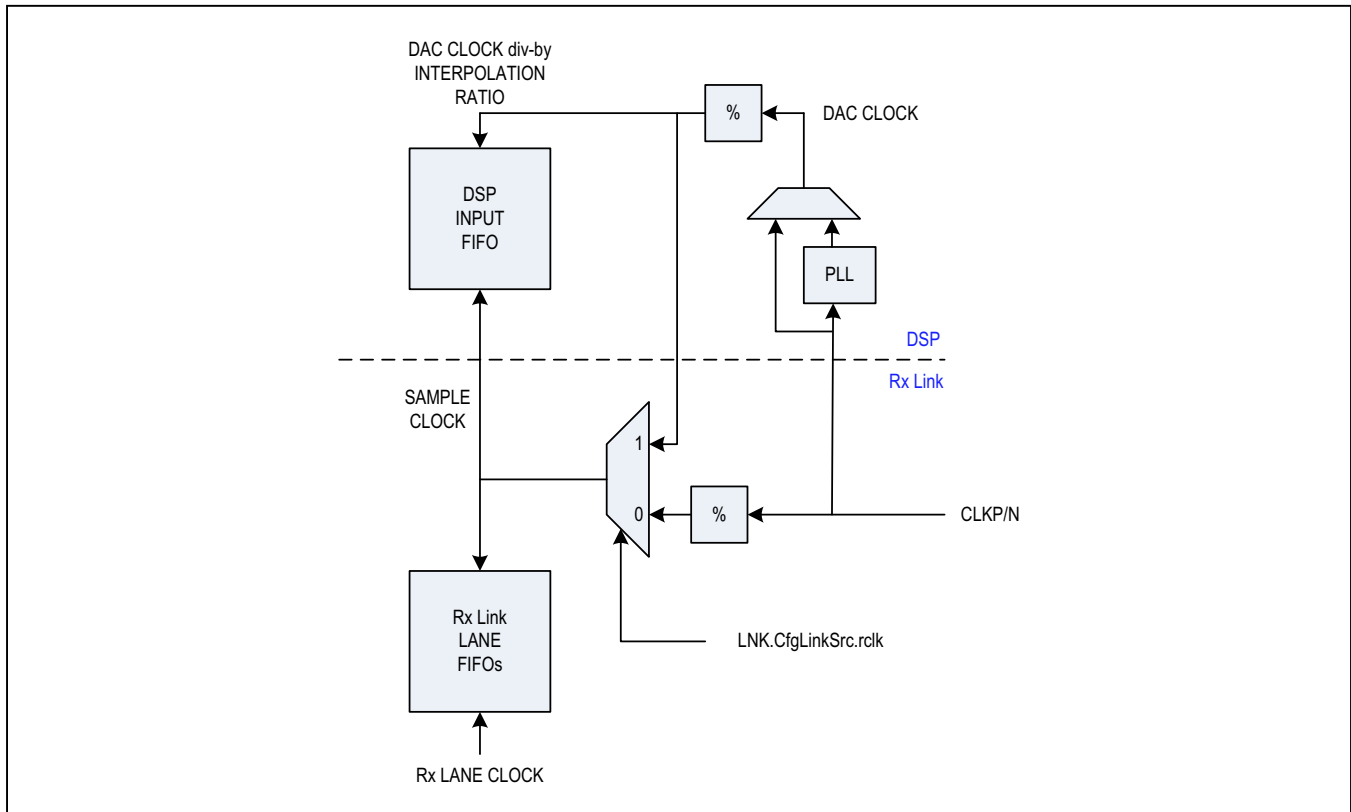


*Figure 40. Rx Link and DSP Clocking*

### Subclass-0 with Device Clock

When there is a device clock present on the CLKP/N pins, the Rx Link sample clock is generated from it and the DSP input FIFO removes the phase difference between this Rx Link sample clock and DSP sample clock. This mode is set by LNK.CfgLinkSrc.rclk=0. The DSP sample clock is stable when the DAC clock is stable through or bypassing the DAC PLL and Interpolation Mode is set via DSP.CfgDSP.R[4:0]. The Rx Link sample clock is stable when the device clock divide mode is selected via LNK.CfgLinkSet.ddiv[1:0]. Once these clocks for the DSP Input FIFO are stable, it needs to be reset to be centered. The Rx Link Lane FIFOs are controlled by the Subclass-0

behavior with minimum latency through the FIFO. The FIFO latency can be increased via LNK.CfgILAD[5:0] in sample clock period increments. The following is the required configuration order for this mode to be stable.

1) Configure DAC PLL registers if DAC PLL is used (DSP.CfgPLL)

2) Configure RxLink device clock divide factor (LNK. CfgLinkSet.ddiv[1:0])

3) Set interpolation mode and reset input FIFO (DSP. CfgDSP.R[3:0], DSP.CfgDSP.RstFIFO)

4) Remove DSP Input FIFO reset (DSP.CfgDSP.Rst-FIFO)

**Subclass-0 without Device Clock**

When there is no device clock present on CLKP/N pins, the RxLink sample clock is sourced from the DSP sample clock clock. This mode is set by LNK.CfgLinkSrc.rclk=1. The DSP sample clock is stable when DAC clock is stable through or bypassing the DAC PLL and interpolation Mode is set via DSP.CfgDSP.R[4:0]. Once this clock for the DSP Input FIFO (same write and read clock) is stable, it needs to be centered by disabling and enabling the FIFO with an adjusted read pointer. The RxLink lane FIFOs are controlled by the subclass0 behavior with minimum latency through the FIFO. The FIFO latency can be increased via LNK.CfgILAD[5:0] in sample clock period increments. The following is the required configuration order for this mode to be stable.

1) Configure DAC PLL registers if DAC PLL is used (DSP.CfgPLL)

2) Set interpolation mode (DSP.CfgDSP.R[3:0])

3) Set the RxLink clock mode (LNK.CfgLinkSrc.rclk=1)

4) Disable the input FIFO and set FIFO read pointer (DSP.CfgFIFO.Off=1, DSP.CfgFIFO.RdPtrAdj[3:0]=6)

5) Enable the input FIFO (DSP.CfgFIFO.Off=0)

6) Disable SYNCN retiming to device clock (LNK.CfgSYNCN.ret=0)

**Subclass-1 with Device Clock**

This is the true JESD204B Subclass1 mode with the SYSREF input synchronous to CLKP/N (device clock) input. The RxLink sample clock is generated from a divide down of device clock. The DSP input FIFO removes the phase difference between the RxLink sample clock and the DSP sample clock. This mode is set by LINK.CfgLinkSrc.rclk=0. The DSP sample clock is stable when DAC clock is stable through or bypassing the DAC PLL and interpolation Mode is set via DSP.CfgDSP.R[4:0]. The RxLink sample clock is stable when the device clock divide mode is selected via LINK.CfgLinkSet.ddiv[1:0]. The Subclass1 deterministic delay process including the LINK.CfgILAD[5:0] sets the RxLink FIFO depths followed by a reset of the DSP input FIFO through the DSP clock divider. The following is the required configuration order for this mode to be stable.

1) Configure DAC PLL registers if DAC PLL is used (DSP.CfgPLL)

2) Enable DSP clock-divider reset from RxLink (DSP.CfgSYNC.ClkDiv_Sync=1)

3) Set interpolation mode (DSP.CfgDSP.R[3:0])

4) Set RxLink device clock divide factor and subclass1 mode (LNK.CfgLinkSset.ddiv[1:0], LNK.CfgLinkSet.sclass[1:0]=01)

5) Enable SYSREF pulses to set RxLink LMFC boundary (LNK.CfgSYSREF.smode[1:0]=10)

**Subclass-1 without Device Clock**

This is a pseudo JESD204B Subclass1 mode with the SYSREF input asynchronous to the CLKP/N input. The RxLink sample clock is sourced from the DSP sample clock. This mode is set by LNK.CfgLinkSrc.rclk=1. The DSP sample clock is stable when DAC clock is stable through or bypassing the DAC PLL and interpolation mode is set via DSP.CfgDSP.R[4:0]. The SYSREF signal centers the DSP Input FIFO through the DSP clock divider followed by the Subclass1 deterministic delay process including the LNK.CfgILAD[5:0] setting RxLink FIFO depths. DSP input FIFO should not be reset through the DSP.CfgDSP.RstFIFO or DSP.CfgDSP.RstDSP in this mode. The SYSREF signal can be a continuous clock or a one-shot pulse. The following is the required configuration order for this mode to be stable.

1) Configure DAC PLL registers if DAC PLL is used (DSP.CfgPLL)

If SYSREF is a continuous clock-like signal:

2) Enable first SYSREF pulse to reset DSP clock divider (DSP.CfgSYNC.DSP_ASync=1)

If SYSREF is a one-shot pulse:

2) Enable continuous SYSREF pulses to reset DSP clock divider (DSP.CfgSYNC.DSP_ASync=1, DSP.CfgSYNC.ClkDiv_Sync=1)

3) Disable SYNCN retiming to device clock (LNK.CfgSYNCN.ret=0)

4) Set interpolation mode (DSP.CfgDSP.R[3:0])

5) Set the RxLink clock mode (LNK.CfgLinkSrc.rclk=1)

6) Set RxLink SYSREF mode (LNK.CfgMDS.rclk=1)

7) Set Subclass1 mode (LNK.CfgLinkSet.sclass[1:0]=01)

8) Enable SYSREF pulses to set RxLink LMFC boundary (LNK.CfgSYSREF.smode[1:0]=10)

## MAX5871 Configuration

The MAX5871 can be configured by following the examples below. There are two groups of registers: fixed and variable. The fixed group of registers given in this example should be used independent of your application. The variable group of registers given in this example should be modified based on the MAX5871 register definition and description for your application, such as DAC sampling rate, DAC clock input, interpolation ratio, SerDes data rate, JESD204B format, and interrupt handling.

## MAX5871 Example Configuration Option-1

Application requirement

DAC Rate = 5898.24MHz

SerDes Rate = 7372.8Mbps

CLKP/N Rate = 1474.56MHz

Equivalent I or Q Sample Rate = 737.28Msps

JESD204B LFS = 411

Interpolation = 8x

NCO Frequency = 800MHz


0x0000,0x99; //GLB.CfgIFA.4Wire=1, SftRst=1 (self-clearing)

0x0010,0x0A; //fDAC=1010b

//DVAL is 32, RVAL is 8, PVAL is 1

0x0181,0x08; //DSP.CfgPLL2.DVAL[1:0]=00b, RVAL0=0, PVAL=1, Bypass=0

0x0182,0x11; //DSP.CfgPLL3.VCOSel=1, DVAL[3:2]=10b, RVAL1=0

0x0180,0x03; //DSP.CfgPLL1.DigTune=1, Reserved=1

0x015A,0x80; //DSP.CfgSYNC.DSP_ASync=1

0x0101,0xB0; //DSP.CfgDSP.R=1011b

0x0427,0x10; //LNK.CfgMDS.rclk=1

0x0412,0x01; //LNK.CfgLinkSrc.rclk=1

0x0402,0x01; //LNK.CfgLinkSet.sclass=01b

0x0403,0x18; //LNK.CfgSYSREF.rsync=1, smode=10b

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0002,0x04; //GLB.CfgDev.CDrst=1

0x0002,0x00; //GLB.CfgDev.CDrst=0

0x0407,0x00; //LNK.CfgSYNCN.ret=0

0x041F,0x04; //LNK.CfgILAmfs.mfsel=4

0x0421,0x03; //LNK.CfgILAsn.snum=3

0x040A,0x0D; //LNK.CfgMLFS.L=4, F=0, S=0, M=1

0x042C,0x0F; //LNK.CfgLnEn.ln=1111b

0x0418,0x0F; //LNK.CfgILALck.lksel=1111b

0x041A,0x05; //LNK.CfgILAD.idly=10

0x0414,0x1C; //LNK.CfgLinkCtl.lcoren=1, fcoren=1, dynfadj=1

0x042D,0x06; //LNK.CfgFIFO.minfd=6

0x042E,0x1A; //LNK.CfgFIFO.maxfd=26

0x0600,0x00; //SER.CfgRst.Rst=0

0x0606,0x03; //SER.CfgRate.RxRateSel=11b

0x0607,0x01; //SER.CfgTrainLn.Ln1IdleGate=0, Ln1DnGate=0

0x0608,0x01; //SER.CfgTrainLn.Ln2IdleGate=0, Ln2DnGate=0

0x0609,0x01; //SER.CfgTrainLn.Ln3IdleGate=0, Ln3DnGate=0

0x060A,0x01; //SER.CfgTrainLn.Ln4IdleGate=0, Ln4DnGate=0

0x060B,0x04; //SER.CfgMisc.BCast=1

0x0704,0x38; //SER.CfgCMU.VCOSEL=10b, FBDIV=11b

0x0706,0x40; //SER.CfgCMU.Cref_divsel1p0=01b

0x0707,0x04; //SER.CfgCMU.cd_tune1p0=100b

0x082F,0x08;

0x082E,0x1F;

0x082D,0x00;

0x082C,0x00;

0x0867,0x00;

0x0866,0x00;

0x0865,0x0C;

0x0864,0x00;

0x084B,0xFF;

0x084A,0x77;

0x0849,0xFD;

0x0848,0x40;

0x0803,0x02;

0x0802,0x10;

0x0801,0x21;

0x0800,0x08;

0x0807,0x04;

0x0806,0xAF;

0x0805,0x40;

0x0804,0x00;

0x0857,0xFC;

0x0856,0x01;

0x0855,0x00;

0x0854,0x35;

0x0863,0x00;

0x0862,0x54;

0x0861,0x00;

0x0860,0x06;

0x0893,0x00;

0x0892,0x51;

0x0891,0x23;

0x0890,0x26;

0x080B,0x0C;

0x080A,0x87;

0x0809,0xD3;

0x0808,0xFF;

0x080F,0x4C;

0x080E,0x15;

0x080D,0x02;

0x080C,0x4E;

0x0813,0x42;

0x0812,0x00;

0x0811,0x20;

0x0810,0x7D;

0x0817,0xFB;

0x0816,0x0A;

0x0815,0x19;

0x0814,0xE9;

0x081B,0x00;

0x081A,0x00;

0x0819,0x07;

0x0818,0x75;

0x081F,0x80;

0x081E,0xFF;

0x081D,0x08;

0x081C,0x00;

0x0823,0x07;

0x0822,0x20;

0x0821,0x10;

0x0820,0x00;

0x0827,0x00;

0x0826,0x3F;

0x0825,0x10;

0x0824,0x00;

0x0833,0x1F;

0x0832,0x7F;

0x0831,0x20;

0x0830,0x00;

0x088F,0x00;

0x088E,0x00;

0x088D,0x80;

0x088C,0x80;

0x08AB,0x00;

0x08AA,0x04;

0x08A9,0x43;

0x08A8,0x01;

0x083F,0xAF;

0x083E,0x34;

0x083D,0xAF;

0x083C,0x80;

0x0843,0x00; //Status

0x0842,0x00;

0x0841,0x00;

0x0840,0x00;

0x0847,0x10;

0x0846,0x00;

0x0845,0x80;

0x0844,0x80;

0x0853,0x2A;

0x0852,0x8B;

0x0851,0x40;

0x0850,0x20;

0x085F,0x7F;

0x085E,0x01;

0x085D,0x3F;

0x085C,0xFF;

0x084F,0x00;

0x084E,0x40;

0x084D,0x00;

0x084C,0x18;

0x086B,0x00;

0x086A,0x00;

0x0869,0x2A;

0x0868,0x25;

0x086F,0xC0;

0x086E,0x00;

0x086D,0x02;

0x086C,0xEE;

0x0873,0x00;

0x0872,0x00;

0x0871,0x00;

0x0870,0x00;

0x087B,0x00;

0x087A,0x7F;

0x0879,0xD5;

0x0878,0x56;

0x087F,0xC5;

0x087E,0x46;

0x087D,0x1C;

0x087C,0x17;

0x0102,0x1C; //DSP.CfgNCOF0=1Ch

0x0103,0xC7; //DSP.CfgNCOF1=C7h

0x0104,0x71; //DSP.CfgNCOF2=71h

0x0105,0x45; //DSP.CfgNCOF3=45h

0x0101,0xB1; //DSP.CfgDSP.R=1011b, NCOLoad=1

0x0100,0x45;   //DSP.CfgChipOM.RclkM=2,   DFMT=1,
Mute=1

0x000F,0x01; //GLB.CfgIFC.Xfer=1

0x0000,0x3C;   //DSP.CfgChipOM.RclkM=2,   DFMT=1,
Mute=0

## JESD204B Subclass-1 SYSREF Signal Functionality

There are two modes of JESD204B Subclass-1 operation: synchronous SYSREF mode and asynchronous SYSREF mode. The synchronous SYSREF mode is as described in the standard with SYSREF timed synchronously to the device clock. The asynchronous SYSREF mode does not require a device clock and so SYSREF has no timing reference. The JESD204B sample clock is sourced from the DSP in this case.

### Synchronous SYSREF Mode

As described for the JESD204B Subclass-1 deterministic delay, the SYSREF input signal is synchronous to the device clock input (CLKP/N) and the sample clock is sourced from the device clock. The SYSREF signal can be generated from a clock generator module in which case the SYSREF will be a divided down version of the device clock. Register configurations exist as below to respond to either the first SYSREF pulse or all SYSREF pulses.

LNK.CfgSYSREF.smode[1:0] – when smode[1] is high, all SYSREF pulses are acted upon. When smode[1] is low, only the first SYSREF pulse after smode[0] is toggled 0->1 will be acted upon. If CfgSYSREF.ignore_en is set, then the ignore function is given a higher priority smode[1:0]=01 will enable first SYSREF only after the CfgSIGN.ign[7:0] pulses are ignored.

This is required for the case of the device clock frequency being higher than what is supported by the MAX5871 and SYSREF timing to the device clock is not truly synchronous. An uncertainty of one device clock in sampling SYSREF is allowed in this case. If all SYSREF pulses are enabled, the internal frame/multiframe clocks may not be stable and so only one SYSREF pulse needs to be enabled for link establishment.

In the case where multiple converters need to be aligned, a register write to enable a single SYSREF pulse may not be suitable as the synchronization of these register writes may be harder. This can be handled by using a hardware enable of SYSREF through the SYSREF_EN pin as shown in the timing diagram below.

LNK.CfgSYSREF.senext – When this bit is set, the CfgSYSREF.smode[1:0] are ignored and the external pin sysref_en is used instead. This allows for better timing control of enabling SYSREF pulses to affect LMFC.

## Asynchronous SYSREF Mode

In this mode, a device clock is not required and SYSREF is used for JESD204B Subclass1 mode through the DSP. The DSP generates the sample clock and a synchronous signal to replace the JESD204B RxLink SYSREF input. This mode is enabled by setting the following configuration register bits.

LNK.CfgLinkSrc.rclk – when set, the sample clock is sourced from RCLK input instead of the device clock. Along with setting this bit high, an equivalent bit in the DSP, CfgSync.DSP_ASync, needs to be set to ignore the VALID output from this block and instead use the SYNCO output (SYSREF passed through) and generate RSYNC based on it. This affects the multi-DAC synchronization and the CfgMDS.rclk also needs to be set for the link to replace SYSREF with RSYNC at the same time RCLK is used for sample clock.

LNK.CfgMDS.rclk – when set, RSYNC input from DSP/DAC replaces the SYSREF input for multi-DAC synchronization when there is no device clock supplied. This bit should be used in conjunction with CfgLinkSrc.rclk.

DSP.CfgSync.DSP_ASync – when set, asynchronous SYSREF reset to the DSP is enabled.

The SYSREF_EN input signal is ignored in this mode, the SYSREF_EN pin (also called SYSREFEN) should be connected to the VDD2 supply. The same issue described in the synchronous SYSREF mode exists here if SYSREF is a continuous clock-like signal due to its asynchronous timing. Instead, if SYSREF is generated as a one-shot pulse, then the register bit DSP.CfgSync.ClkDiv_Sync should be set high for the DSP to respond to all the SYSREF pulses as shown below.

DSP.CfgSync.ClkDiv_Sync – when set and DSP_Async=1, enable continuous asynchronous SYSREF reset to the clock-divider block. When cleared and DSP_Async=1, enable first asynchronous SYSREF reset to the clock-divider block.

If the SYSREF signal is generated as a continuous clock, then the register bit DSP.CfgSync.ClkDiv_Sync should be set low for the DSP to respond to one of the SYSREF pulses as shown below.
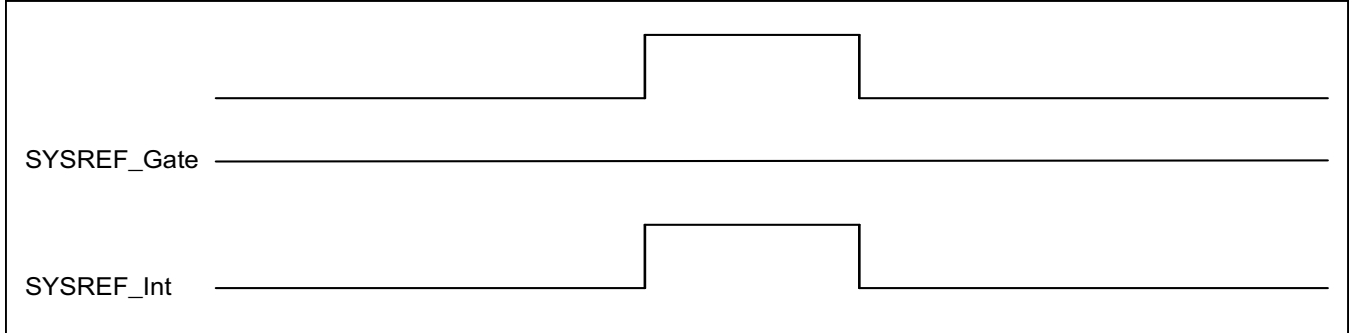


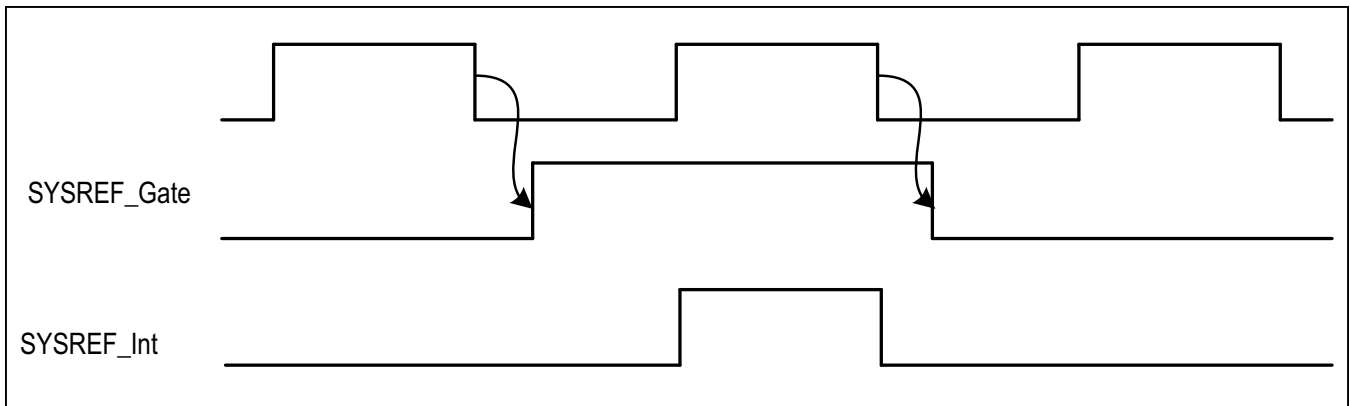Figure 41. Asynchronous SYSREF Mode with One-Shot Pulse



Figure 42. Asynchronous SYSREF Mode with Continuous Pulses

## Applications Guidelines

### Power Sequence

The MAX5871 typically does not require a specific power sequence on which power supplies should be up first, and which is next. It is recommended that all the supplies are powered up around the same time.

### Power Supply AVCLK

Power supply AVCLK is the most sensitive clock. To achieve specified DAC performance, this supply should NOT be shared with other 1.0V supplies. It should absolutely not be shared with digital $V_{DD}$ 1.0V supply.

### Power-On RESETB and SPI Configuration

During the initial power-on, the RESETB pin should be held low during the power-on of the device. In addition, RESETB has an internal pulldown resistor about 32kΩ. This pin should be pull-high after all the power supplies are completely on.

Another way to handle the RESETB is to pull the RESETB to low after the power supplies are fully up, and then pull the RESETB to high.

There is a delay time required after the RESETB is high to SPI configuration can be started. The delay time is to allow the device finishing the initialization process. The delay is related to the CLKP/N frequency. It is about 250µs with CLKP/N device clock frequency of 1.47GHz.

### Delay Time TD_DivRst Estimation

Adding proper delay time before resetting the internal divider is important to make sure that the internal divider starts with a stable clock after the DAC PLL (or external CLKP/N) is fully locked and settled. The minimum time is estimated as (220/PFD_FREQ), where PFD_FREQ is the input frequency of the DAC PLL phase frequency detector in PLL on mode. For example, when CLKP/N frequency is at 982.68MHz, the reference divider RVAL is set to be 1/4, PFD_FREQ = 982.68/4 = 245.67MHz. The TD_DivRst is estimated as 4.3ms.

### Pin DACREF Consideration

The 1.27kΩ resistor from FSADJ (B2) should connect directly to DACREF (B1). This should be placed on the same side as the MAX5871 package and as close as possible to the package. Also, 1µF capacitors connected to REFIO(A1) and CSBP (A2) should connect to DACREF, not GND. These should also be placed on the same layer as the DAC package, avoiding VIAs in all these traces if possible. DACREF is not connected to GND externally.

### DAC PLL Consideration

Connections to PLL_COMP(A12) and VCOBYP(B11)—loop filter for the PLL (see Figure 29). Place external components on the PCB layer opposite the CLK and OUTPUT circuits to prevent them from coupling. The recommended filter between PLL_COMP(A12) and VCOBYP(B11) is 650Ω in series with 4.7nF. The capacitor, C1, reduces noise from GND(A11) to VCOBYP(B11). Place C1 directly under the balls/vias of the package to make this loop as small as possible. The exact values of C1 and C2 vary because they depend on PCB layout, and may or may not be required for optimal performance.

### Pin SDO Consideration

In 4-wire SPI interface mode, SDO is used as a data output. When connecting multiple SDOs together using CSB to access the MAX5871, it is recommended to have a pullup 10kΩ resistor on the input of FPGA or ASIC to prevent floating (need a different term) bus. When SDO is not selected, it outputs tri-state (need a different term due to copyright issues),

### Clock Requirement

The MAX5871 can be operated with DAC PLL ON or DAC PLL OFF.

When DAC PLL is OFF, a clock requirement document is available upon request.

When DAC PLL is ON, the DAC PLL bandwidth is set to around 100kHz. It means that any phase noise/jitter of the reference clock at frequency offsets higher than 100kHz will be filtered out by the PLL loop and its impact on the DAC performance will be minimal.

However, for offsets smaller than 100kHz, the reference clock phase noise will dominate. At those offsets, the reference clock phase noise will be translated to the DAC output phase noise according to the formula:

$$PNout \ [dBc/Hz] = PNref \ [dBc/Hz] + 20 \times log(f_C/f_{REF})$$

Where:

PNout – DAC output phase noise

PNref – PLL reference clock phase noise

$f_C$ – DAC output frequency

$f_{REF}$ – PLL reference clock frequency

In addition to the reference clock phase noise and jitter, the allowable spur level in the reference clock spectrum should be calculated using graphs and equations that are available upon request.

## NCO Frequency

NCO frequency can have two types of errors from the NCO and DAC clocks used. One type of error is from NCO itself due to finite word length. The frequency error can be calculated by $f_{error} = f_{desired} - f_{DAC}/((218) \times (233) \times 2)$. This is about 1.11µHz error at 5GHz DAC clock rate that is negligible.

Register DFW has 19 bits and NFW has 18 bits. To minimize NCO frequency error, DFW can be always programmed to 0x3FFFF and set NFW based on the fractional portion of the calculated FCW. This limits the NCO frequency error to 1.11µHz. The MATLAB code however can give an error of 0Hz if possible.

Another error is related to DAC input sampling clock. The NCO synthesizes frequency, which is an exact faction of the DAC core clock frequency. That fraction value can be calculated using equation provided in the data sheet. Any percentage error in the DAC input clock, either with PLL enabled or disabled will result in the same percentage error at the NCO output. For example, if the DAC input clock has a tolerance of 10ppm, the NCO output frequency will also have a tolerance of 10ppm.

The DAC PLL does not introduce any frequency error once it is locked. The PLL output frequency is exactly equal to the input reference frequency multiplied by the selected PLL multiplication factor.

## Latency

There are two types of latencies in MAX5871: JESD204B latency and DAC latency.

The JESD204B Rx link layer includes a lane processing latency and this combined with the transmit link latency and the channel latency, the Subclass-1 deterministic delay should be set through the MAX5871 configuration. This process is to be characterized from silicon evaluation. The lane processing delay portion of the JESD204B RxLink is 200 SerDes bit clocks. In addition to this, there would be a FIFO delay in sample clock periods as configured for Subclass1 deterministic delay.

The DAC latency is given in the Electrical Characteristics table in the unit of DAC clock periods.

## Turn off JESD204B Transmitter

The MAX5871 JESD204B consists of both receiver and transmitter blocks. The transmitter is only for manufacturer test purposes. To make sure the transmitters are turned off to save power consumption, the following configuration can be used:

Write 0x0849 = 0xC1  to turn off SerDes TX

## PRBS Sequence

PRBS7 and PRBS 23 are supposed to be inverted according to Table 3 in http://www.xilinx.com/support/documentation/application_notes/xapp884_PRBS_GeneratorChecker.pdf

The MAX5871 Rx PHY has an option to invert the data by setting PHY.MISC_REG2.Rx_parallel_data_invert (bit 4).

## DSP FIFO Reading

When reading the DSP FIFO register, the number of ones indicates the FIFO level. The 0x1F depth indicates that the level is 5, meaning that the read pointer is behind the write pointer by 5. The FIFO level should be used only for debug. The error conditions are DSP.STATUS.FCOL and DSP.STATUS.F1A while the third status DSP.STATUS.F2A is a warning condition (close to overflow or underflow, one specifically can be determined through DSP.iFIFOLevel).

## DAC Output Impedance Model and Matching Network

The DAC output impedance model is available in an s-parameter file that can be used to design an output matching network if needed.

For the best engineering practice, the following guidelines can help in the output PCB design:

- DAC OUTP and OUTN routes to the matching network should be as short as possible. From the matching network to any filter should be as short as possible.

- DAC OUTP and OUTN should be routed symmetrically to eliminate any mismatch.

- The environment around OUTP and OUTN should be symmetrical. This means that the environment on one signal needs to match the other signal.

- If OUTP and OUTN cannot be made to be short trace routes, then the routes need to match length with mirror symmetry and 50Ω routed impedance.

- When crossing other signals/supplies routed on other layers, OUTP and OUTN should cross at a 90-degree angle to these signals/supplies.

- OUTP and OUTN should be routed on an outer board layer and away from supply decoupling.

- AVCLK network should not be placed and routed in the proximity of OUTP and OUTN.

**Thermal Considerations**

The use of as much ground plane as possible on the component layer is recommended for the PCB design. The system design should make use of additional heatsinking directly in contact with the MAX5871 to improve the thermal performance. The thermal numbers are based on JEDEC standard 51-12. All the application thermal modeling is required at the system design. A Delphi model is available for system thermal simulation.

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------|-----------|-------------|
| MAX5871EXE+ | -40ºC to +85ºC | 144-FCCSP |

*+Denotes a lead-free/RoHS-compliant package.*

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PIN-PACKAGE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|-------------|--------------|-------------|------------------|
| 144 FCCSP | X14400F+1 | 21-0732 | — |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 3/15 | Initial release | — |
| 1 | 7/19 | Updated Electrical Characteristics, Pin Description table, Figure 11, DSP configuration table, and MAX5871 Configuration | 9, 20, 30, 66, 100–104 |