

Serial-in / Parallel-out Driver Series

# 2-input Serial-in / Parallel-out Drivers

**BU2090F BU2090FS**

**Description**

BU2090F/BU2090FS are an open drain output driver. It incorporates a built-in shift register and a latch circuit to turn on a maximum of 12 Outputs by a 2-line interface, linked to a microcontroller. An open-drain output provides maximum 25mA current.

**Key Specifications**

- Power supply voltage range: 2.7V to 5.5V
- Output voltage: 0V to 25V
- Operating temperature range: -40°C to +85°C

**Features**

- LED can be driven directly
- 12 bit parallel output
- This product can be operated on low voltage

**Package**

SOP16  
SSOP-A16

W(Typ) x D(Typ) x H(Max)  
10.00mm x 6.20mm x 1.71mm  
6.60mm x 6.20mm x 1.71mm

**Applications**

- Drive of LED
- Drive of Solenoid
- Drive of Relay



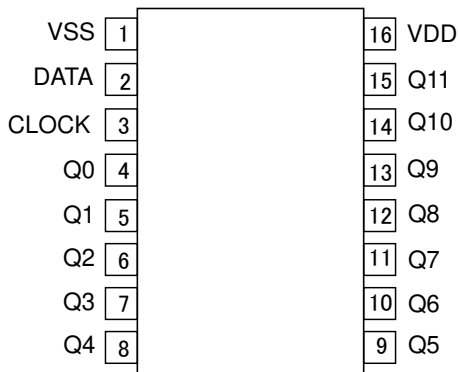
SOP16  
BU2090F



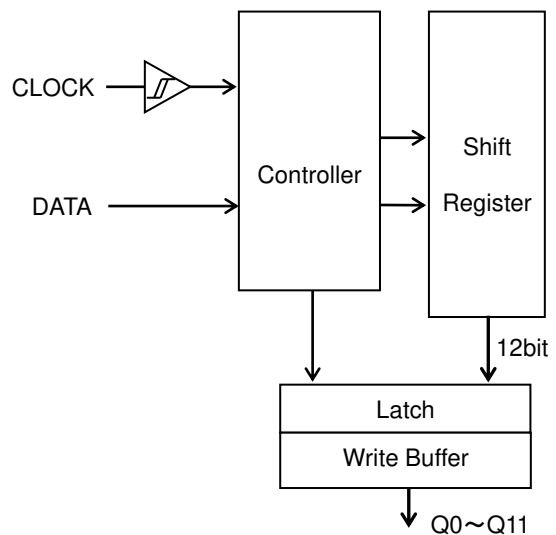
SSOP-A16  
BU2090FS

**Pin Configurations**

(Top View)



**Block Diagrams**



## Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	VSS	-	Ground
2	DATA	I	Serial data input
3	CLOCK	I	Serial clock input
4	Q0	O	Parallel data output (Nch Open-Drain )
5	Q1		
6	Q2		
7	Q3		
8	Q4		
9	Q5		
10	Q6		
11	Q7		
12	Q8		
13	Q9		
14	Q10		
15	Q11		
16	VDD	-	Power supply

## Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Power Supply Voltage	$V_{DD}$	-0.3 to +7.0	V
Input Voltage	$V_{IN}$	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Voltage	$V_O$	$V_{SS}-0.3$ to +25	V
Operating Temperature	$T_{opr}$	-40 to +85	°C
Storage Temperature	$T_{stg}$	-55 to +125	°C
Power Dissipation	$P_D$	0.50 (Note 1)	W
		0.65 (Note 2)	

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 5.0mW per 1°C above 25°C.

(Note 2) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 6.5mW per 1°C above 25°C.

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions ( $T_A=25^\circ\text{C}$ ,  $V_{SS}=0\text{V}$ )

Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{DD}$	+2.7 to +5.5	V
Output voltage	$V_O$	0 to +25	V

**Electrical Characteristics**

DC Characteristics

(unless otherwise noted,  $V_{DD}=5V$ ,  $V_{SS}=0V$ ,  $T_A = 25^\circ C$ )

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input High-level voltage	$V_{IH}$	3.5	-	-	V	
Input Low-level voltage	$V_{IL}$	-	-	1.5	V	
Output Low-level voltage	$V_{OL}$	-	-	2.0	V	$I_{OL}=20mA$
Input High-level current	$I_{IH}$	-	-	2.0	$\mu A$	$V_{IN}=V_{DD}$
Input Low-level current	$I_{IL}$	-	-	-2.0	$\mu A$	$V_{IN}=0$
“H” output leak current	$I_{OZH}$	-	-	10	$\mu A$	$V_O=25V$
“L” output leak current	$I_{OZL}$	-	-	-5.0	$\mu A$	$V_O=0V$
Static dissipation current	$I_{DD}$	-	-	5.0	$\mu A$	

Timing Characteristics

(Unless otherwise noted,  $V_{DD}=5V$ ,  $V_{SS}=0V$ ,  $T_A = 25^\circ C$ )

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Minimum clock frequency	$t_w$	500	-	-	ns	
Data shift set up time	$t_{SU}$	200	-	-	ns	
Data shift hold time	$t_H$	200	-	-	ns	
Data latch set up time	$t_{LSUH}$	50	-	-	ns	
Data latch hold time	$t_{LHH}$	250	-	-	ns	
Data latch “L” set up time	$t_{LSUL}$	200	-	-	ns	
Data latch “L” hold time	$t_{LHL}$	250	-	-	ns	

Waveform of Timing Characteristics

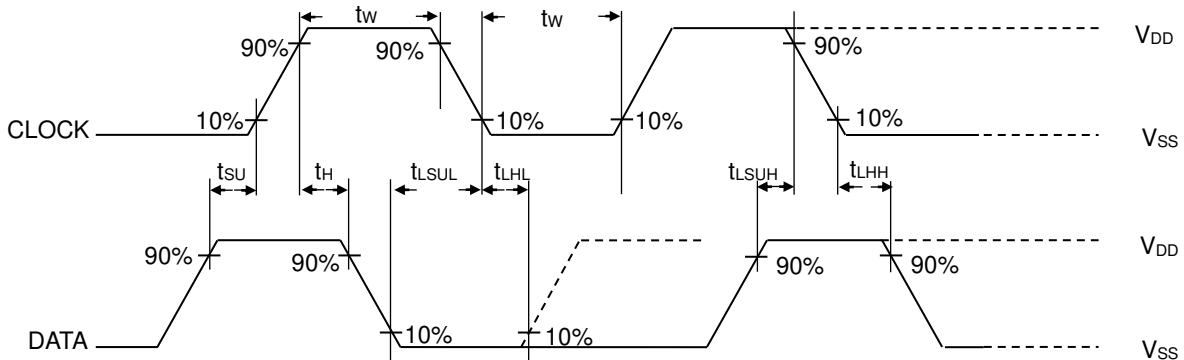


Figure 1. Waveform of Timing Characteristics

Test Circuits

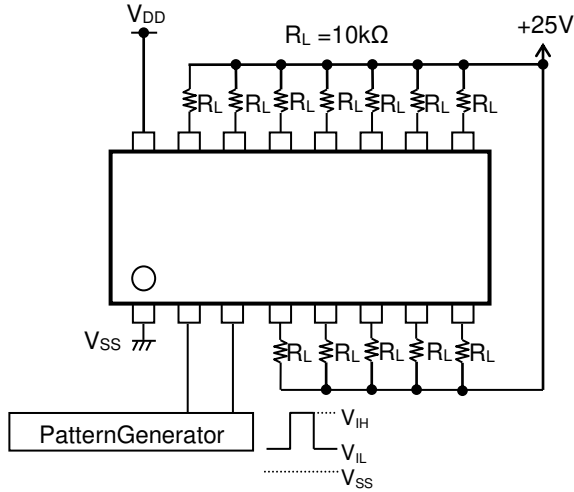


Figure 2. Test Circuit of Input H/L Voltage

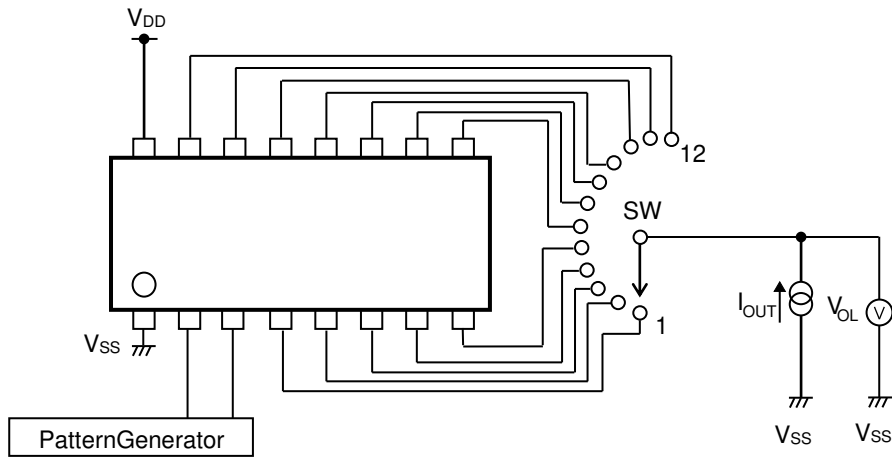


Figure 3. Test Circuit of Output L Voltage

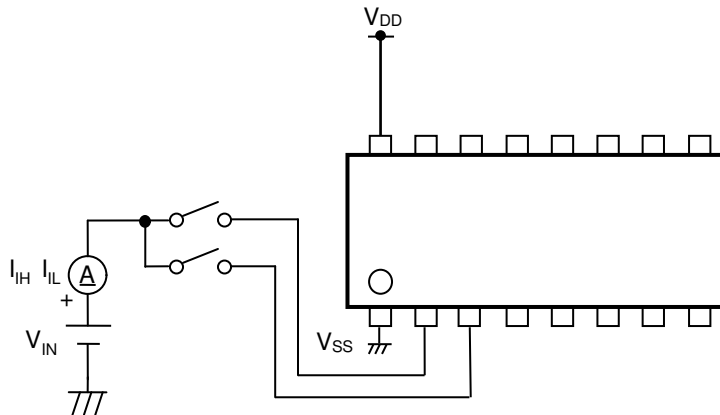


Figure 4. Test Circuit of Input H/L Current

Test Circuits - continued

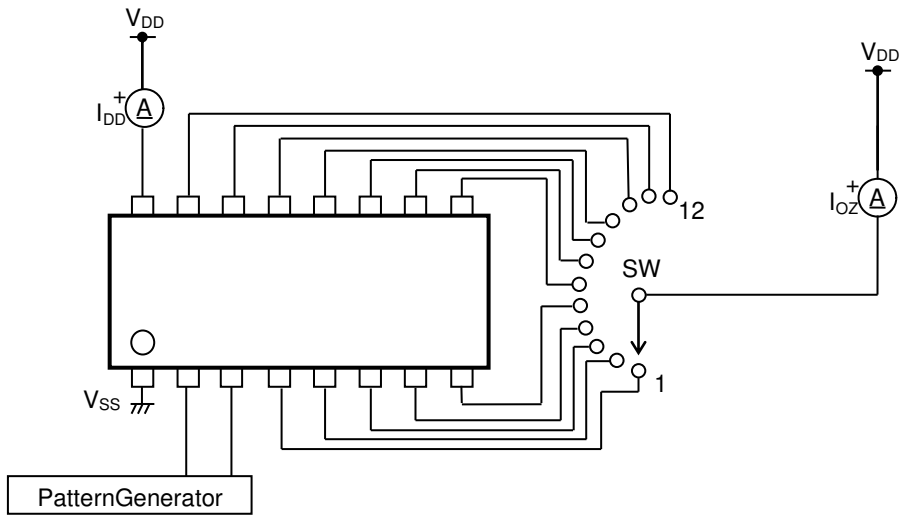


Figure 5. Test Circuit of Output Leak Current / Static Dissipation Current

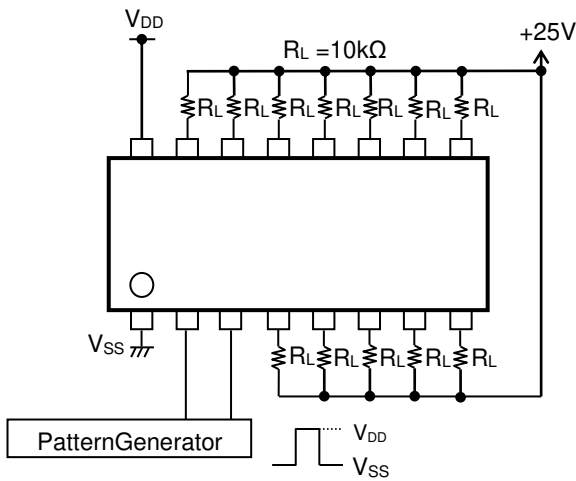


Figure 6. Test Circuit of Timing Characteristics

**Power Dissipation**

Power dissipation(total loss) indicates the power that can be consumed by IC at  $T_A=25^{\circ}\text{C}$ (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol  $\theta_{JA}$  ( $^{\circ}\text{C}/\text{W}$ ).The temperature of IC inside the package can be estimated by this thermal resistance. Figure 11 shows the model of thermal resistance of the package. Thermal resistance  $\theta_{JA}$ , ambient temperature  $T_A$ , maximum junction temperature  $T_{Jmax}$ , and power dissipation  $P_D$  can be calculated by the equation below:

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad (^{\circ}\text{C}/\text{W})$$

Derating curve in Figure 12 indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance  $\theta_{JA}$ . Thermal resistance  $\theta_{JA}$  depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition.

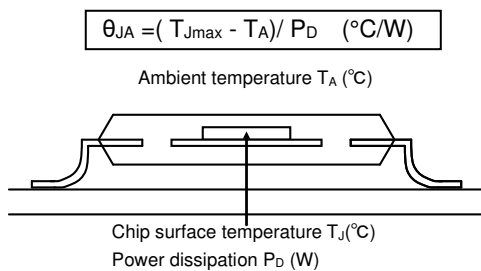


Figure 7. Thermal resistance

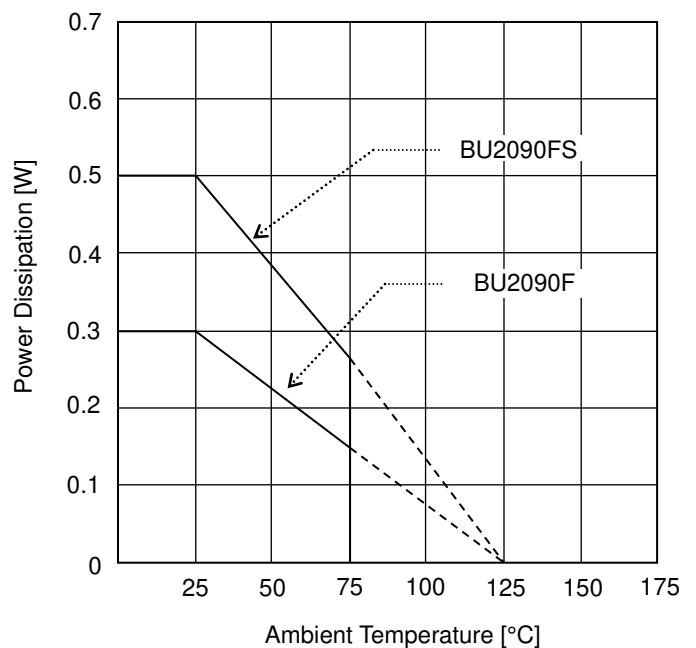
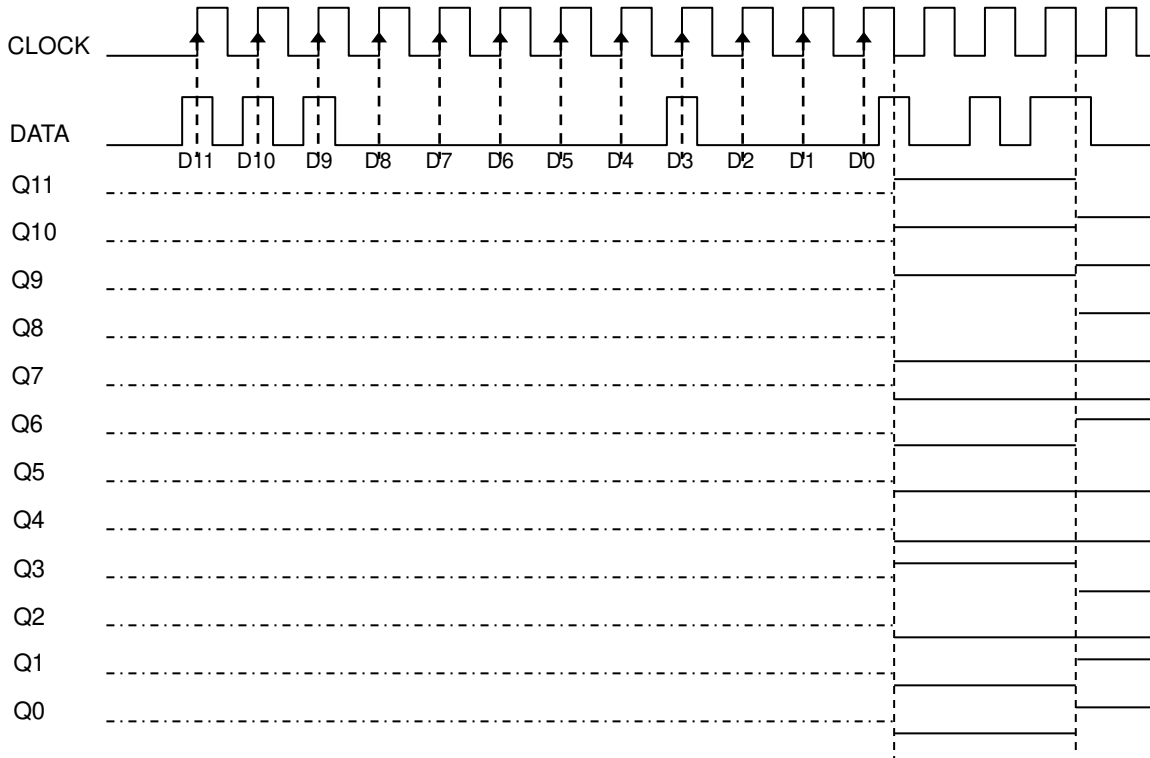


Figure 8. Derating Curve

Timing Chart

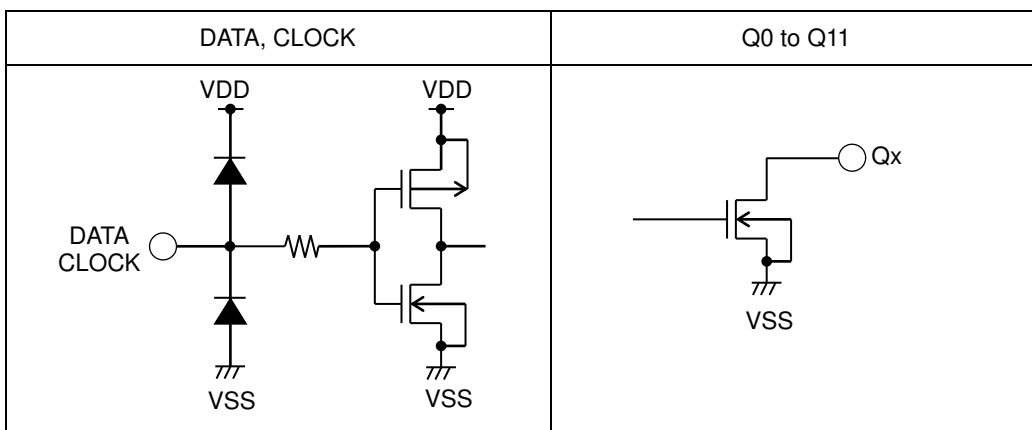


Note3) - - - - - Indicates undefined output.

Note4) Output terminal is provided with a pull-up resistor.

Figure 9. Timing chart

I/O Equivalence Circuits



## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.



Operational Notes – continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

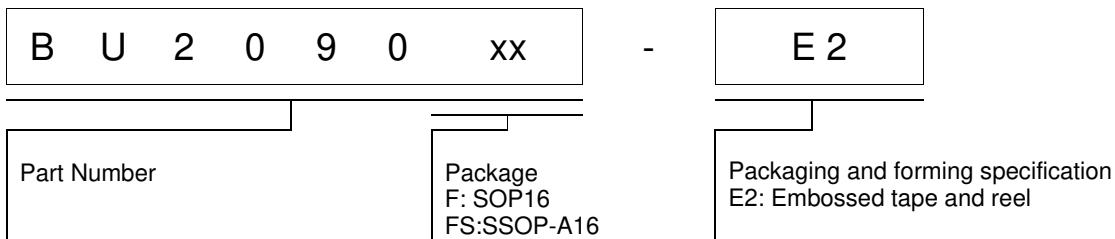
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

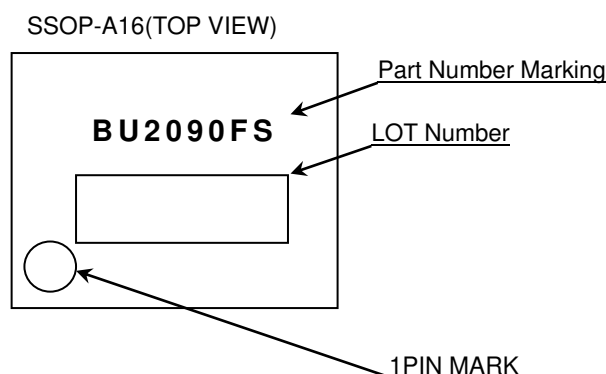
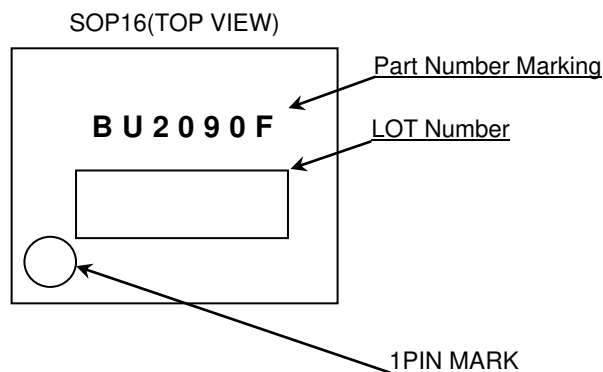
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Ordering Information

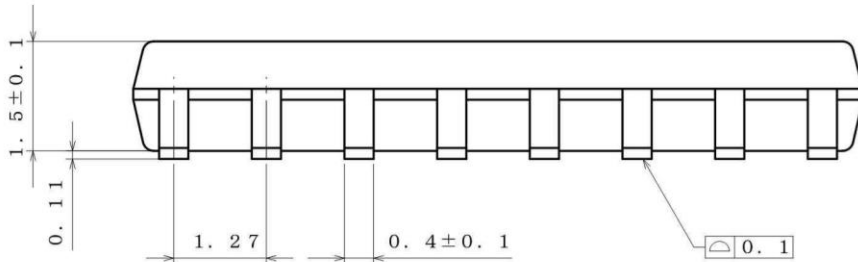
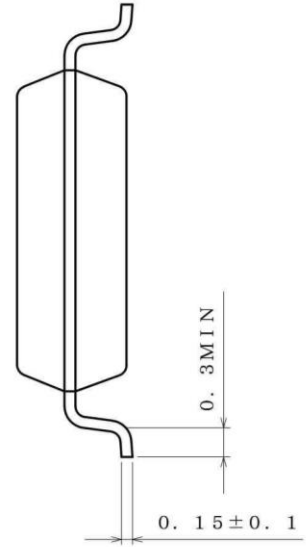
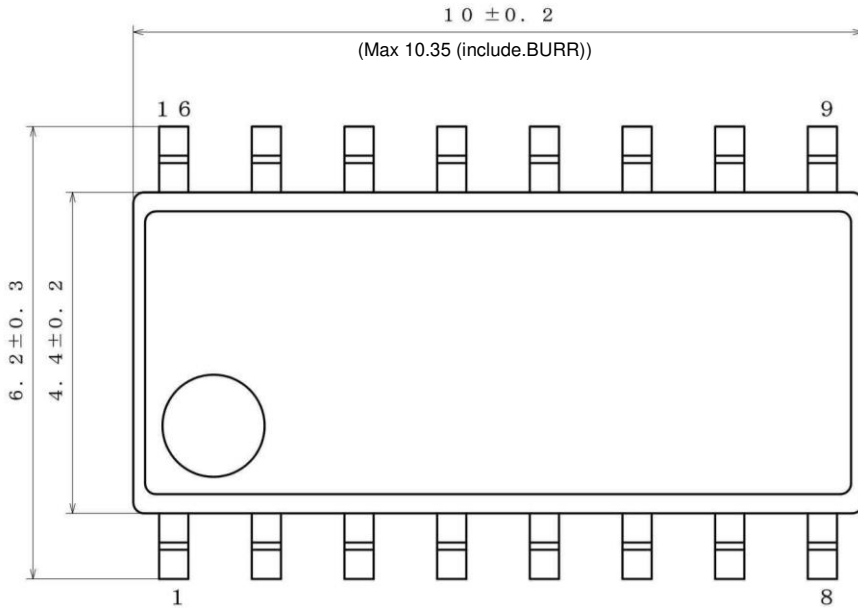


Marking Diagrams



Physical Dimension, Tape and Reel Information

Package Name	SOP16
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(UNIT : mm)  
PKG : SOP16  
Drawing No. : EX114-5001

**<Tape and Reel information>**

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand )

Reel

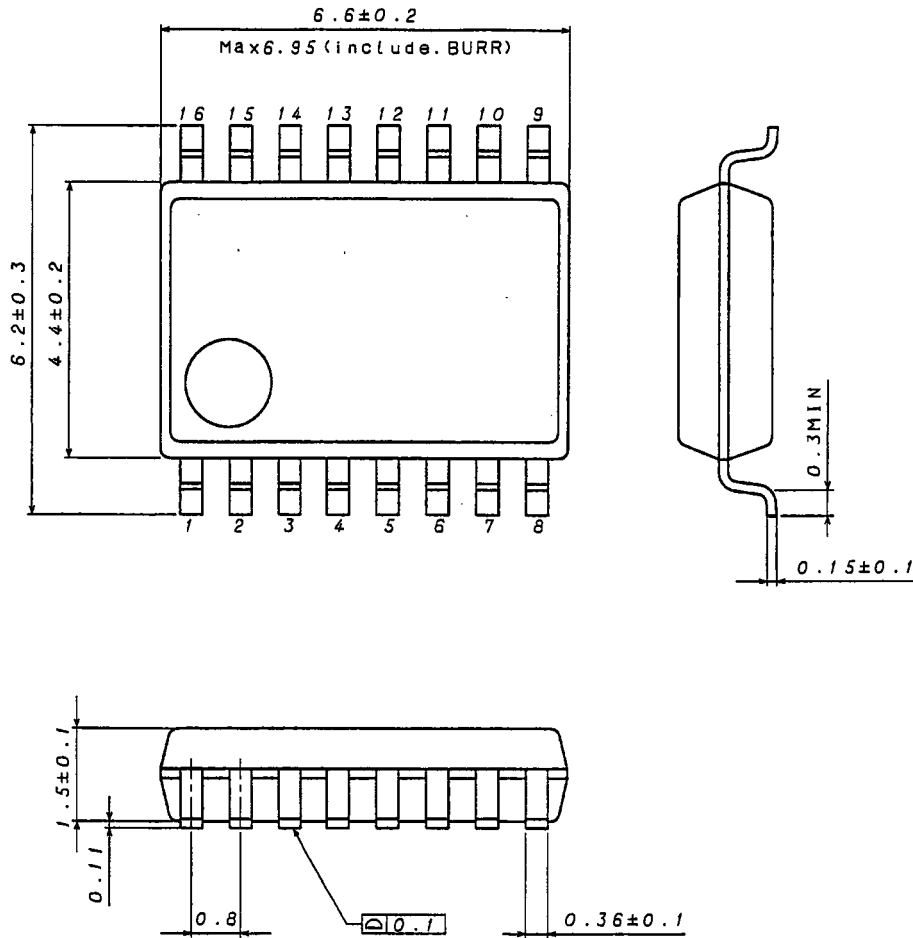
1pin

Direction of feed

\* Order quantity needs to be multiple of the minimum quantity.

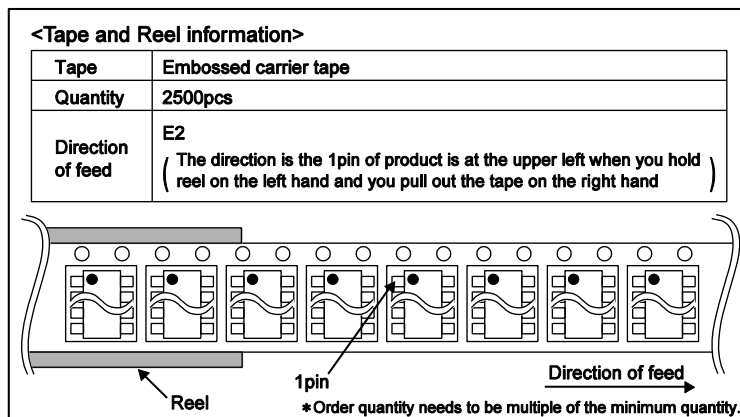
Physical Dimension, Tape and Reel Information

Package Name	SSOP-A16
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(UNIT : mm)

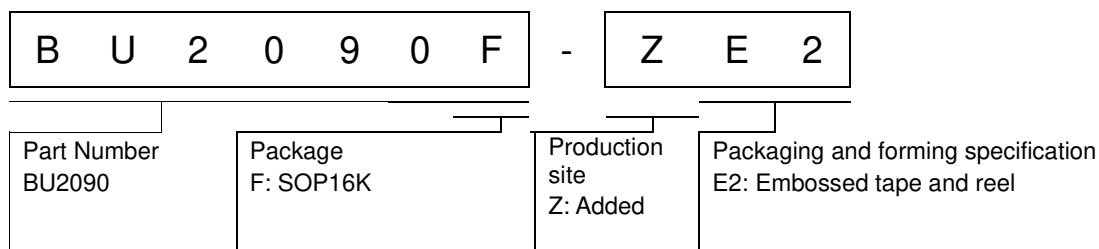
PKG:SSOP-A16  
Drawing No.EX131-5002



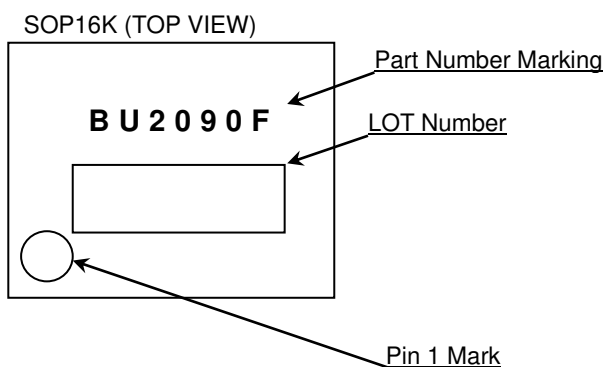
**Revision History**

Date	Revision	Changes
25.Oct.2013	001	New Release
18.Sep.2015	002	Page.8,9 Updated Operational Notes.
11.Dec.2020	003	P.12-2, 12-3, Updated packages and part numbers.

Ordering Information

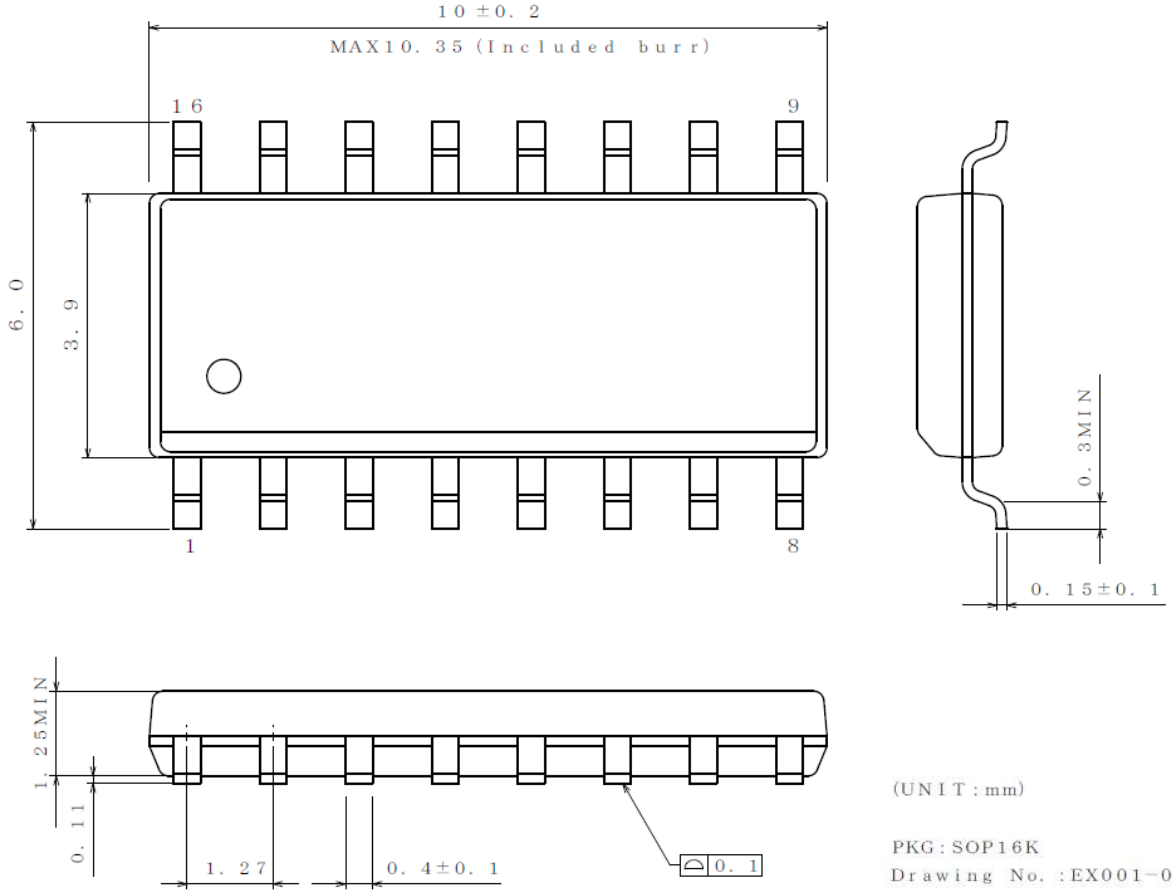


Marking Diagram



Physical Dimension and Packing Information

Package Name	SOP16K
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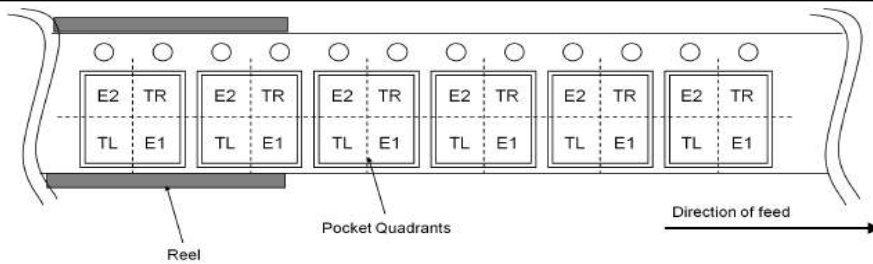
(UNIT : mm)

PKG : SOP16K

Drawing No. : EX001-0106

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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CLASS IV		CLASS III	

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  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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