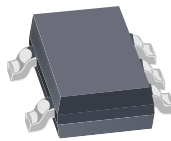


Chopper-Stabilized Precision Hall-Effect Switch with Advanced Diagnostics

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- Unipolar switch points
- Externally enabled diagnostics feature
- Diagnostics feature exercises the entire magnetic and electrical signal path within the IC
- Resistant to physical stress
- Superior temperature stability through advanced chopper stabilization techniques
- Output short-circuit protection
- Internal regulator enables operation from unregulated supplies
- Reverse-battery protection
- Solid-state reliability
- Small surface-mount package

PACKAGE: 5-pin SOT23W (suffix LH)



Approximate footprint



DESCRIPTION

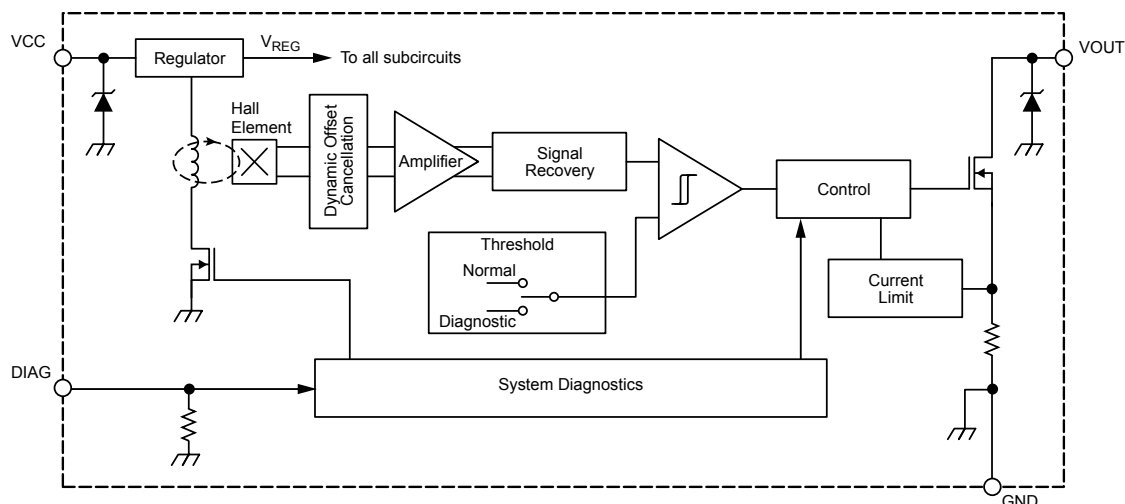
The A1160 is a unipolar, Hall-effect switch with an externally enabled diagnostic function. In normal operating mode, the A1160 functions as a standard, unipolar Hall-effect switch. The output transistor turns on (output signal switches low) in the presence of a sufficient magnetic field ($>B_{OP(max)}$). Additionally, the output transistor of the A1160 switches off (output signal switches high) when the magnetic field is removed ($<B_{RP(min)}$).

The A1160 includes conductive coils in close proximity to the Hall element. When the diagnostic feature is enabled, these coils are energized. The energized coils generate an internal magnetic field that can be sensed by the Hall element. While in Diagnostic mode, the output of the A1160 provides a square wave output, which confirms the IC is properly sensing the internally generated magnetic field. The Diagnostic mode exercises the entire magnetic and electrical signal path internal to the IC, fully confirming functionality. Therefore, use of the A1160 either eliminates the need for redundant sensors in safety critical applications or increases robustness in safety critical applications that require redundant sensors (drive-by-wire systems and so forth).

The A1160 Hall-effect sensor IC is extremely temperature-stable and stress-resistant, especially suited for operation

Continued on the next page...

Functional Block Diagram



A1160

Chopper-Stabilized Precision Hall-Effect Switch with Advanced Diagnostics

DESCRIPTION (continued)

at temperature ranges up to 150°C. Superior high-temperature performance is made possible through advanced dynamic offset cancellation techniques, which reduce the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress. This device includes on a single silicon chip: a voltage regulator, Hall-voltage generator, small-signal amplifier,

chopper stabilization, Schmitt trigger, and a open-drain output able to sink up to 25 mA. An on-board regulator permits operation with supply voltages of 3.8 to 24 V.

The A1160 is provided in a 5-pin SOT23W. The package is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Packing*
A1160LLHLX-T	10,000 pieces per 13-in. reel

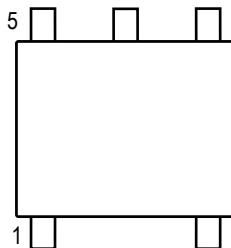
*Contact Allegro™ for additional packing options.



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		30	V
Reverse Supply Voltage	V_{RCC}		-18	V
Forward Diagnostic Enable Voltage	V_{DIAG}		5.5	V
Reverse Diagnostic Enable Voltage	V_{RDIAG}		-0.5	V
Output-Off Voltage	V_{OUT}		30	V
Continuous Output Current	I_{OUT}		25	mA
Reverse Output Current	I_{ROUT}		-50	mA
Operating Ambient Temperature	T_A	L temperature range	-40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		-65 to 170	°C

Pinout Diagram



Terminal List

Name	Number	Function
DIAG	1, 3	Diagnostics enable (use either pin 1 or pin 3)
VCC	2	Connects power supply to chip
GND	4	Ground
VOUT	5	Output from circuit

OPERATING CHARACTERISTICS: Valid across full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Operating, $T_J < 165^\circ\text{C}$	3.8	–	24	V
		V_{CC} required for diagnostic functionality	3.8	–	24	V
Output Leakage Current	I_{OUTOFF}	$V_{OUT} = 24\text{ V}$, $B < B_{RP}$	–	–	10	μA
Output Saturation Voltage	$V_{OUT(SAT)}$	$I_{OUT} = 20\text{ mA}$, $B > B_{OP}$	–	185	400	mV
Output Current Limit	I_{OM}	$B > B_{OP}$	30	–	60	mA
Power-On Time [3]	t_{PN}	$V_{CC} > 3.8\text{ V}$, $B < B_{RP}(\text{min}) - 10\text{ G}$, $B > B_{OP}(\text{max}) + 10\text{ G}$	–	–	25	μs
Chopping Frequency	f_C		–	400	–	kHz
Output Rise Time [3][4]	t_r	$R_{LOAD} = 820\ \Omega$, $C_L = 20\text{ pF}$	–	0.2	2	μs
Output Fall Time [3][4]	t_f	$R_{LOAD} = 820\ \Omega$, $C_L = 20\text{ pF}$	–	0.1	2	μs
Supply Current [5]	$I_{CC(ON)}$	$B < B_{RP}$, $V_{CC} = 12\text{ V}$	–	–	5	mA
	$I_{CC(OFF)}$	$B > B_{OP}$, $V_{CC} = 12\text{ V}$	–	–	5	mA
	$I_{CC(DIAG)}$	$V_{CC} = 12\text{ V}$, $DIAG = 1$	–	16	25	mA
Reverse Battery Current	I_{RCC}	$V_{RCC} = -18\text{ V}$	–	–	-10	mA
Supply Zener Clamp Voltage	V_{ZSUP}	$I_{CC} = 8\text{ mA}$, $T_A = 25^\circ\text{C}$	30	–	–	V
Output Zener Voltage	V_{ZOUT}	$I_{OUT} = 3\text{ mA}$, $T_A = 25^\circ\text{C}$	28	–	–	V
PWM Carrier Frequency	f_{PWMout}	With Diagnostic mode enabled	–	3	–	kHz
DIAGNOSTIC CHARACTERISTICS						
Duty Cycle (Diagnostic Mode) [6]	D_{FAIL}	$DIAG = 1$, device malfunction	–	≈ 0 or ≈ 100	–	%
	D_{PASS}	$DIAG = 1$, device normal	40	50	60	%
DIAG Pin Input Resistance	R_{DIAG}	Internal pulldown resistor	–	1	–	M Ω
DIAG Pin Input Low Voltage Threshold	V_{IL}	Device in Normal mode	–	–	0.6	V
DIAG Pin Input High Voltage Threshold	V_{IH}	Device in Diagnostic mode	1.5	–	5.0	V
Diagnostic Enable Time	t_D	Diagnostic feature should be enabled for at least t_D in order to obtain accurate PWM signal	1	–	–	ms
Diagnostic Disable Time	t_{DIS}	Time from DIAG pin release (high to low transition) until valid normal sensor IC output	–	–	25	μs

Continued on the next page...

OPERATING CHARACTERISTICS (continued): Valid across full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
Magnetic Characteristics [7]						
Operate Point	B_{OP}		115	180	245	G
Release Point	B_{RP}		60	125	190	G
Hysteresis	B_{HYS}	$B_{OP} - B_{RP}$	30	55	80	G
Maximum External Field in Diagnostic Mode [8]	$B_{EXT(DIAG)}$		800	10,000	–	G
Drift Detection Threshold						
Operate Point Drift	$B_{OP(DRIFT)}$		30	–	420	G
Release Point Drift	$B_{RP(DRIFT)}$		15	–	325	G

[1] Typical data is at $T_A = 25^\circ\text{C}$ and $V_{CC} = 12\text{ V}$ and it is for design information only.

[2] 1 G (gauss) = 0.1 mT (millitesla).

[3] Power-On Time, Output Rise Time, and Output Fall Time are ensured through device characterization and not final test.

[4] C_L = oscilloscope probe capacitance.

[5] In Diagnostic mode the supply current level is different from the Normal mode operation current level. This is important when determining the power derating for Diagnostic mode.

[6] When the A1160 passes the diagnostic tests, it outputs a 50% duty cycle signal. Any other output indicates the test failed. Please see the Diagnostic Mode of Operation section for more information.

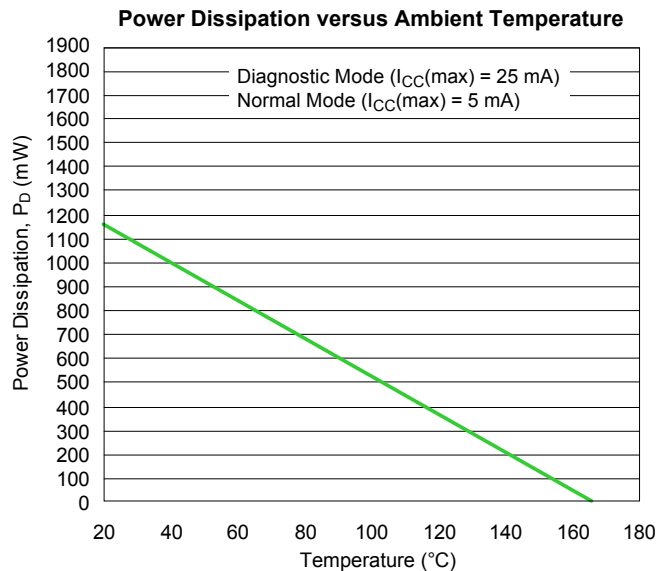
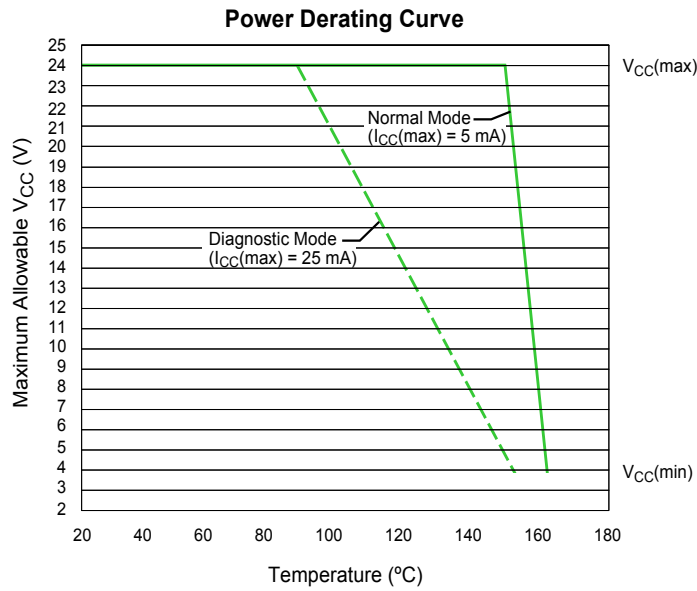
[7] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields.

[8] 800 G is the maximum test capability due to practical equipment limitations. Design simulations show that a 10,000 G external field will not adversely affect the A1160 in Diagnostic mode when a 1% sensitivity mismatch between the Hall elements in the IC is assumed.

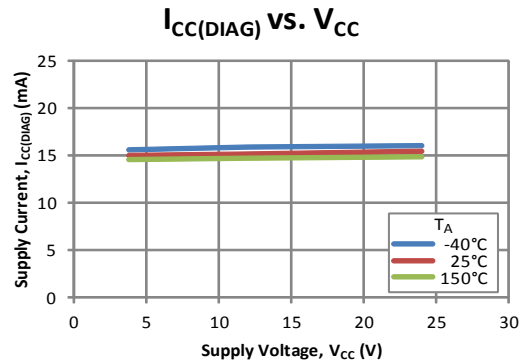
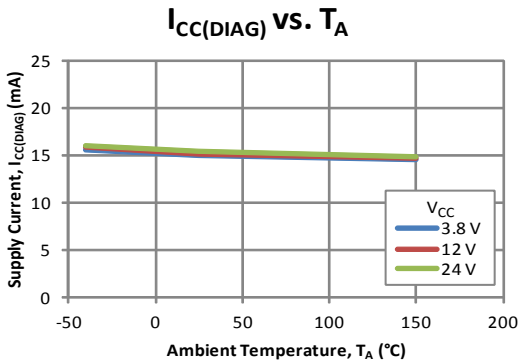
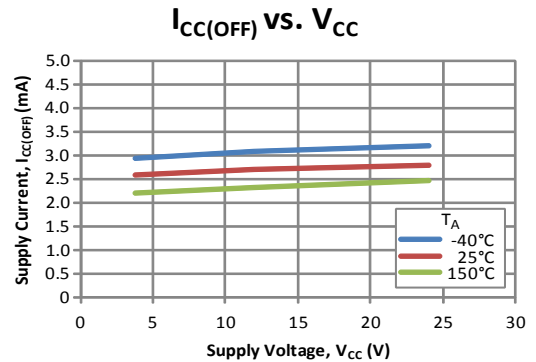
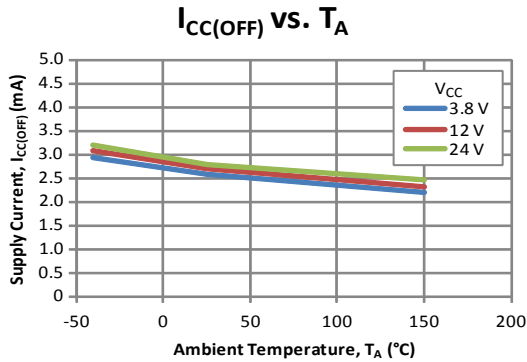
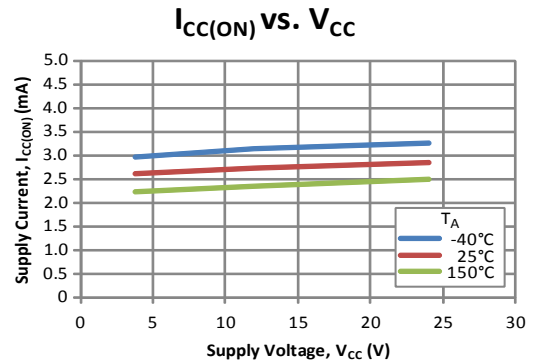
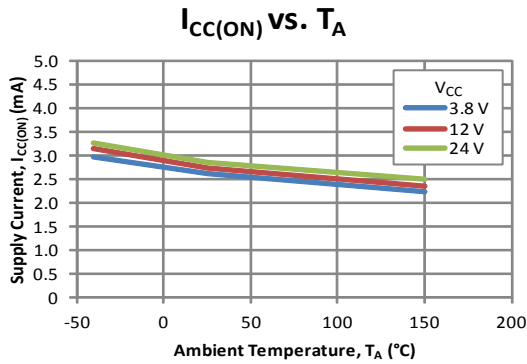
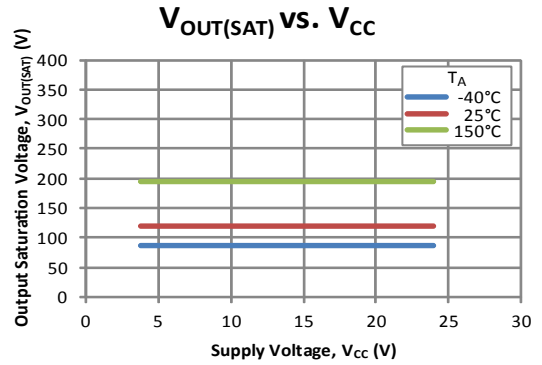
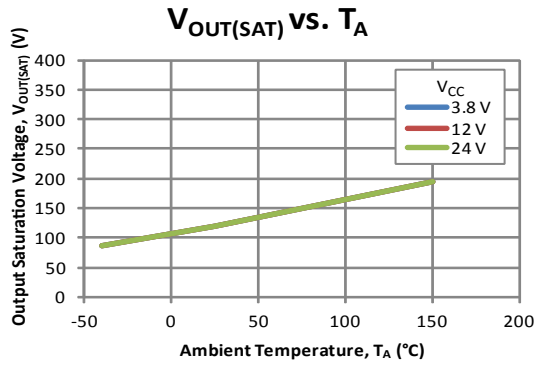
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

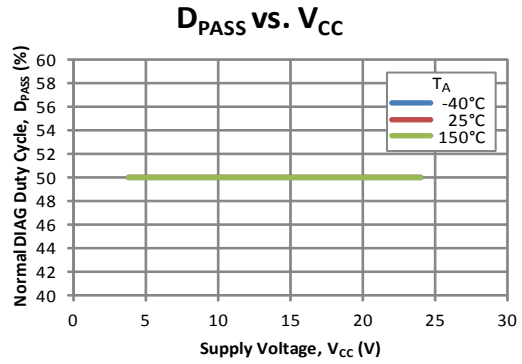
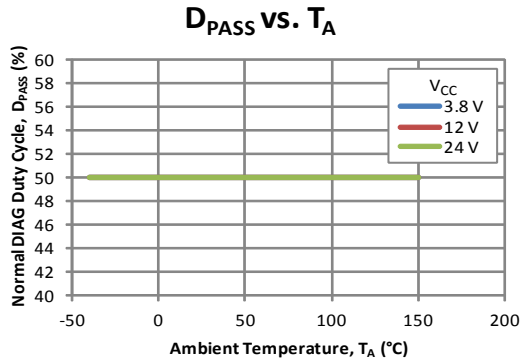
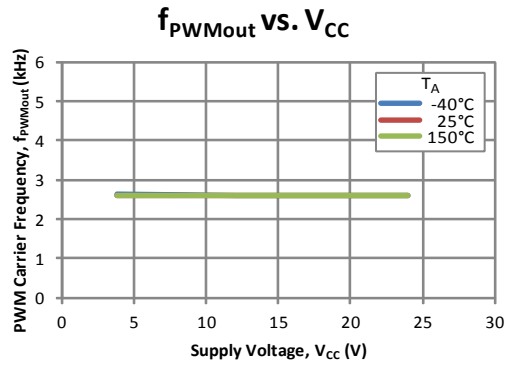
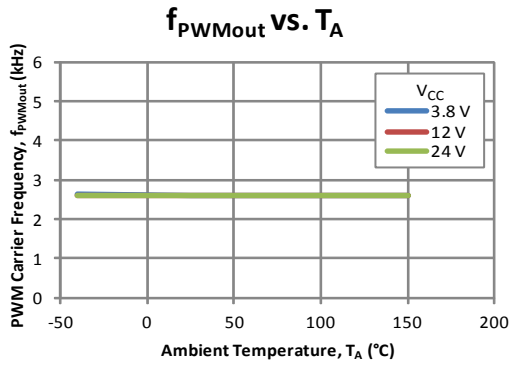
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	124	$^{\circ}C/W$

*Additional thermal information available on the Allegro website

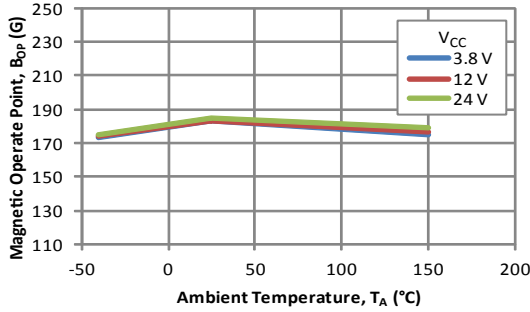


CHARACTERISTIC PERFORMANCE

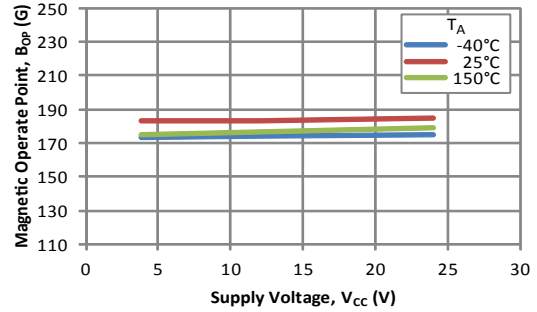




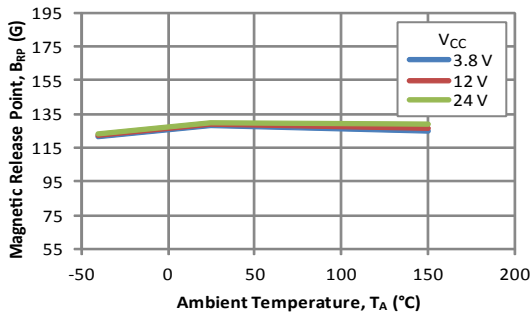
B_{OP} vs. T_A



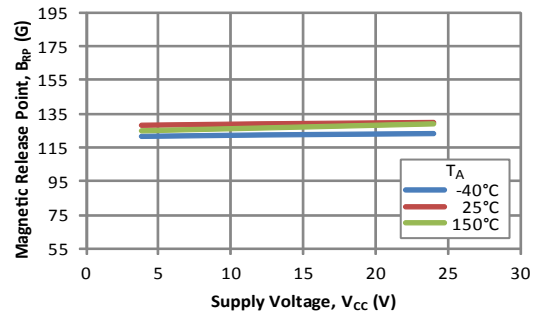
B_{OP} vs. V_{CC}



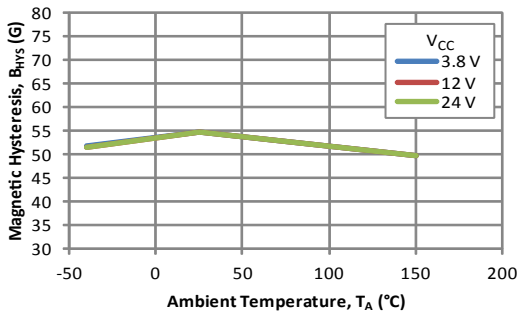
B_{RP} vs. T_A



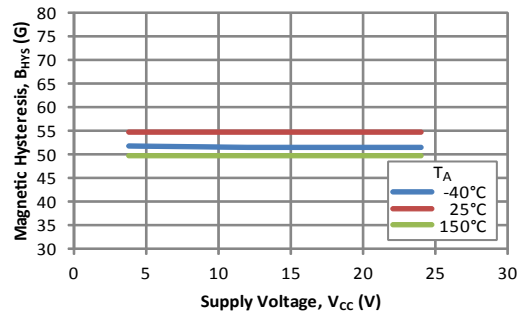
B_{RP} vs. V_{CC}



B_{HYS} vs. T_A



B_{HYS} vs. V_{CC}



FUNCTIONAL DESCRIPTION

Operation

The output of the A1160 switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} . After turn-on, the output is capable of sinking 25 mA and the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced below the release point, B_{RP} , the output goes high (turns off). This is illustrated in figure 1.

The difference in the magnetic operate and release points is the hysteresis, B_{HYS} , of the IC. This built-in hysteresis allows clean switching of the output, including when in the presence of external mechanical vibration and electrical noise.

Powering-on the IC in the hysteresis range (applied magnetic lower than B_{OP} but also higher than B_{RP}) results in output at the high state. The output will not switch until there is a valid transition beyond B_{OP} or B_{RP} . The correct output state is attained after the first excursion beyond B_{OP} or B_{RP} .

Applications

It is strongly recommended that an external bypass capacitor be connected between the supply and ground of the A1160 (in close proximity to the device) to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in figure 2, a 0.1 μ F capacitor is typical.

Extensive applications information on magnets and Hall-effect sensor ICs is available on the Allegro website, including the following application notes:

- *Hall-Effect IC Applications Guide*, AN27701
- *Soldering Methods for Allegro's Products – SMT and Through-Hole*, AN26009

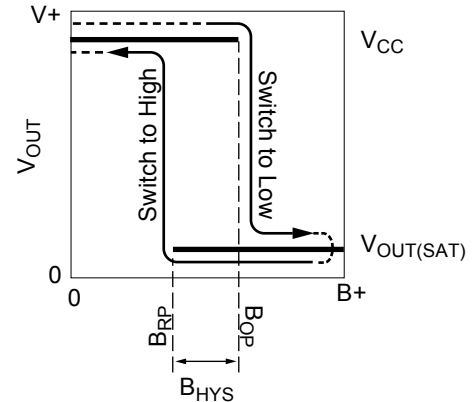


Figure 1. Switching behavior of Hall effect switches. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B- direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

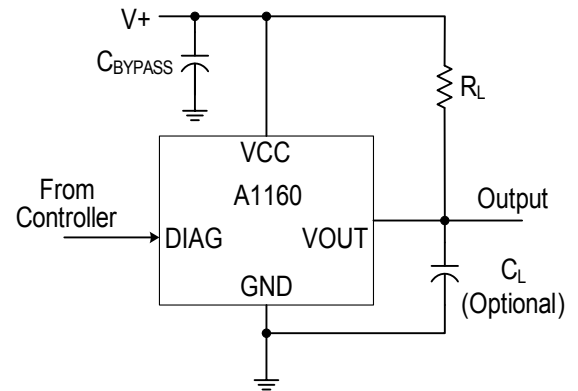


Figure 2. Typical application circuit

Diagnostic Mode of Operation

The Diagnostic mode is accessed by applying a voltage of V_{IH} on the diagnostic enable pin (DIAG). The Diagnostic mode uses an internally generated magnetic signal to exercise the signal path. This signal is compared to two reference signals in the Schmitt trigger.

If the diagnostic signal is between the two reference signals, the device is considered to be working within specification and a 50% PWM signal is set at the output pin (VOUT), as shown in figure 3. If the diagnostic signal is above the upper reference or below the lower reference, the output PWM is set at a fixed value that is either at nearly 0% or at nearly 100% duty cycle.

The Diagnostic mode of operation not only detects catastrophic failures but also identifies drifts in the magnetic switch points. If B_{OP} or B_{RP} drift to values below or above the values stated in the Drift Detection Threshold section of the Operating Characteristics table, the output PWM is set at a fixed value that is either at nearly 0% or at nearly 100% duty cycle.

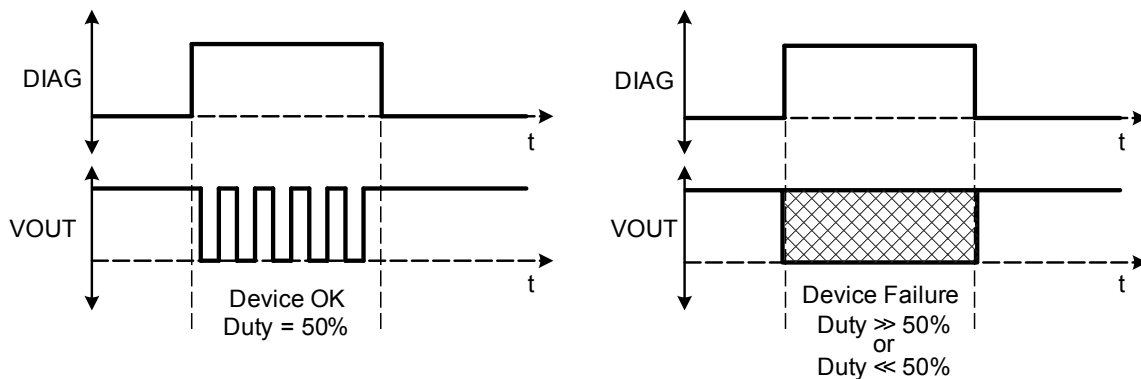


Figure 3. Diagnostics Functional Diagram. When the A1160 passes the diagnostic test, a 50% duty cycle signal is sent out (left panel). In the event of a failure, the output will be forced either high or low (right panel). Diagnostic mode is only active when the DIAG input pin is pulled high.

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall IC. This makes it difficult to process the signal while maintaining an accurate, reliable output across the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The unwanted offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This configuration is illustrated in figure 4.

The chopper stabilization technique uses a 400 kHz, high

frequency clock. For demodulation process, a sample-and-hold technique is used, where the sampling is performed at twice the chopper frequency (800 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high frequency chopping approach minimizes the effect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital sensor IC families with lower sensitivity to jitter. For more information on those products, contact your Allegro sales representative.

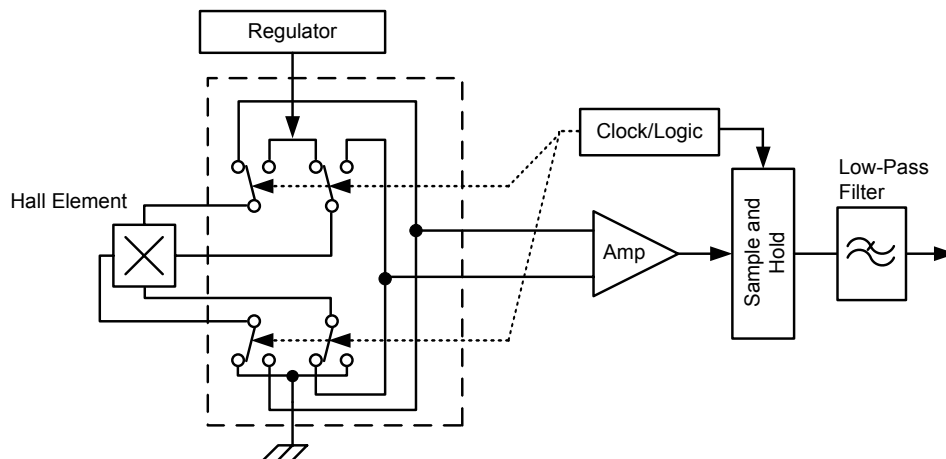


Figure 4. Chopper stabilization circuit (Dynamic Quadrature Offset Cancellation)

Package LH, 5-Pin SOT23W

For Reference Only – Not for Tooling Use

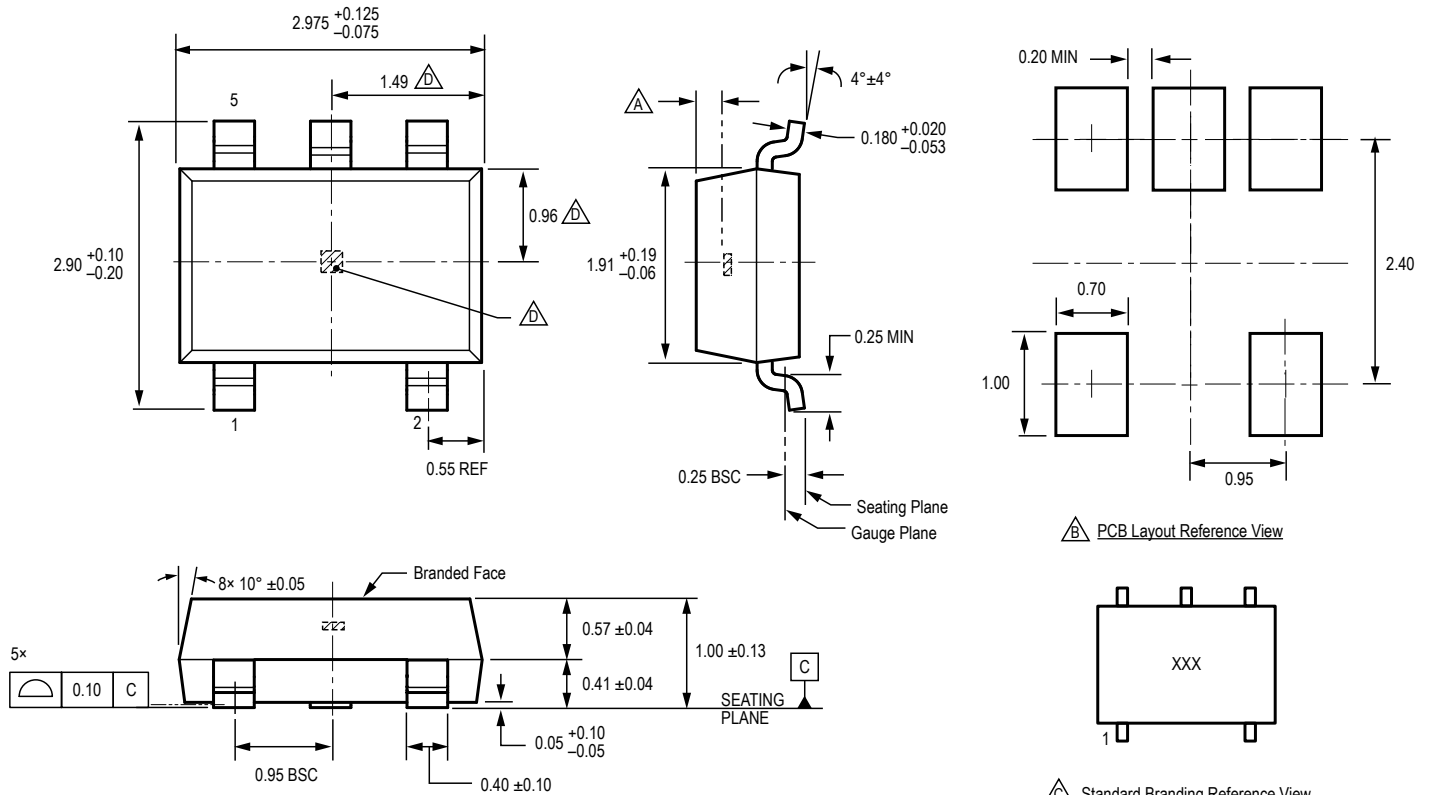
(Reference Allegro DWG-0000628, Rev. 1)

NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.28 ± 0.04 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale, location application dependant

B PCB Layout Reference View

C Standard Branding Reference View

Line 1: 3 characters

Line 1: Last 3 digits of Part Number

REVISION HISTORY

Number	Date	Description
–	December 12, 2013	Initial Release
1	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
2	January 25, 2019	Minor editorial updates
3	February 4, 2020	Minor editorial updates
4	May 27, 2020	Updated Diagnostic Enable Time test condition (page 3)
5	June 3, 2022	Updated package drawing (page 12)

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