NP100P04PLG

-40V – -100A – P-channel Power MOS FET

Application : Automotive

R07DS1513EJ0101
Rev.1.01
Jul. 14, 2022

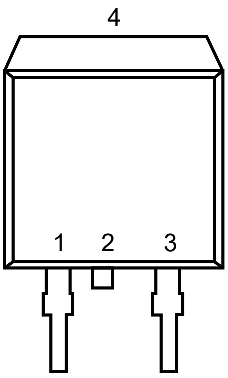
Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

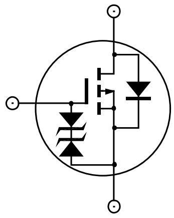
- Super low on-state resistance : $R_{DS(on)}$ = 3.7 mΩ Max. (V_{GS} = -10 V, I_D = -50 A)
  $R_{DS(on)}$ = 5.1 mΩ Max. (V_{GS} = -4.5 V, I_D = -50 A)
- Low input capacitance : Ciss = 15100 pF Typ.
- Built-in gate protection diode
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

Outline



1. Gate
2. Drain
3. Source
4. Drain(Fin)

MP-25ZP (TO-263)



Equivalent circuit

Absolute Maximum Ratings

(T_a=25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	-40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_c = 25 °C)	$I_{D(DC)}$	∓100	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1	∓300	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	200	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Notes2	74	A
Single Avalanche Energy	E_{AS} Notes2	550	mJ

Notes 1. PW ≤ 10 μs , Duty Cycle ≤ 1%
2. Starting T_{ch}=25℃ , V_{DD} =-20V , R_G = 25 Ω , V_{GS} = -20 → 0V , L = 100μH

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ Notes3	0.75	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ Notes3	83.3	°C/W

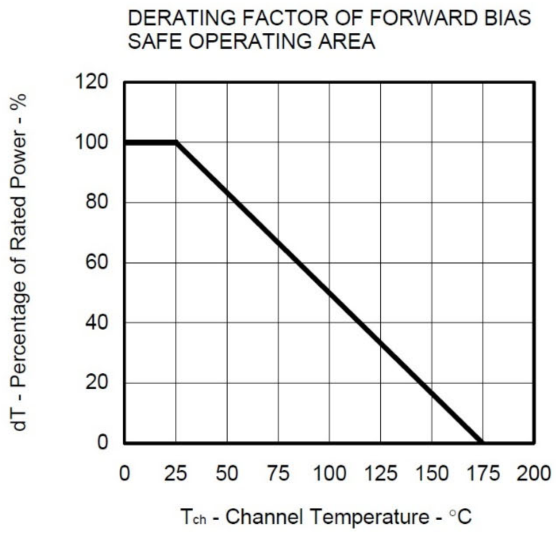
Electrical Characteristics

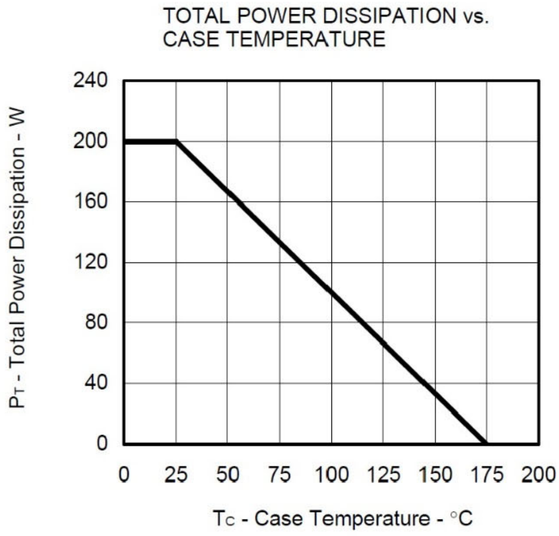
(T_a=25°C)

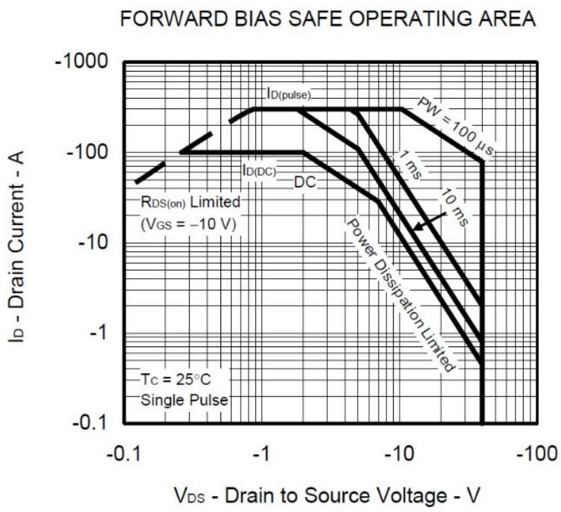
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	V_{DS} = -40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	∓10	μA	V_{GS} = ∓ 20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.0	-1.6	-2.5	V	V_{DS} = -10 V, I_D = -1 mA
Forward Transfer Admittance	| yfs | Notes4	43	88	—	S	V_{DS} = -10 V, I_D = -50 A
Drain to Source On-state Resistance	$R_{DS(on)1}$ Notes4	—	2.8	3.7	mΩ	V_{GS} = -10 V, I_D = -50 A
	$R_{DS(on)2}$ Notes4	—	3.4	5.1	mΩ	V_{GS} = -4.5 V, I_D = -50 A
Input Capacitance	C_{iss}	—	15100	—	pF	V_{DS} = -10 V
Output Capacitance	C_{oss}	—	2400	—	pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss}	—	1130	—	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$	—	38	—	ns	V_{DD} = -20 V
Rise Time	t_r	—	30	—	ns	I_D = -50 A
Turn-off Delay Time	$t_{d(off)}$	—	300	—	ns	V_{GS} = -10 V
Fall Time	t_f	—	100	—	ns	R_G = 0 Ω
Total Gate Charge	Q_g	—	320	—	nC	V_{DD} = -32 V
Gate to Source Charge	Q_{gs}	—	37	—	nC	V_{GS} = -10 V
Gate to Drain Charge	Q_{gd}	—	85	—	nC	I_D = -100A
Body Diode Forward Voltage	$V_{F(S-D)}$ Notes4	—	0.91	1.5	V	I_F = -100 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	70	—	ns	I_F = -100 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	123	—	nC	di/dt = -100 A/μs

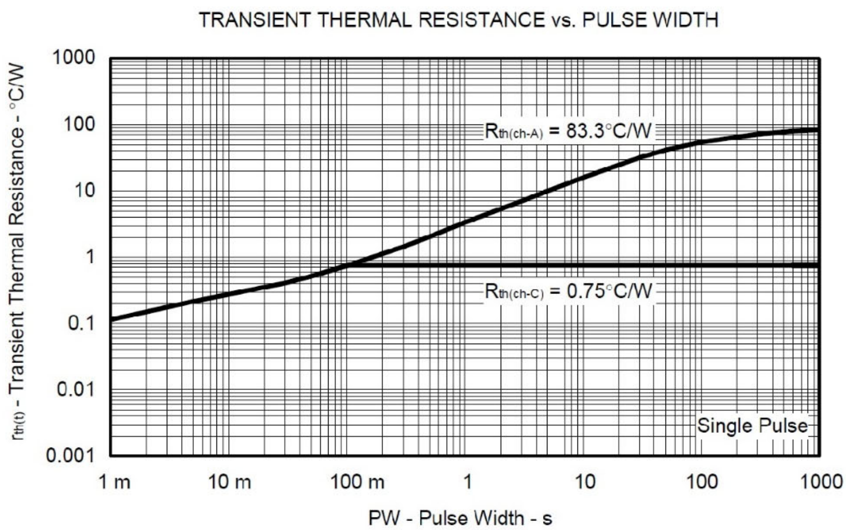
Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.
4. Pulse test.

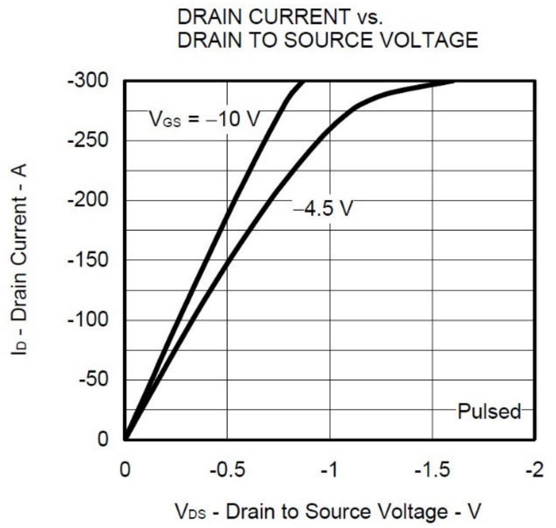
Typical Characteristics

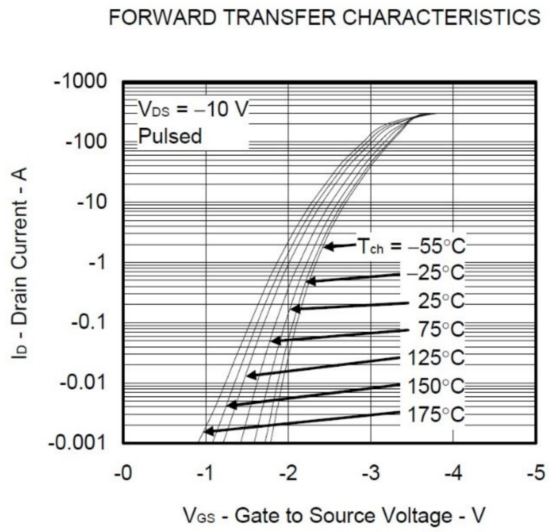


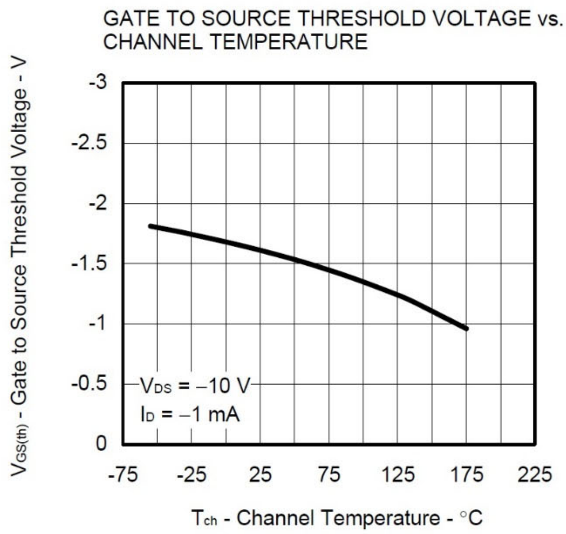


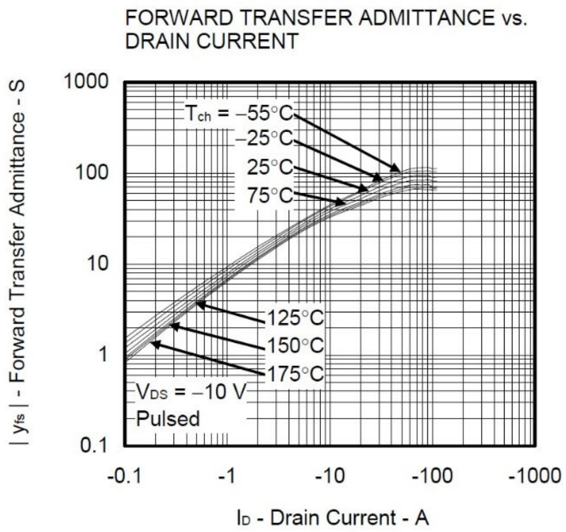


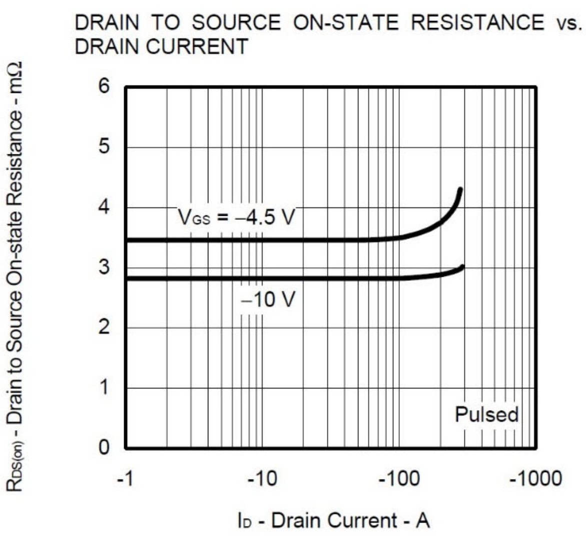


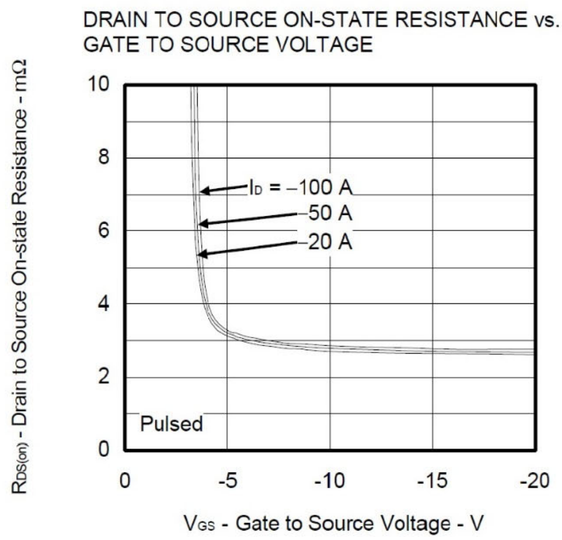

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE
VGS = –10 V
–4.5 V
Pulsed
ID - Drain Current - A
VDS - Drain to Source Voltage - V


FORWARD TRANSFER CHARACTERISTICS
VDS = –10 V
Pulsed
Tch = –55°C
–25°C
25°C
75°C
125°C
150°C
175°C
ID - Drain Current - A
VGS - Gate to Source Voltage - V

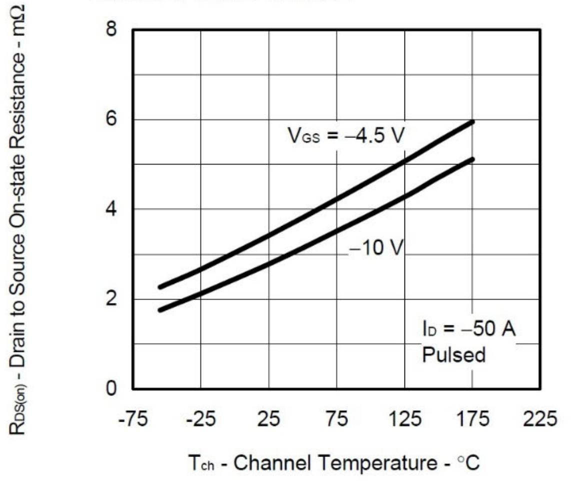

GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE
VDS = –10 V
ID = –1 mA
VGS(th) - Gate to Source Threshold Voltage - V
Tch - Channel Temperature - °C


FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT
Tch = –55°C
–25°C
25°C
75°C
125°C
150°C
175°C
VDS = –10 V
Pulsed
| yfs | - Forward Transfer Admittance - S
ID - Drain Current - A

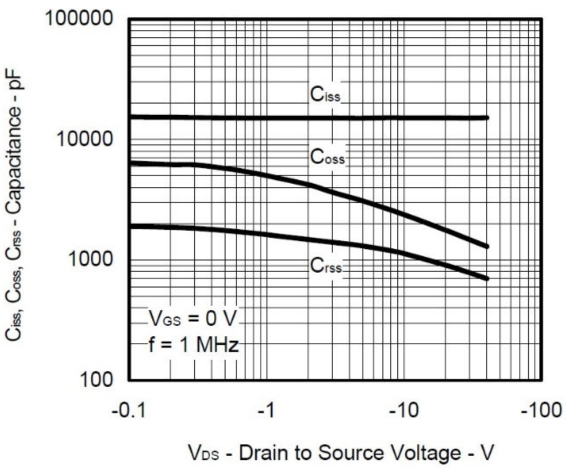

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT
VGS = –4.5 V
–10 V
Pulsed
RDS(on) - Drain to Source On-state Resistance - mΩ
ID - Drain Current - A


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE
ID = –100 A
–50 A
–20 A
Pulsed
RDS(on) - Drain to Source On-state Resistance - mΩ
VGS - Gate to Source Voltage - V

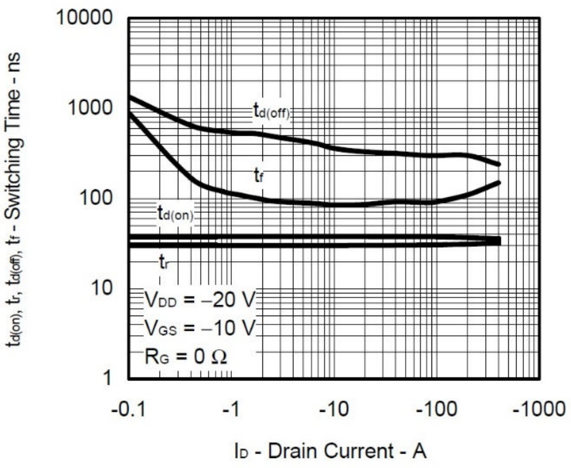
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



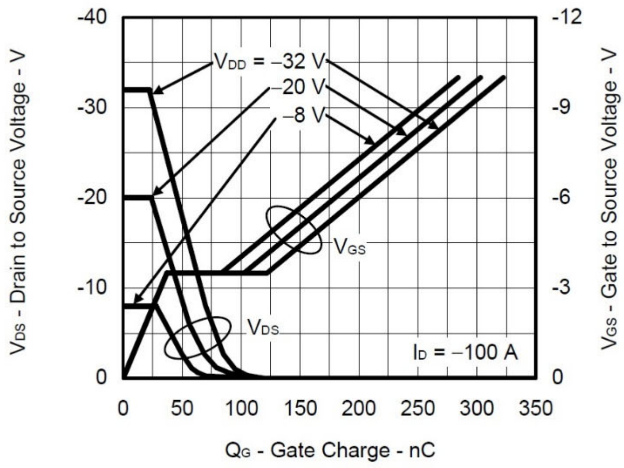
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



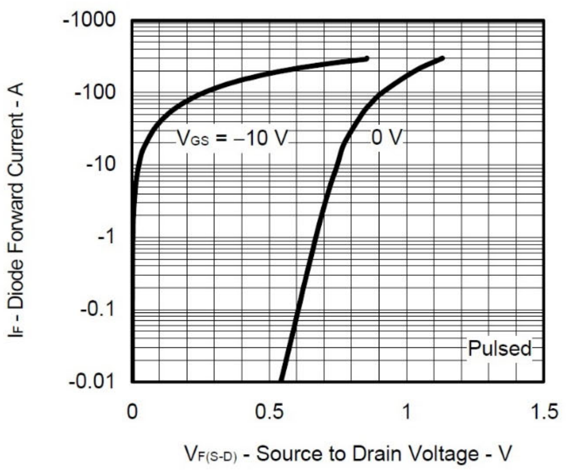
SWITCHING CHARACTERISTICS



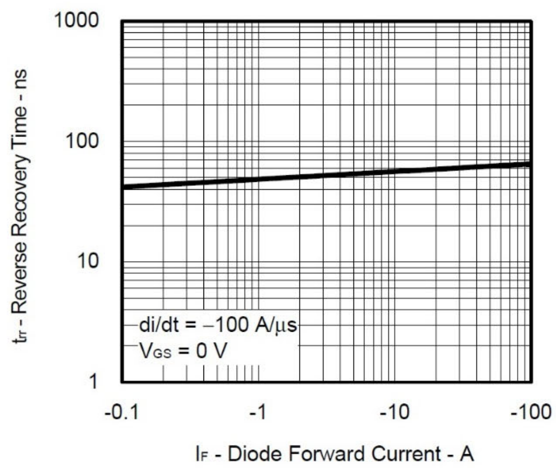
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



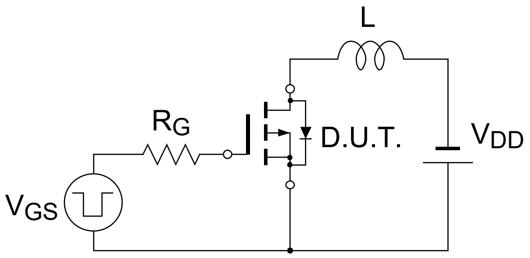
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



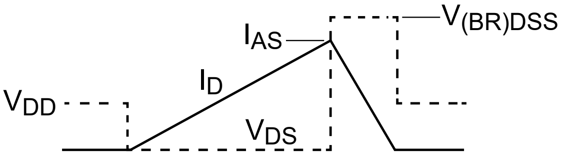
Test Circuit

Avalanche

Test Circuit



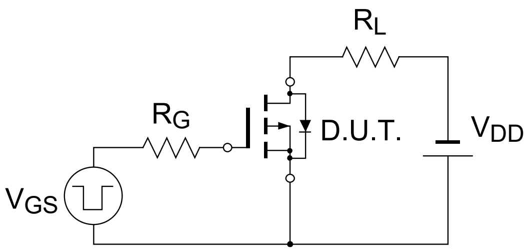
Waveform



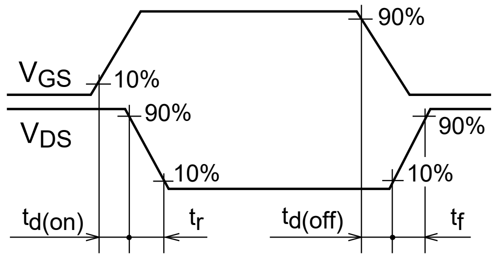
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

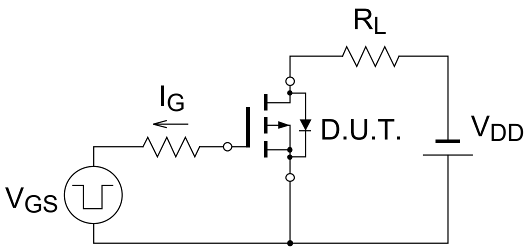


Waveform

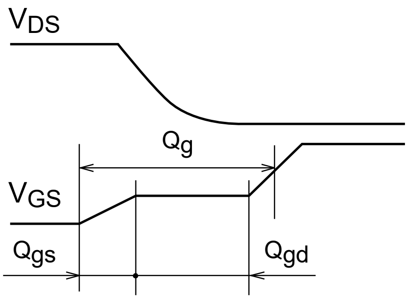


Gate Charge

Test Circuit

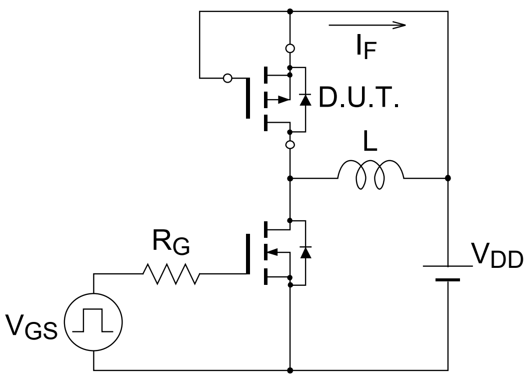


Waveform

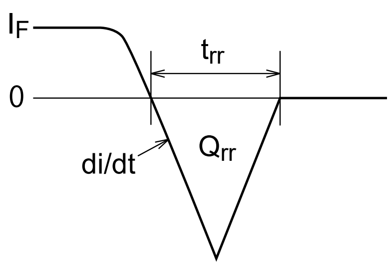


Reverse Recovery

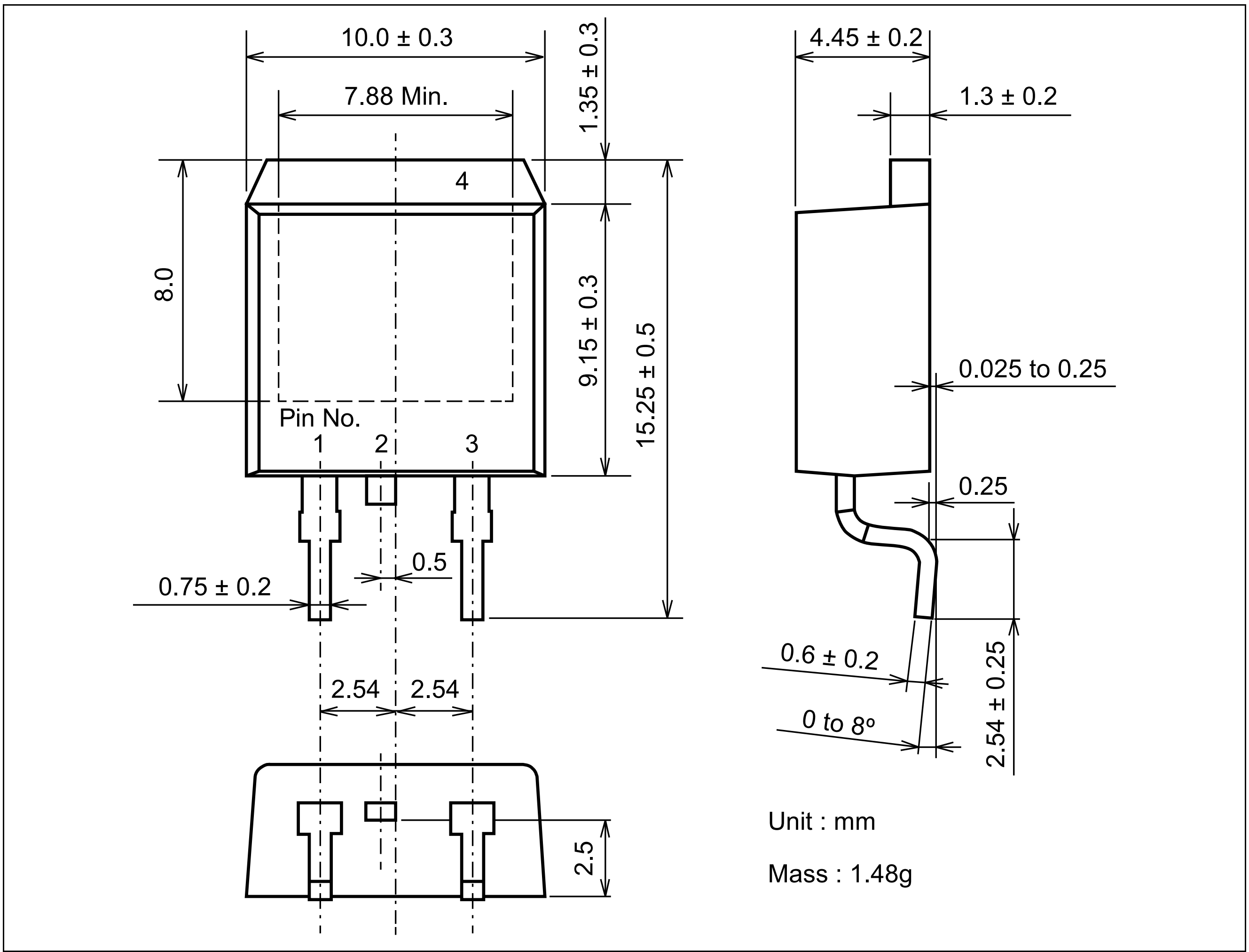
Test Circuit



Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping container
NP100P04PLG-E1-AY	800pcs/reel	Taping

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Notice

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Contact information

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