1.7 GHz, Ultra Low Distortion, Wideband Op Amp

Check for Samples: LMH6702QML

FEATURES

- **V_S = ±5V, T_A = 25°C, A_V = +2V/V, R_L = 100Ω, V_{OUT} = 2V_{PP}, Typical Unless Noted:**
- **Available with Radiation Ensurance**
  - **High Dose Rate 300 krad(Si)**
  - **ELDRS Free 300 krad(Si)**
- **−3dB Bandwidth (V_{OUT} = 0.2 V_{PP}) 720 MHz**
- **Low Noise 1.83nV/√Hz**
- **Fast Settling to 0.1% 13.4ns**
- **Fast Slew Rate 3100V/µs**
- **Supply Current 12.5mA**
- **Output Current 80mA**
- **Low Intermodulation Distortion (75MHz) −67dBc**
- **Improved Replacement for CLC409 and CLC449**

APPLICATIONS

- **Flash A/D Driver**
- **D/A transimpedance Buffer**
- **Wide Dynamic Range IF Amp**
- **Radar/Communication Receivers**
- **Line Driver**
- **High Resolution Video**

DESCRIPTION

The LMH6702 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefitting from TI's current feedback architecture, the LMH6702 offers unity gain stability at exceptional speed without need for external compensation.

With its 720MHz bandwidth (A_V = 2V/V, V_O = 2V_{PP}), 10-bit distortion levels through 60MHz (R_L = 100Ω), 1.83nV/√Hz input referred noise and 12.5mA supply current, the LMH6702 is the ideal driver or buffer for high-speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers, requiring a wideband amplifier offering exceptional signal purity, will find the LMH6702's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

The LMH6702 is constructed using TI's VIP10 complimentary bipolar process and TI's proven current feedback architecture.

Connection Diagrams

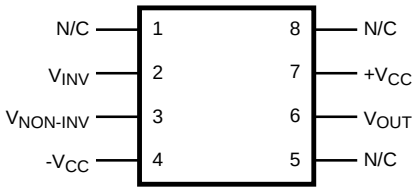

Figure 1. 8-Lead CDIP (NAB)
Top View

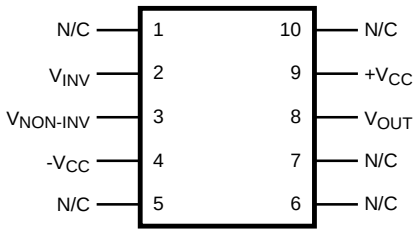

Figure 2. 10-Lead CLGA (NAC)
Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})	±6.75V_{DC}
Common Mode Input Voltage (V_{CM})	V^- to V^+
Power Dissipation (P_D) (2)	1W
Junction Temperature (T_J)	+175°C
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature Range	-65°C ≤ T_A ≤ +150°C
Thermal Resistance	
θ_{JA}	
CDIP (Still Air)	170°C/W
CDIP (500LF/Min Air Flow)	100°C/W
CLGA (Still Air)	220°C/W
CLGA (500LF/Min Air Flow)	150°C/W
θ_{JC}	
CDIP	35°C/W
CLGA	37°C/W
Package Weight (Typical)	
CDIP	1078mg
CLGA	227mg
ESD Tolerance (3)	1000V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) Human body model, 1.5kΩ in series with 100pF.

Recommended Operating Conditions

Supply Voltage (V_{CC})	±5V_{DC} to ±6V_{DC}
Gain Range	±1 to ±10
Ambient Operating Temperature Range (T_A)	-55°C to +125°C

Quality Conformance Inspection

MIL-STD-883, Method 5005, Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LMH6702 Electrical Characteristics DC Parameters(1)(2)

The following conditions apply, unless otherwise specified.
R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{BN}	Input Bias Current, Noninverting			-15	+15	µA	1, 2
				-21	+21	µA	3
I_{BI}	Input Bias Current, Iverting			-30	+30	µA	1, 2
				-34	+34	µA	3
V_{IO}	Input Offset Voltage			-4.5	+4.5	mV	1, 3
				-6.0	+6.0	mV	2
I_{CC}	Supply Current, no load	R_L = ∞			15	mA	1, 2, 3
PSSR	Power Supply Rejection Ratio	-V_{CC} = -4.5V to -5.0V, +V_{CC} = +4.5V to +5.0V		45		dB	1, 2, 3

(1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative cur rent shall be defined as convential current flow out of a device terminal.
(2) Pre and Post irradiation limits are identical to those listed under the DC parameter tables above. Post irradiation testing is conducted at room temperature, +25°C, only. Testing is performed as specified in MIL-STD-883 Test Method 1019 Condition A. The ELDRS-Free part is also tested per Test Method 1019 Conditions D.

LMH6702 Electrical Characteristics AC Parameters (1)(2)

The following conditions apply, unless otherwise specified.
R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
HD_3	3rd Harmonic Distortion	2V_{PP} at 20MHz			-62	dBc	4
GFPL	Gain Flatness Peaking	0.1MHz to 75MHz, V_O < 0.5V_{PP}			0.4	dB	4
GFPH	Gain Flatness Peaking	> 75MHz, V_O < 0.5V_{PP}			2.0	dB	4
GFRH	Gain Flatness Rolloff	75MHz to 125MHz, V_O<0.5V_{PP}			0.2	dB	4
HD_2	2nd Harmonic Distortion	2V_{PP} at 20MHz			-52	dBc	4

(1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative cur rent shall be defined as convential current flow out of a device terminal.
(2) These parameters are not post irradiation tested.

LMH6702 Electrical Characteristics Drift Values Parameters(1)

The following conditions apply, unless otherwise specified.
R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω
"Delta not required on B level product. Delta required for S-level product at Group B5 only, or as specified on the Internal Processing Instruction (IPI)."

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{BN}	Input Bias Current Noninverting			-0.3	+0.3	µA	1
I_{BI}	Input Bias Current Inverting			-3.0	+3.0	µA	1
V_{IO}	Input Offset Voltage			-0.3	+0.3	mV	1

(1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative cur rent shall be defined as convential current flow out of a device terminal.

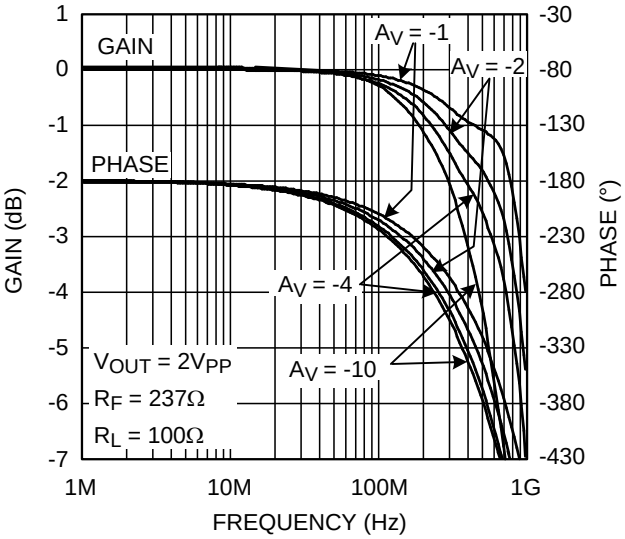


Figure 3. Inverting Frequency Response

Typical Performance Characteristics

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; Unless Specified).

Non-Inverting Frequency Response

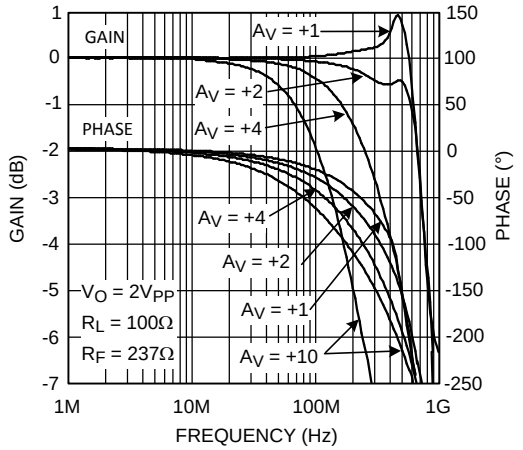


Figure 4.

Inverting Frequency Response

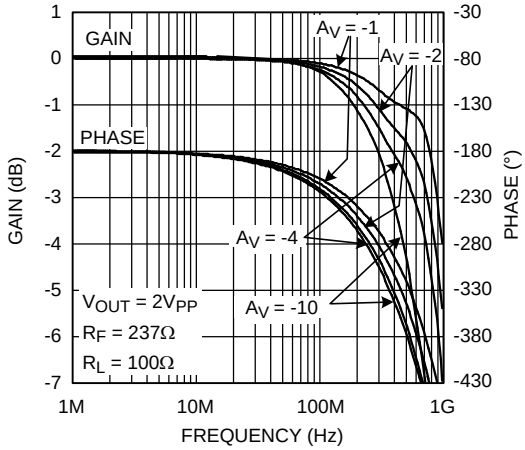


Figure 5.

Small Signal Bandwidth

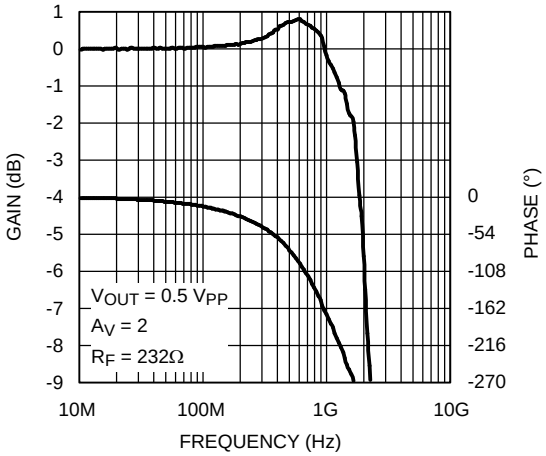


Figure 6.

Frequency Response for Various R_L's, A_V = +2

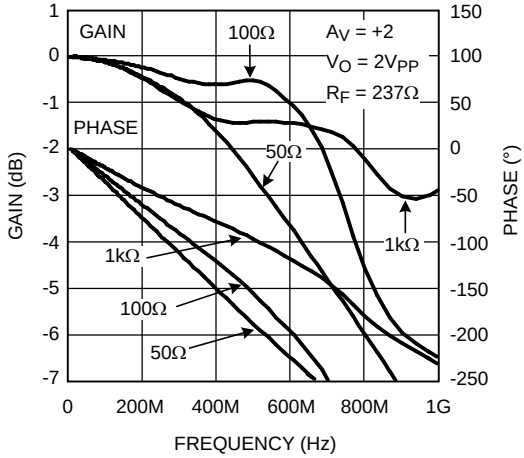


Figure 7.

Frequency Response for Various R_L's, A_V = +4

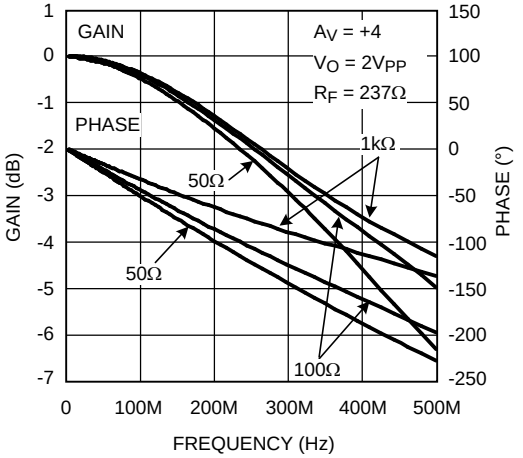


Figure 8.

Step Response, $2V_{PP}$

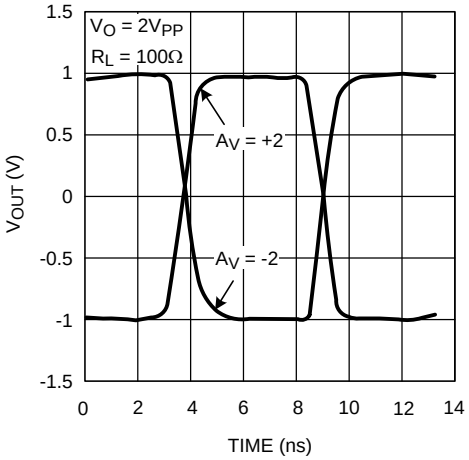


Figure 9.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; Unless Specified).

Step Response, $6V_{PP}$

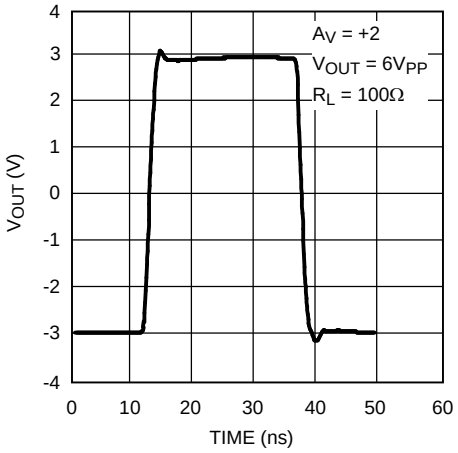


Figure 10.

Percent Settling vs. Time

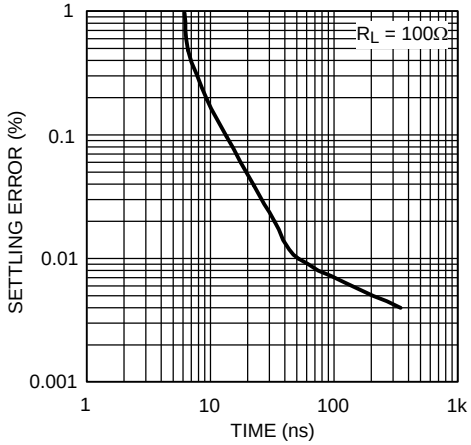


Figure 11.

R_S and Settling Time vs. C_L

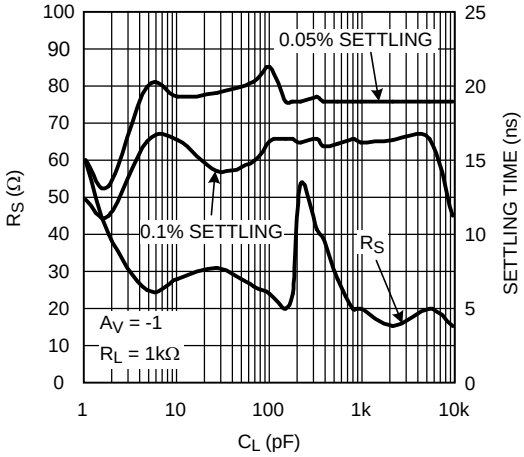


Figure 12.

Input Offset for 3 Representative Units

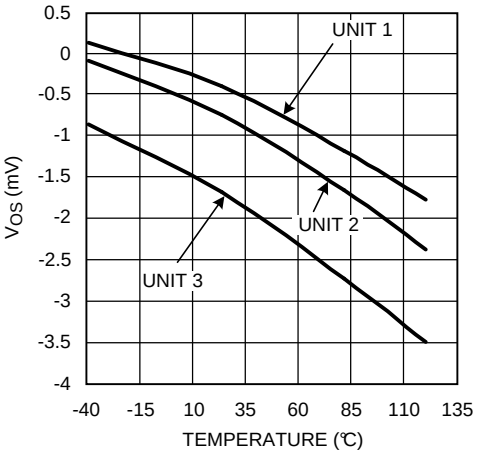


Figure 13.

Inverting Input Bias for 3 Representative Units

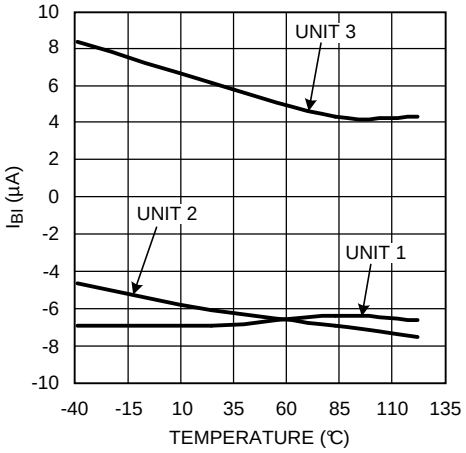


Figure 14.

Non-Inverting Input Bias for 3 Representative Units

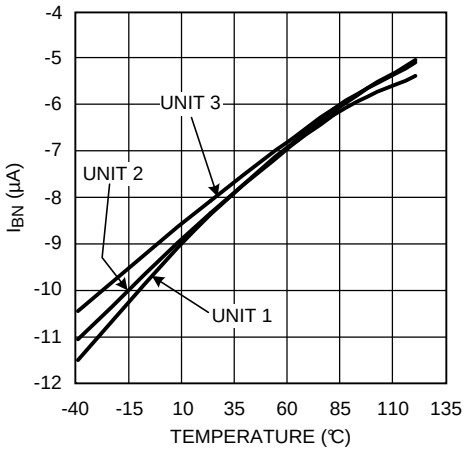


Figure 15.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; Unless Specified).

Noise

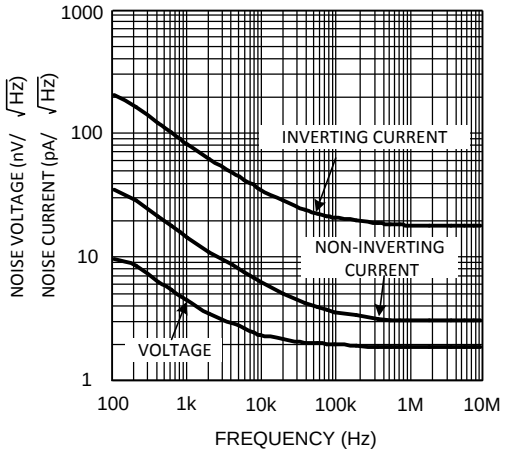


Figure 16.

CMRR, PSRR, R_{OUT}

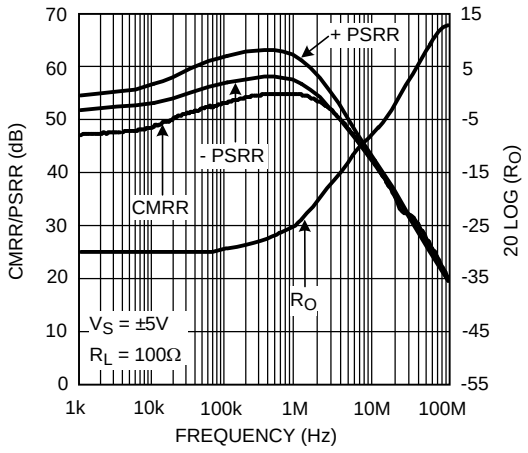


Figure 17.

Transimpedance

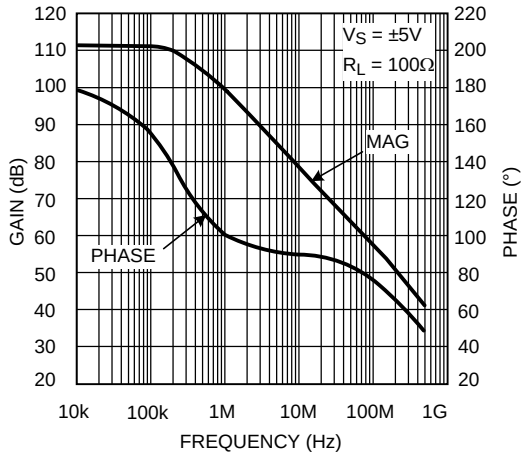


Figure 18.

DG/DP (NTSC)

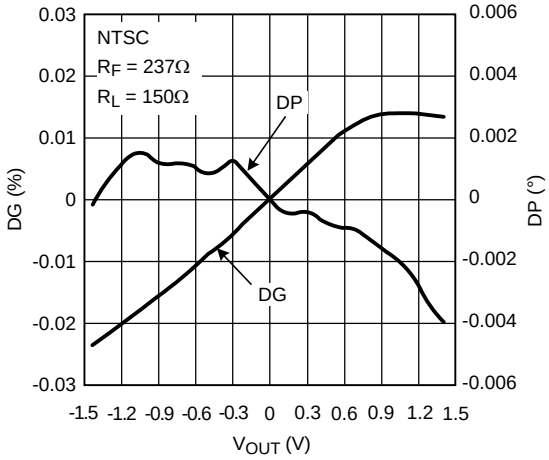


Figure 19.

DG/DP (PAL)

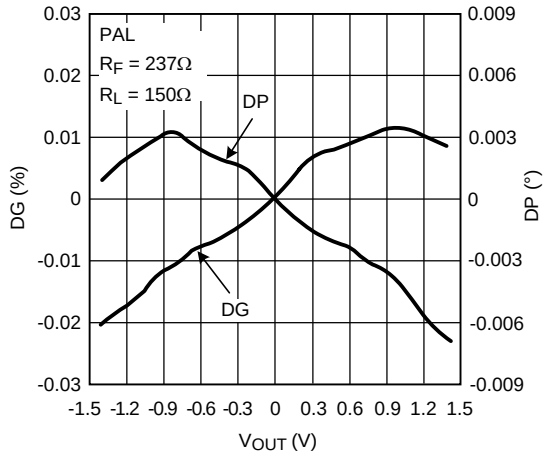


Figure 20.

APPLICATION SECTION

FEEDBACK RESISTOR

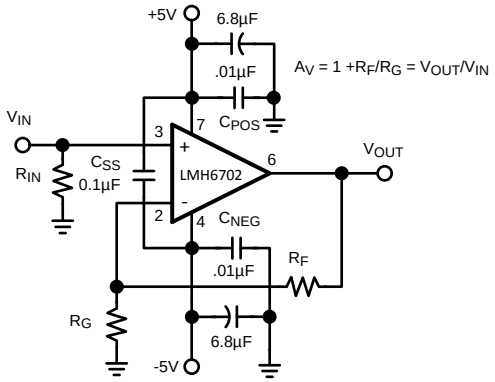


Figure 21. Recommended Non-Inverting Gain Circuit

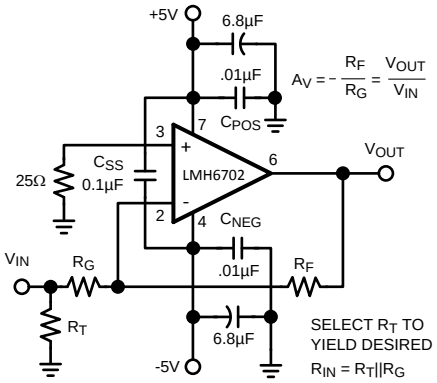


Figure 22. Recommended Inverting Gain Circuit

The LMH6702 achieves its excellent pulse and distortion performance by using the current feedback topology. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6702 is optimized for use with a 237Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 SNOA366 discusses this in detail along with the occasions where a different R_F might be advantageous.

HARMONIC DISTORTION

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6702 distortions. The capacitor C_{SS}, shown across the supplies in Figure 21 and Figure 22, is critical to achieving the lowest 2nd harmonic distortion. For absolute minimum distortion levels, it is also advisable to keep the supply decoupling currents (ground connections to C_{POS}, and C_{NEG} in Figure 21 and Figure 22) separate from the ground connections to sensitive input circuitry (such as R_G, R_T, and R_{IN} ground connections). Splitting the ground plane in this fashion and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to "Star Connection" layout technique) ensures minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd order distortion).

If this lay out technique has not been observed on a particular application board, designer may actually find that supply decoupling caps could adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. Figure 23 below shows actual HD2 data on a board where the ground plane is "shared" between the supply decoupling capacitors and the rest of the circuit. Once these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10MHz-20MHz, as shown in Figure 23 below:

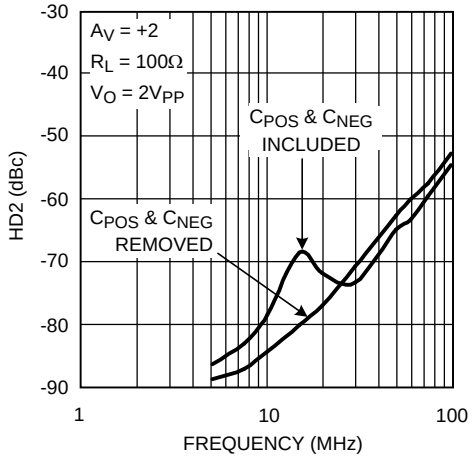


Figure 23. Decoupling Current Adverse Effect on a Board with Shared Ground Plane

At these extremely low distortion levels, the high frequency behavior of decoupling capacitors themselves could be significant. In general, lower value decoupling caps tend to have higher resonance frequencies making them more effective for higher frequency regions. A particular application board which has been laid out correctly with ground returns "split" to minimize coupling, would benefit the most by having low value and higher value capacitors paralleled to take advantage of the effective bandwidth of each and extend low distortion frequency range.

CAPACITIVE LOAD DRIVE

Figure 24 shows a typical application using the LMH6702 to drive an ADC.

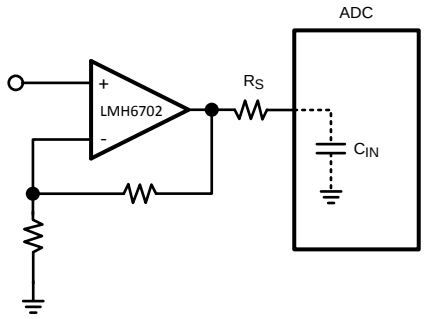


Figure 24. Input Amplifier to ADC

The series resistor, R_S, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of "R_S and Settling Time vs. C_L" in the Typical Performance Characteristics section is an excellent starting point for selecting R_S. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1kΩ). Sensitivity to capacitive loading is greatly reduced once the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, R_S value may be reduced. The exact value may best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, care must be taken when the device is lightly loaded and some capacitance is present at the output. Due to the much higher frequency response of the LMH6702 compared to the CLC409, there could be increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load). As already mentioned, this susceptibility is most noticeable when the LMH6702's resistive load is light. Parasitic capacitance can be minimized by careful lay out. Addition of an output snubber R-C network will also help by increasing the high frequency resistive loading.

Referring back to Figure 24, it must be noted that several additional constraints should be considered in driving the capacitive input of an ADC. There is an option to increase R_S, band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. Increasing R_S too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the "convert" signal. Also, C_{IN} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_S is increased. Only slight adjustments up or down from the recommended R_S value should therefore be attempted in optimizing system performance.

DC ACCURACY AND NOISE

Example below shows the output offset computation equation for the non-inverting configuration using the typical bias current and offset specifications for A_V = + 2:

Output Offset : $V_O = (\pm I_{BN} \cdot R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm I_{BI} \cdot R_F$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for A_V = +2, R_F = 237Ω, R_{IN} = 25Ω:

$V_O = (\pm 6\mu A \cdot 25\Omega \pm 1mV) (1 + 237/237) \pm 8\mu A \cdot 237 = \pm 4.20mV$

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7 SNOA365. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 SNOA375 for a full discussion of noise calculations for current feedback amplifiers.

PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 SNOA367 for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6702QMLMF	SOT-23-5	CLC730216
LMH6702QMLMA	Plastic SOIC	CLC730227

Table 1. Revision History

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New Corporate format Release	R. Malone	1 MDS data sheet converted in corporate data sheet format. Added reference to QMLV products and Drift Table. MDS MNLMH6702–X, Rev. 1A0 will be archived.
09/28/05	B	Features, Ordering Information Table and Notes	R. Malone	Added radiation reference to Features, Rad NSID & SMD to Ordering Table and Note 5 to AC & DC Electrical tables. Note to note section.
11/07/05	C	Update AC electrical's and Notes	R. Malone	Added note to AC electrical's and note section. LMH6702QML Revision B data sheet will be archived.
07/26/2011	D	Update Features, Ordering Information and Footnotes	Larry M.	Added 'High Dose Rate' 300 krad(Si) and ELDRS Free 300 krad(Si). Deleted NS Part numbers LMH6702J-QML and LMH6702WG-QML. Added NS Part number LMH6702WGFLQMLV.Modified note. LMH6702QML Revision C data sheet will be archived.
10/05/2011	E	Update Ordering Information, and Footnotes	Kirby K..	Added NS Part number LMH6702JFLQMLV 300 krad(Si) .Modified note and note. Revision D data sheet will be archived.
03/18/2013	E	All	-	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0254601VPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T	Samples
5962-0254601VZA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T	Samples
5962F0254601VPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T	Samples
5962F0254601VZA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T	Samples
5962F0254602VPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702JFLQV 5962F02546 02VPA Q ACO 02VPA Q >T	Samples
LMH6702J-QMLV	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T	Samples
LMH6702JFLQMLV	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702JFLQV 5962F02546 02VPA Q ACO 02VPA Q >T	Samples
LMH6702JFQMLV	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T	Samples
LMH6702WG-QMLV	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGQMLV Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										5962-02546 01VZA ACO 01VZA >T	
LMH6702WGFQMLV	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

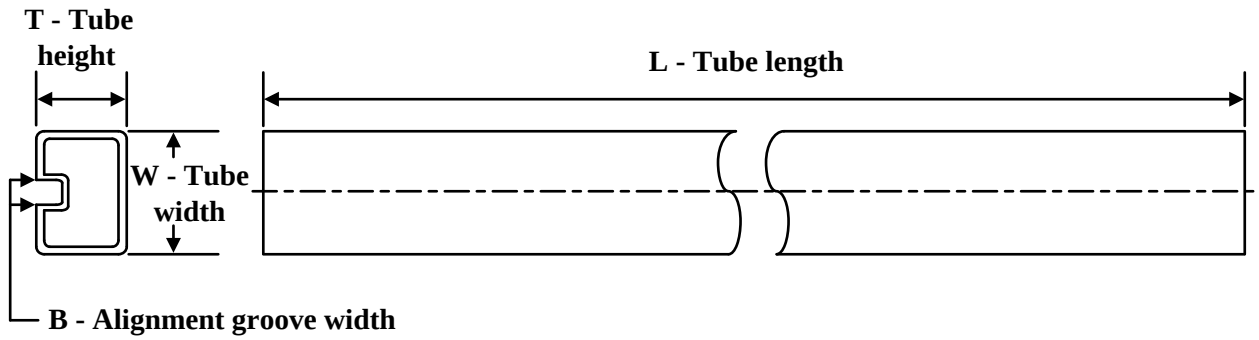
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

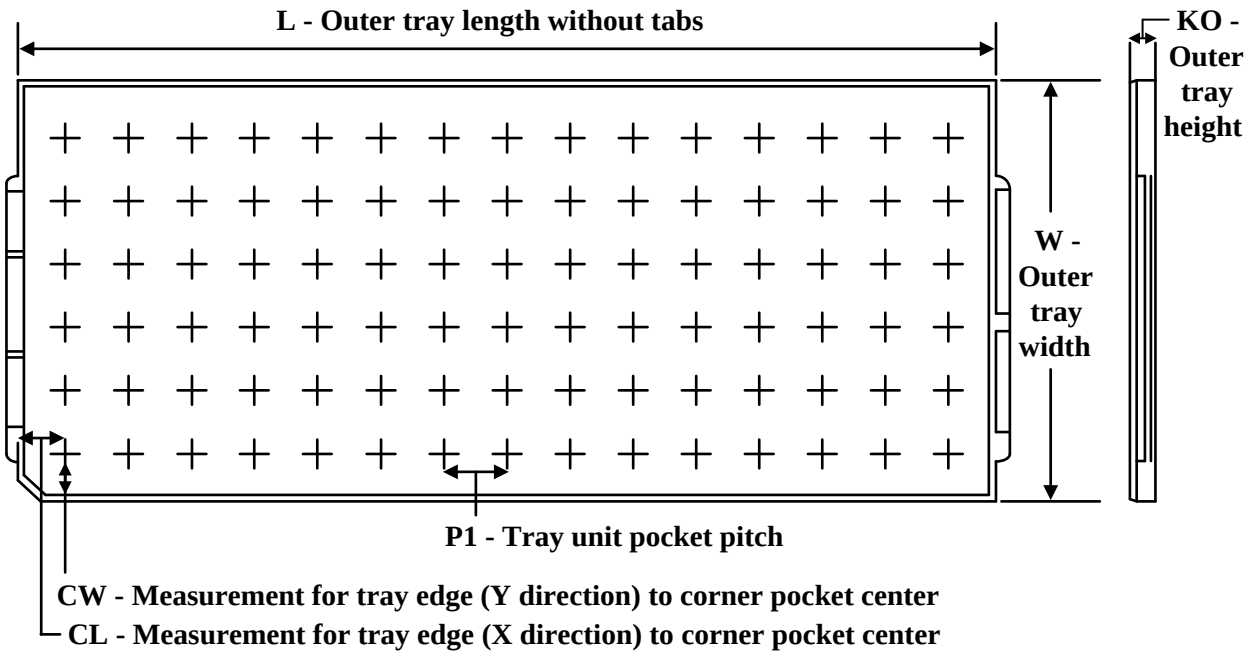
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0254601VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962F0254601VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
LMH6702J-QMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LMH6702JFQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA

TRAY

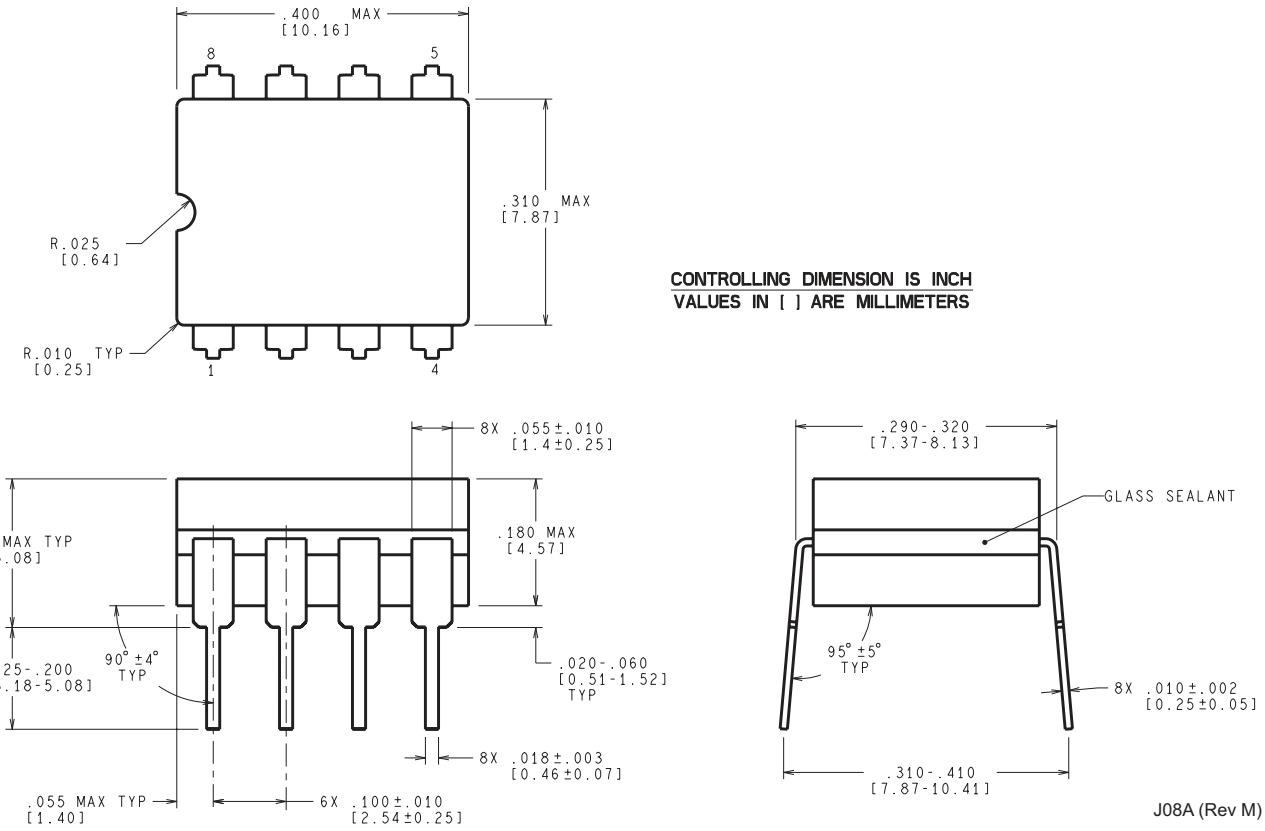


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-0254601VZA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
5962F0254601VZA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LMH6702WG-QMLV	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LMH6702WGFQMLV	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08

NAB0008A

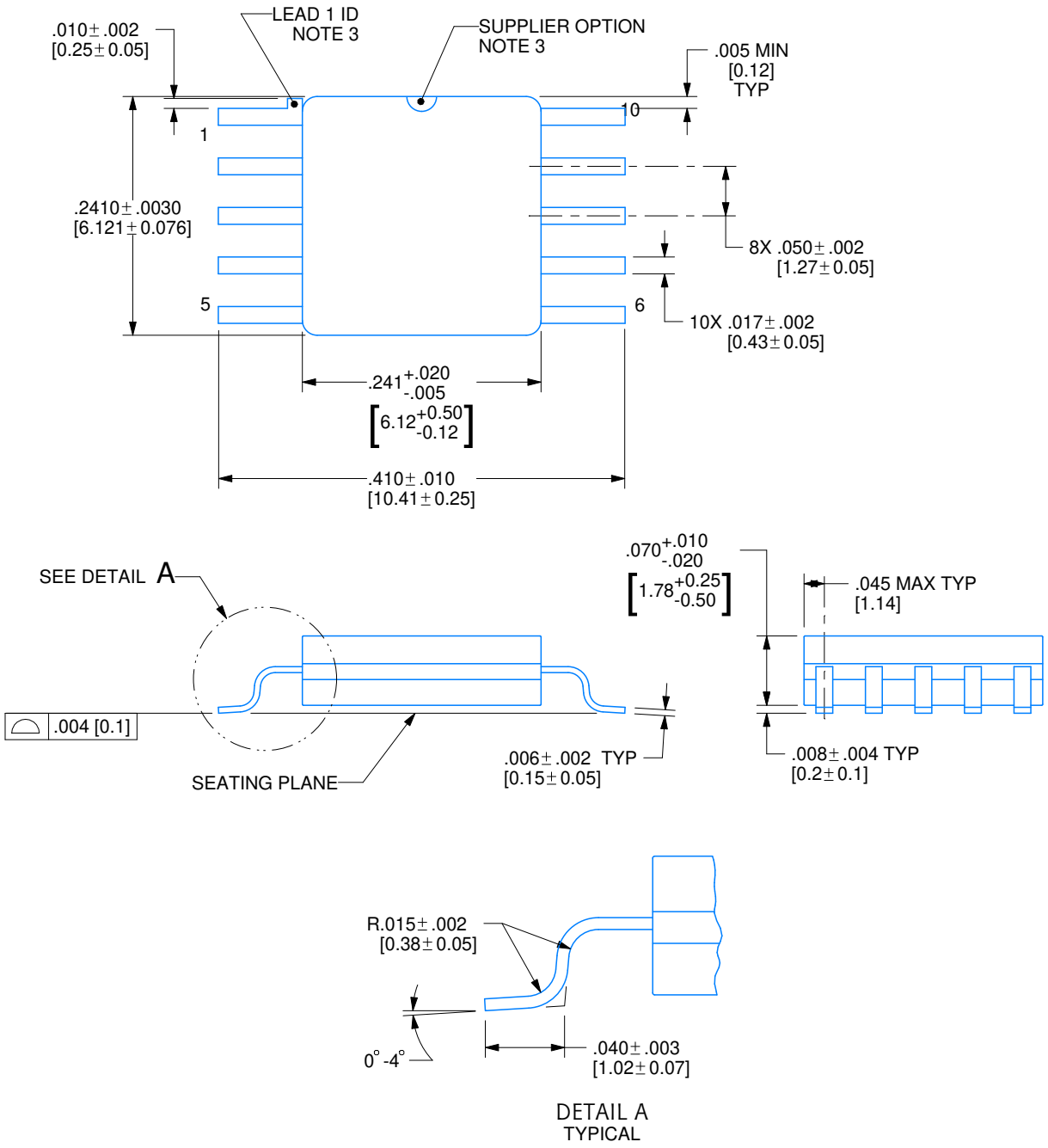

.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

NAC0010A

PACKAGE OUTLINE

CFP - 2.33mm max height

CERAMIC FLATPACK



4215196/D 08/2022

NOTES:

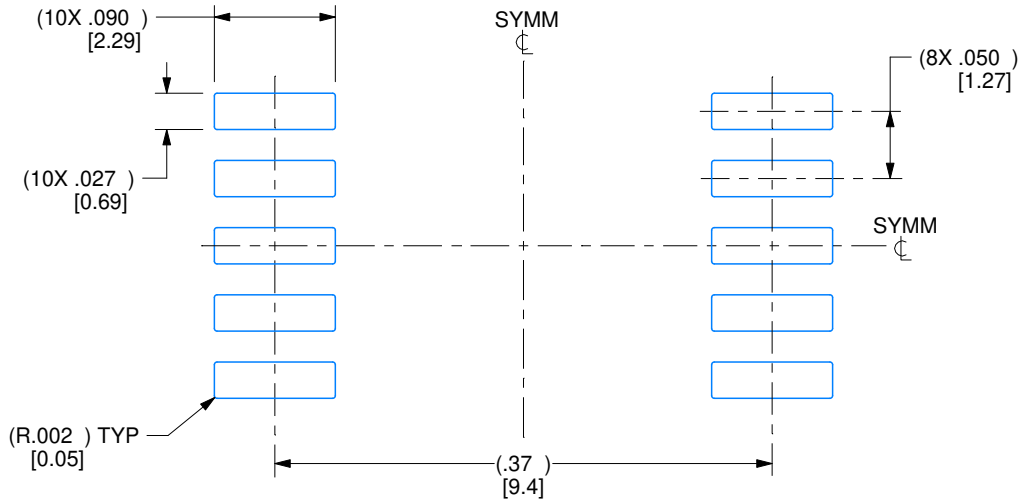
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

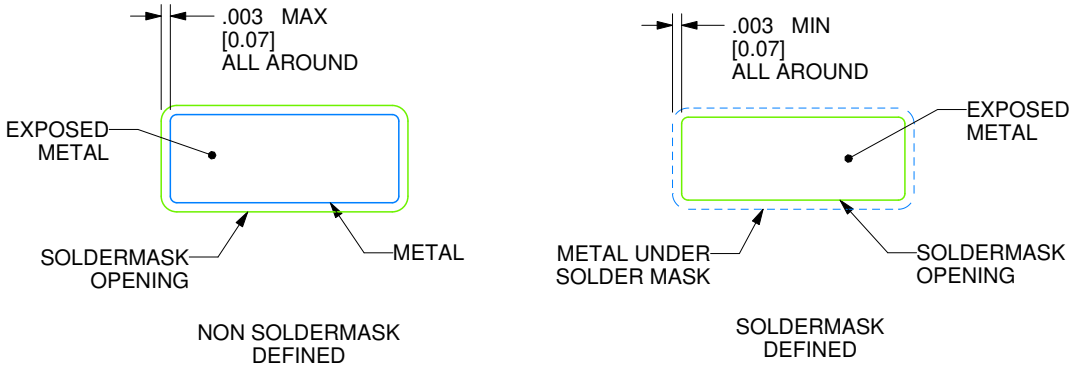
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



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REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265