



N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)		
30	0.050 at V _{GS} = 10 V	3.4		
30	0.085 at V _{GS} = 4.5 V	2.6		

FEATURES

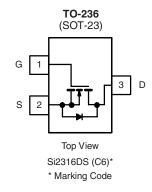
- Halogen-free Option Available
- TrenchFET® Power MOSFET

Pb-free Available

Available
RoHS
COMPLIANT

APPLICATIONS

· Battery Switch



Ordering Information: Si2316DS-T1

Si2316DS-T1-E3 (Lead (Pb)-free)

Si2316DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	A = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Dusin Comment /T 450 0008 b	T _A = 25 °C	- I _D	3.4	2.9	
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 70 °C		2.7	2.3	
Pulsed Drain Current ^b		I _{DM}	16		Α
Continuous Source Current (Diode Conduction) ^{a, b}		I _S	0.8		
D	T _A = 25 °C	P _D	0.96	0.7	W
Power Dissipation ^{a, b}	T _A = 70 °C	- FD	0.6	0.45	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Manipulation to Applicate	t ≤ 5 s	R _{thJA}	100	130		
Maximum Junction-to-Ambient ^a	Steady State	' ¹thJA	140	175	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	60	75		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Pulse width limited by maximum junction temperature.
- * Pb containing terminations are not RoHS compliant, exemptions may apply.

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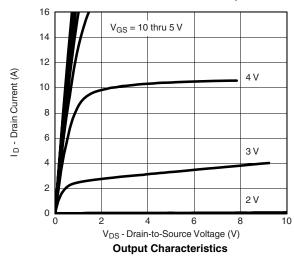
SPECIFICATIONS T _A = 25 °C, unless otherwise noted							
			Limits				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.8			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	I _{DSS} -	V _{DS} = 30 V, V _{GS} = 0 V			0.5		
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
	1	$V_{DS} \ge 4.5 \text{ V}, V_{GS} = 10 \text{ V}$	6				
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 4.5 \text{ V}, V_{GS} = 4.5 \text{ V}$	4			Α	
	Б	$V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$		0.042	0.050	Ω	
Drain-Source On-Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 2.6 \text{ A}$		0.068	0.085		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 4.5 \text{ V}, I_D = 3.4 \text{ A}$		6.0		S	
Diode Forward Voltage	V_{SD}	I _S = 0.8 A, V _{GS} = 0 V		0.8	1.2	V	
Dynamic ^b	•			•	•		
Total Gate Charge	Q_g			4.3	7		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$		0.65		nC	
Gate-Drain Charge	Q_{gd}			1.2		1	
Input Capacitance	C _{iss}			215			
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	90		pF		
Reverse Transfer Capacitance	C _{rss}			55		1	
Switching	•				•		
Turn-On Delay Time	t _{d(on)}			9	15		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		9	15		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1.0 A, V_{GEN} = 10 V, R_G = 6 Ω		14	20	ns -	
Fall Time	t _f			6	12		

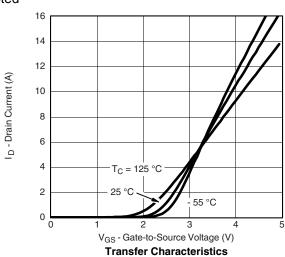
Notes:

- a. Pulse test; PW $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



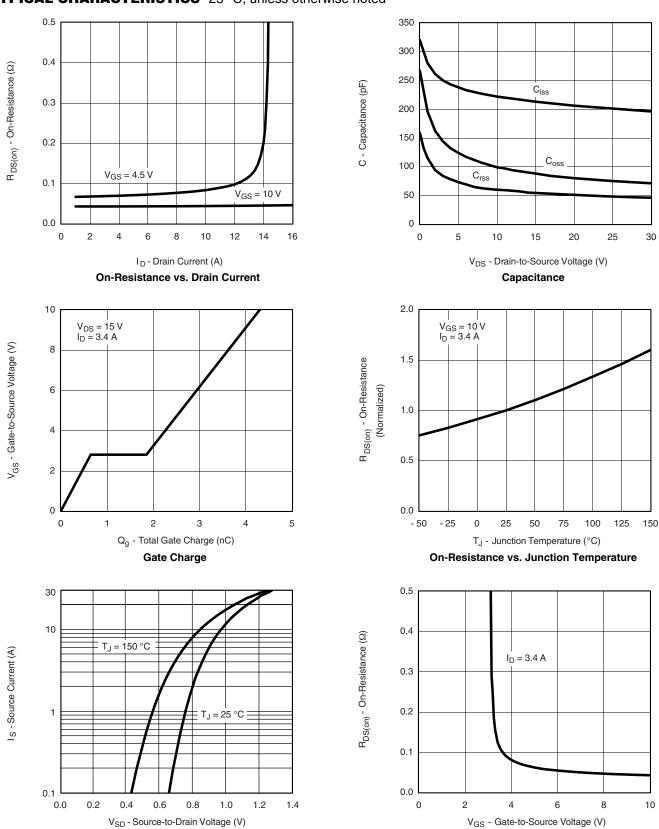








TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



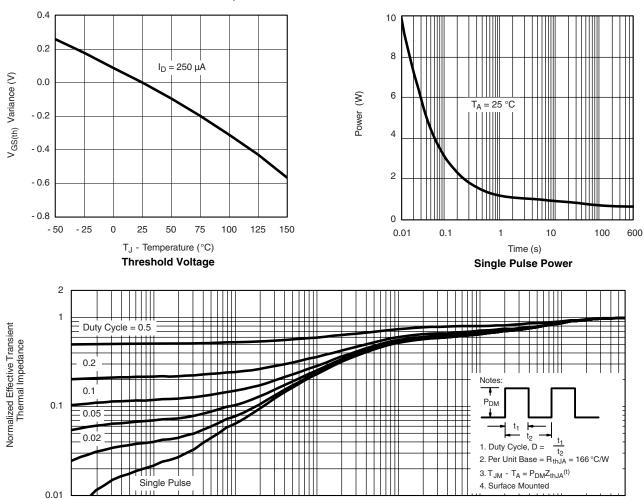
Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Ambient

10-1

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71798.

10-4

10-3

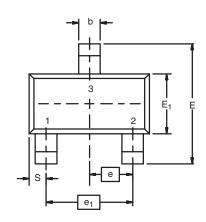
10-2

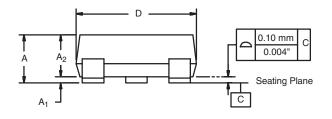
100

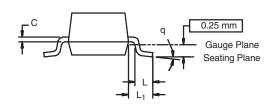
600

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SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES			
	Min	Max	Min	Max		
Α	0.89	1.12	0.035	0.044		
A ₁	0.01	0.10	0.0004	0.004		
A ₂	0.88	1.02	0.0346	0.040		
b	0.35	0.50	0.014	0.020		
С	0.085	0.18	0.003	0.007		
D	2.80	3.04	0.110	0.120		
Е	2.10	2.64	0.083	0.104		
E ₁	1.20	1.40	0.047	0.055		
е	0.95 BSC		0.0374 Ref			
e ₁	1.90 BSC		0.074	0.0748 Ref		
L	0.40	0.60	0.016	0.024		
L ₁	0.64 Ref		0.025 Ref			
S	0.50 Ref		0.020 Ref			
q	3°	8°	3°	8°		
FCN: S-03946-Rev K 09-	lul-01					

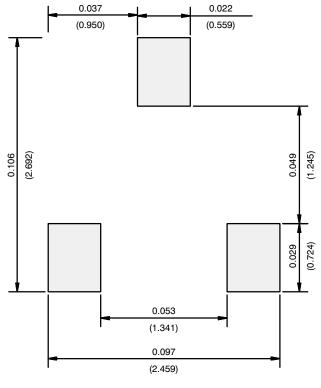
ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01



RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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