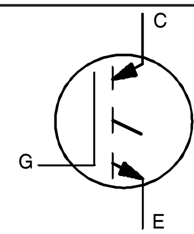
International
IOR Rectifier

IRG4BC30WPbF

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability
- Lead-Free



n-channel

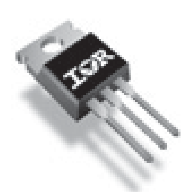
$V_{CES} = 600V$

$V_{CE(on)}$ max. $= 2.70V$

$@V_{GE} = 15V$, $I_C = 12A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	–––	80	
Wt	Weight	1.44	–––	g

02/04/10

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.34	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.1	2.7	V	I_C = 12A; V_{GE} = 15V
		—	2.45	—		I_C = 23A; See Fig.2, 5
		—	1.95	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	11	16	—	S	V_{CE} = 100 V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	76	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.6	11		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	
t_r	Rise Time	—	16	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	99	150		I_C = 12A, V_{CC} = 480V
t_f	Fall Time	—	67	100		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.13	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.13	—		See Fig. 9, 10, 13, 14
E_{ts}	Total Switching Loss	—	0.26	0.35		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	17	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.55	—	mJ	See Fig. 11,13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	980	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	71	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	18	—		ƒ = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

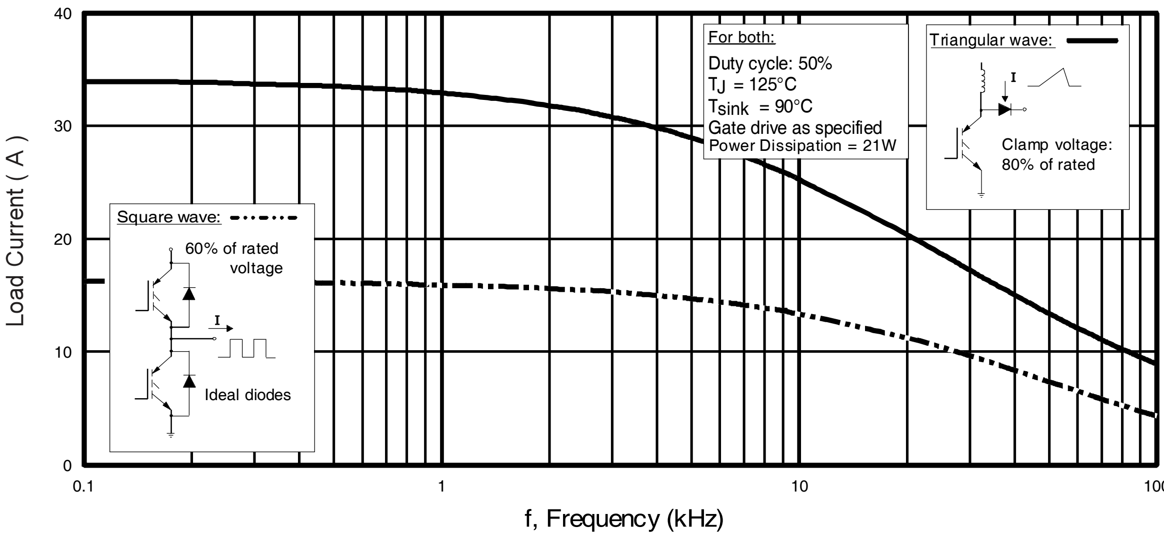


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

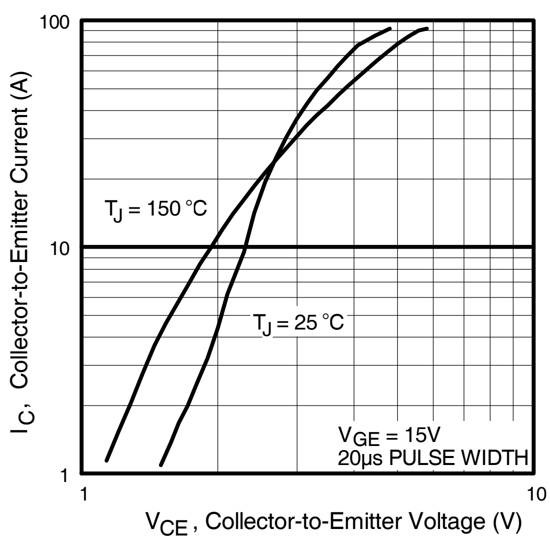


Fig. 2 - Typical Output Characteristics

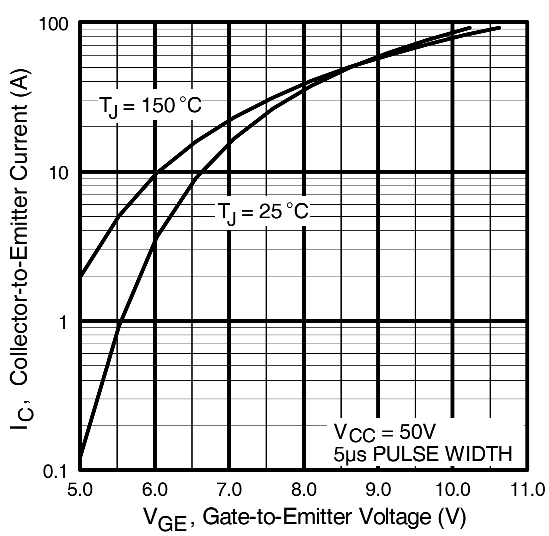


Fig. 3 - Typical Transfer Characteristics

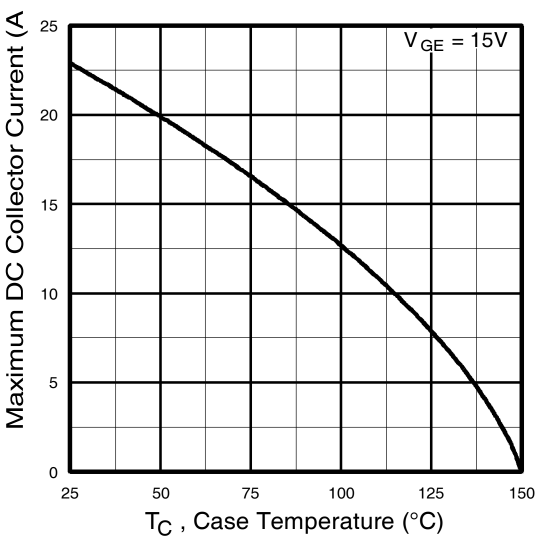


Fig. 4 - Maximum Collector Current vs. Case Temperature

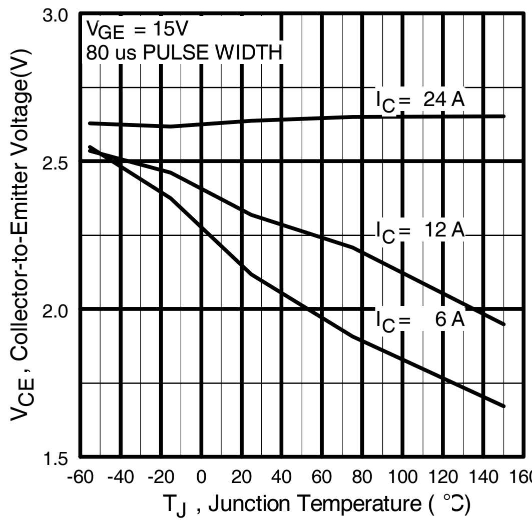


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

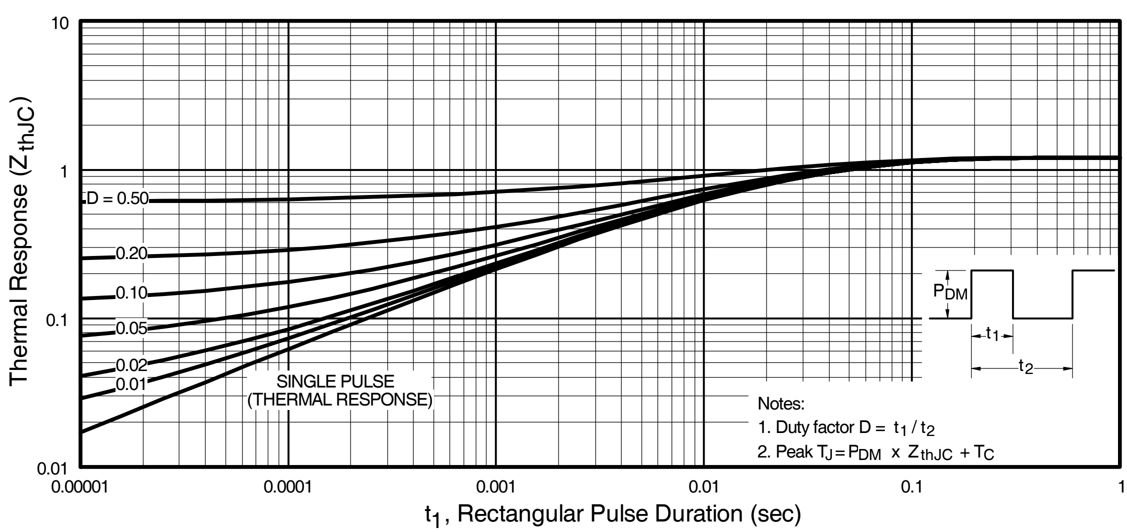


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

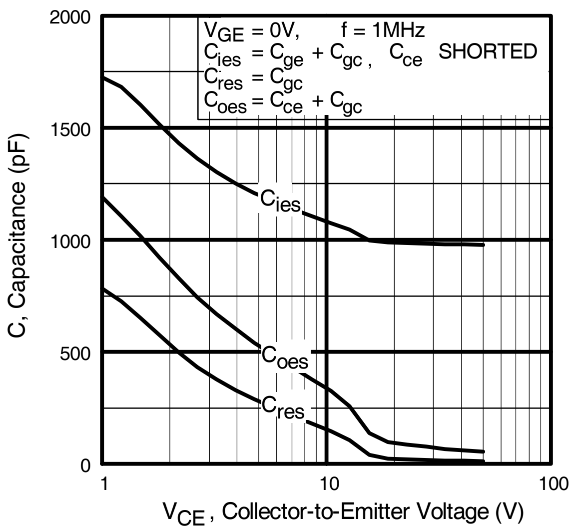


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

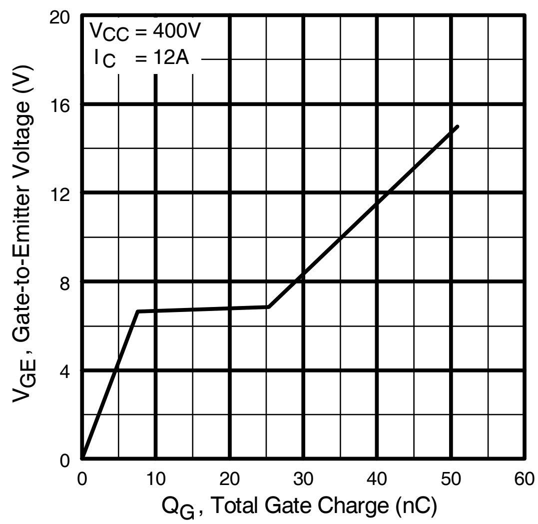


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

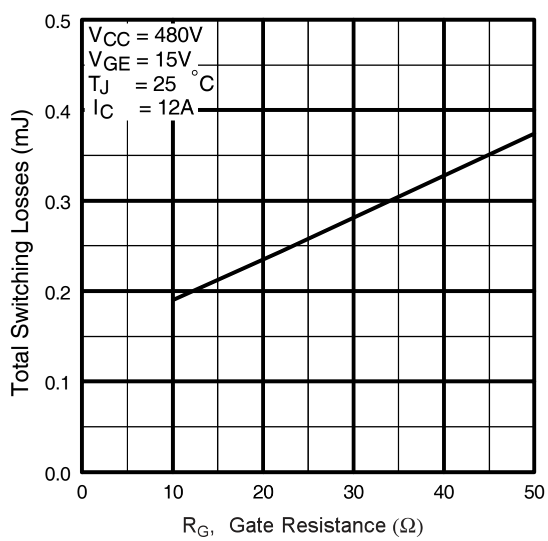


Fig. 9 - Typical Switching Losses vs. Gate Resistance

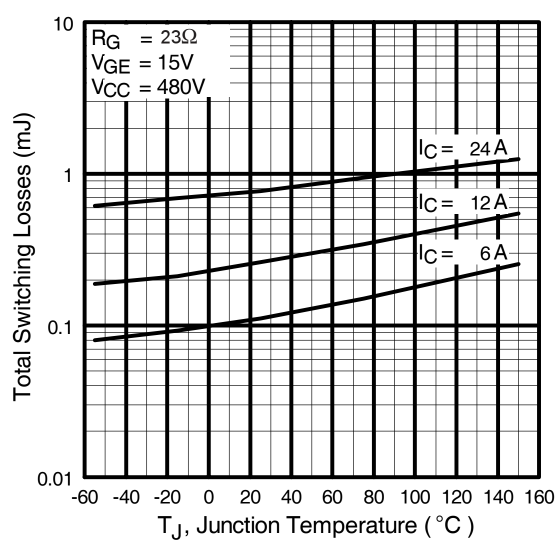


Fig. 10 - Typical Switching Losses vs. Junction Temperature

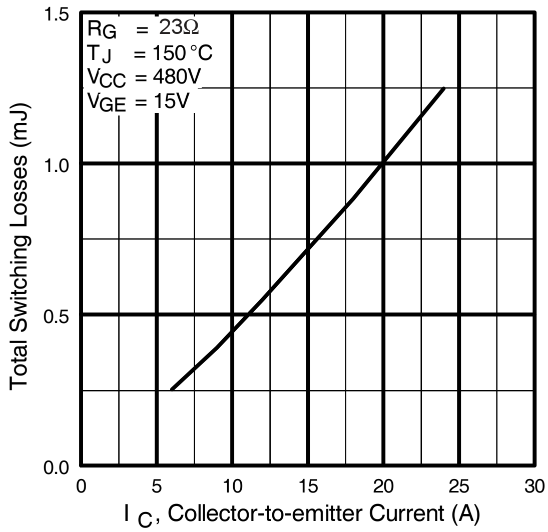


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

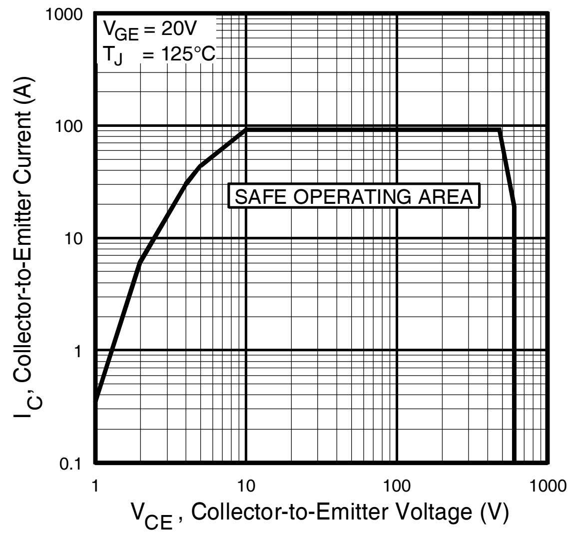


Fig. 12 - Turn-Off SOA

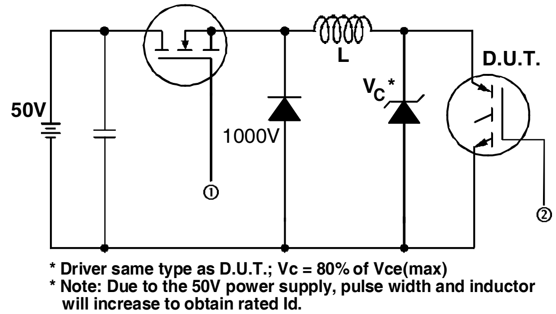


Fig. 13a - Clamped Inductive Load Test Circuit

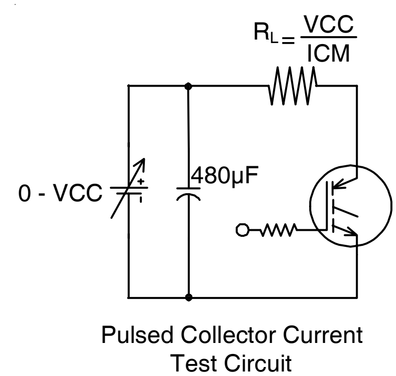


Fig. 13b - Pulsed Collector Current Test Circuit

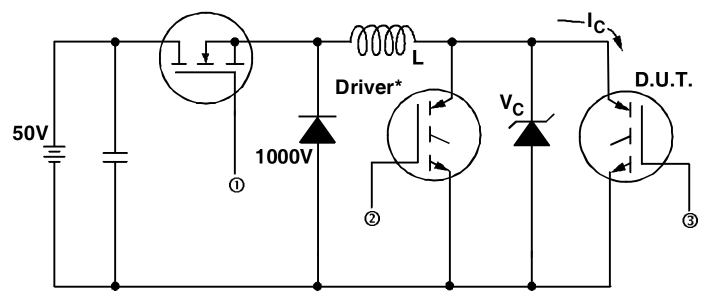


Fig. 14a - Switching Loss Test Circuit

* Driver same type as D.U.T., VC = 480V

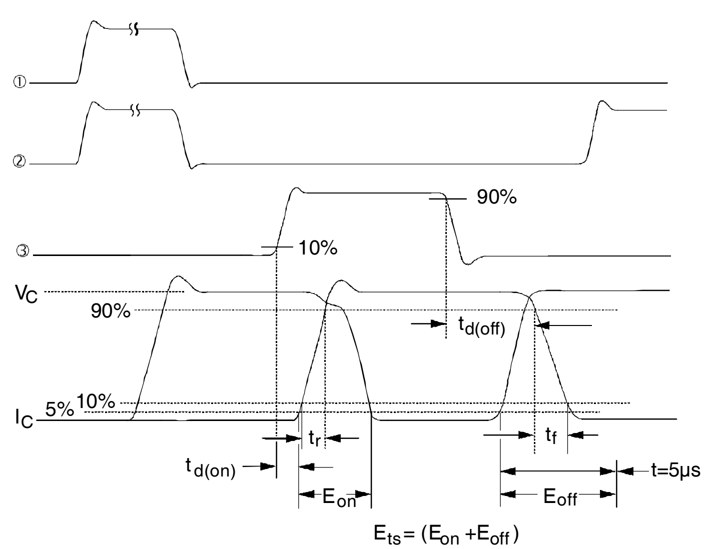
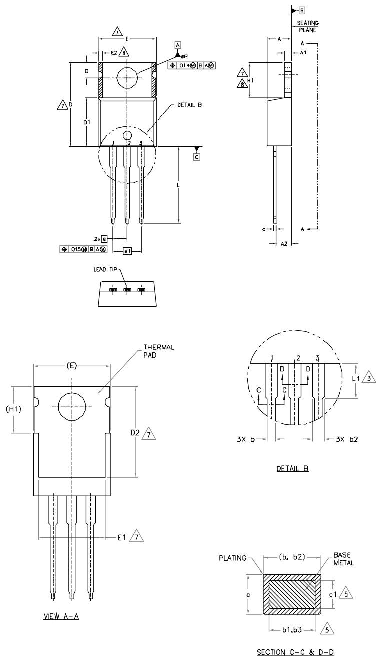


Fig. 14b - Switching Loss Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.- CONTROLLING DIMENSION : INCHES.
7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3 - EMITTER

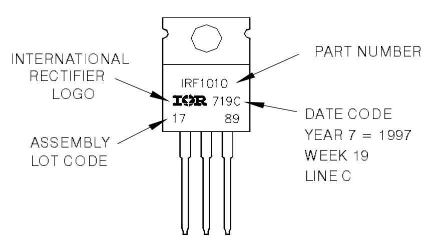
DIODES

1.- ANODE
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.

International
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