

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	87P50 Series	8048I Series
	8048 Series	
	8048L Series	
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
All Input or Output Voltages with Respect to V _{SS}	-0.5V to +7V	-0.5V to +7V
Power Dissipation	1.5W	1.5W

Note: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Features	INS8048 Series	INS8048L Series	INS8048I Series	NS87P50 Series
▪ -40 to +85°C Operation			X	
▪ 8-Bit CPU, RAM, ROM, I/O in a Single Package	X	X	X	
▪ 2.5 μs Cycle, 6 MHz Clock; 1.36 μs Cycle, 11 MHz Clock	X	X	X	X
▪ Very Low Power, High Speed Operation		X		
▪ On-Chip Oscillator Circuit and Clock (or External Source)	X	X	X	X
▪ 27 I/O Lines	X	X	X	X
▪ Expandable Memory and I/O	X	X	X	X
▪ 8-Bit Timer/Counter	X	X	X	X
▪ Single-Level Interrupt	X	X	X	X
▪ 96 Instructions (Most Single-Byte)	X	X	X	X
▪ Binary and BCD Arithmetic	X	X	X	X
▪ Single +5V Power Supply	X	X	X	X
▪ Low Standby Power Mode	X	X	X	X
▪ Low Voltage Standby	2.2V Min	2.2V Min	2.2V Min	2.6V Min

DC Electrical Characteristics

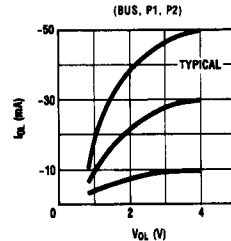
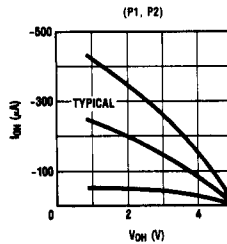
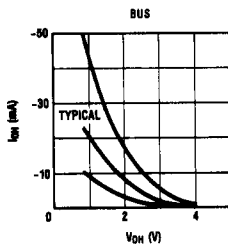
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise specified. (NS8048, INS8048L)

$T_A = 40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise specified. (NS8048I) (Note 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage (Except XTAL1, XTAL2, $\overline{\text{RESET}}$)		-0.5		0.8	V
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)		-0.5		0.6	V
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, $\overline{\text{RESET}}$)		2.0		V_{CC}	V
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)		3.8		V_{CC}	V
V_{OL}	Output Low Voltage (Bus)	$I_{OL} = 2\text{ mA}$			0.45	V
V_{OL1}	Output Low Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	$I_{OL} = 1.8\text{ mA}$			0.45	V
V_{OL2}	Output Low Voltage ($\overline{\text{PROG}}$)	$I_{OL} = 1.0\text{ mA}$			0.45	V
V_{OL3}	Output Low Voltage (Ports and Others)	$I_{OL} = 1.6\text{ mA}$			0.45	V
V_{OH}	Output High Voltage (Bus)	$I_{OH} = -400\ \mu\text{A}$	2.4			V
V_{OH1}	Output High Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	$I_{OH} = -100\ \mu\text{A}$	2.4			V
V_{OH2}	Output High Voltage (Ports and Others)	$I_{OH} = -40\ \mu\text{A}$	2.4			V
I_{LI}	Input Leakage Current (T1, INT, EA)	$V_{SS} \leq V_{IN} \leq V_{CC}$			± 10	μA
I_{LI1}	Input Leakage Current Ports	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$			-500	μA
I_{LI2}	Input Leakage Current (SS, $\overline{\text{RESET}}$)	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$			-300	μA
I_{LO}	Output Leakage Current (Bus, T_0) High Impedance State	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$			± 10	μA
$I_{DD} 64$	Standby Current (Note 1)	8048, 8048I, 8048L			5/4	mA
$I_{DD} 128$	Standby Current (Note 1)	8049, 8049I, 8049L			7/5	mA
$I_{DD} 256$	Standby Current (Note 1)	8050, 8050I, 8050L			10/10	mA
$I_{DD} + I_{CC}$	Total Supply (Note 1)	8048, 8048I, 8048L			65/55	mA
$I_{DD} + I_{CC}$	Total Supply (Note 1)	8049, 8049I, 8049L			70/60	mA
$I_{DD} + I_{CC}$	Total Supply (Note 1)	8050, 8050I, 8050L			80/65	mA
V_{DD}	Standby Power Supply (8048, 8048I, 8048L Series)		2.2		V_{CC}	V

Note 1: For industrial device $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Note 2: Combination of low power and industrial temperature devices not accepted.



AC Characteristics $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ($-40^\circ\text{C to } +85^\circ\text{C}$ for 8048I), $V_{CC} = V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	f(t_{CY}) (Note 3)	11 MHz		Units
			Min	Max	
t_{LL}	ALE Pulse Width (Note 1)	$7/30 t_{CY} - 170$	150		ns
t_{AL}	Address Setup to ALE (Note 1)	$2/15 t_{CY} - 110$	70		ns
t_{LA}	Address Hold from ALE (Note 1)	$1/15 t_{CY} - 40$	50		ns
t_{CC1}	Control Pulse Width (\overline{RD} , \overline{WR}) (Note 1)	$1/2 t_{CY} - 200$	480		ns
t_{CC2}	Control Pulse Width (\overline{PSEN}) (Note 1)	$2/5 t_{CY} - 200$	350		ns
t_{DW}	Data Setup Before \overline{WR} (Note 1)	$13/30 t_{CY} - 200$	390		ns
t_{WD}	Data Hold After \overline{WR} (Notes 1, 2)	$1/15 t_{CY} - 50$	40		ns
t_{DR}	Data Hold (\overline{RD} , \overline{PSEN}) (Notes 1, 4)	$1/10 t_{CY} - 30$	0	110	ns
t_{RD1}	\overline{RD} to Data in (Note 1)	$2/5 t_{CY} - 170$		370	ns
t_{RD2}	\overline{PSEN} to Data in (Note 1)	$3/10 t_{CY} - 170$		240	ns
t_{AW}	Address Setup to \overline{WR} (Note 1)	$1/3 t_{CY} - 150$	300		ns
t_{AD1}	Address Setup to Data (\overline{RD}) (Note 1)	$21/30 t_{CY} - 220$		730	ns
t_{AD2}	Address Setup to Data (\overline{PSEN}) (Note 1)	$1/2 t_{CY} - 200$		480	ns
t_{AFC1}	Address Float to \overline{RD} , \overline{WR} (Notes 1, 2)	$2/15 t_{CY} - 40$	140		ns
t_{AFC2}	Address Float to \overline{PSEN} (Notes 1, 2)	$1/30 t_{CY} - 40$	10		ns
t_{LAFC1}	ALE to Control (\overline{RD} , \overline{WR}) (Note 1)	$1/5 t_{CY} - 75$	200		ns
t_{LAFC2}	ALE to Control (\overline{PSEN}) (Note 1)	$1/10 t_{CY} - 75$	60		ns
t_{CA1}	Control to ALE (\overline{RD} , \overline{WR} , \overline{PROG}) (Note 1)	$1/15 t_{CY} - 40$	50		ns
t_{CA2}	Control to ALE (\overline{PSEN}) (Note 1)	$4/15 t_{CY} - 40$	320		ns
t_{CP}	Port Control Setup to \overline{PROG} (Note 1)	$1/10 t_{CY} - 80$	50		ns
t_{PC}	Port Control Hold from \overline{PROG} (Note 1)	$4/15 t_{CY} - 260$	100		ns
t_{PR}	\overline{PROG} to P2 Input Valid (Note 1)	$17/30 t_{CY} - 140$		630	ns
t_{PF}	Input Data Hold from \overline{PROG} (Notes 1, 4)	$1/10 t_{CY}$	0	140	ns
t_{DP}	Output Data Setup (Note 1)	$2/5 t_{CY} - 290$	260		ns
t_{PD}	Output Data Hold (Note 1)	$1/10 t_{CY} - 90$	40		ns
t_{PP}	\overline{PROG} Pulse Width (Note 1)	$7/10 t_{CY} - 250$	700		ns
t_{PL}	Port 2 I/O Setup to ALE (Note 1)	$4/15 t_{CY} - 200$	160		ns
t_{LP}	Port 2 I/O Hold to ALE (Note 1)	$1/10 t_{CY} - 120$	15		ns
t_{PV}	Port Output From ALE (Note 1)	$3/10 t_{CY} + 100$		510	ns
t_{CY}	Cycle Time (Note 3)		1.36	15	μs
t_{OPRR}	T_0 Rep Rate	$3/15 t_{CY}$	270		ns

Note 1: Control outputs $C_L = 80$ pF, Bus outputs $C_L = 150$ pF.

Note 2: Bus High Impedance Load = 20 pF.

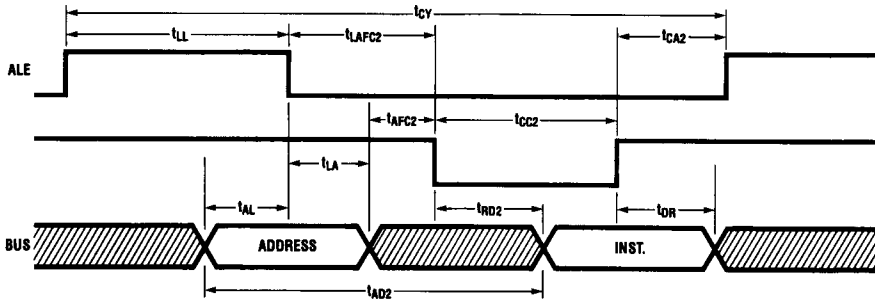
Note 3: $t_{CY} = 15/f$ (assumes 50% duty cycle).

Note 4: Maximum spec listed is for user information only to prevent system bus contention.

Note 5: $V_{IH} = 3.8V$, $V_{IL} = 0.45V$.

Timing Waveforms (Continued)

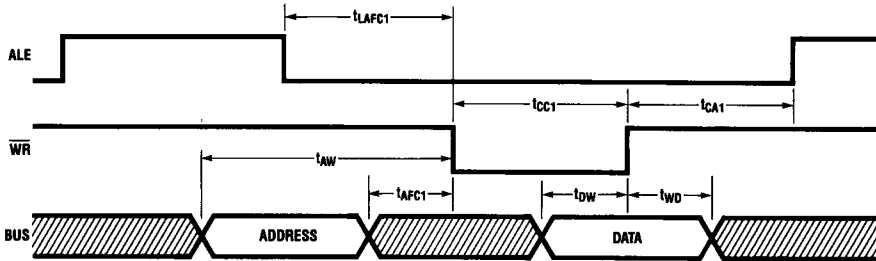
Instruction Fetch from External Program Memory



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Note: Diagonal lines indicate interval of high impedance.

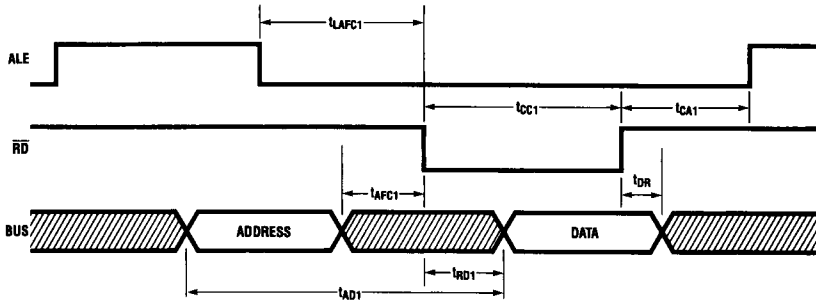
Write to External Data Memory



TL/C/5488-6

Note: Diagonal lines indicate interval of high impedance.

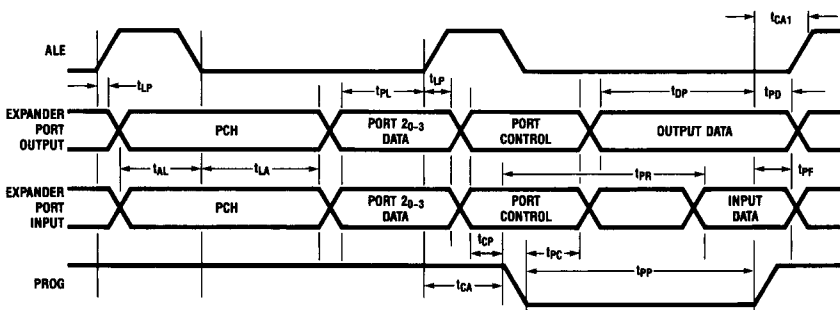
Read from External Data Memory



TL/C/5488-7

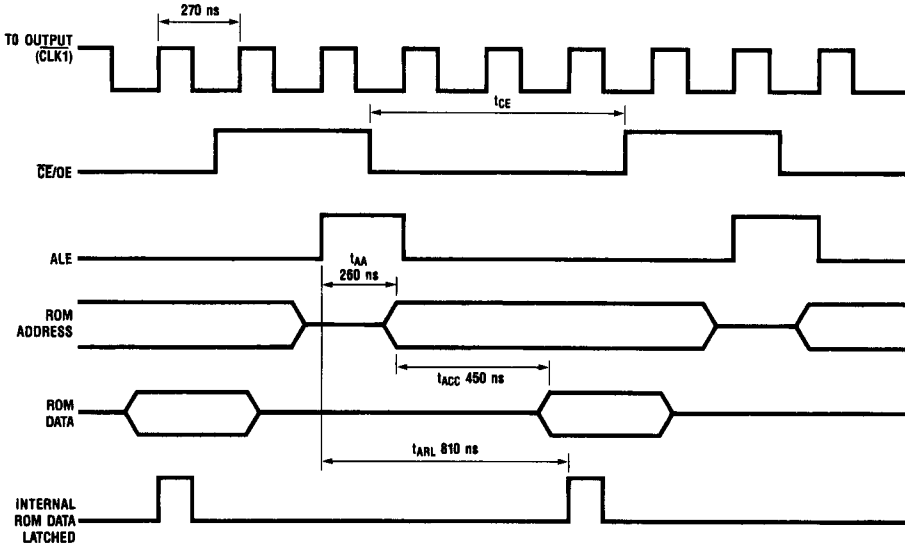
Note: Diagonal lines indicate interval of high impedance.

Port 2 Timing



TL/C/5488-8

NS87P50U Piggy-Back Microcomputer EPROM Timing



Frequency = 11 MHz

TL/C/5488-11

AC Electrical Characteristics

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $V_{DD} = 3.6\text{V to } 5.5\text{V}$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{ACC}	ROM Address Setup to ROM Data (6 MHz Access Time)	6 MHz			850	ns
t_{ACC}	ROM Address Setup to ROM Data (11 MHz Access Time)	11 MHz			450	ns
t_{CE}	Chip Enable and Output Enable Active	11 MHz			870	ns
t_{AA}	ALE to ROM Address Setup	11 MHz			260	ns
t_{ARL}	ALE to ROM Data Latch	11 MHz			810	ns

Other AC Electrical Characteristics same as 48-Series.

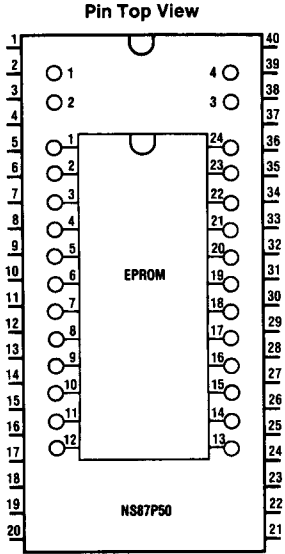
DC Electrical Characteristics

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = V_{DD} = +5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC1}	Current Available to EPROM	$V_{CC} = 5\text{V}$			150	mA
I_{PP}	V_{PP} Current	$V_{PP} = 5\text{V}$			5	mA
I_{DD}	256 Words on Standby Current				20	mA
$I_{DD} + I_{CC}$	Total Supply Current (without EPROM)	$T_A = 25^\circ\text{C}$ All Outputs Open		60	100	mA
V_{DD}	Standby Power Supply		2.6		V_{CC}	V

Other DC Electrical Characteristics same as 48-Series.

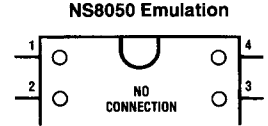
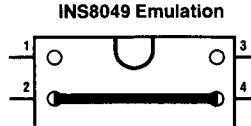
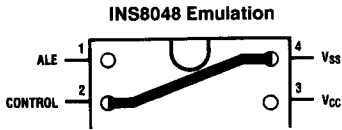
Connection Diagrams



EPROM Pin Descriptions

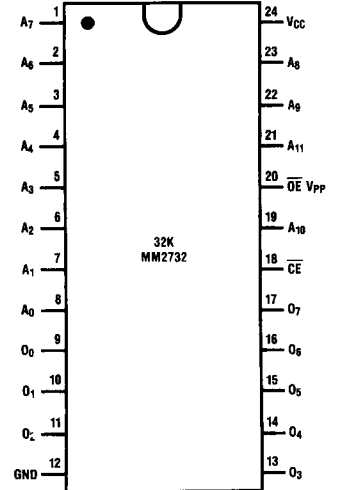
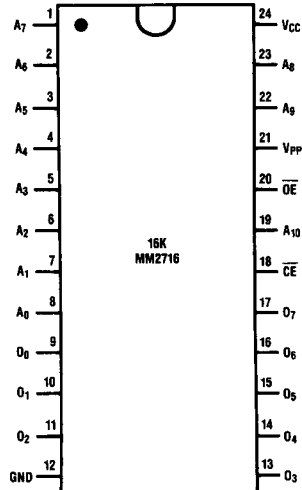
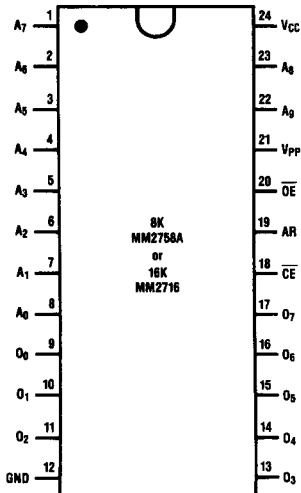
A_0-A_9	Addresses
\overline{CE}/PGM	Chip Enable Program
\overline{OE}	Output Enable
O_0-O_7	Outputs
A_R	Select Reference Input Level— V_{SS}
V_{PP}	+5V
V_{CC}	+5V
GND	Power Ground
A_R	Ground

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TL/C/5488-13

EPROM



TL/C/5488-14

Functional Pin Descriptions

INPUT SIGNALS

Reset (RESET): An active low (0) input that initializes the processor and is used to verify program memory.

Single Step (SS): Active low (0) input which, in conjunction with ALE, can single step the processor through each instruction.

External Access (EA): An active high (1) input that forces all program memory fetches to reference external program memory.

Testable Input 0 (T0): Testable input pin using conditional branch functions JT0 (T0 = 1) or JNT0 (T0 = 0). T0 can be designated as the clock output using instruction ENT0 CLK. For NS8050U, T0 is also used as the SK clock output for MASTER and SK clock input for SLAVE in the MICRO-WIRE/PLUS mode. Done FLIP FLOP is tested by testing T0.

Testable Input 1 (T1): Testable input pin using conditional branch functions JT1 (T1 = 1) or JNT1 (T1 = 0). T1 can be designated as the Timer/Counter input from an external source using instruction STRT CNT.

Interrupt (INT): An active low input that initiates an interrupt when interrupt is enabled. Interrupt is disabled after a RESET. Also can be tested with instruction JNI (INT = 0).

OUTPUT SIGNALS

Read Strobe (RD): An active low output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory.

Write Strobe (WR): An active low output strobe activated during a Bus write. Used as a Write Strobe to External Data Memory.

Program Store Enable (PSEN): An active low output that occurs only during an external program memory fetch.

Address Latch Enable (ALE): An active high output that occurs once during each cycle and is useful as a clock output. The negative going edge of ALE strobes the address into External Data or Program Memory.

Program (PROG): This output (active out) provides the output strobe for INS8243 I/O Expander.

INPUT/OUTPUT SIGNALS

Crystal Input (XTAL1, XTAL2): These two pins connect the crystal for internal oscillator operation. XTAL1 is the timing input for external source.

Port 1 (P10–P17): 8-bit quasi-bidirectional port.

Port 2 (P20–P27): 8-bit quasi-bidirectional port. During an external program memory fetch, the 4 high-order program counter bits occur at P20–P23. They also serve as a 4-bit I/O Expander Bus when the INS8243 I/O Expander is used.

Bus (DB₀–DB₇): True bidirectional port, either statically latched or synchronous. Can be written to using WR Strobe, or Read from using RD Strobe. During an External Program Memory fetch, the 8 lower-order program counter bits are present at this port. The addressed instruction appears on this bus when PSEN is low. During an external RAM data transaction, this port presents address and data under control of ALE, RD, WR.

V_{SS}: Processor Ground potential.

V_{DD}: V_{DD} functions as the Low Power Standby Voltage. Can be tied to V_{CC} if power-down operation is not required.

V_{CC} (Pin 40): Primary power source for 48-Series devices.

NS8050U MICROWIRE Mode Pin Descriptions

Pin 1, Serial Clock (SK): Input or output clocking signal to the MICROWIRE/PLUS serial circuitry.

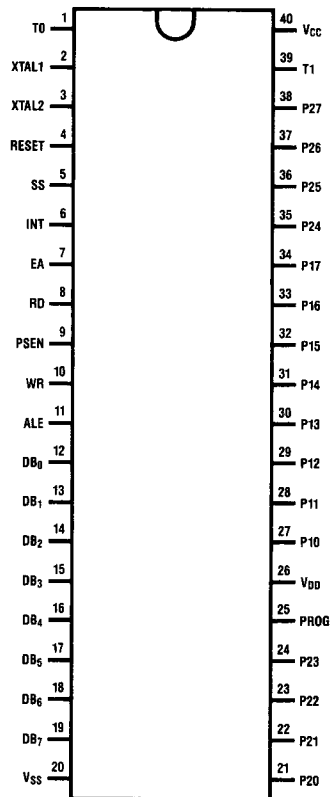
Pin 38, Serial Input (SI): Serial input to the 8-bit MICRO-WIRE/PLUS shift register.

Pin 37, Serial Output (SO): Serial output from the 8-bit MICRO-WIRE/PLUS shift register.

Pin 3, XTAL2: High-impedance input to oscillator circuit.

Pin 2, XTAL1: Low-impedance output from oscillator circuit.

Connection Diagram



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Order Number INS8048, INS8048J, INS8048L, INS8049, INS8049I, INS8049L, NS8040U, NS8050I, NS8050L, NS8050U, NS87P50, NS87P50I and NS87P50U
See NS Package Number D40G or N40A

Functional Description

The following paragraphs contain the functional description of the major elements of the 48-Series microcomputer/microprocessor. (Figure 1) is a block diagram of the 48-Series devices. The data paths are illustrated in simplified form

to show how the various logic elements communicate with each other to implement the instruction set common to all devices.

48-Series Block Diagram

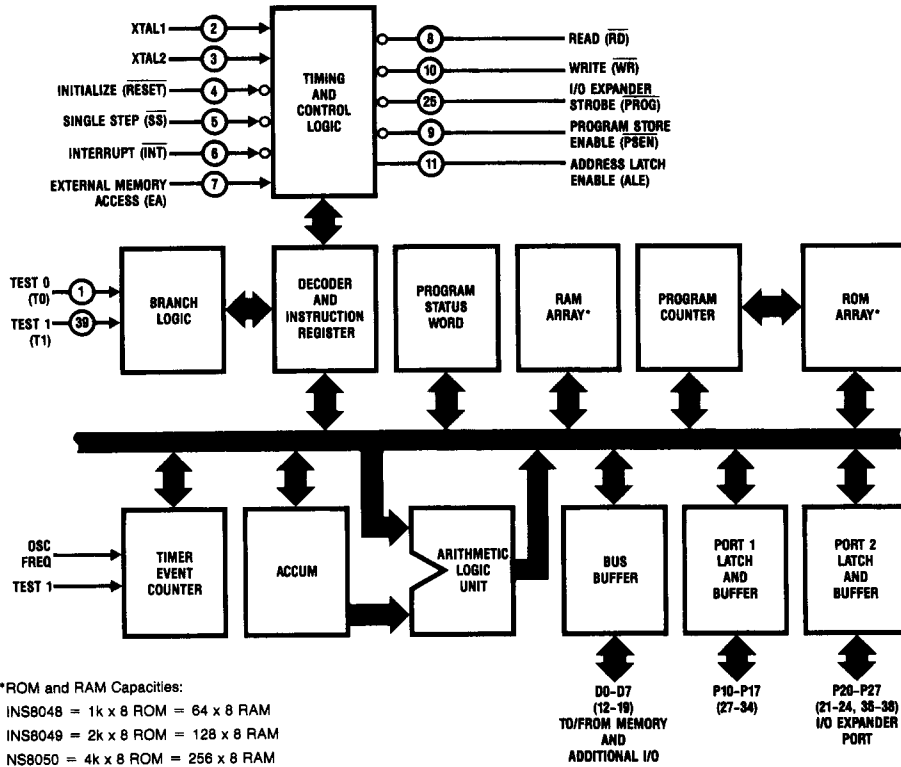


FIGURE 1. 48-Series Detailed Block Diagram

TL/C/5488-16

Functional Description (Continued)

PROGRAM MEMORY

The Program Memory (ROM) contained on the INS8048/49/50 devices is comprised of 1024, 2048 or 4096 8-bit bytes, respectively. As is seen by examining the 48-Series instruction set, these bytes may be program instructions, program data or ROM addressing data. The ROM for the above devices must be mask programmed at the National Semiconductor factory. The ROMless microcomputers, INS8035, INS8039 and INS8040, use external program memory. This makes program development straightforward using standard UV erasable PROMs to emulate a possible future single chip (using the on-board ROM) system. ROM addressing, up to a maximum of 4k, is accomplished by a 12-bit Program Counter (PC). The INS8048 and INS8049 will automatically address external memory when the boundary of their internal memories, 1k and 2k respectively, are exceeded. The binary value of the address selects one of the 8-bit bytes contained in ROM. A new address is load-

ed into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential binary count value.

With reference to the Program Memory Map (see Figure 2) there are three ROM addresses which provide for the control of the microcomputer.

1. Memory Location 0000—Asserting the RESET (negative true) input to the microcomputer forces the first instruction to be fetched from address 0000.
2. Memory Location 0003—Asserting the interrupt (negative true) input to the microcomputer (when interrupt is enabled) forces a jump to subroutine.
3. Memory Location 0007—A Timer/Counter interrupt that results from Timer/Counter overflow (when enabled) forcing a jump to subroutine.

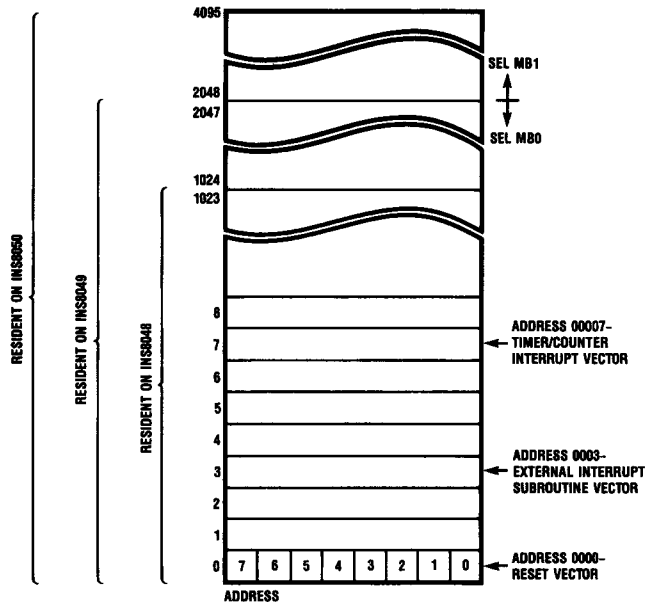


FIGURE 2. INS8048/49/50 Resident ROM Program Memory Map

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Functional Description (Continued)

DATA MEMORY (RAM)

The resident RAM data memory is arranged as 64 (INS8035/8048), 128 (INS8039/8049), or 256 (NS8040/8050) bytes. RAM addressing is implemented indirectly via either of two 8-bit RAM pointer registers R0 and R1. These pointer registers are essentially the first two locations in the RAM (see Figure 3), addressing 00 and 01. RAM addressing may also be performed directly by 11 direct register instructions. The register area of the RAM array is made up of eight working registers that occupy either the first bank (0), locations 0 to 7, or the second bank (1), locations 24 to 31. The second bank of working registers is selected by using the Register Bank Switch instruction (SEL RB). If this bank is not used for working registers, it can be used as user RAM.

There is an 8-level stack after Bank 0 that occupies address locations 8 to 23. These RAM locations are addressed indirectly through R0, R1 or the 3-bit Stack Pointer (SP). The stack pointer keeps track of the return address and pushes each return address down into the stack. There are 8 levels of subroutine nesting possible in the stack because each address occupies 10 bits or more using two bytes in RAM. When the level of subroutine nesting is less than 8, the stacks not used may be utilized as user RAM locations.

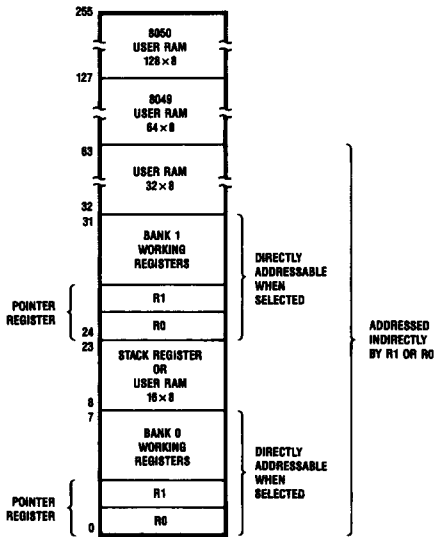


FIGURE 3. 8048-Series Resident RAM Data Memory Map

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INPUT/OUTPUT

The 48-series devices have 27 lines of input/output organized as three 8-bit ports plus three test inputs. The three ports may be used as inputs, outputs or bidirectional ports. Ports 1 and 2 differ from Port 3 (Bus Port) in that they are quasi-bidirectional ports. Ports 1 and 2 can be used as input and output while being statically latched. If more I/O lines are required, Port 2 can also serve as a 4-bit I/O bus expander when used in conjunction with the INS8243 I/O Expander.

The bus port is a true bidirectional port and is either statically latched or synchronous. It can be written to using \overline{WR} strobe or read from using \overline{RD} strobe. During an external program memory fetch, the 8 lower-order program counter bits are present at this port. The addressed instruction appears on this bus when \overline{PSEN} is low. During an external RAM data transaction, this port presents address and data under control of ALE, \overline{RD} , and \overline{WR} .

POWER-DOWN MODE

During the power-down mode, V_{DD} , which normally maintains the RAM cells, is the only pin that receives power. V_{CC} , which serves the CPU and ports, is dropped from a voltage of nominal 5 to 0 after the CPU is reset, so that the RAM cells are unaltered by the loss of power. When power is restored, the processor goes through the normal power-on procedure.

MICROWIRE FUNCTIONS

New functions applicable to microwire mode are as follows:

The SK output frequency is selected by writing into the P27 latch as follows:

- 0 = Instruction Cycle Divided by 1
- 1 = Instruction Cycle Divided by 4

The SO output is enabled or disabled by writing into the P26 latch as follows:

- 0 = Enabled
- 1 = Disabled

The DONE flip-flop is tested with the JTO, JNTO instructions.

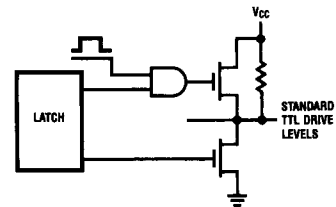


FIGURE 4. Ports 1 and 2 Input/Output Circuit

TL/C/5488-19

Instruction Set

Table I details the 96 instructions common to both the microcomputers and the microprocessors. The table provides the mnemonic, function, and description, instruction code, number of cycles and, where applicable, flag settings.

TABLE I. Instruction Set

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
CONTROL								
EN I		Enable the External Interrupt Input.	1	1				
DIS I		Disable the External Interrupt Input.	1	1				
ENT0 CLK		Enable T0 as the Clock Output.	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0–2047) of Program Memory.	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048–4095) of Program Memory.	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0–7) of Data Memory.	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24–31) of Data Memory.	1	1				
DATA MOVES								
MOV A, #data	(A) ← data	Move Immediate the specified data into the Accumulator.	2	2				
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated register into the Accumulator.	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move Indirect the contents of data memory location into the Accumulator.	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1				
MOV Rr, #data	(Rr) ← data; r = 0–7	Move Immediate the specified data into the designated register.	2	2				
MOV Rr, A	(Rr) ← (A); r = 0–7	Move Accumulator contents into the designated register.	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move Indirect Accumulator contents into data memory location.	1	1				
MOV @ Rr, #data	((Rr)) ← data; r = 0–7	Move Immediate the specified data into data memory.	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the Program Status Word.	1	1	•	•	•	
MOVP A, @ A	(PC 0–7) ← (A) (A) ← ((PC))	Move the content of program memory location in the current page addressed by the content of Accumulator into the Accumulator.	2	1				
MOVP3 A, @ A	(PC 0–7) ← (A) (PC 8–10) ← 011 (A) ← ((PC))	Move the content of program memory location in page 3 addressed by the content of Accumulator into the Accumulator.	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Move Indirect the contents of external data memory into the Accumulator.	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Move Indirect the contents of the Accumulator into external data memory.	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0–7	Exchange the Accumulator and designated register's contents.	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0–1	Exchange Indirect contents of Accumulator and location in data memory.	1	1				
XCHD A, @ Rr	(A0–A3) ← (((Rr)) 0–3); R = 0–1	Exchange Indirect 4-bit contents of Accumulator and data memory.	1	1				

TABLE I. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
ACCUMULATOR (Continued)								
RLA	$(A_n + 1) \leftarrow (A_n)$ for $n = 0-6$ $(A0) \leftarrow (A7)$	Rotate Accumulator left by 1-bit without carry.	1	1				
RLC A	$(A_n + 1) \leftarrow (A_n); n = 0-6$ $(A0) \leftarrow (C)$ $(C) \leftarrow (A7)$	Rotate Accumulator left by 1-bit through carry.	1	1	•			
RR A	$(A_n) \leftarrow (A_n + 1); n = 0-6$ $(A7) \leftarrow (A0)$	Rotate Accumulator right by 1-bit without carry.	1	1				
RRC A	$(A_n) \leftarrow (A_n + 1); n = 0-6$ $(A7) \leftarrow (C)$ $(C) \leftarrow (A0)$	Rotate Accumulator right by 1-bit through carry.	1	1	•			
SWAP	$(A4-A7) \leftrightarrow (A0-A3)$	Swap the 2 4-bit nibbles in the Accumulator.	1	1				
XRL A, #data	$(A) \leftarrow (A) \text{ XOR data}$	Logical XOR Immediate specified data with Accumulator.	2	2				
XRL A, Rr	$(A) \leftarrow (A) \text{ XOR } (Rr)$ for $r = 0-7$	Logical XOR contents of designated register with Accumulator.	1	1				
XRL A, @ Rr	$(A) \leftarrow (A) \text{ XOR } ((Rr))$ for $r = 0-1$	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1				
BRANCH								
DJNZ Rr, addr	$(Rr) \leftarrow (Rr) - 1; r = 0-7$ if $(Rr) \neq 0$; $(PC 0-7) \leftarrow \text{addr}$	Decrement the specified register and test contents.	2	2				
JBb addr	$(PC 0-7) \leftarrow \text{addr}$ if $Bb = 1$ $(PC) \leftarrow (PC) + 2$ if $BB = 0$	Jump to specified address if Accumulator bit is set.	2	2				
JC addr	$(PC 0-7) \leftarrow \text{addr}$ if $C = 1$ $(PC) \leftarrow (PC) + 2$ if $C = 0$	Jump to specified address if carry flag is set.	2	2				
JFO addr	$(PC 0-7) \leftarrow \text{addr}$ if $F0 = 1$ $(PC) \leftarrow (PC) + 2$ if $F0 = 0$	Jump to specified address if Flag F0 is set.	2	2				
JFI addr	$(PC 0-7) \leftarrow \text{addr}$ if $F1 = 1$ $(PC) \leftarrow (PC) + 2$ if $F1 = 0$	Jump to specified address if Flag F1 is set.	2	2				
JMP addr	$(PC 8-10) \leftarrow 8-10$ $(PC 0-7) \leftarrow \text{addr } 0-7$ $(PC 11) \leftarrow \text{DBF}$	Direct Jump to specified address with the 2k address block.	2	2				
JMPP @ A	$(PC 0-7) \leftarrow ((A))$	Jump Indirect to specified address pointed to by the Accumulator in current page.	2	1				
JNC addr	$(PC 0-7) \leftarrow \text{addr}$ if $C = 0$ $(PC) \leftarrow (PC) + 2$ if $C = 1$	Jump to specified address if carry flag is low.	2	2				
JNI addr	$(PC 0-7) \leftarrow \text{addr}$ if $I = 0$ $(PC) \leftarrow (PC) + 2$ if $I = 1$	Jump to specified address if interrupt is low.	2	2				
JNT0 addr	$(PC 0-7) \leftarrow \text{addr}$ if $T0 = 0$ $(PC) \leftarrow (PC) + 2$ if $T0 = 1$	Jump to specified address if Test 0 is low.	2	2				
JNT1 addr	$(PC 0-7) \leftarrow \text{addr}$ if $T1 = 0$ $(PC) \leftarrow (PC) + 2$ if $T1 = 1$	Jump to specified address if Test 1 is low.	2	2				

TABLE I. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
BRANCH (Continued)								
JNZ addr	$(PC) \leftarrow \text{addr}$ if $A \neq 0$ $(PC) \leftarrow (PC) + 2$ if $A = 0$	Jump to specified address if Accumulator is non-zero.	2	2				
JFT addr	$(PC) \leftarrow \text{addr}$ if $TF = 1$ $(PC) \leftarrow (PC) + 2$ if $TF = 0$	Jump to specified address if Timer Flag is set to 1.	2	2				
JT0 addr	$(PC) \leftarrow \text{addr}$ if $T0 = 1$ $(PC) \leftarrow (PC) + 2$ if $T0 = 0$	Jump to specified address if Test 0 is a 1.	2	2				
JT1 addr	$(PC) \leftarrow \text{addr}$ if $T1 = 1$ $(PC) \leftarrow (PC) + 2$ if $T1 = 0$	Jump to specified address if Test 1 is a 1.	2	2				
JZ addr	$(PC) \leftarrow \text{addr}$ if $A = 0$ $(PC) \leftarrow (PC) + 1$ if $A = 1$	Jump to specified address if Accumulator is 0.	2	2				
INPUT/OUTPUT								
ANL BUS, # data	$(BUS) \leftarrow (BUS) \text{ AND data}$	Logical AND Immediate specified data with contents of BUS.	2	2				
ANL Pp, # data	$(Pp) \leftarrow (Pp) \text{ AND data};$ $p = 1-2$	Logical AND Immediate specified data with designated port (1 or 2).	2	2				
ANLD Pp, A	$(Pp) \leftarrow (Pp) \text{ AND}$ $(A0-A3); p = 4-7$	Logical AND contents of Accumulator with designated port (4-7).	2	1				
IN A, Pp	$(A) \leftarrow (Pp); p = 1-2$	Input data from designated port (1-2) into Accumulator.	2	1				
INS A, BUS	$(A) \leftarrow (BUS)$	Input strobed BUS data into Accumulator.	2	1				
MOVD A, Pp	$(A0-A3) \leftarrow (Pp);$ $p = 4-7 (A4-A7) \leftarrow 0$	Move contents of designated port (4-7) into Accumulator.	2	1				
MOVD Pp, A	$(Pp) \leftarrow (A0-A3);$ $p = 4-7$	Move contents of Accumulator to designated port (4-7).	2	1				
ORL BUS, # data	$(BUS) \leftarrow (BUS) \text{ OR data}$	Logical OR Immediate specified data with contents of BUS.	2	2				
ORLD Pp, A	$(Pp) \leftarrow (Pp) \text{ OR } (A0-A3);$ $p = 4-7$	Logical OR contents of Accumulator with designated port (4-7).	2	1				
ORL Pp, # data	$(Pp) \leftarrow (Pp) \text{ OR data};$ $p = 1-2$	Logical OR Immediate specified data with designated port (1-2).	2	2				
OUTL BUS, A	$(BUS) \leftarrow (A)$	Output contents of Accumulator onto BUS.	2	1				
OUTL Pp, A	$(Pp) \leftarrow (A); p = 1-2$	Output contents of Accumulator to designated port (1-2).	2	1				
REGISTERS								
DEC Rr	$(Rr) \leftarrow (Rr) - 1; r = 0-7$	Decrement by 1 contents of designated register.	1	1				
INC Rr	$(Rr) \leftarrow (Rr) + 1; r = 0-7$	Increment by 1 contents of designated register.	1	1				
INC @ Rr	$((Rr)) \leftarrow ((Rr)) + 1;$ $r = 0-1$	Increment Indirect by 1 the contents of data memory location.	1	1				

TABLE I. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
SUBROUTINE								
CALL addr	((SP) ← (PC) ((SP) ← (PSW 4-7) (SP) ← (SP) + 1 (PC 8-10) ← addr 8-10 (PC 0-7) ← addr 0-7 (PC 11) ← DBF	Call designated Subroutine.	2	2				
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	2	1				
RETR	(SP) ← (SP) - 1 (PC) ← ((SP)) (PSW 4-7) ← ((SP))	Return from Subroutine restoring Program Status Word.	2	1	•	•		
FLAGS								
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	1				•
MISCELLANEOUS								
NOP		No operation	1	1				
MICROWIRE INSTRUCTIONS								
XCHM	A ↔ SIO	Reset DONE flip-flop, Clock counter. SK designated as an output. MICROWIRE/PLUS mode selected.						
XCHS	A ↔ SIO	Reset DONE flip-flop, Clock counter. SK designated as an input. MICROWIRE/PLUS mode selected.						

Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
b	Bit Designator (b = 0-7)
BS	Bank Switch
Bus	Bus Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number of Expression (8 bits)
DBF	Memory Bank Flip-Flop
F0, F1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

Symbol	Description
p	Port Designator (p = 1, 2 or 4-7)
PSW	Program Status Word
r	Register Designator (r = 0, 1 or 0-7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
\$	Program Counter's Current Value
(x)	Contents of Register
((xx))	Contents of Memory Location Addressed by the Contents of Register
	Replaced by

Typical Applications (Continued)

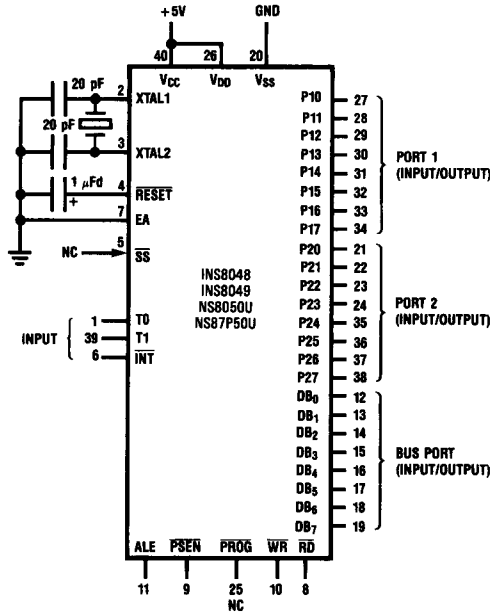
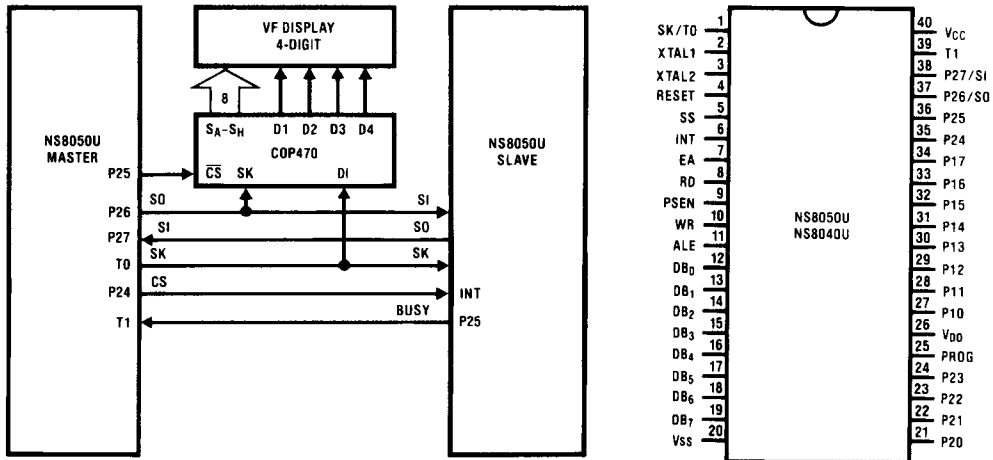


FIGURE 7. Stand-Alone 48-Series

TL/C/5488-22

NS8050U Applications

Block and Connection Diagrams



TL/C/5488-23

TL/C/5488-24

Top View

NS8050U Applications (Continued)

MICROWIRE/PLUS consists of a three wire communications port with a clocked 8-bit shift register. The three lines consist of Serial Output (SO), Serial Input (SI) and Serial Clock (SK) and the Shift register is referred to as the Serial Input/Output Register. One 8050U is designated the master and it supplies the clock for the MICROWIRE/PLUS system and initiates data transfer. All transfers are between the master and one or more slaves. A slave can be any MICROWIRE peripheral or another 8050U with MICROWIRE/PLUS.

MICROWIRE Peripherals**DATA ACQUISITION**

COP43X 8-bit A/D converters

FREQUENCY GENERATORS AND COUNTERS

COP452 Frequency generator and counter

DISPLAY DRIVERS

COP470 Four-digit vacuum fluorescent display driver

COP472 Triplex liquid crystal display controller

MM5445, 5446, Vacuum fluorescent display driver
5447, 5448

MM5450, 5451 LED display driver

MM5452, 5453 Liquid crystal display driver

MM5480, 5481 LED display driver

MM5484, 5485 16- and 11-segment LED display driver

MM58201 Multiplexed LCD driver

MM58248 High-voltage display driver

MEMORIES

COP498 Low-power CMOS RAM and timer

COP499 Low-power CMOS RAM

COP494 256-bit, 5V only EEPROM

COP495 1024-bit, 5V only EEPROM

RADIO TUNING

DS890X AM/FM digital phase-locked loop synthesizer

Peripheral device information may be found in the COPS Microcontrollers Databook.