USB Type-C DFP with Charging Port Controller and Integrated 36V 3.5A Synchronous Buck Converter

General Description

The RTQ2117C combines a USB Type-C Downstream Facing Port (DFP) controller, charging port controller, USB 2.0 high-speed data line (D+/D-) switch and a 3.5A synchronous buck converter.

The RTQ2117C monitors the Type-C Configuration Channel (CC) lines to detect an Upstream Facing Port (UFP) device attach event, then turns on external VBUS MOSFET to apply power to VBUS and communicates the selectable VBUS current sourcing capability.

The RTQ2117C provides the electrical signatures on D+/D- to support charging schemes compatible with the USB 2.0 Battery Charging Specification BC1.2 and Chinese Telecommunication Industry Standard YD/T 1591-2009. Auto-detect mode is also integrated which supports USB 2.0 Battery Charging Specification BC1.2 Dedicated Charging Port (DCP), Divider 3 mode and 1.2V shorted mode to comply with the legacy fast charging mode of mobile devices.

The RTQ2117C integrates a high efficiency, monolithic synchronous buck converter that can deliver up to 3.5A output current from a 3V to 36V wide range input supply and is protected from load-dump transients up to 42V.

The RTQ2117C has constant current control to achieve adjustable USB current limit and implement the current sense signal for adjustable USB power output voltage with load line compensation. The converter includes optional spread-spectrum frequency modulation to overcome EMI issue and complete protection for safe and smooth operation in all applied conditions. Protection features include cycle-by-cycle current limit for protection against shorted outputs, soft-start control to eliminate input current surge during start-up, input under-voltage lockout, output under-voltage protection, output over-voltage protection and over-temperature protection.

The RTQ2117C is fully specified over the temperature range of T_J = −40°C to 125°C and available in WETD-VQFN-40L 6x6.

The RTQ2117C can be used to support Type-C connectors including the Type C-to-C dongle and the Type C-to-B dongle. Type-A connector support is provided by the RTQ2117C.

Features

- **USB Type C DFP Controller**
  - **Compliant to USB-IF Standards**
    - **USB Type-C Specification Release 2.0**
    - **CC Logic, VCONN Source and Discharge**
    - **USB Cable Polarity Detection**
    - **VCONN 1W**
  - **Connector Attach/Detach Detection**
  - **STD/1.5A/3A Capability Advertisement on CC**
  - **Gate Driver for External Blocking FET Control**
  - **Auto Discharge VBUS when CC Pins Detach**
- **CDP/SDP Mode per USB BC1.2**
- **USB Charging Port Controller**
  - **Automatic DCP Modes**
    - **DCP Shorted Mode and YD/T 1591-2009**
    - **2.7V Divider 3 Mode**
    - **1.2V Mode**
- **High Bandwidth 1.2GHz Data Switches**
- **Support Mode Change Among SDP/CDP/DCP Auto**
- **Keep Data Communication During Worst Cold Crank Situation at 3V**
- **36V 3.5 A Synchronous Buck Converter**
  - **3V to 36V Input Voltage Range**
  - **3.5A Continuous Output Current**
  - **CC/CV Mode Control**
  - **Adjustable and Synchronizable Switching Frequency : 300kHz to 2.2MHz**
  - **Selectable PSM/PWM at Light Load**
  - **Adjustable Soft-Start**
  - **Adjustable USB Power Output Voltage between 5V and 5.5V with Load Line Compensation**
  - **Optional Spread-Spectrum Frequency Modulation for EMI Reduction**

- **Protection Function**
  - **VCONN with Current Limit**
  - **CC Pin OVP Protection**
  - **DS+/DS- OVP Protection**
  - **Over-Temperature Protection**
  - **Cycle-by-Cycle Over-Current Limit Protection**
  - **Input Under-Voltage Protection**
  - **VBUS Over-Voltage Protection**
  - **Adjacent Pin-Short Protection**
- **Power Good Indicator**
- **Enable Control**
- **HBM 8kV on CC1/CC2/DS+/DS- Pins**
- **Wettable Flank Package**
- **AEC-Q100 Grade 1 Qualified**

Applications

- Automotive Car Chargers
- USB Power Chargers

Ordering Information

RTQ2117C□□-QA

- Grade
  QA : AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  QVT : WETD-VQFN-40L 6x6 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

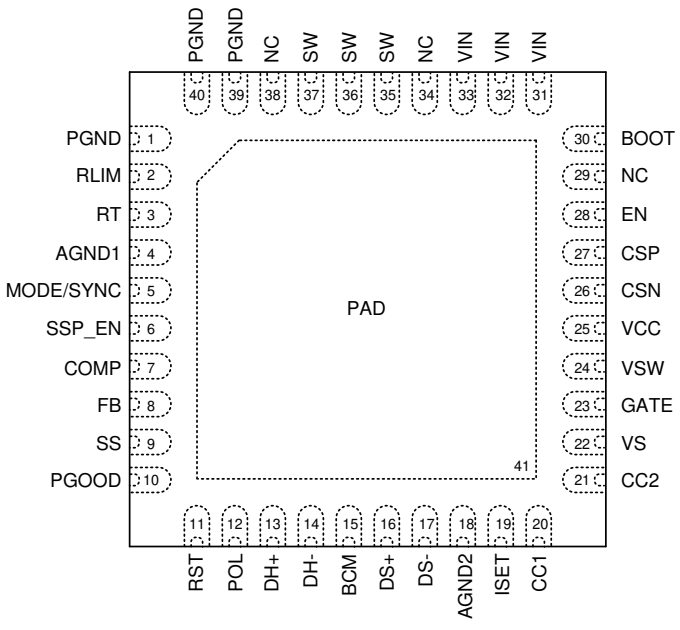
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RTQ2117CGQVT : Product Number
QA : Automotive Product Grade
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



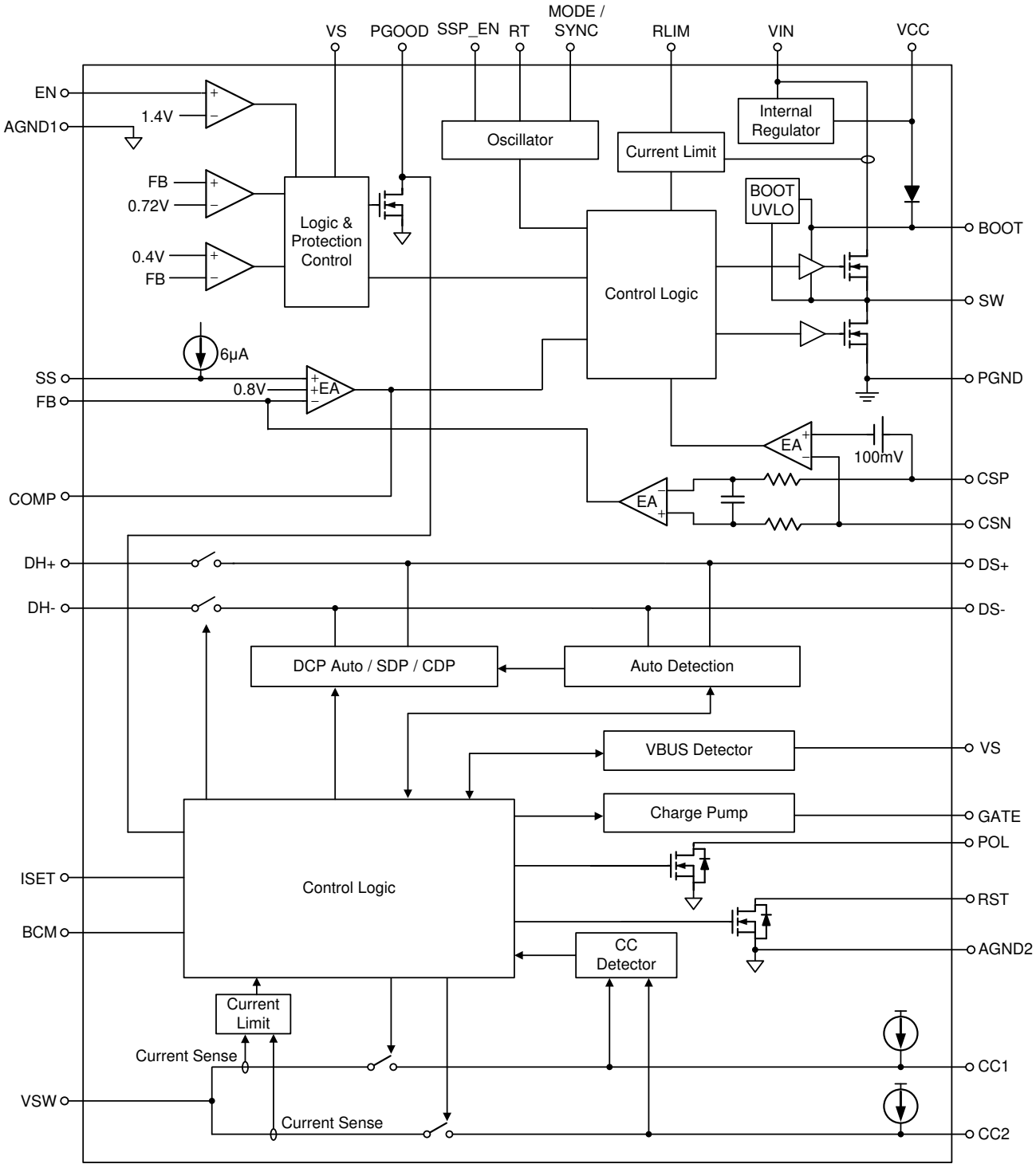
WETD-VQFN-40L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 39, 40	PGND	Power ground.
2	RLIM	Current limit setup pin. Connect a resistor from this pin to ground to set the current limit value. The recommended resistor value is ranging from 33kΩ (for typ. 5.5A) to 91kΩ (for typ. 2.3A).
3	RT	Oscillator frequency setup pin. Connect a resistor from this pin to ground to set the switching frequency. The recommended resistor value is ranging from 174kΩ (for typ. 300kHz) to 21kΩ (for typ. 2.2MHz).
4	AGND1	Analog ground 1.
5	MODE/SYNC	Mode selection and external synchronous signal input. Ground this pin or leave this pin floating enables the power saving mode operation at light load. Apply a DC voltage of 2V or higher or tie to VCC for FPWM mode operation. Tie to a clock source for synchronization to an external frequency.
6	SSP_EN	Spread spectrum enable input. Connect this pin to VCC to enable spread spectrum. Float this pin or connect it to Ground to disable spread spectrum.
7	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
8	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.8V.
9	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and ground to set the soft-start time.
10	PGOOD	Open-drain power-good indication output. The power-good function is activated after soft-start is finished. Connect a resistor from PGOOD to VCC. PGOOD is pulled high when both V_{OUT} > 90% and V_{SS} > 2.1V. PGOOD is pulled low when V_{OUT} < 85%, V_{OUT} > 120% and OTP.
11	RST	Open drain logic output for battery charging mode change output discharge.
12	POL	Polarity open drain logic output. Pull to low when CC1 pin is connected to the CC line in cable.
13	DH+	D+ data line to USB host controller.
14	DH-	D- data line to USB host controller.
15	BCM	Battery charging mode control pin : high → CDP, low → SDP, floating → DCP_Auto.
16	DS+	D+ data line to upstream connector.
17	DS-	D- data line to upstream connector.
18	AGND2	Analog ground 2.
19	ISET	Type-C current capability advertisement control : low → 1.5A, floating → default USB power, high → 3A.
20	CC1	Type-C Configuration Channel (CC) pins. Initially used to determine when an attachment has occurred and what the orientation detected.
21	CC2	Type-C Configuration Channel (CC) pins. Initially used to determine when an attachment has occurred and what the orientation detected.
22	VS	VBUS sensing, connected to VBUS through 200Ω external resistor.

Pin No.	Pin Name	Pin Function
23	GATE	High voltage open-drain gate driver to control external N-Channel blocking MOSFET.
24	VSW	VCONN input supply. Internal power switch connects VSW to CC1 or CC2.
25	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 1μF, X7R ceramic capacitor from VCC to ground for normal operation.
26	CSN	Current sense negative input. Do not float this pin.
27	CSP	Current sense positive input. Do not float this pin.
28	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
29, 34, 38	NC	No internal connection.
30	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.
31, 32, 33	VIN	Power input. The input voltage range is from 3V to 36V after soft-start is finished. Connect input capacitors between this pin and PGND. It is recommended to use a 4.7μF, X7R and a 0.1μF, X7R capacitors.
35, 36, 37	SW	Switch node. SW is the switching node that supplies power to the output and connect the output LC filter from SW to the output load.
41 (Exposed pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram



Operation

The RTQ2117C combines a USB Type-C Downstream Facing Port (DFP) controller, charging port controller, USB 2.0 high-speed data line (D+/D-) switch and a 3.5A synchronous buck converter.

The RTQ2117C integrates 70mΩ high-side and 70mΩ low-side MOSFETs to achieve high efficiency conversion. The current mode control architecture supports fast transient response with simple compensation.

The RTQ2117C supports the common USB charging schemes : USB Battery Charging Specification BC1.2, Chinese Telecommunications Industry Standard YD/T 1591-2009, Divider 3 Mode and 1.2V Short Mode. The device monitors the Type-C Configuration Channel (CC) lines to determine when an USB device is attached. If Type-C connector is used and UFP is attached, the RTQ2117C turns on external VBUS MOSFET to apply power on VBUS. Pass through operation for USB Hi-Speed (480Mbps) and USB Full-Speed (12Mbps) is also supported.

Main Control Loop (CV Regulation)

The RTQ2117C includes a high efficiency step down converter utilizes the peak current mode control. An internal oscillator initiates turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage for constant voltage control (V_{REF_CV}) to generate a CV compensation signal (V_{COMP}) on the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and inductor current ramps-down. While the high-side switch is off, inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Constant Current (CC) Regulation

The RTQ2117C offers average current control loop also. The control loop behavior is basically the same as the peak current mode in constant voltage regulation. The difference is the COMP will be also governed by the output of the internal current error amplifier when FB voltage is below the regulation target. The output current control is obtained by sensing the voltage drop across an external sense resistor (R_{SENSE}) between CSP and CSN, as shown in Figure 1. The internal reference voltage for the current error amplifier is V_{REF_CC} (100mV, typically). If the output current increase and the current sense voltage (V_{CS}, i.e. $V_{CSP} - V_{CSN}$) is equal to V_{REF_CC}, the current error amplifier output will clamp the COMP lower to achieve average current control and vice versa. Once the output current decrease and current sense voltage is less than 100mV, the CV loop dominates the COMP again and the output voltage goes back to the regulation voltage determined by resistor divider from the output to the FB pin and ground accordingly.

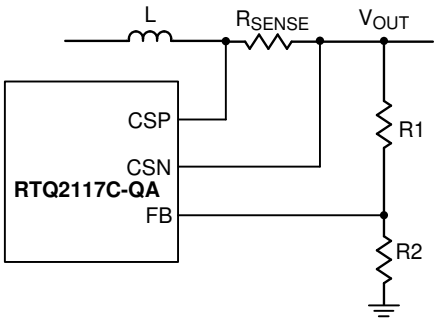


Figure 1. Average Current Setting

MODE Selection and Synchronization

The RTQ2117C provides an MODE/SYNC pin for Forced-PWM Mode (FPWM) and Power Saving Mode (PSM) operation selection at light load. If $V_{MODE/SYNC}$ rises above a logic-high threshold voltage (V_{IH_SYNC}) of the MODE/SYNC input, the device is locked in FPWM. If $V_{MODE/SYNC}$ is held below a logic-low threshold voltage (V_{IL_SYNC}) of the MODE/SYNC input, the device operates in PSM at light load to improve efficiency. The RTQ2117C can also be synchronized with an external clock ranging from

300kHz to 2.2MHz by MODE/SYNC pin.

Forced-PWM Mode

Forced-PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{SK_L} is imposed to prevent damage to the low-side MOSFET switch of the regulator. The converter synchronizes to any valid clock signal on the SYNC input when in FPWM.

When constant frequency operation is more important than light load efficiency, pull the MODE/SYNC input high or provide a valid synchronization input. Once activated, this feature ensures that the switching frequency stays away from the AM frequency band, while operating between the minimum and maximum duty cycle limits.

Power Saving Mode

With the MODE/SYNC pin floating or pull low, that is, with a logic low on the MODE/SYNC input, the RTQ2117C operates in power saving mode (PSM) at light load to improve light load efficiency. In PSM, IC starts to switch when V_{FB} is lower than PSM threshold (V_{REF_CV} x 1.005, typically) and stops switching when V_{FB} is high enough. IC detects the peak inductor current (I_{L_PEAK}) and keeps high-side MOSFET switch on until the I_L reaches its minimum peak current level (1A at V_{IN} = 12V, typically) to ensure that IC can provide sufficiency output current with each switching pulse. Zero-current detection is also activated to prevent that I_L becomes negative and to ensure no external discharging current from the output capacitor. During non-switching period, most of the internal circuit is shut down, and the supply current drops to quiescent current to reduce the quiescent power consumption. With lower output loading, the non-switching period is longer, so the effective switching frequency becomes lower to reduce the switching loss and switch driving loss.

Maximum Duty Cycle Operation

The RTQ2117C is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time becomes smaller than minimum off time, the RTQ2117C starts to enable skip off time function and keeps high-side MOSFET switch on continuously. The RTQ2117C implements skip off time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high-side MOSFET switch at any condition. The BOOT UVLO usually actives at extremely high conversion ratio or the higher VOUT application operates at very light load. With such conditions, the low-side MOSFET switch may not have sufficient turn-on time to charge the BOOT capacitor. The device monitors BOOT pin capacitor voltage and force to turn on the low-side MOSFET switch when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_L}$ (typically, 2.3V). Meanwhile, the minimum off time is extended to 150ns (typically) hence prolong the BOOT capacitor charging time. The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.4V).

Internal Regulator

The device integrates a 5V linear regulator (V_{CC}) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{IN} is below 5V. The V_{CC} can be used as the PGOOD pull-up supply but it is “NOT” allowed to power other device or circuitry. The VCC pin must be bypassed to ground with a minimum value of effective VCC capacitance is 0.7μF. In many applications, a 1μF, X7R is recommended and it needs to be placed as close as possible to the VCC

pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Enable Control

The RTQ2117C provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{ENL}) of the enable input (EN), switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLOH}). If V_{EN} is held below 0.4V, the converter will enter into shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (5μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}) while the VIN voltage is higher than V_{UVLO}, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. The current source of EN typically sinks 1.2μA.

Soft-Start

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RTQ2117C provides an SS pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor C_{SS} connected from the SS pin to ground. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically, 6μA) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. If the output is for some reasons pre-biased to a certain voltage during start-up, the device will not start switching until the voltage difference between SS pin and FB pin is larger than 400mV (typically). And only when this ramp voltage is higher than the feedback voltage V_{FB}, the switching will be resumed. The output voltage can then ramp up smoothly to its targeted regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected. After the SS pin voltage rises above 2V (typically), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high. The typical start-up waveform shown in Figure 2 indicate the sequence and timing between the output voltage and related voltage.

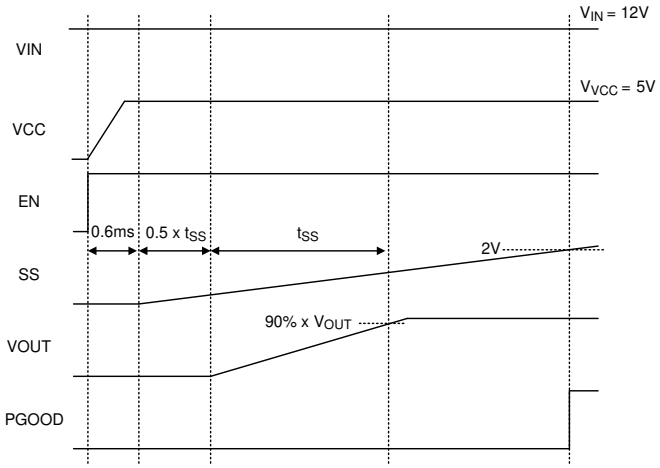


Figure 2. Start-Up Sequence

Power Good Indication

The RTQ2117C features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to V_{CC} or an external voltage below 5.5V. The power-good function is activated after soft start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH1}) (typically 90% of the reference voltage), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} exceeds V_{TH_PGHL1} (typically 120% of the reference voltage), the PGOOD pin will be pulled low, moreover, IC turns off high-side MOSFET switch and turns on low-side MOSFET switch until the inductor current reaches I_{SK_L} if MODE pin is set high. If the V_{FB} is still higher than V_{TH_PGHL1}, the high-side MOSFET switch remains prohibited and the low-side MOSFET switch will turn-on again at next cycle. If MODE pin is set low, IC turns off low-side MOSFET switch once the inductor current reaches zero current unless $V_{BOOT-SW}$ is too low. For V_{FB} higher than V_{TH_PGHL1}, V_{PGOOD} can be pulled high again if V_{FB}

drops back by a power-good high threshold (V_{TH_PGLH2}) (typically 117% of the reference voltage). When V_{FB} fall short of power-good low threshold (V_{TH_PGHL2}) (typically 85% of the reference voltage), the PGOOD pin will be pulled low. Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pulldown device (10Ω, typically) will pull the PGOOD pin low.

The power good indication profile is shown in Figure 3.

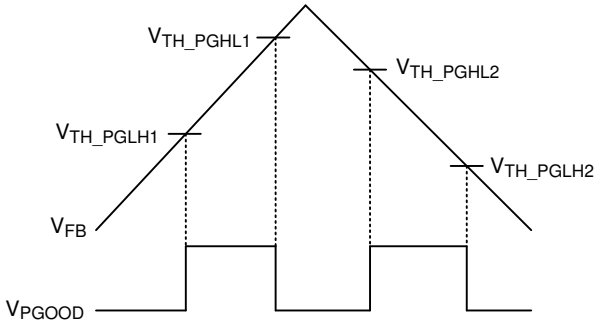


Figure 3. The Logic of PGOOD

Spread-Spectrum Operation

Due to the periodicity of the switching signals, the energy concentrates in one particular frequency and also in its harmonics. These levels or energy is radiated and therefore this is where a potential EMI issue arises. The RTQ2117C have optional spread-spectrum function and SSP_EN pin can be programmed to turn on/off the spread spectrum, further simplifying compliance with the CISPR and automotive EMI requirements. The spread spectrum can be active when soft-start is finished and zero-current is not detected. If V_{SSP_EN} rises above a logic-high threshold voltage (2V, typically) of the SSP_EN input, the device enable spread spectrum operation. The spread-spectrum is implemented by a pseudo random sequence and uses +6% spread of the switching frequency. For example, when the RTQ2117C is programmed to 2.1MHz, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RTQ2117C still guarantees that the 2.1MHz switching frequency setting does not drop into the AM band limit of 1.8MHz. However, the spread spectrum can't be active when the device is synchronized with an external clock by MODE/SYNC pin.

Input Under-Voltage Lockout

In addition to the EN pin, the RTQ2117C also provides enable control through the VIN pin. If V_{EN} rises above V_{ENH} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage V_{IN} goes below the UVLO falling threshold voltage (V_{UVLOL}), this switching will be inhibited; if V_{IN} rises above the UVLO rising threshold (V_{UVLOH}), the device will resume switching. Note that V_{IN} = 3V is only design for cold crank requirement, normal input voltage should be larger than UVLO threshold to turn on.

High-Side Switch Peak Current Limit Protection

The RTQ2117C includes a cycle-by-cycle high-side switch peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The high-side MOSFET switch peak current limit of the RTQ2117C is adjustable by placing a resistor on the RLIM pin. The recommended resistor value is ranging from 33kΩ (for typ. 5.5A) to 91kΩ (for typ. 2.2A) and it is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less resistors. The inductor current through the high-side MOSFET switch will be measured after a certain amount of delay when the high-side MOSFET switch being turned on. If an over-current condition occurs, the converter will immediately turn off the high-side MOSFET switch and turn on the low-side MOSFET switch to prevent the inductor current exceeding the high-side MOSFET switch peak current limit (I_{LIM_H}).

Low-Side Switch Current-Limit Protection

The RTQ2117C not only implements the high-side switch peak current limit but also provides the sourcing current limit and sinking current limit for low-side MOSFET switch. With these current protections, the IC can easily control inductor current at both side switch and avoid current runaway for short-circuit condition.

For the low-side MOSFET switch sourcing current limit, there is a specific comparator in internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit which is high-side MOSFET switch current limit (I_{LIM_H}) multiplied by 0.95, the new switching cycle is not initiated until inductor current drops below the low-side MOSFET switch sourcing current limit.

For the low-side MOSFET switch sinking current limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch.

Output Under-Voltage Protection

The RTQ2117C includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off the high-side MOSFET and then turn off the low-side MOSFET when the inductor current drop to zero. If the output under-voltage condition continues for a period of time, the RTQ2117C enters output under-voltage protection with hiccup mode and discharges the C_{SS} by an internal discharging current source I_{SS_DIS} (typically, 80nA). During hiccup mode, the device remains shut down. After the V_{SS} is discharged to less than 150mV (typically), the RTQ2117C attempts to re-start up again, the internal charging current source I_{SS} gradually increases the voltage on C_{SS}. The high-side MOSFET switch will start switching when voltage difference between SS pin and FB pin is larger than 400mV (i.e. $V_{SS} - V_{FB} >$ 400mV, typically). If the output under-voltage condition is not removed, the high-side MOSFET switch stop switching when the voltage difference between SS pin and FB pin is 700mV (i.e. $V_{SS} - V_{FB}$ = 700mV, typically) and then the I_{SS_DIS} discharging current source begins to discharge C_{SS}.

Upon completion of the soft-start sequence, if the output under-voltage condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the output under-voltage condition is cleared.

Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. A short circuit protection and recovery profile is shown in Figure 4.

Since the C_{SS} will be discharged to 150mV when the RTQ2117C enters output under-voltage protection, the first charging time (t_{SS_DIS1}) can be calculated as follow

$$t_{SS\_DIS1} = C_{SS} \times \frac{V_{SS} - 0.15}{I_{SS\_DIS}}$$

The equation below assumes that the V_{FB} will be 0 at short-circuited condition and it can be used to calculate the C_{SS} charging time (t_{SS_DIS2}) and charging time (t_{SS_CH}) during hiccup mode.

$$t_{SS\_DIS2} = C_{SS} \times \frac{0.55}{I_{SS\_DIS}}$$

$$t_{SS\_CH} = C_{SS} \times \frac{0.55}{I_{SS\_CH}}$$

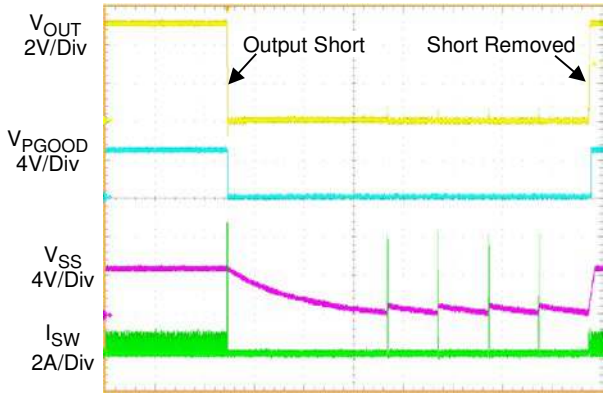


Figure 4. Short Circuit Protection and Recovery

Over-Temperature Protection

The RTQ2117C includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Pin-Short Protection

The RTQ2117C provides pin-short protection for neighbor pins. The internal protection fuse will be burned out to prevent IC smoke, fire and spark when BOOT pin is shorted to VIN pin

VBUS Reset

To allow a charging port to renegotiate current with a portable device, the RTQ2117C uses the automatic VBUS reset function. When battery charging mode (BCM) is changed, the discharge circuit at the RST pin becomes active. This will pull SS pin to low by RST. Then the RTQ2117C turns off buck converter to disconnect power source to VBUS, then discharges VBUS by internal discharge circuit. And then turns on buck converter to reassert the VBUS voltage. If timeout event occurs, the system will do VBUS reset again until no timeout event occurred. The VBUS reset sequence for battery charging mode change as shown in Figure 5 and the reset time table as shown in Table 1.

The following conditions will trigger VBUS reset event, when re-power on.

- D+/D- OVP event
- Release OVP/UVP/OTP event
- FB pin drops below PGOOD level (typ. = 85%)

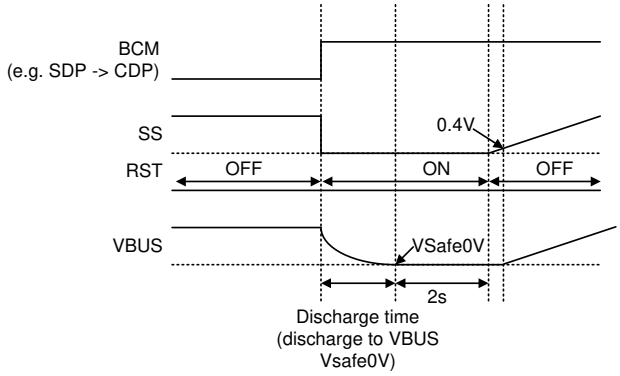


Figure 5. VBUS Reset Time Sequence

Table 1. VBUS Reset Time

BCM	Reset Time
DCP to CDP	400ms
CDP to DCP	2s
SDP to CDP	2s
CDP to SDP	2s
SDP to DCP	2s
DCP to SDP	400ms

Data Switch

The RTQ2117C implements a high-bandwidth data switch can support USB 2.0 Hi-Speed (480Mbps) communication modes. When the RTQ2117C is set to CDP or SDP mode, the data switch will be kept on for communication between Device and HOST unit. When VCC achieves POR level, the data switch is turned on after an internal delay time, 800μs (typically). When EN is disable, the VCC voltage is discharged to POR level and data switch is turned off at this time. The discharge time depends on external capacitor of VCC pin. The sequence is shown as Figure 6 and Figure 7.

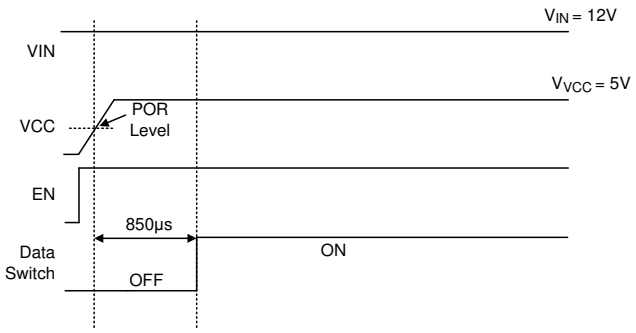


Figure 6. Data Switch On Sequence

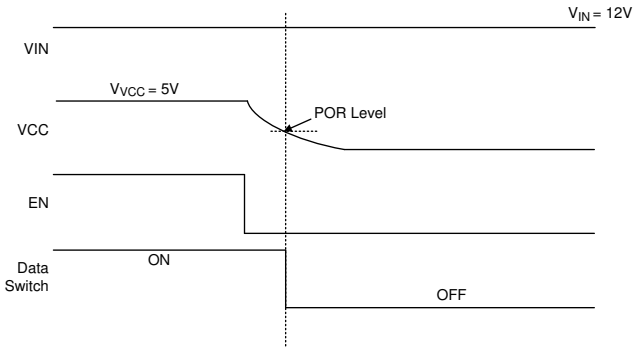


Figure 7. Data Switch Off Sequence

DS+ DS- Over-Voltage Protection

The RTQ2117C includes a data over-voltage protection function against the condition that DS+ or DS- suffers high voltage to let charging detection abnormal or damage the HOST device through data switch. When the voltage at DS+ or DS- is over protection trip threshold, 3.85V (typically), the PGOOD will be pull low after 100μs and data switch will also be turned off after a fast response time, 5μs (typically). It is keep until the voltage is lower than threshold. Then, the PGOOD is released after 100μs and data switch recovery after a fast response time, 5μs (typically). When detect the rising edge of PGOOD, the VOUT/VBUS will be reset for a 400ms. This behavior will let charged devices re-attach and start the charging detection operation again. The sequence is shown as Figure 8.

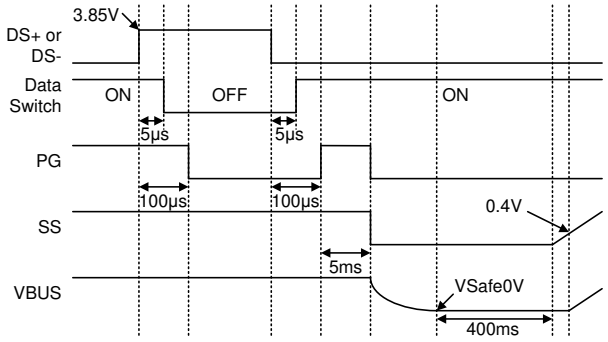


Figure 8. Data Over-Voltage Protection Sequence

USB Type-C Connection Detection

The RTQ2117C implements the Type-C control function as an only DFP role. The VBUS will be released by the blocking switch controlled from the gate pin of USB controller. When the device is connected, the UFP provides the Rd on the both its CC pins and DFP will monitor it from CC1 or CC2 to start the attached operation. Take the CC2 as an example, Figure 9 shows the CC2 attached sequence. The VBUS will be released in 150ms as DFP is attached. After DFP is detached, CC2 is changed to open in 10ms and starts to wait the VBUS down to Vsafe0V. Then, CC2 will be back to high. The sequence is shown as in Figure 10. If the waiting time is over 675ms, the CC will be forced to high.

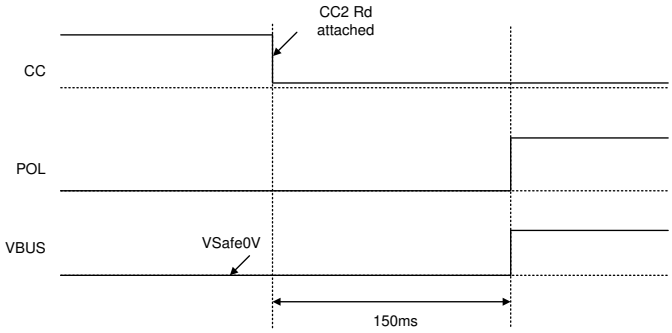


Figure 9. Type-C Attached Sequence

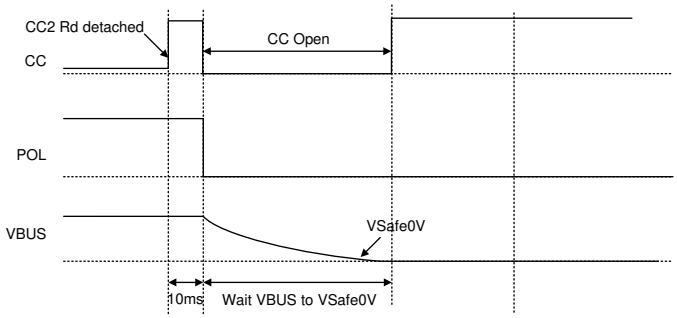


Figure 10. Type-C Detached Sequence

CC Over-Voltage Protection

The RTQ2117C includes a CC over-voltage protection function. When the voltage at CC1 or CC2 is over protection trip threshold, 5.8V (typically), the PGOOD will be pull low and gate will also be turned off after a fast response time. Then, the VBUS starts to discharge in 35ms. When the over voltage event at CC pin is removed, the PGOOD will go back to high and CC starts to wait another attached operation. The sequence is shown as Figure 11.

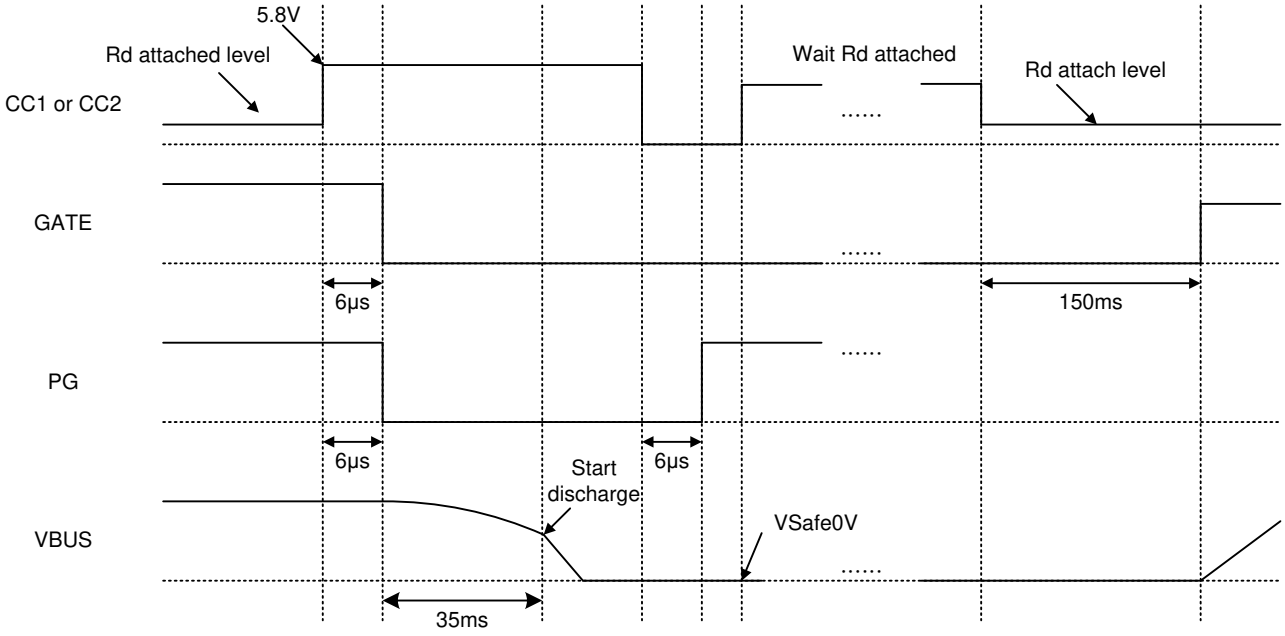


Figure 11. CC Over-Voltage Protection Sequence

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 42V
- Switch Voltage, SW ---------- –0.3V to 42V
  <50ns ---------- –5V to 46.3V
- BOOT Voltage, V_{BOOT} ---------- –0.3V to 48V
- BOOT to SW, $V_{BOOT} – V_{SW}$ ---------- –0.3V to 6V
- EN, CSP, CSN, SS Voltage ---------- –0.3V to 42V
- DS+, DS- Voltage ---------- –0.3V to 20V
- CC1, CC2, VS, GATE Voltage ---------- –0.3V to 24V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WETD-VQFN-40L 6x6 ---------- 3.7W
- Package Thermal Resistance (Note 2)
  WETD-VQFN-40L 6x6, θ_{JA} ---------- 27°C/W
  WETD-VQFN-40L 6x6, θ_{JC} ---------- 6.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model)
  DS+, DS-, CC1, CC2, VS Pins to AGND2 ---------- 8kV
  Other Pins ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 3V to 36V
- Output Voltage ---------- 0.8V to 5.5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(V_{IN} = 12V, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}	Soft-start is finished	3	--	36	V
V_{IN} Under-Voltage Lockout Threshold	V_{UVLOH}	V_{IN} rising	3.6	3.8	4	V
	V_{UVLOL}	V_{IN} falling	2.7	2.85	3	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.82V, not switching, BCM = 0, V_{CC} = 5V, Type-C unattached	--	150	200	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage for Constant Voltage regulation	V_{REF_CV}	3V < V_{IN} < 36V, PWM, T_A = T_J = 25°C	0.792	0.8	0.808	V
		3V < V_{IN} < 36V, PWM, T_A = T_J = −40°C to 125°C	0.788	0.8	0.812	
Enable Voltage						
Enable Threshold Voltage	V_{IH}	V_{EN} rising	1.15	1.25	1.35	V
	V_{IL}	V_{EN} falling	0.9	1.05	1.15	
Current Limit						
High-Side Switch Current Limit 1	I_{LIM_H1}	R_{LIM} = 91kΩ	1.87	2.2	2.53	A
High-Side Switch Current Limit 2	I_{LIM_H2}	R_{LIM} = 47kΩ	3.52	4	4.48	A
High-Side Switch Current Limit 3	I_{LIM_H3}	R_{LIM} = 33kΩ	4.84	5.5	6.16	A
Low-Side Switch Sinking Current Limit	I_{SK_L}	From drain to source	--	2	--	A
Switching						
Switching Frequency 1	f_{SW1}	R_{RT} = 174kΩ	264	300	336	kHz
Switching Frequency 2	f_{SW2}	R_{RT} = 51kΩ	0.88	0.98	1.08	MHz
Switching Frequency 3	f_{SW3}	R_{RT} = 21kΩ	1.98	2.2	2.42	MHz
SYNC Frequency Range			0.3	--	2.2	MHz
SYNC Switching High Threshold	V_{IH_SYNC}		--	--	2	V
SYNC Switching Low Threshold	V_{IL_SYNC}		0.4	--	--	V
SYNC Switching Clock Duty Cycle	D_{SYNC}		20	--	80	%
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Minimum Off-Time	t_{OFF_MIN}		--	65	80	ns
Internal MOSFET						
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$		--	70	130	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$		--	70	130	mΩ
High-Side Switch Leakage Current	I_{LEAK_H}	V_{EN} = 0V, V_{SW} = 0V	--	--	1	μA
Soft-Start						
Soft-Start Internal Charging Current	I_{SS}		4.5	6	7.2	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good						
Power Good High Threshold 1	V_{TH_PGLH1}	V_{FB} rising, PGOOD from low to high	85	90	95	%
Power Good Low Threshold 1	V_{TH_PGHL1}	V_{FB} rising, PGOOD from high to low	115	120	125	
Power Good Low Threshold 1	V_{TH_PGHL2}	V_{FB} falling, PGOOD from high to low	80	85	90	%
Power Good High Threshold 1	V_{TH_PGLH2}	V_{FB} falling, PGOOD from low to high	112	117	122	
Power Good Leakage Current	I_{LK_PGOOD}	PGOOD signal good, $V_{FB} = V_{REF}$, $V_{PGOOD} = 5.5V$	--	--	0.5	μA
Power Good Sink Current Capability	I_{SK_PGOOD}	PGOOD signal fault, I_{PGOOD} sinks 0.2mA	--	--	0.3	V
Error Amplifier						
Error Amplifier Trans-conductance	gm	$-10\mu A < I_{COMP} < 10\mu A$	665	950	1280	μA/V
COMP to Current Sense Trans-Conductance	gm_{CS}		4.5	5.6	6.7	A/V
Load Line Compensation						
Load Line Compensation Current	I_{LC}	$V_{CSP} - V_{CSN} = 100mV$, $5V < V_{OUT} < 5.5V$	--	2	--	μA
		$V_{CSP} - V_{CSN} = 50mV$, $5V < V_{OUT} < 5.5V$	--	0.95	--	
Constant Current Regulation						
Reference Voltage for Constant Current Regulation	V_{REF_CC}	$V_{CSP} - V_{CSN}$, $3.3V < V_{CSP}$ and $V_{CSN} < 6V$	--	100	--	mV
Spread Spectrum						
Spread-Spectrum Range	SS	Spread-spectrum option only	--	+6	--	%
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		--	175	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	°C
Switching Pin Discharge Resistance		Force 1V	--	100	160	Ω
Output Under-Voltage Protection						
UVP Trip Threshold	V_{UVP}	UVP detect	0.35	0.4	0.45	V
BCM/ISET						
Input Pin L → H Threshold Voltage	V_{TH}		1.05	1.15	1.25	V
Input Pin H → L Threshold Voltage	V_{TL}		0.3	0.4	0.5	V
Floating Voltage			0.7	0.8	0.9	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GATE						
Output Source Current			--	12	--	μA
VGATE			9	9.5	10	V
RGATE			0.5	1	2	kΩ
Type-C						
DFP 80μA CC Current	$I_{CC\_DFP80\mu}$	CC = 0.5V, V_{CC} = 5V	64	80	96	μA
DFP 180μA CC Current	$I_{CC\_DFP180\mu}$	CC = 1V, V_{CC} = 5V	166	180	194	μA
DFP 330μA CC Current	$I_{CC\_DFP330\mu}$	CC = 1.5V, V_{CC} = 5V	304	330	356	μA
VBUS Discharge Resistor	R_{VBUS}		45	55	65	Ω
VCONN Switch On-Resistance	$R_{DS(ON)\_VCONN}$		--	1	1.5	Ω
VCONN Current Limit	I_{LIM_VCONN}		300	350	400	mA
CC Protection Threshold	V_{OV_CC}	V_{CC} = 5V	5.5	5.7	5.9	V
VBUS Protection Threshold	V_{OV_VBUS}	V_{CC} = 5V	5.5	5.7	5.9	V
High-Bandwidth Analog Switch						
DH+/DH- ↔ DS+/DS- Switch On Resistance	$R_{DS(ON)\_SW}$	DH+/DH- = 0V, 0.4V I_{ON} = 8mA (Note 5)	--	5	--	Ω
Switch Resistance Mismatch between DH+/DH- Channel	$R_{DS(ON)\_SW\_MIS}$	DH+/DH- = 0V, 0.4V I_{ON} = 8mA (Note 5)	--	0.03	--	Ω
DH+/DH-/DS+/DS- Switch Off-State Capacitance	C_{OFF}	f_{SW} = 240MHz (Note 5)	--	2	--	pF
DH+/DH-/DS+/DS- Switch On-State Capacitance	C_{ON}	f_{SW} = 240MHz (Note 5)	--	4.2	--	pF
Off-State Isolation	O_{IRR}	f_{SW} = 240MHz, DH+/DH- = 400mV_{PP}, R_L = 50Ω, C_L = 0pF on DS+/DS- (Note 5)	--	–30	--	dB
Differential –3dB Bandwidth	f_{BW}	DH+/DH- = 400mV_{PP}, R_L = 50Ω, C_L = 0pF on DS+/DS- (Note 5)	--	1.2	--	GHz
Propagation Delay	t_{PD}	(Note 5)	--	0.25	--	ns
Skew between Opposite Transitions of the Same Port (t_{PHL}- t_{PLH})	t_{SK}	Rising/falling time of DH+/DH- = 500ps (10-90%) at 240MHz, C_L= 5pF, R_L = 50Ω (Note 5)	--	0.1	--	ns
DCP Shorted Mode						
DS+/DS- Shorting Resistance	R_{DCP_SHORT}	DS+ = 0.8V, I_{DS-} = 1mA	--	--	200	Ω
Resistance Between DS+/DS- and Ground	R_{DCHG_SHORT}	DS+/DS = 0.8V	300	--	--	kΩ
1.2V Shorted Mode						
DS+ Output Voltage	$V_{DP\_1.2V}$		1.12	1.2	1.28	V
DS+ Output Impedance	$R_{DP\_1.2V}$		80	102	130	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Divider 3 Mode						
DS+ Output Voltage	$V_{DP\_2.7V}$		2.57	2.7	2.84	V
DS- Output Voltage	$V_{DM\_2.7V}$		2.57	2.7	2.84	V
DS+ Output Impedance	$R_{DP\_2.7V}$		24	30	36	kΩ
DS- Output Impedance	$R_{DM\_2.7V}$		24	30	36	kΩ
Charging Downstream Port						
DS- CDP Output Voltage	V_{DM_SRC}		0.5	--	0.7	V
DS+ Rising Lower Window Threshold for V_{DM_SRC} Activation	V_{DAT_REF}		0.25	--	0.4	V
DS+ Rising Upper Window Threshold for V_{DM_SRC} De-Activation	V_{LGC_SRC}		0.8	--	2	V
DS+ Sink Current	I_{DP_SINK}		50	--	150	μA
D+, D- Analog USB Switches						
Analog Signal Range			0	--	3.6	V
Protection Trip Threshold	V_{OV_D}		3.7	3.85	4.15	V
Protection Response Time	t_{FP_D}	V_{IN} = 4V, $V_{HVD\pm}$ = 3.3V to 4.3V step, R_L = 15kΩ on $D_\pm$, delay to $V_{D\pm}$ < 3V (Note 5)	--	5	--	μs

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer is filled with copper. θ_{JC} is measured at the exposed pad of the package.

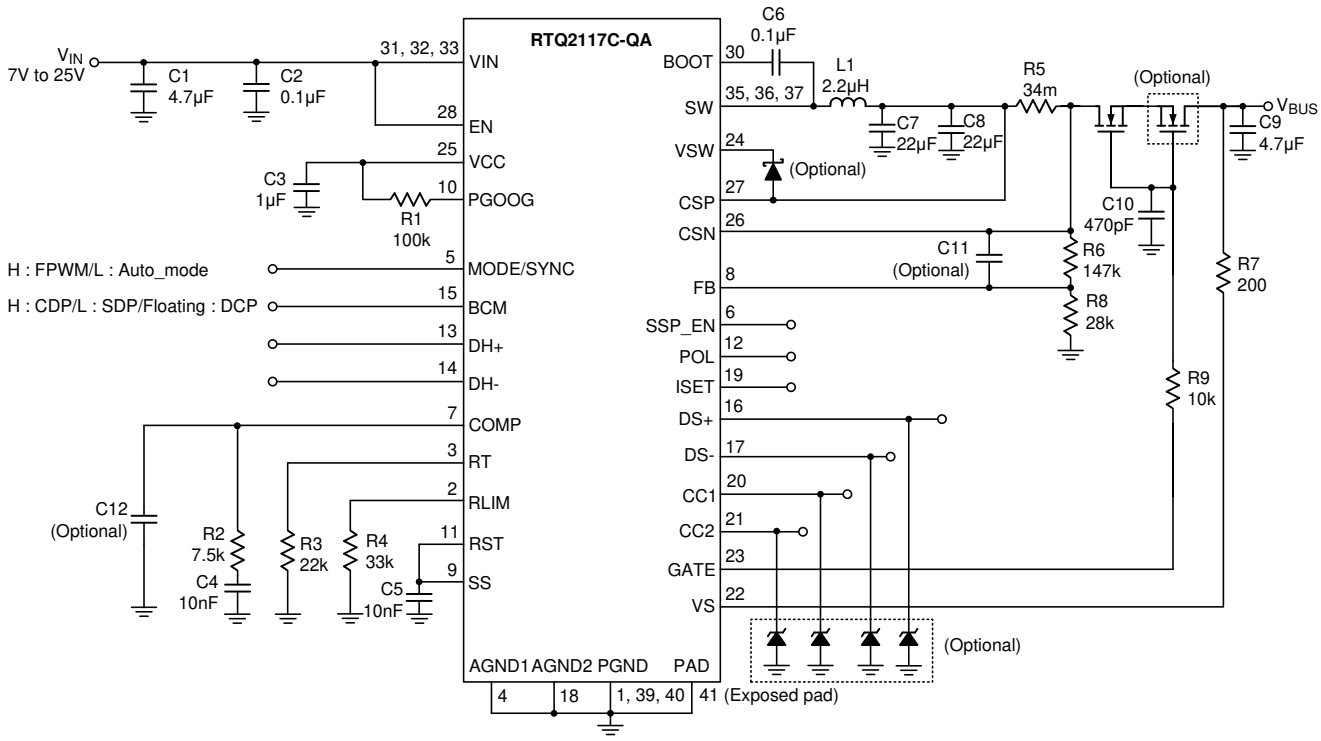
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

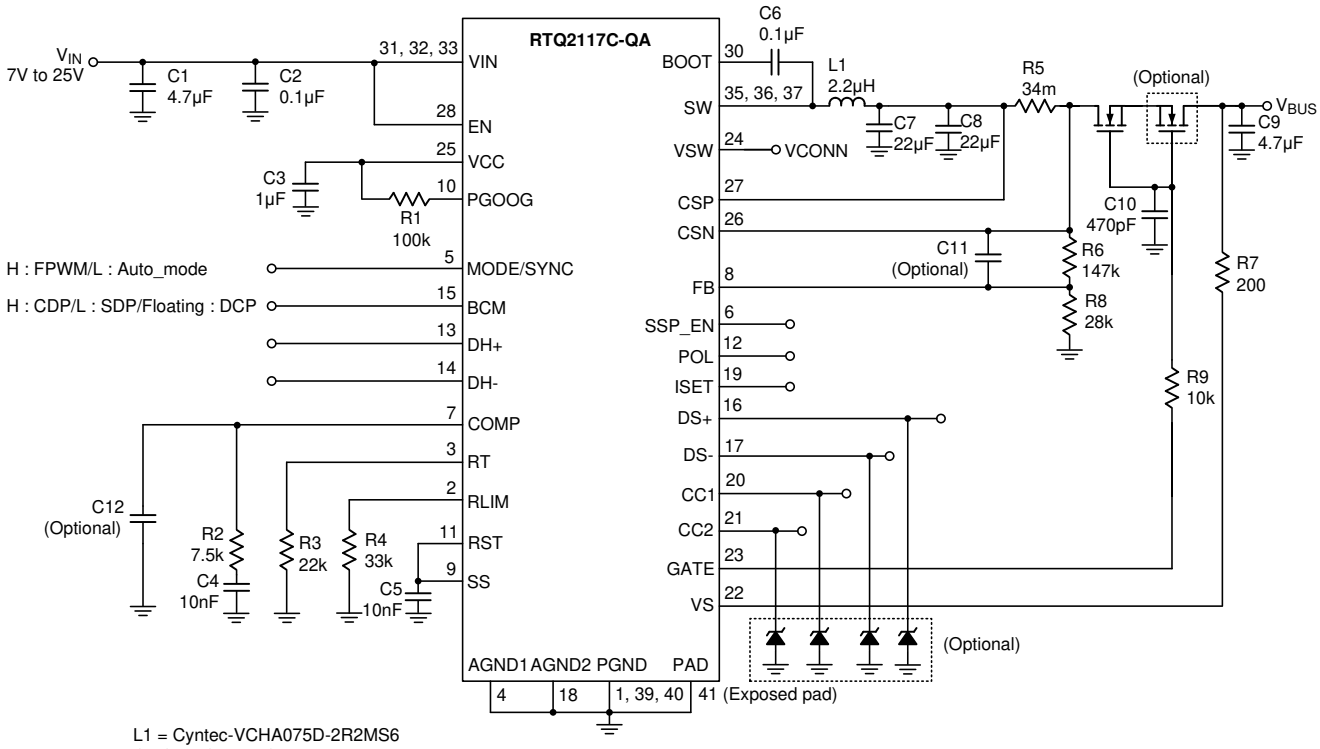
Typical Application Circuit

Step-Down Circuit with:
Cable Drop Compensation : 240mV@2.4A
Average Current Limit : 2.9A
2100kHz, 5V, 3A Step-Down Converter

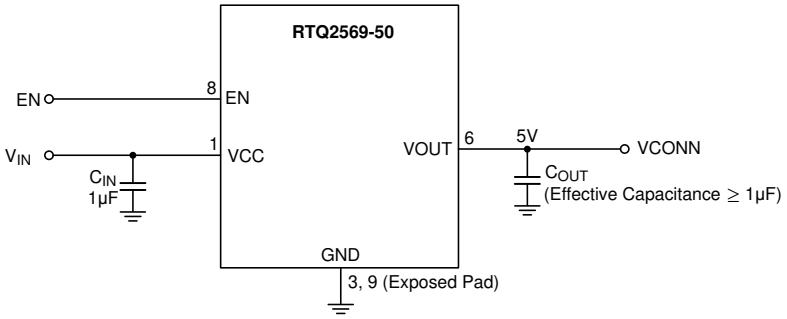


L1 = Cyntec-VCHA075D-2R2MS6
C7/C8 = GRM31CR71A226KE15L
C1 = GRM31CR71H475KA12L

Step-Down Circuit with :
Cable Drop Compensation : 240mV@2.4A
Average Current Limit : 2.9A
Suitable for VBUS connected to high voltage
2100kHz, 5V, 3A Step-Down Converter

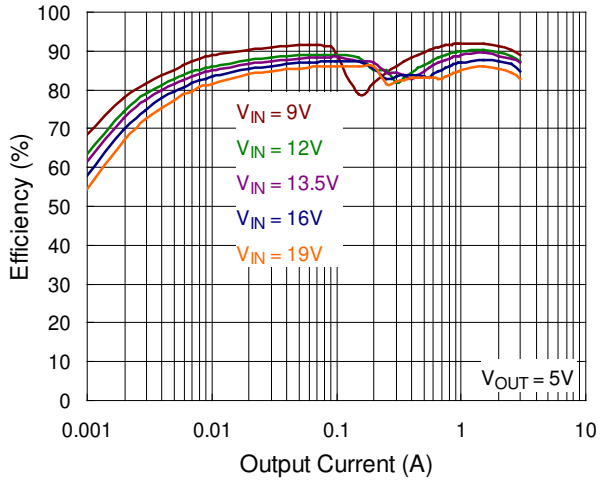


L1 = Cyntec-VCHA075D-2R2MS6
C7/C8 = GRM31CR71A226KE15L
C1 = GRM31CR71H475KA12L

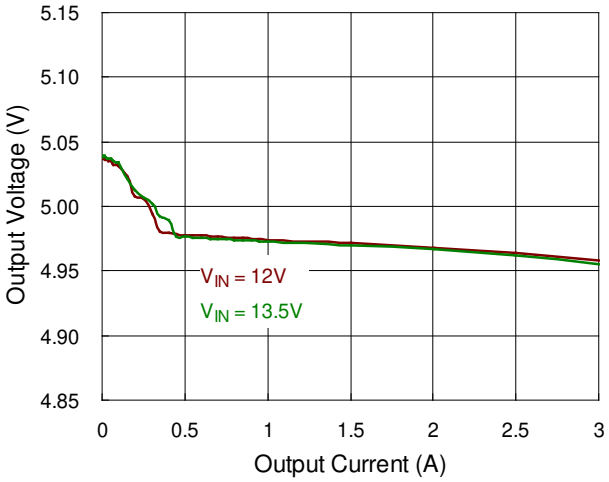


Typical Operating Characteristics

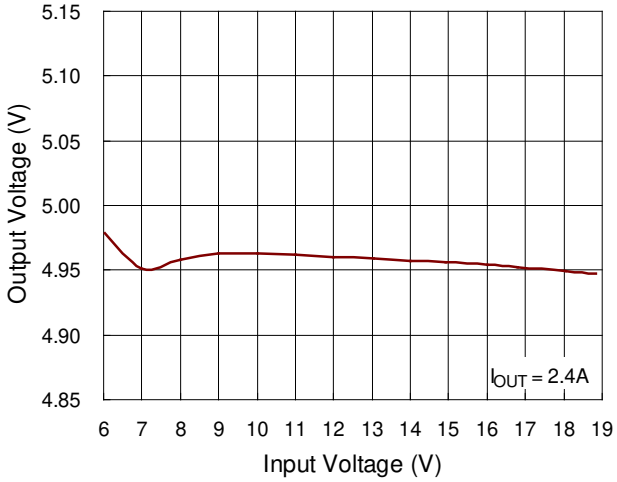
Efficiency vs. Output Current



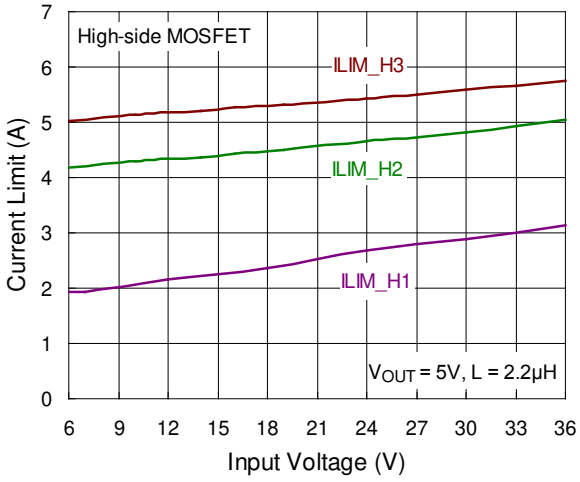
Output Voltage vs. Output Current



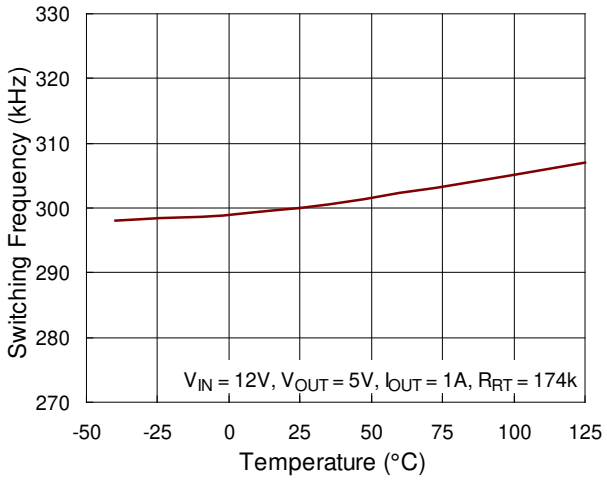
Output Voltage vs. Input Voltage



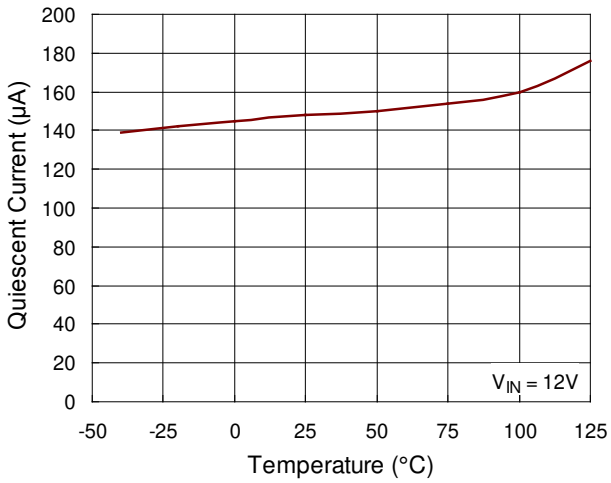
Current Limit vs. Input Voltage



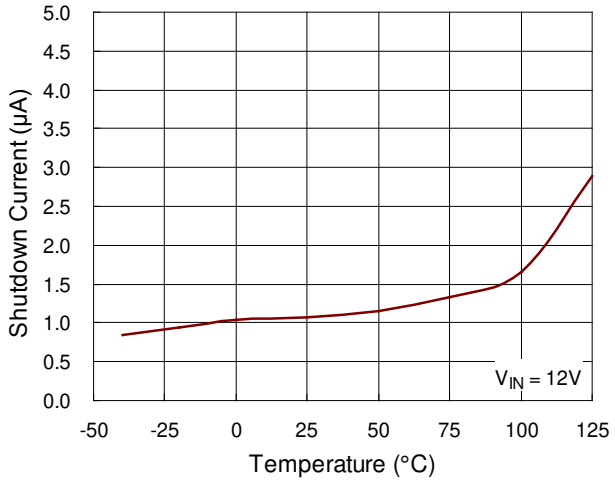
Switching Frequency vs. Temperature



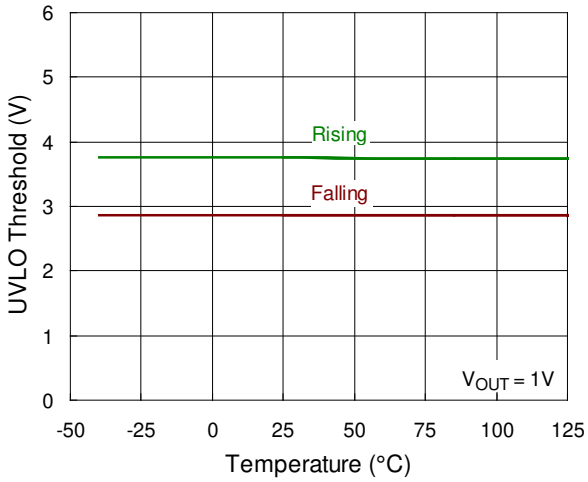
Quiescent Current vs. Temperature



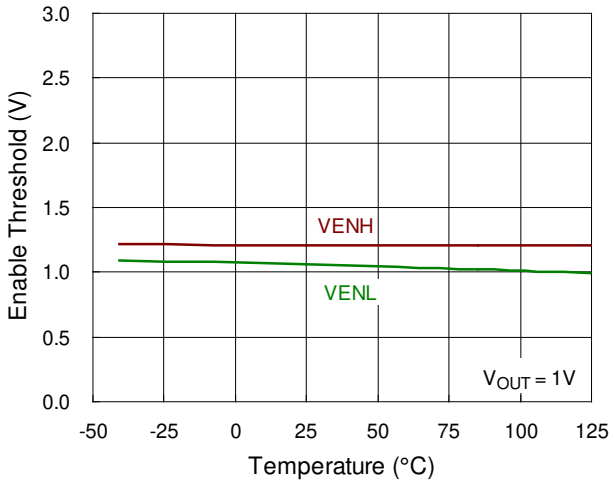
Shutdown Current vs. Temperature



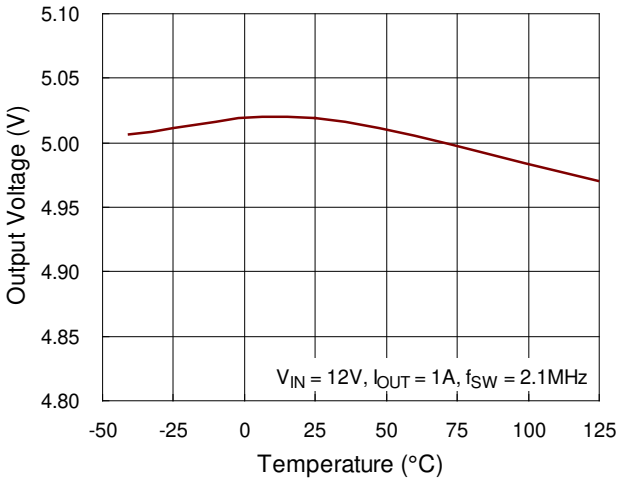
UVLO Threshold vs. Temperature



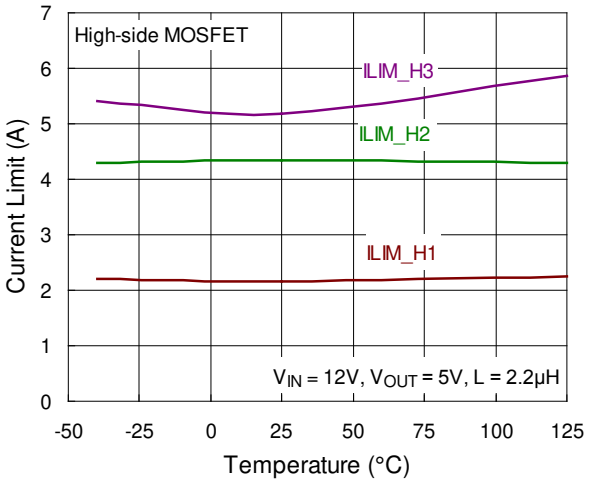
Enable Threshold vs. Temperature



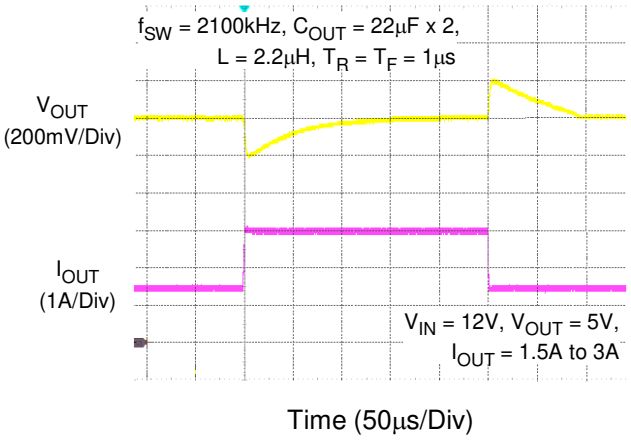
Output Voltage vs. Temperature



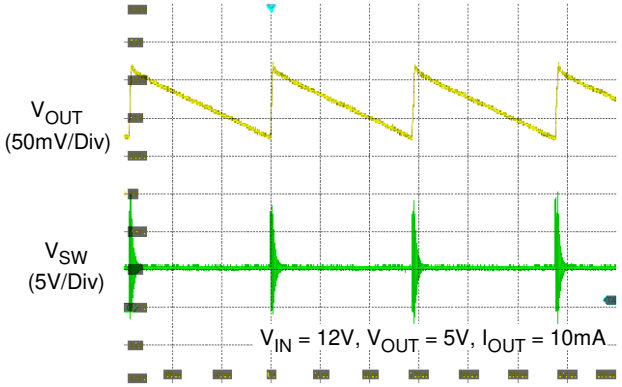
Current Limit vs. Temperature



Load Transient Response

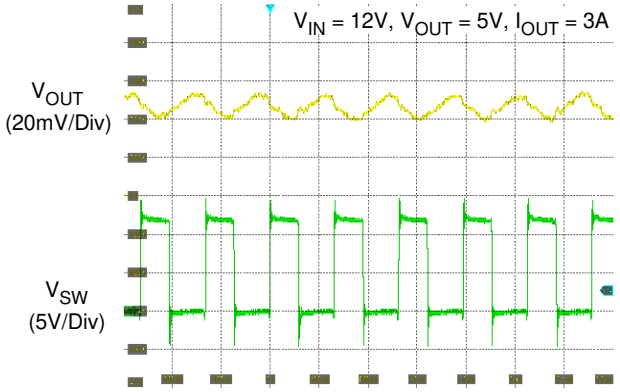


Output Ripple Voltage



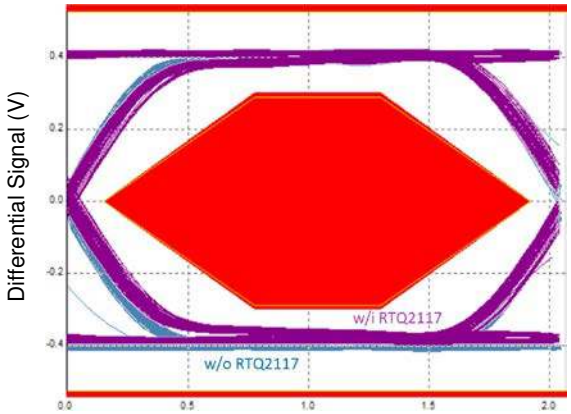
Time (40μs/Div)

Output Ripple Voltage



Time (400ns/Div)

Eye Diagram



Time (ns)

Application Information

A general RTQ2117C application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the selection of operating mode by setting the MODE/SYNC pin voltage and the operating frequency by using external resistor RT. Next, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}. Next, feedback resistors and compensation circuit are selected to set the desired output voltage, crossover frequency, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as the EN, external soft-start, PGOOD, inductor peak current limit, synchronization, spread spectrum, average current limit, and adjustable output voltage with cable drop compensation.

FPWM/PSM Selection

The RTQ2117C provides an MODE/SYNC pin for Forced-PWM Mode (FPWM) and Power Saving Mode (PSM) operation selection at light load. To optimize efficiency at light loads, the RTQ2117C can be set in PSM. The $V_{MODE/SYNC}$ is held below a logic-low threshold voltage (V_{IL_SYNC}) of the MODE/SYNC input, that is, with the MODE/SYNC pin floating or pull low, the device operates in PSM at light load to improve light load efficiency. If it is necessary to keep switching harmonics out of the signal band, the RTQ2117C can operate in FPWM. The device is locked in PWM mode when $V_{MODE/SYNC}$ rises above a logic-high threshold voltage (V_{IH_SYNC}) of the MODE/SYNC input. The FPWM trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, fast transient response, and constant switching frequency.

Switching Frequency Setting

The RTQ2117C offers adjustable switching frequency setting and the switching frequency can be set by using external resistor RT. Switching frequency range is from 300kHz to 2.2MHz. Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage. An additional constraint on operating frequency are the minimum on-time and minimum off-time. The minimum on-time, t_{ON_MIN}, is the smallest duration of time in which the high-side switch can be in its “on” state. This time is 60ns (typically). In continuous mode operation, the minimum on-time limit imposes a maximum operating frequency, f_{SW_MAX}, of :

$$f_{SW\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times V_{IN\_MAX}}$$

where V_{IN_MAX} is the maximum operating input voltage. The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2117C is capable of turning on the low-side MOSFET switch, tripping the current comparator and turning the MOSFET switch back off. The minimum off time is 65ns (typically). If the switching frequency should be constant, the required off time needs to be larger than minimum off time. Below shows minimum off time calculation with loss terms consideration,

$$t_{OFF\_MIN} \leq \frac{1-\left[\frac{V_{OUT} + I_{OUT\_MAX} \times \left(R_{DS(ON)\_L} + R_L\right)}{V_{IN\_MIN} - I_{OUT\_MAX} \times \left(R_{DS(ON)\_H} - R_{DS(ON)\_L}\right)}\right]}{fsw}$$

where $R_{DS(ON)\_H}$ is the on resistance of the high-side MOSFET switch; $R_{DS(ON)\_L}$ is the on resistance of the low-side MOSFET switch; R_L is the DC resistance of inductor.

Through external resistor R_{RT} connect between RT pin and GND to set the switching frequency f_{SW}. The failure modes and effects analysis (FMEA) consideration is applied to RT pin setting to avoid abnormal switching frequency operation at failure condition. It includes failure scenarios of short-circuit to GND and the pin is left open. The switching frequency will be 2.35MHz (typically) when the RT pin short to GND and 250kHz (typically) when the pin is left open. The equation below shows the relation between setting

frequency and R_{RT} value.

$$R_{RT(k\Omega)} = 74296 \times fsw^{-1.06}$$

Where f_{SW} (kHz) is the desire setting frequency. It is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less resistors. The Figure 12 shows the relationship between switching frequency and R_{RT} resistor.

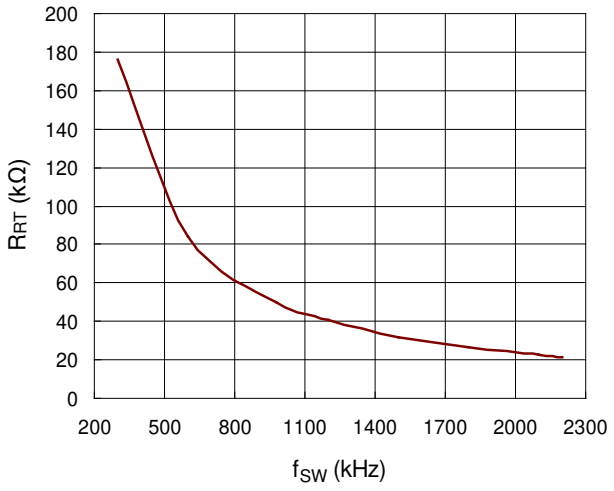


Figure 12. Switching Frequency vs. R_{RT} Resistor

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This result in additional phase lag in the loop and reduce the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold, increases the AC losses in the inductor and may trigger low-side switch sinking current limit at FPWM. It also causes insufficient slope compensation and ultimately loop instability as duty cycle approaches or exceeds 50%. When duty cycle exceeds 50%, below condition needs to be satisfied :

$$2.1 \times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (3A).

To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

Where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 200mV$

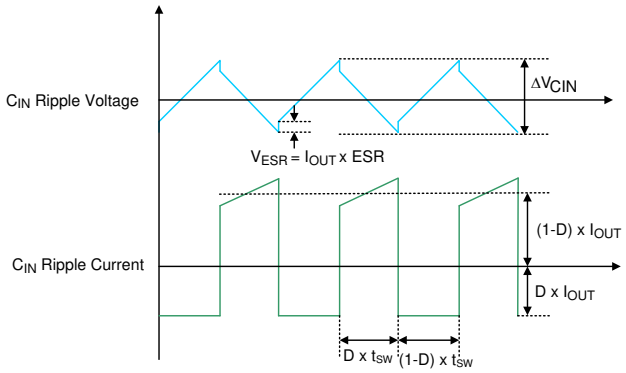


Figure 13. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is commonly to use the worse $I_{RMS} \cong$ 0.5 x I_{OUT_MAX} at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for witching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2117C circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. It is recommended to connect a 4.7μF, X7R capacitors between VIN pin to PGND pin for 2.1MHz switching frequency. The larger input capacitance is required when a lower switching frequency is used. For filtering high frequency noise, additional small capacitor 0.1μF should be placed close to the part and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

Where the ΔI_L is the peak-to-peak inductor ripple current. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, which can be calculated from below.

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The recommended dielectric type of the capacitor is X7R best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 14. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF\_CV} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage of constant voltage control V_{REF_CV}, is 0.8V (typically).

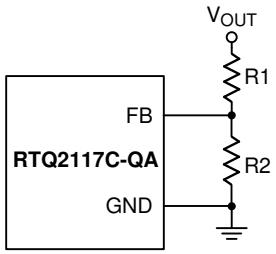


Figure 14. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is not larger than 170kΩ for noise immunity consideration. The resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF\_CV})}{V_{REF\_CV}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used. Note that the resistance of R1 relates to cable drop compensation setting. The resistance of R1 should be designed to match the needs of the voltage drop application, see the adjustable output voltage with cable drop compensation section.

Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. Typical symptoms of an unstable power supply include : audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power MOSFETs and so on.

In most cases, the peak current mode control architecture used in the RTQ2117C only requires two external components to achieve a stable design as shown in Figure 15. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device. Around the crossover frequency the peak current mode control (PCMC) equivalent circuit of Buck converter can be simplified as shown in Figure 16. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the

slope compensation is ignored, the actual cross over frequency will usually be lower than the crossover frequency used in the calculations. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot take full account of circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, then on linearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the following steps to calculate the compensation components :

1. Set up the crossover frequency, fc. For stability purposes, our target is to have a loop gain slope that is –20dB/decade from a very low frequency to beyond the crossover frequency. In general, one-twentieth to one- tenth of the switching frequency (5% to 10% of f_{SW}) is recommended to be the crossover frequency. Do “NOT” design the crossover frequency over 80kHz when switching frequency is larger than 800kHz. For dynamic purposes, the higher the bandwidth, the faster the load transient response. The downside to high bandwidth is that it increases the regulators susceptibility to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.
2. R_{COMP} can be determined by :

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF\_CV} \times gm\_CS} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_CS} \times \frac{R1 + R2}{R2}$$

where

gm is the error amplifier gain of trans-conductance (950μA/V)

gm_cs is COMP to current sense (5.6A/V)

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading (R_L). Calculate C_{COMP} :

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero and optional CCOMP2 can be used to cancel this zero

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency.

$$C_{COMP2} = \frac{1}{2 \times \pi \times \frac{f_{SW}}{2} \times R_{COMP}}$$

NOTE : Generally, C_{COMP2} is an optional component to be used to enhance noise immunity.

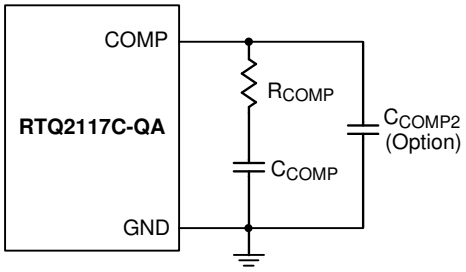


Figure 15. External Compensation Components

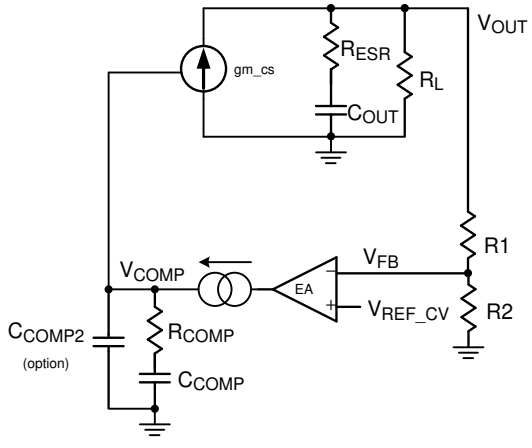


Figure 16. Simplified Equivalent Circuit of Buck with PCMC

Internal Regulator

The device integrates a 5V linear regulator (VCC) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{VIN} is below 5V. The VCC can be used as the PGOOD pull-up supply but it is "NOT" allowed to power other device or circuitry. The VCC pin must be bypassed to ground with a minimum of 0.7μF, X7R ceramic capacitor, placed as close as possible to the VCC pin. In many applications, a 1μF, 16V, 0603, X7R is a suitable choice. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between BOOT pin and SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage equal to approximately V_{VCC} each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications a 0.1μF, 0603 ceramic capacitor with X7R is recommended and the capacitor should have a 6.3 V or higher voltage rating.

External Bootstrap Diode (Option)

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side switch and improve efficiency when the input voltage is below 5.5V, the recommended application circuit is shown in Figure 17. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2117C. Note that the $V_{BOOT-SW}$ must be lower than 5.5V. Figure 18 shows efficiency comparison between with and without Bootstrap Diode.

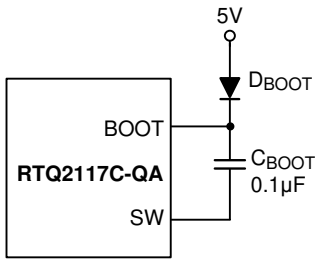


Figure 17. External Bootstrap Diode

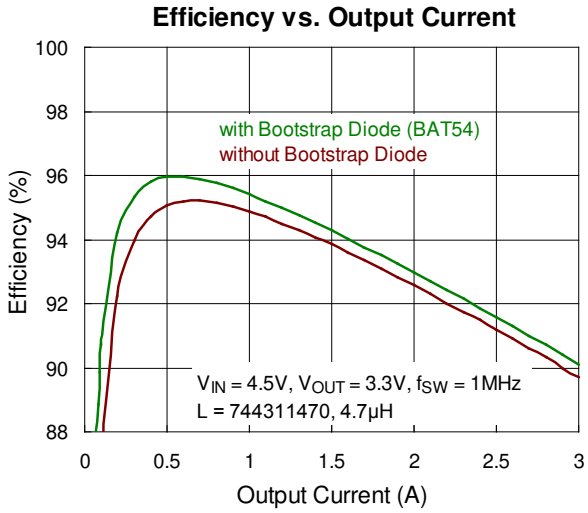


Figure 18. Efficiency Comparison between with and without Bootstrap Diode

External Bootstrap Resistor (Option)

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small bootstrap resistor R_{BOOT} between the BOOT pin and the external bootstrap capacitor as shown in Figure 19. The recommended range for the R_{BOOT} is several ohms to 10 ohms and it could be 0402 or 0603 in size.

This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. In order to improve EMI performance and enhancement of the internal MOSFET switch, the recommended application circuit is shown in Figure 20, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

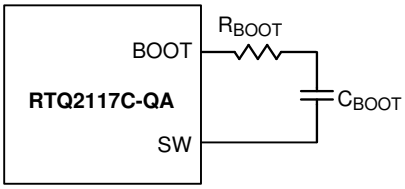


Figure 19. External Bootstrap Resistor at the BOOT Pin

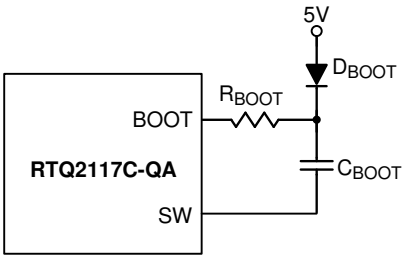


Figure 20. External Bootstrap Diode and Resistor at the BOOT Pin

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 21, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V).

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 22. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 23.

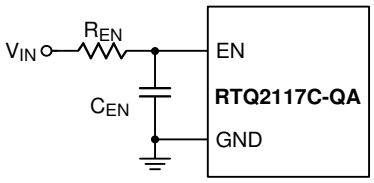


Figure 21. Enable Timing Control

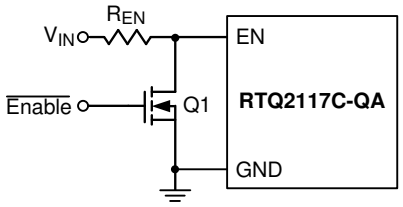


Figure 22. Logic Control for the EN Pin

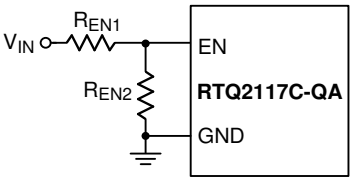


Figure 23. Resistive Divider for Under-Voltage Lockout Threshold Setting

Soft-Start

The RTQ2117C provides adjustable soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. For the RTQ2117C, the soft-start timing can be programmed by the external capacitor C_{SS} between SS and GND. An internal current source I_{SS} (6μA) charges an external capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft start interval. The typical soft start time (t_{SS}) which is V_{OUT} rise from zero to 90% of setting value is calculated as follows :

$$t_{SS} = C_{SS} \times \frac{0.8}{I_{SS}}$$

If a heavy load is added to the output with large capacitance, the output voltage will never enter regulation because of UVP. Thus, the device remains in hiccup operation. The C_{SS} should be large enough to ensure soft-start period ends after C_{OUT} is fully charged.

$$C_{SS} \geq C_{OUT} \times \frac{I_{SS} \times V_{OUT}}{0.8 \times I_{COUT\_CHG}}$$

where I_{COUT_CHG} is the C_{OUT} charge current which is related to the switching frequency, inductance, high-side MOSFET switch peak current limit and load current.

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 5.5V, VCC or the output of the RTQ2117C if the output voltage is regulated under 5.5V. It is recommended to connect a 100kΩ between an external voltage source to PGOOD pin.

Inductor Peak Current Limit Setting

The current limit of high-side MOSFET switch is adjustable by an external resistor connected to the RLIM pin. The recommended resistor value is ranging from 33kΩ (for typ. 5.5A) to 91kΩ (for typ. 2.2A) and it is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less resistors. When the inductor current reaches the current limit threshold, the COMP voltage will be clamped to limit the inductor current. Inductor current ripple current also should be considered into current limit setting. It recommends setting the current limit minimum is 1.2 times as high as the peak inductor current. Current limit minimum value can be calculate as below :

Current limit minimum = ($I_{OUT(MAX)}$ + 1 / 2 inductor current ripple) x 1.2. Through external resistor R_{LIM} connect to RLIM pin to setting the current limit value.

The current limit value below offer approximate formula equation :

$$R_{LIM}(k\Omega) = \frac{178.8}{I_{SET} - 0.2531} - 1$$

Where I_{SET} is the desire current limit value (A)

The failure modes and effects analysis (FMEA) consideration is also applied to RLIM pin setting to avoid abnormal current limit operation at failure condition. It includes failure scenarios of short-circuit to GND and the pin is left open. The inductor peak current limit will be 6.2A (typically) when the RLIM pin short to GND and 1.4A (typically) when the pin is left open. Note that the inductor peak current limit variation increases as the tolerance of R_{LIM} resistor increases. As the R_{LIM} resistor value is small, the inductor peak current limit will probably be operated as RLIM pin short to GND, and vice versa. The R_{LIM} resistance variation range is limited from 30kΩ to 100kΩ to eliminate the undesired inductor peak current limit. When choosing a R_{LIM} other than the recommended range, please make sure that there is no problem by evaluating it with real machine.

Synchronization

The RTQ2117C can be synchronized with an external clock ranging from 300kHz to 2.2MHz which is applied to the MODE/SYNC pin. The external clock duty cycle must be from 20% to 80% and amplitude should have valleys that are below V_{IL_SYNC} and peaks above V_{IH_SYNC} (up to 6V). The RTQ2117C will not enter PSM operation at light load while synchronized to an external clock, but instead will operate in FPWM to maintain regulation.

Average Current Limit

The RTQ2117C implements Constant Current Control to achieve average current limit. The constant current of CC mode control is set by external sense resistance (R_{SENSE}).

The average current is set according to the following equation :

$$\text{Average Current Limit} = \frac{V_{REF\_CC}}{R_{SENSE}}$$

where the reference voltage of constant current regulation V_{REF_CC}, is 100mV (typically) and the V_{REF_CC} variation is around ±10%. The average current limit function is recommended to operate with CSP/CSN voltages range from 3.3 V to 6V.

Adjustable Output Voltage with Cable Drop Compensation

The RTQ2117C provides cable drop compensation function at CV regulation. If the trace from the RTQ2117C output terminator to the load is too long, there will be a voltage drop on the long trace which is

variable with load current. The RTQ2117C is capable of compensating the output voltage drop to keep a constant voltage at load, whatever the load current is.

The compensation voltage (V_{O_OFFSET}) is based on cable drop compensation current (I_{LC}) and divide upper side resistor R1, which can be calculated as following formula :

$$V_{O\_OFFSET} = I_{LC} \times R1$$

The cable drop compensation current variation is ±10%, and it is a function of current sense voltage (V_{CS}) :

$$I_{LC}(\mu A) = 21 \times (V_{CS} - 0.00476)$$

where current sense voltage is the voltage difference between CSP and CSN, that is the voltage across a current sense resistor (R_{SENSE}). The Figure 24 shows the relationship between cable drop compensation current (I_{LC}) and V_{SENSE}.

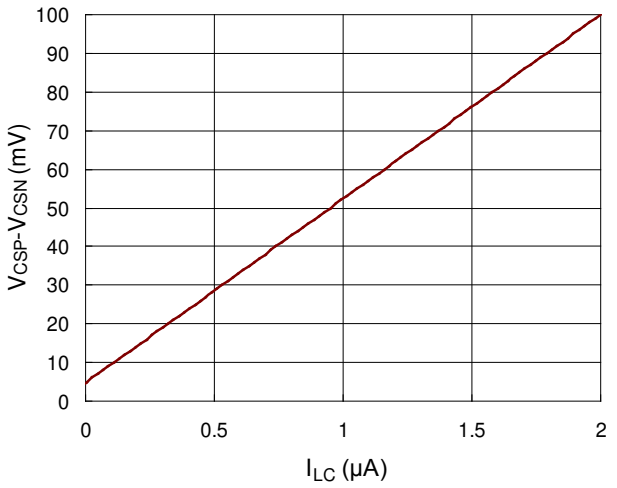


Figure 24. I_{LC} vs. $V_{CSP} - V_{CSN}$

According to the formula above, the desired compensation voltage which is set at rated output current can be calculated as below

$$V_{O\_OFFSET} = 21 \times (R_{SENSE} \times I_{OUT} - 0.00476) \times 10^{-6} \times R1$$

Where I_{OUT} is the rated output current.

Choose the R_{SENSE} with rated load current and reserve some de-rating margin for better thermal and life consideration. In order to avoid the undesired CC control loop interruption, the current sense voltage is selected should be the lower value of 100mV. If the system implements constant current control to achieve average current limit, the R_{SENSE} is set based on the average current limit equation.

Considering CV regulation with cable drop compensation situation, the desire cable drop compensation is 0.24V at rated 2.4A loading and R_{SENSE} is selected as 34mΩ, the R1 can be calculated as below :

$$R1 = \frac{V_{O\_SFFSET}}{21 \times (R_{SENSE} \times I_{OUT} - 0.00476) \times 10^{-6}} = 148.7k\Omega$$

Select 147kΩ for R1. The resistance of R2 can then be obtained as below :

$$R2 = \frac{R1 \times V_{REF\_CV}}{V_{OUT} - V_{REF\_CV}} = 28k\Omega$$

In this case, 147kΩ is available for resistance of R1 and 28kΩ is available for resistance of R2. The R1 and R2 values can be calculated based on above equation. If the R1 and R2 values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current will be noticeable. Make sure the current flowing through the FB resistive divider is larger than $5x10^{-6}$. In addition, a feed-forward capacitor C_{FF} may be required to improve output voltage ripple at PSM.

The power dissipation on sensing resistor will be :

$$P_{RSENSE} = R_{SENSE} \times I_{OUT}^2 = 306mW$$

Choose current sense resistor power rated with 50% de-rating rule of thumb for better heat and life consideration, 1W size is well enough for this case. Hence, the 34mΩ, 1W size R_{SENSE} is determined and with aid of the cable drop compensation feature, the RTQ2117C can compensate the 0.24V voltage drop to maintain excellent output voltage accuracy at rated 2.4A load current. Note that the R_{SENSE} should be connected as close to the CSP/CSN with short, direct traces, creating Kelvin connection to ensure that noise and current sense voltage errors do not corrupt the differential current sense signals between the CS and VOUT pins. The cable drop compensation function is recommended to operate with CSP/CSN voltages range from 3.3 V to 6V.

Configuration Channel and Plug Orientation Detection

The function of the Configuration Channel (CC) is to detect connections and configure the interface across the USB Type-C cables and connectors as shown in Table 2.

Functionally the Configuration Channel (CC) is used to serve the following purposes:

- Attach/Detach detection
- Plug orientation and cable twist detection to establish USB data bus routing
- Establish DFP and UFP roles between two connected ports
- Discover and configure power
- If UFP is attached by Type-C connector, the device turns on external VBUS MOSFET to apply
- Power on VBUS. Reversible Type-C plug orientation is detected by the POL pin when a UFP is connected. By using POL the RTQ2117C implements the SS+ function with SS+ MUX as shown in Figure 25.

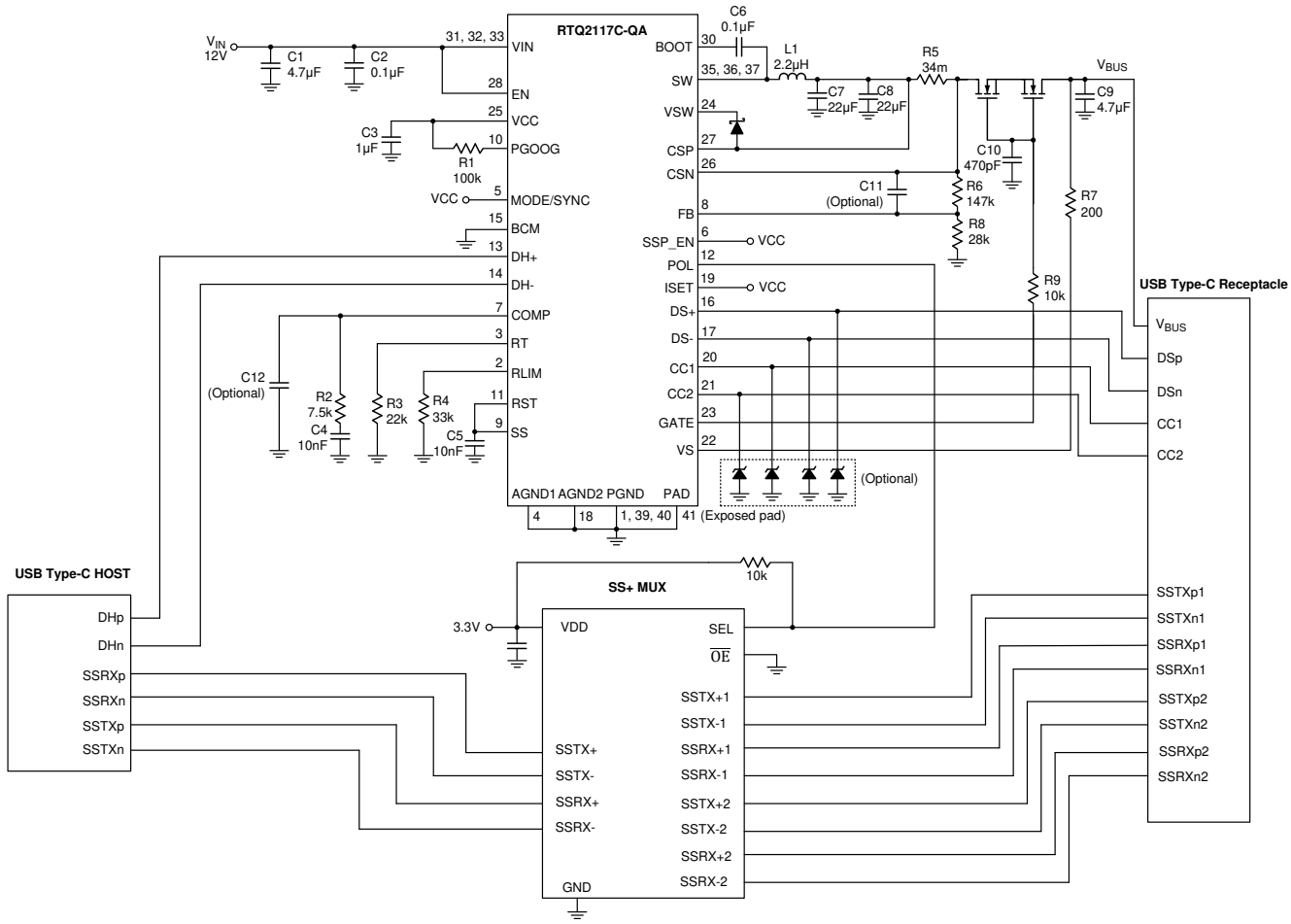


Figure 25. Polarity Application for SS+ MUX

Table 2. Shows RTQ2117C Response to Various Attachments.

RTQ2117C Type-C Detection	CC1	CC2	VBUS	VCONN on CC1 or CC2	POL
Un-attached	OPEN	OPEN	OFF	NO	LOW
UFP Attached	RD	OPEN	ON	NO	LOW
	OPEN	RD	ON	NO	Hi-Z
Only Power Cable Attached	RA	OPEN	OFF	NO	LOW
	OPEN	RA	OFF	NO	LOW
Power Cable & UFP Attached	RD	RA	ON	CC2	LOW
	RA	RD	ON	CC1	Hi-Z
Debug Accessory (Not Support)	RD	RD	--	--	--
Audio Adapter Accessory (Not Support)	RA	RA	--	--	--

Battery Charging Mode Control

USB Battery Charging Specification BC1.2 lists three different port types: Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). The RTQ2117C supports USB BC1.2 SDP/CDP and DCP auto-detect Mode and set by BCM pin.

Standard Downstream Port (SDP) USB 2.0/USB 3.0

An SDP is a traditional USB port that follows USB 2.0/3.0 protocol, and supplies a maximum of 500mA for USB 2.0 and 900mA for USB 3.0 per port. Communication through USB data lines is supported, and the host controller must be active to allow charging.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5A current. It provides power and meets USB 2.0 requirements for device enumeration. USB 2.0 communications is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device, and allows for additional current draw by the client device.

DCP Auto Mode

The DCP Auto Mode only provides power but does not support data connection to an upstream port. The RTQ2117C integrates an auto-detect state machine that supports all the DCP charging schemes listed below :

- Shorted
- Divider 3
- 1.2V shorted

Shorted mode complies with BC1.2 DCP and Chinese Telecommunications Industry Standard YD/T 1591-2009, defining that the D+/D- data lines should be shorted together with a maximum series impedance of 200Ω.

In Divider3 charging scheme the device applies 2.7V/2.7V to D+/D- data lines.

1.2V shorted charging scheme applies 1.2V to the shorted D+/D- data lines.

The DCP auto mode starts in Divider 3 Mode, however if a BC1.2 or YD/T 1591-2009 compliant device is attached, it responds by operating in BC1.2 shorted mode briefly then moves to 1.2V shorted mode. The complete detection Flow as shown in Figure 26.

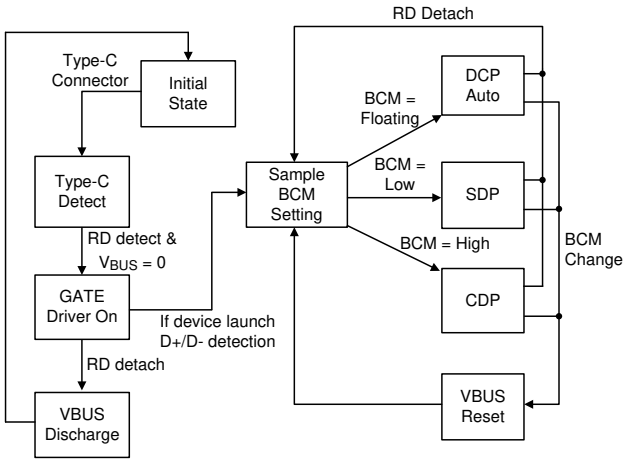


Figure 26. Detection Flow

CDP/SDP Auto Switch

The RTQ2117C is equipped with a CDP/SDP auto-switch feature to support some popular phones in the market that are not compliant to the BC1.2 specification, as they fail to establish data connection in CDP mode. These phones use primary detection (used to distinguish between an SDP and different types of Charging Ports) to only identify ports as SDP or DCP. They do not recognize CDP ports. When connected to a CDP port, these phones classify the port as a DCP and only charges. To fix this problem, the RTQ2117C employs a CDP/SDP Auto Switch scheme to ensure these BC1.2 non-compliant phones establishes data connection.

ISET and BCM Configuration

The RTQ2117C has both Type-C and Auto-detection function. Table 3 shows ISET and BCM setting for different application.

Table 3

RTQ2117C		
ISET	**BCM**	**Comment**
HiZ	0	Default USB power.
HiZ	HiZ	Violate Type-C 1.2 spec.
HiZ	1	Violate Type-C 1.2 spec.
0	0	1.5A
0	HiZ	1.5A
0	1	1.5A
1	0	3A
1	HiZ	3A
1	1	3A

Thermal Considerations

In many applications, the RTQ2117C does not generate much heat due to its high efficiency and low thermal resistance of its WETD-VQFN-40L 6x6 package. However, in applications in which the RTQ2117C is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RTQ2117C stop switching the power MOSFETs until the temperature drops about 15°C cooler.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$$

where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The device thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RTQ2117C is used in applications where V_{IN} = 12V, I_{OUT} = 2.4A, f_{SW} = 2100kHz, V_{OUT} = 5V. The efficiency at 5V, 2.4A is 89% by using Cyntec-VCHA075D-2R2MS6 (2.2μH, 9.5mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website of 18.8mW in this case. In this case, the power dissipation of the RTQ2117C is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.41W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 50°C/W by using the RTQ2117C evaluation board with 4 layers PCB, 1OZ for all layers. the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 1.41W \times 50°C/W + 25°C = 95.5°C$$

Figure 27 shows the RTQ2117C $R_{DS(ON)}$ versus different junction temperature. If the application calls for a higher ambient temperature, we might recalculate the device power dissipation and the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature.

Using 50°C ambient temperature as an example, the change of the equivalent $R_{DS(ON)}$ can be obtained from Figure 27 and yields a new power dissipation of 1.467W. Therefore, the estimated new junction temperature is

$$T_J' = 1.467W \times 50°C/W + 50°C = 123.3°C$$

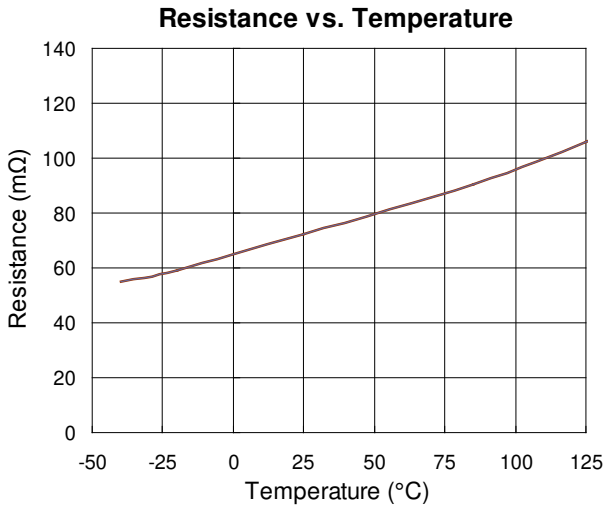


Figure 27. Derating Curve of Maximum Power Dissipation

Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2117C :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN3} as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the C_{VCC} as close to VCC pin as possible.
- Place bootstrap capacitor, C_{BOOT}, as close to IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2117C to additional ground planes within the circuit board and on the bottom side.

- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Reducing the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of output capacitor.
- Place the feedback components near the IC.
- Place the compensation components near the IC.
- Connect all analog grounds to common node and then connect the common node to the power ground with a single point.
- Minimize current sense voltage errors by using Kelvin connection for PCB routing of the CSP pin, CSN pin and current sense resistor (R_{SENSE}).

Figure 28 to Figure 31 are the layout example.

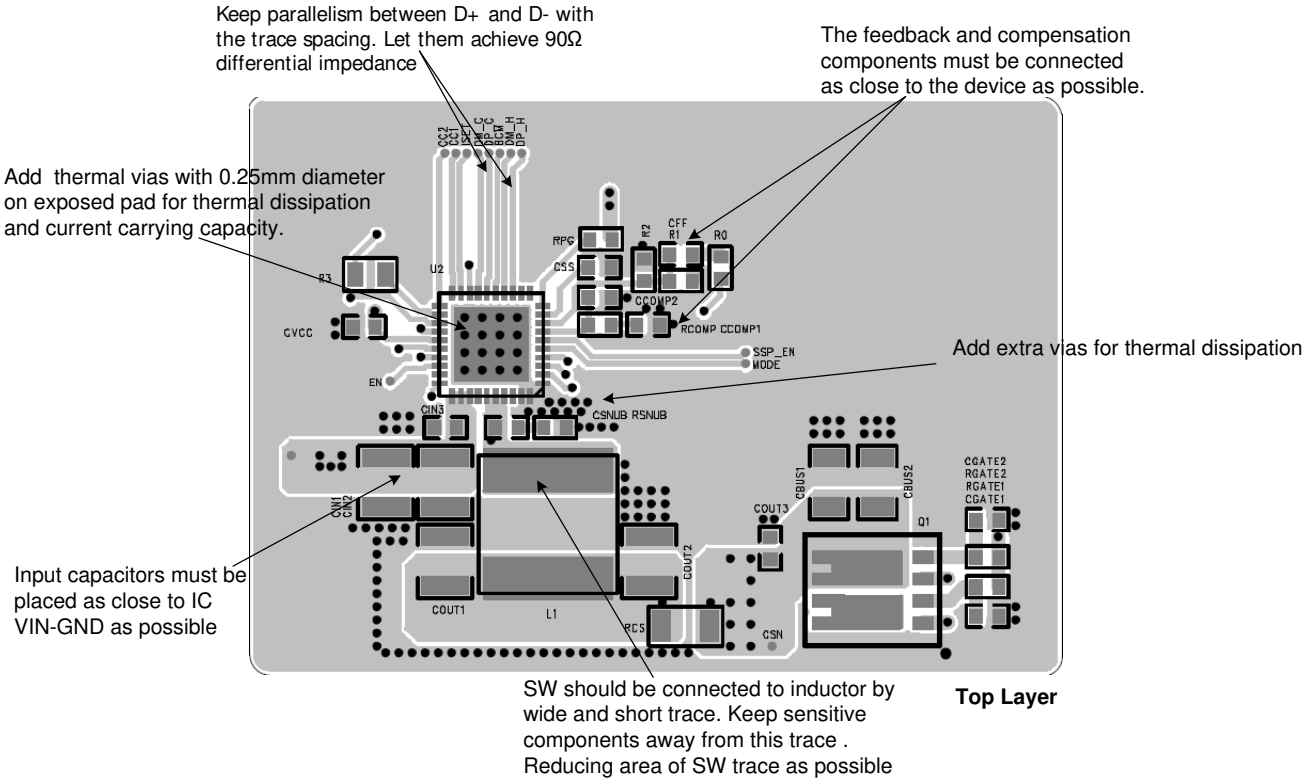


Figure 28. Layout Guide (Top Layer)

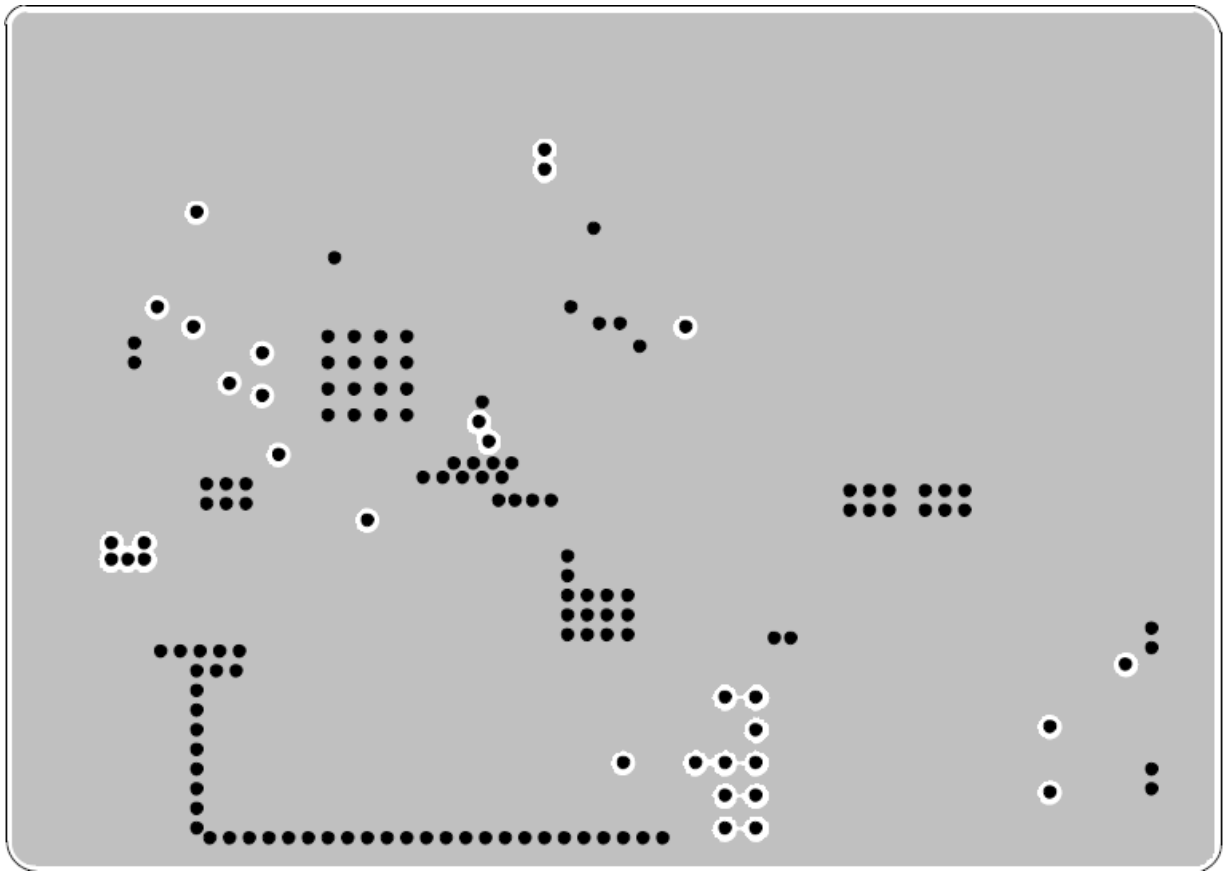


Figure 29. Layout Guide (2 Inner Layer)

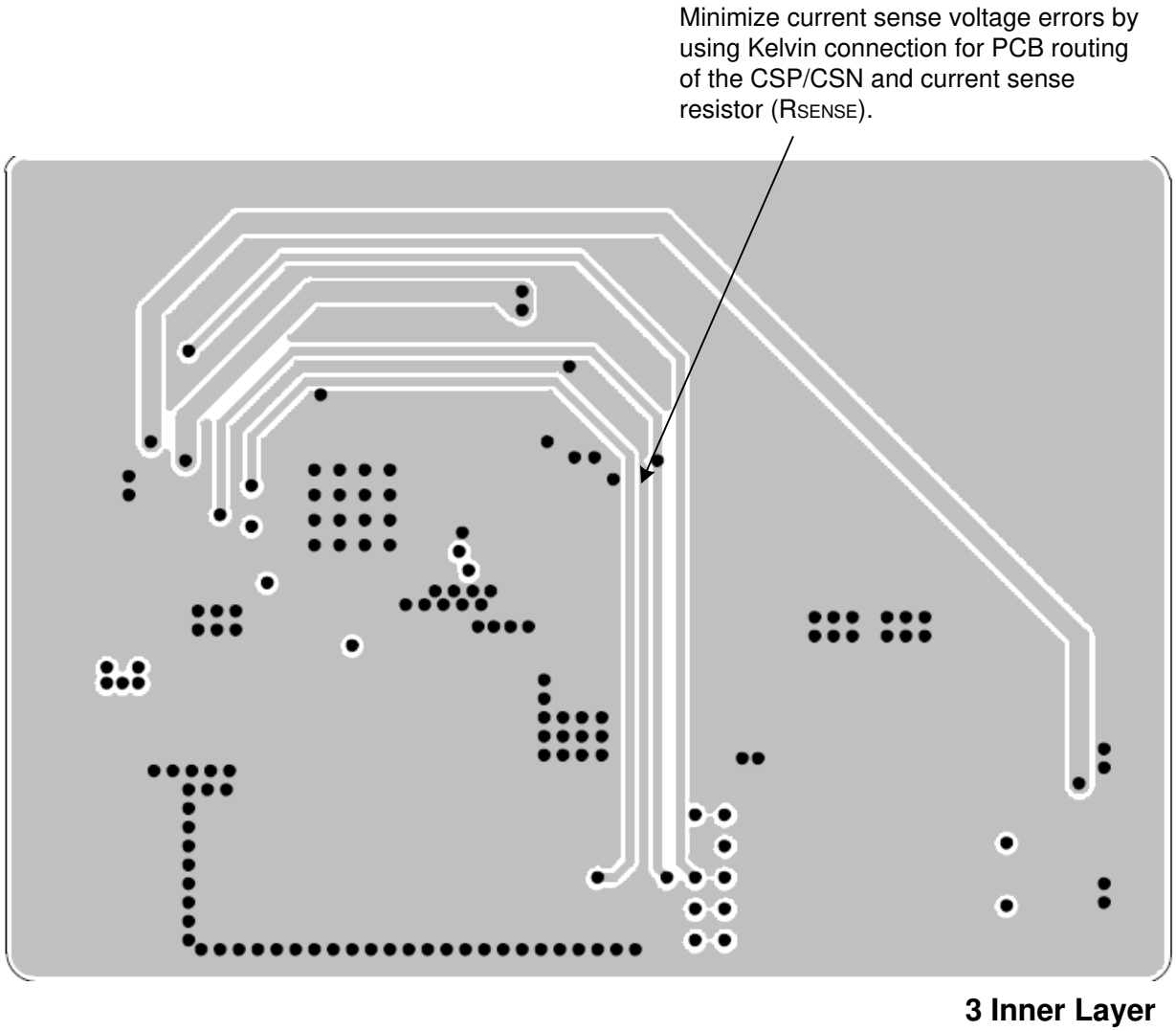


Figure 30. Layout Guide (3 Inner Layer)

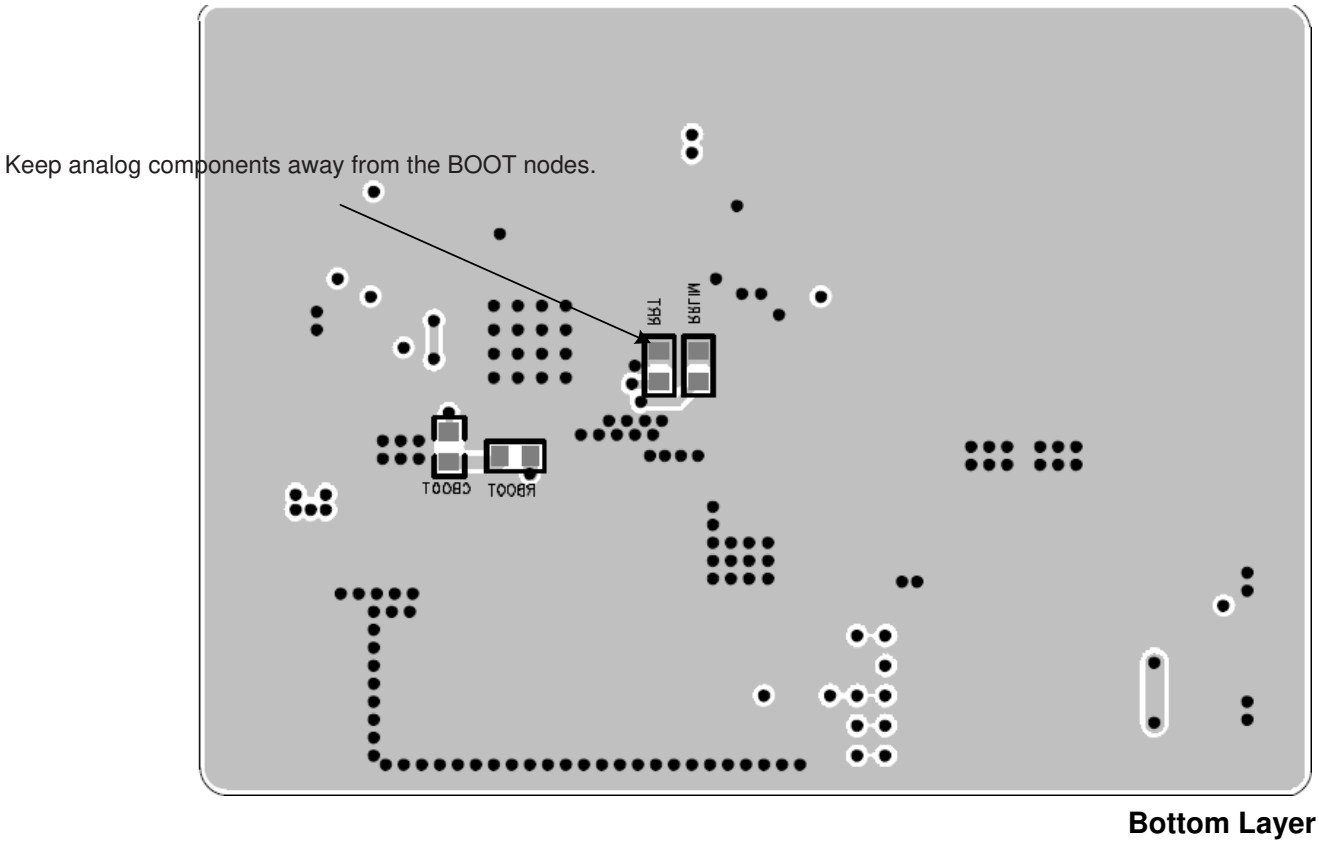
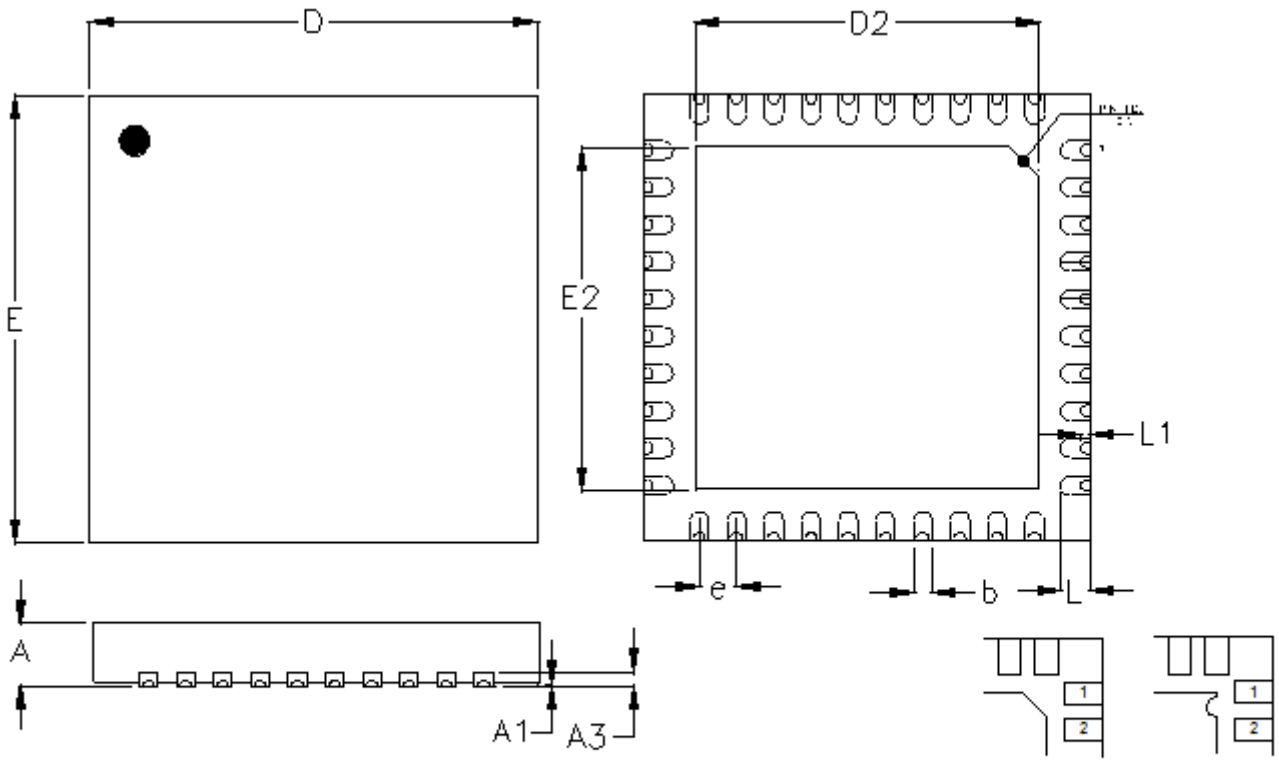


Figure 31. Layout Guide (Bottom Layer)

Outline Dimension



DETAIL A

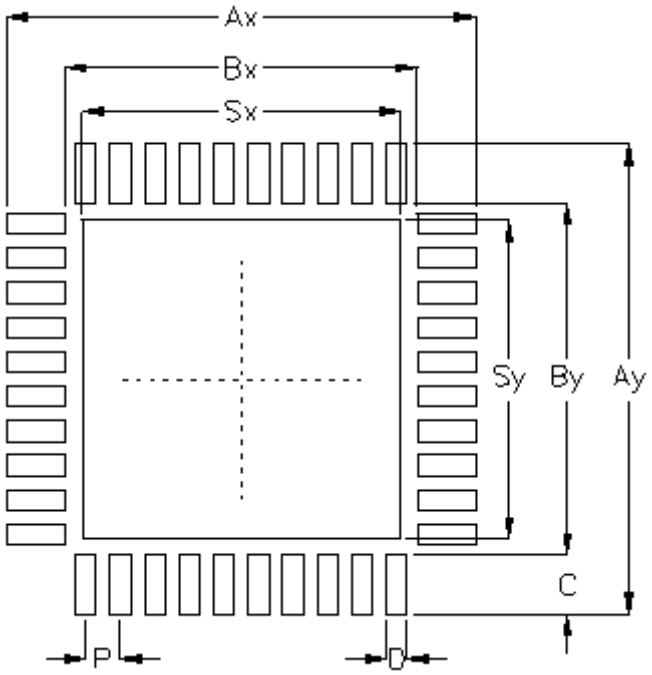
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	5.950	6.050	0.234	0.238
D2	4.550	4.650	0.179	0.183
E	5.950	6.050	0.234	0.238
E2	4.550	4.650	0.179	0.183
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.075	0.175	0.003	0.007

WETD V-Type 40L QFN 6x6 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WETD-V/W/U/XQFN6x6-40	40	0.50	6.80	6.80	5.10	5.10	0.85	0.30	4.60	4.60	±0.05

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