Dual/Hex Low-Side Switch with Both SPI and Parallel Input Control

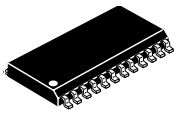
The 33397 is a low-side switch that is user configurable to be either two 333 mΩ outputs (dual mode) or six 900 mΩ outputs (hex mode). Each output is internally current limited and short-circuit protected. Output fault detection capability includes “off state” open loads and “on state” short-to-battery conditions. Faults for each output are latched into the fault register and serially shifted out during serial communication.

Features

- User Configurable to be Either Two 333 mΩ Outputs (Dual Mode) or Six 900 mΩ Outputs (Hex Mode)
- Output Inductive Energy Clamps
- Parallel Input (3.3 V and 5.0 V Compatible) or Serial Peripheral Interface (SPI) Control
- 8-Bit SPI Control and Fault Diagnostics
- Short-to-Battery Detection and Shutdown with Automatic Retry
- OFF-State Open-Circuit Detection
- Programmable Overvoltage Shutdown (V_{PWR} Pin)
- Undervoltage Shutdown (V_{DD} Pin)
- Sleep Mode—$I_{DD} \leq 25$ μA (1.0 μA Typical)

33397

DUAL/HEX LOW-SIDE SWITCH



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42344B
24-PIN SOICW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33397DW/R2	-40 to 125°C	24 SOICW
MCZ33397EG/R2		

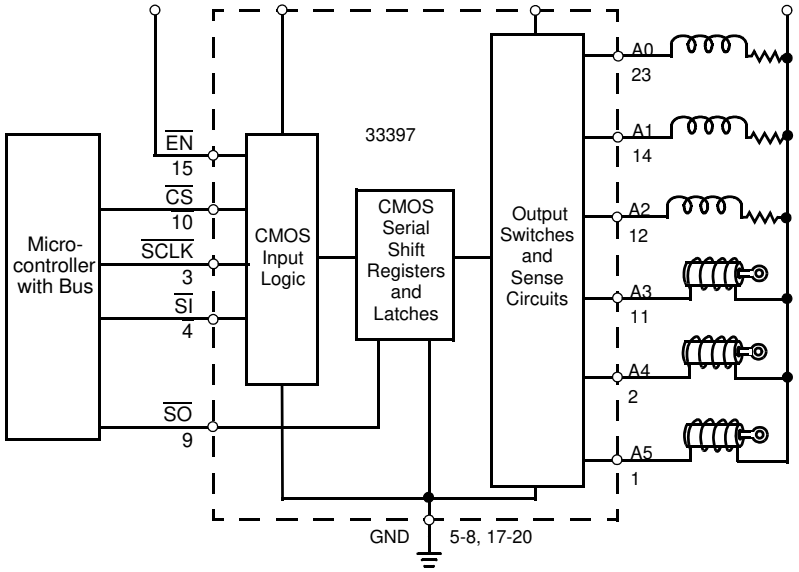


Figure 1. 33397 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

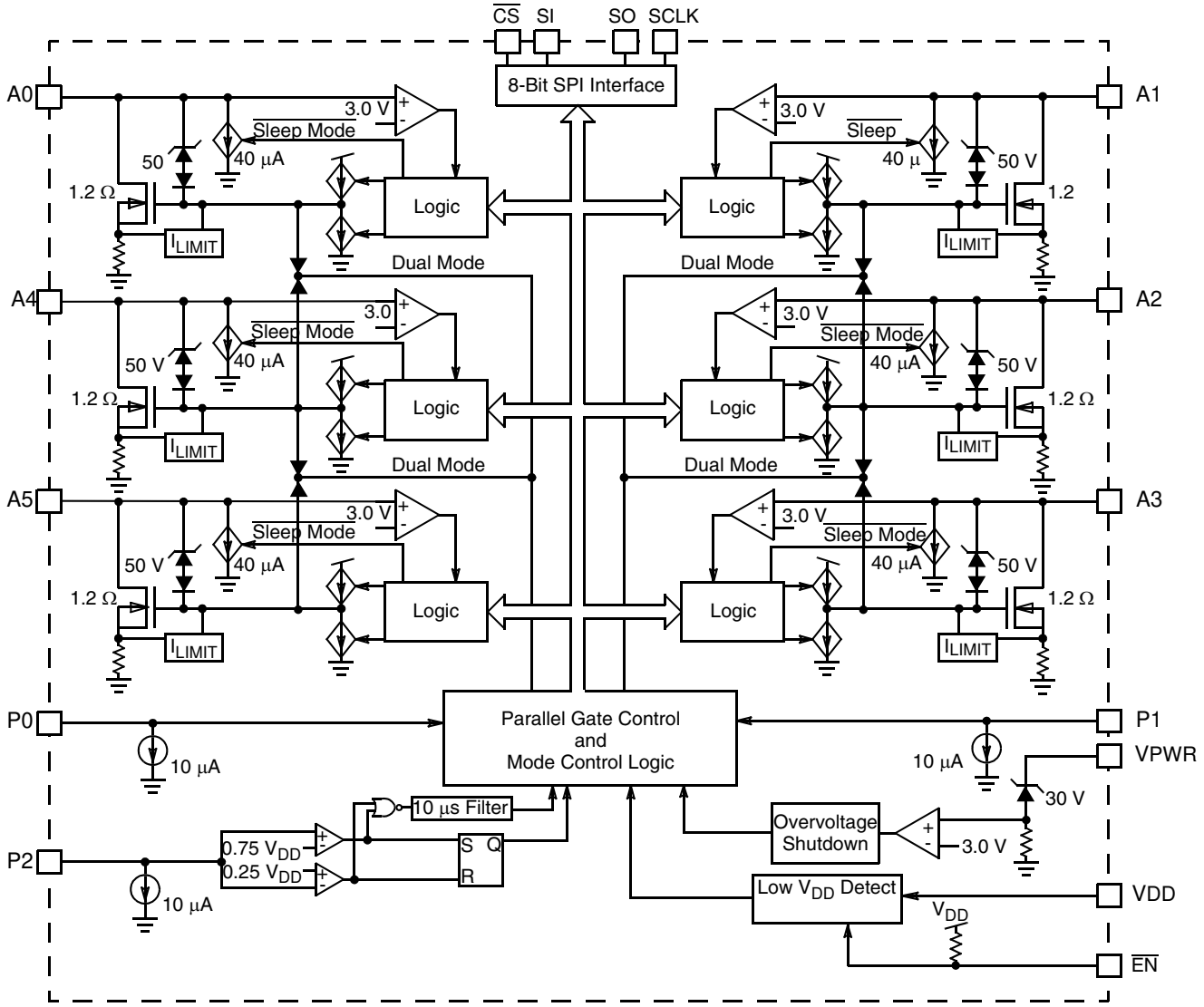


Figure 2. 33397 Simplified Internal Block Diagram

PIN CONNECTIONS

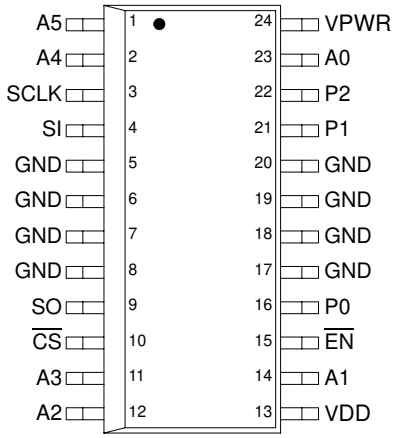


Figure 3. 33397 Pin Connections

Table 1. 33397 Pin Definitions

Pin Number	Pin Name	Definition
1, 2, 11, 12, 14, 23	A0−A5	Power outputs
3	SCLK	SPI clock input
4	SI	SPI serial input
5−8, 17−20	GND	Power and signal ground
9	SO	SPI serial output
10	$\overline{CS}$	SPI chip select
13	VDD	Supply input pin
15	$\overline{EN}$	Enable
16	P0	In hex mode, P0 controls output A0. In dual mode, P0 controls outputs A0, A4, and A5 simultaneously
21	P1	In hex mode, P1 controls output A1. In dual mode, P2 controls outputs A1, A2, and A3 simultaneously
22	P2	In hex mode, P2 controls output A2. P2 is also the mode control pin. If $0.25*V_{DD}<P2<0.75*V_{DD}$ for more than 10 µs, the 33397 will change to dual mode
24	VPWR	Overvoltage threshold shutdown monitoring pin (not a power supply pin for the IC)

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{PWR}	50	V
Logic Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Pin Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
ESD Voltage (1) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Single Pulse Output Clamp Energy I_O=500 mA, T_J=150°C (Hex Mode) I_O=1.5 A, T_J=150°C (Dual Mode)	 J_{CLAMP1} J_{CLAMP1}	 50 100	mJ
Recommended SPI Operating Frequency	f_{OP}	3.5	MHz
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (2), (3)	T_{PPRT}	Note 3	°C
Thermal Resistance, Junction-to-Lead (4)	$R_{\theta J-L}$	15	°C/W

Notes

1. ESD1 performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω), ESD2 performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
4. Leads 5, 6, 7, 8, 17, 18, 19, and 20 are soldered to a heat-sinking ground plane. See Figure 14.

STATIC ELECTRICAL CHARACTERISTICS)

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
VPWR Supply Current (All Outputs ON)	$I_{PWR(ON)}$	–	1.0	50	μA
VPWR Sleep State Supply Current V_{PWR}=17 V, SPI Bit 7=1, $\overline{EN}$=5.0 V	$I_{PWR(SS)}$	–	1.0	10	μA
Overvoltage Shutdown	$V_{P(OV)}$	30	33	38	V
Overvoltage Shutdown Hysteresis	$V_{P(OV)Hys}$	0.3	0.5	1.5	V
Logic Supply Current (All Outputs ON)	I_{DD}	–	1.20	5.0	mA
Logic Supply Current (Sleep State: $\overline{EN}$=5.0 V, SPI Bit 7=1)	I_{DDSS}	–	1.0	25	μA
Logic Supply Undervoltage Inhibit Threshold	$V_{DD(LVI)}$	2.5	3.0	3.5	V
INPUT					
Input Voltage (P0, P1, P2, $\overline{EN}$, SI, SCLK, $\overline{CS}$) High Low	 V_{IH} V_{IL}	 0.8 –	 – –	 – 0.2	V_{DD}
Dual Mode Threshold (P2) Upper Threshold Lower Threshold	 V_{DMH} V_{DML}	 0.7 0.2	 0.75 0.25	 0.8 0.3	V_{DD}
Input Current Pull-Down (P0, P1)-V_{IN}=V_{DD} Pull-Down (P2)-V_{IN}=V_{DD} Pull-Up ($\overline{CS}$)-V_{IN}=0 V Pull-Up ($\overline{EN}$)-V_{IN}=0 V Pull-Up (SCLK, SI)-V_{IN}=2.5 V	 I_{INPD} I_{INPD} I_{INPU} I_{INPU} I_{INPU}	 10 5.0 -20 -100 -10	 20 10 -10 – 0	 30 30 -5.0 -10 10	μA
OUTPUT					
Output Drain to Source ON Resistance (Hex Mode) (6) I_O=0.35 A, T_J=-40°C I_O=0.35 A, T_J=25°C I_O=0.35 A, T_J=150°C	$R_{DS(ON)}$	 0.39 0.51 0.51	 0.5 0.7 1.0	 1.2 1.2 1.2	Ω
Output Voltage Clamp I_{DS}=20 mA, Output Off I_{DS}=200 mA, Output Off	BV_{DSS}	 50 50	 55 56	 60 60	V
Output Leakage Current (Hex Mode) $\overline{EN}$=H, bit 7=1, V_{DRAIN}=24 V	$I_{O(SS)}$	 0.0	 –	 10	μA
Output Logic Voltage (SO), I_{LOAD}=1.0 mA High Low	 V_{OH} V_{OL}	 0.8 –	 – –	 – 0.2	V_{DD}
Output Tristate Leakage (SO), V_{SO}=2.5 V	I_{SOT}	-10	–	10	μA

Notes

5. This parameter is specified for hex mode. In dual mode, the parameter will be three times smaller.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted

Characteristic	Symbol	Min	Typ	Max	Unit
FAULT DETECTION					
Output Self-Limiting Current (Hex Mode) (6) Outputs Programmed ON	$I_{O(LIM)}$	1.0	1.5	2.0	A
Output Fault Detect Threshold Voltage Outputs Programmed OFF, $\overline{EN}$=0	$V_{OF(TH)}$	0.5	0.6	0.7	V_{DD}
Output OFF Open Load Detect Current Output Programmed OFF, $\overline{EN}$=0	$I_{O(OFF)}$	20	40	80	μA

Notes

6. This parameter is specified for hex mode. In dual mode, the parameter will be three times smaller.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics
Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT TIMING					
Output Rise Time V_{PWR}=14 V, R_{LOAD}=25 Ω, 20–80%	t_R	1.0	1.2	10	µs
Output Fall Time V_{PWR}=14 V, R_{LOAD}=25 Ω, 80–20%	t_F	1.0	2.0	10	µs
Output Turn-On Propagation Delay	t_{PON}	1.0	4.0	10	µs
Output Turn-Off Propagation Delay	t_{POFF}	1.0	4.0	10	µs
FAULT TIMING					
Output Short-to-Battery Fault Filter Time	t_{SS}	30	50	90	µs
Output Refresh Timer	t_{REF}	3.0	4.1	6.0	ms
Output Refresh Timer Duty Cycle	D	0.2	1.56	3.0	%
Output Off-State Open Circuit Fault Filter Time	t_{OOF}	30	50	90	µs
SPI/MISCELLANEOUS TIMING					
SO Disable Time (10 K Pull-Up Resistor on SO) $\overline{CS}$=0.8 V to SO > 0.8*V_{DD}	t_{SODIS}	–	80	110	ns
SO Enable Time (10 K Pull-Up Resistor on SO) $\overline{CS}$=0.8 V to SO Low Impedance	t_{SOEN}	–	80	110	ns
SO Rise Time CL < 200 pF	t_{SORISE}	–	30	50	ns
SO Fall Time CL < 200 pF	t_{SOFALL}	–	30	50	ns
SO Valid Time Falling Edge of SCLK to SO Valid	t_{VALID}	–	65	80	ns
Required Time Between Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	–	100	140	ns
Required Time Between SI to Rising Edge of SCLK	t_{SU}	–	25	45	ns
POR/$\overline{EN}$ Wake-Up Timer	t_{POR}	20	40	60	µs
Mode Change Timer (P2)	t_{MODE}	5.0	10	25	µs

TIMING DIAGRAMS

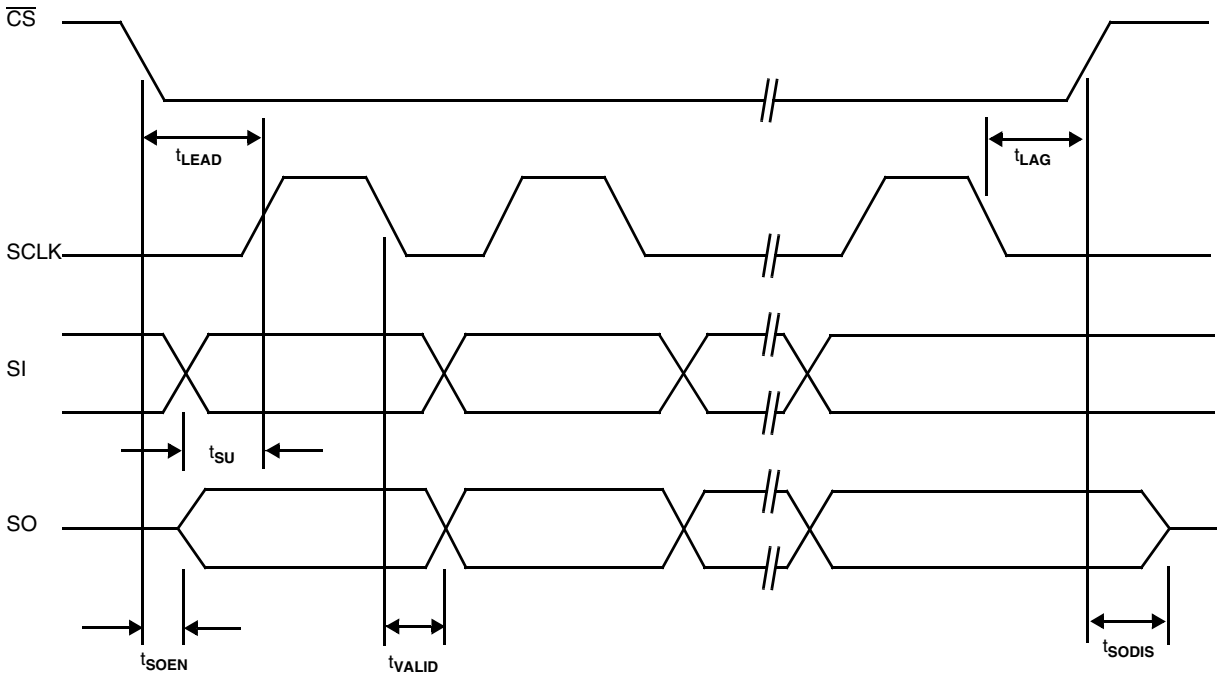
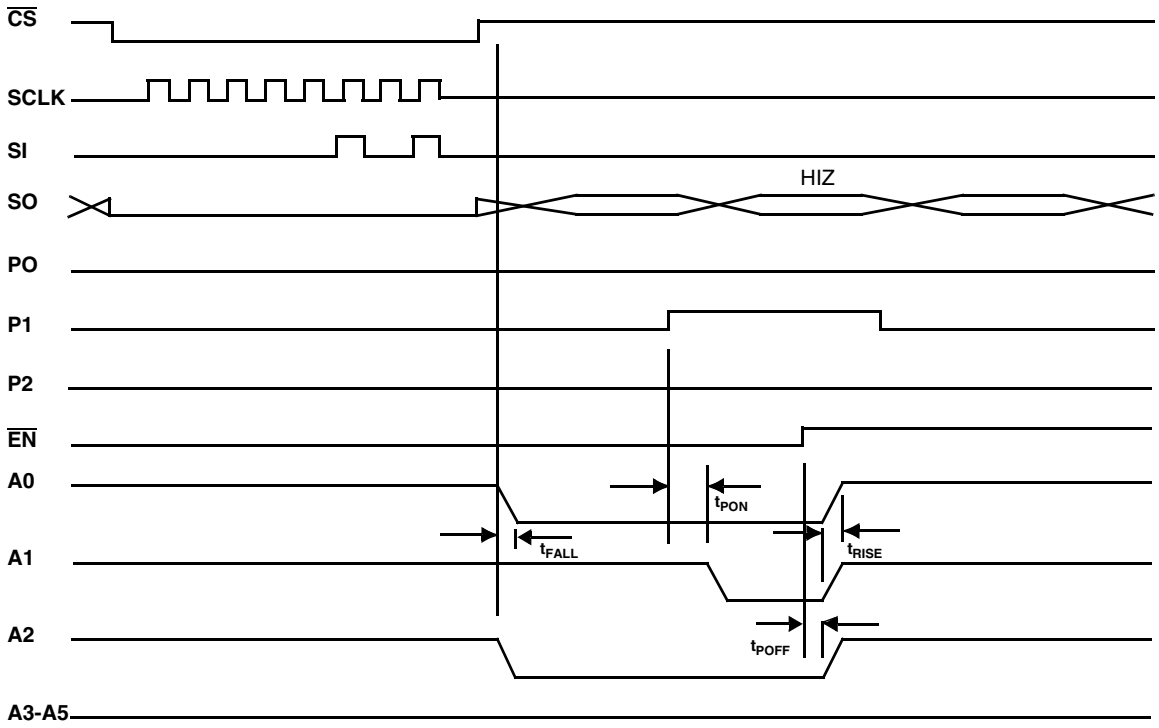


Figure 4. SPI Timing Diagram



Note: In hex mode, the outputs are controlled by the SPI or by the parallel inputs. However, P0, P1, and P2 only control A0, A1, and A2, respectively. When $\overline{EN}$ goes high, the part is disabled.

Figure 5. Operation Waveforms for Hex Control

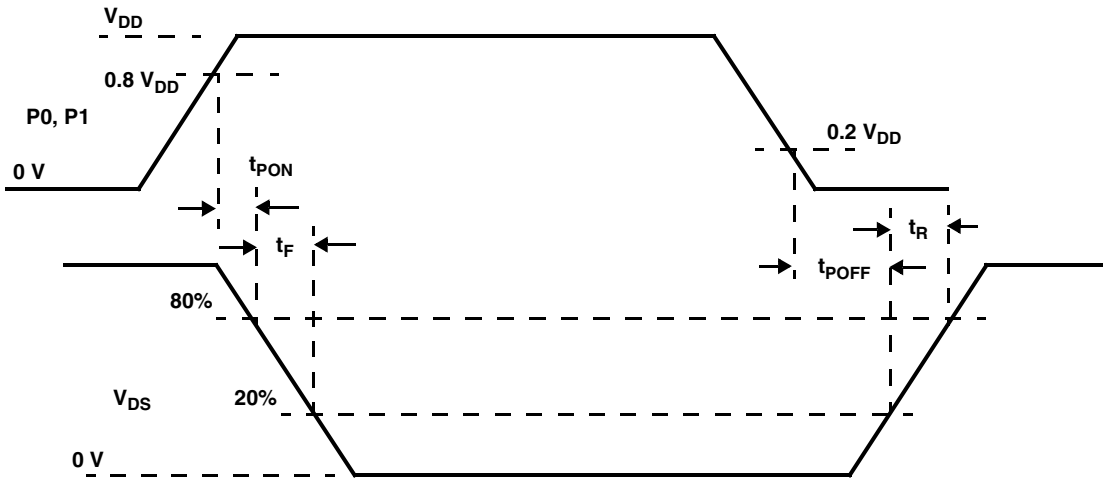


Figure 6. Response Times

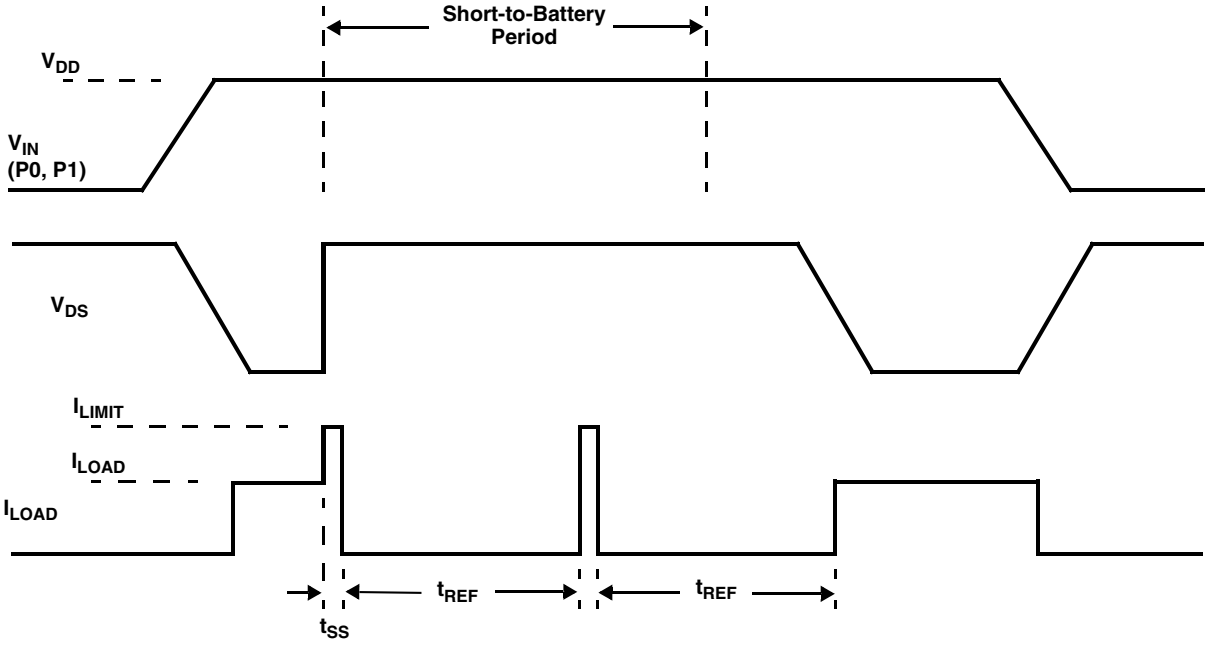


Figure 7. Short-to-Battery Fault

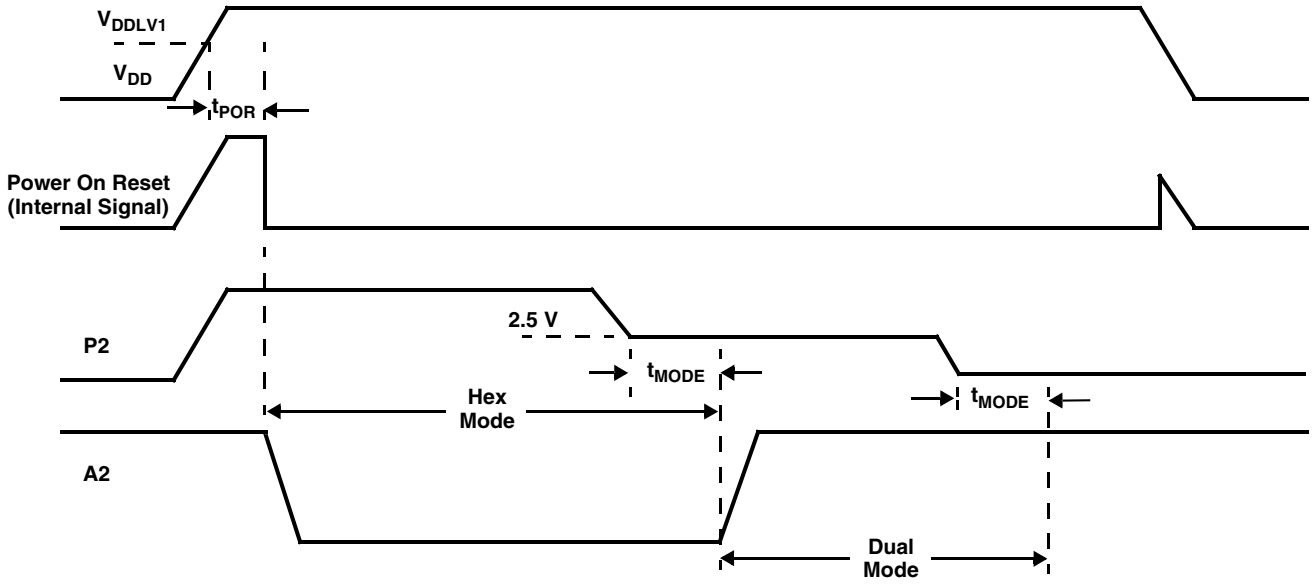


Figure 8. Power-On Reset and Mode Select

TYPICAL SWITCHING WAVEFORMS

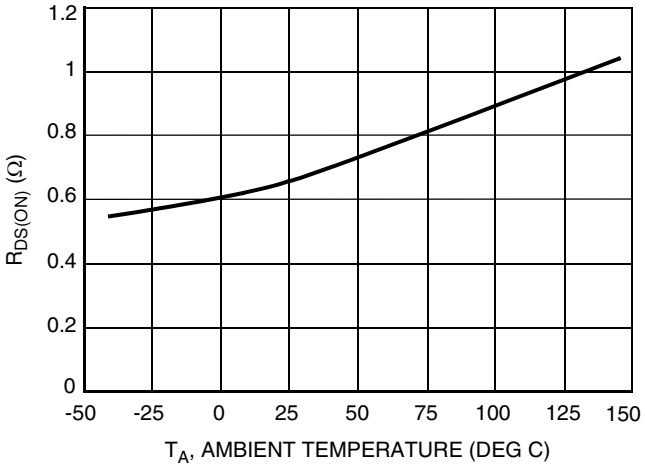


Figure 9. Output on Resistance vs. Temperature

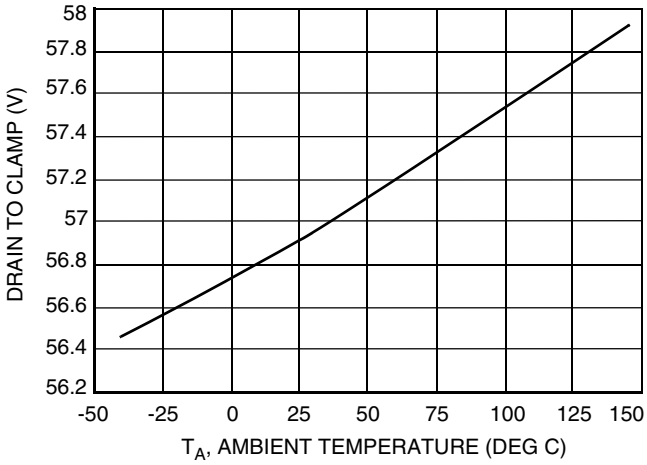


Figure 10. Drain to Source Clamp vs. Temperature

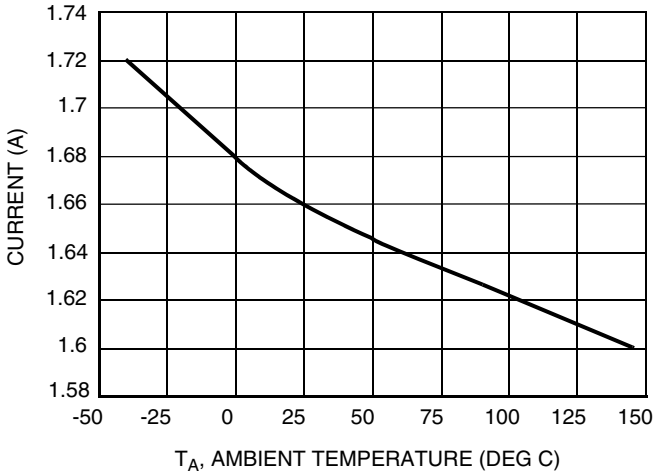


Figure 11. Current Limit vs. Temperature

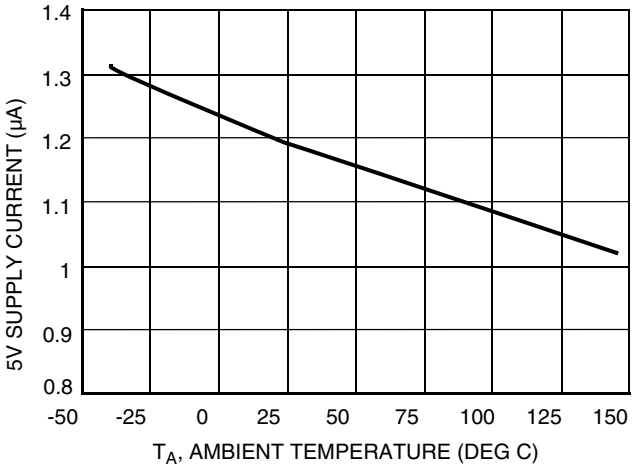


Figure 13. I_{DD} vs. Temperature

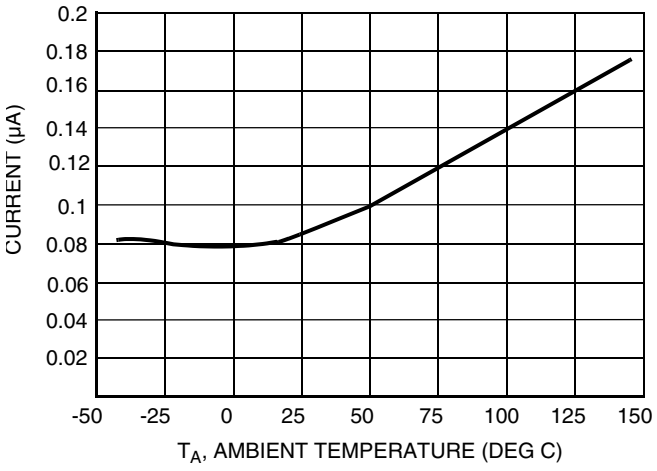


Figure 12. I_{VPWR} vs. Temperature

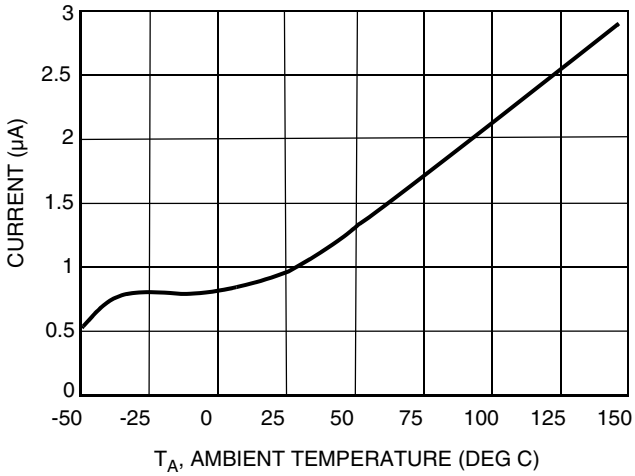
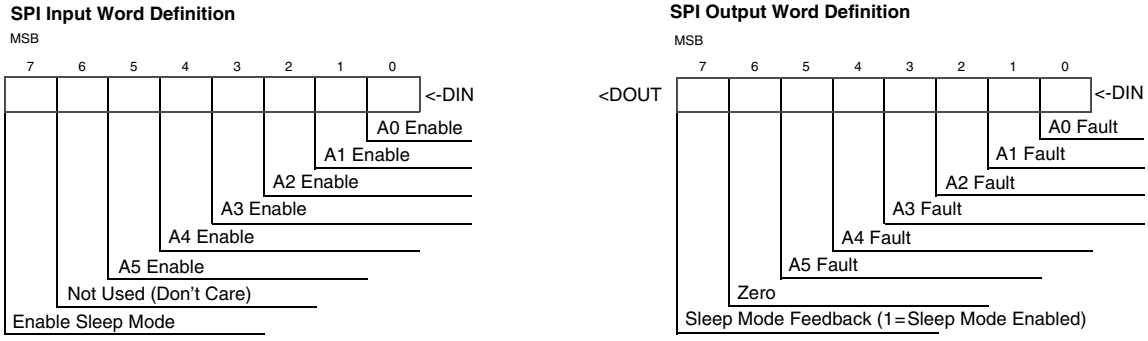


Figure 14. I_{DD} Sleep State vs. Temperature



The device will power up with sleep mode enabled.
In dual mode, input bits 0, 4, and 5 must all be high to turn on combinational output A0, A4, and A5 via the SPI.
In dual mode, input bits 1, 2, and 3 must all be high to turn on combinational output A1, A2, and A3 via the SPI.

Figure 15. SPI Input/Output Word Definition

33397

Table 5. Truth Table

Inputs			EN	SPI Bit7	Outputs						Comments
P0	P1	P2			A0	A1	A2	A3	A4	A5	
0	0	0	0	X	OFF	OFF	OFF	*	*	*	HEX MODE * = Outputs A3, A4, and A5 are SPI controlled only. X = Don't care. Outputs A0, A1, and A2 are controlled either via SPI or inputs P0, P1, and P2.
0	0	1	0	X	OFF	OFF	ON	*	*	*	
0	1	0	0	X	OFF	ON	OFF	*	*	*	
0	1	1	0	X	OFF	ON	ON	*	*	*	
1	0	0	0	X	ON	OFF	OFF	*	*	*	
1	0	1	0	X	ON	OFF	ON	*	*	*	
1	1	0	0	X	ON	ON	OFF	*	*	*	
1	1	1	0	X	ON	ON	ON	*	*	*	
0	0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	HEX MODE Outputs A3, A4, and A5 are always OFF. Outputs are not controlled via SPI. Outputs A0, A1, and A2 are only controlled via inputs P0, P1, and P2. Sleep mode disabled.
0	0	1	1	0	OFF	OFF	ON	OFF	OFF	OFF	
0	1	0	1	0	OFF	ON	OFF	OFF	OFF	OFF	
0	1	1	1	0	OFF	ON	ON	OFF	OFF	OFF	
1	0	0	1	0	ON	OFF	OFF	OFF	OFF	OFF	
1	0	1	1	0	ON	OFF	ON	OFF	OFF	OFF	
1	1	0	1	0	ON	ON	OFF	OFF	OFF	OFF	
1	1	1	1	0	ON	ON	ON	OFF	OFF	OFF	
0	0	2.5 V	0	X	OFF	OFF	OFF	OFF	OFF	OFF	DUAL MODE Outputs are also controlled via SPI. SPI fully functional.
0	1	2.5 V	0	X	OFF	ON	ON	ON	OFF	OFF	
1	0	2.5 V	0	X	ON	OFF	OFF	OFF	ON	ON	
1	1	2.5 V	0	X	ON	ON	ON	ON	ON	ON	
0	0	2.5 V	1	0	OFF	OFF	OFF	OFF	OFF	OFF	DUAL MODE Outputs are not controlled via SPI. Outputs are controlled via inputs P0 and P1. Sleep mode disabled.
0	1	2.5 V	1	0	OFF	ON	ON	ON	OFF	OFF	
1	0	2.5 V	1	0	ON	OFF	OFF	OFF	ON	ON	
1	1	2.5 V	1	0	ON	ON	ON	ON	ON	ON	
X	X	X	1	1	OFF	OFF	OFF	OFF	OFF	OFF	All outputs disabled. SPI is reset and ignored. No fault detection.

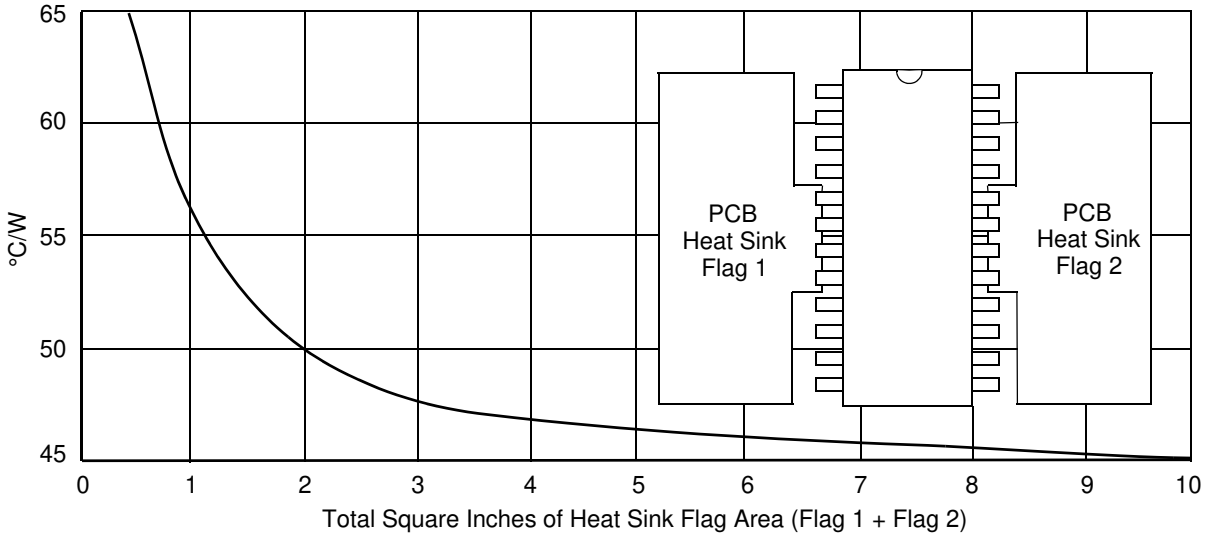


Figure 16. Approximate Thermal Resistance Using PCB Heat Sinking

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33397 is a versatile dual-mode low-side switch that can be output-configured as two 333 mΩ open drain outputs in the dual mode or as six 900 mΩ open drain outputs in the hex mode ($R_{DS(ON)}$ @ 25°C).

Each open drain output has internal current limit and short-circuit protection. Current limit is typically 1.5 A, with 2.0 A maximum. The outputs can be input controlled via parallel inputs or the SPI. Three inputs provide parallel control, while a serial 8-bit word provides SPI control of the outputs. Output fault detection capability includes OFF-state open loads and ON-state short-to-battery conditions. Individual output faults are latched into the fault register and serially shifted out during serial communication to the 33397. The 33397 has both overvoltage and undervoltage shutdown.

A low quiescent current sleep slate feature can be enabled or disabled on command via the SPI port.

FUNCTIONAL PIN DESCRIPTION

VDD

Logic power supply pin.

A0–A5

A0–A5 are the drains of the 1.2 Ω (max.) MOSFETs. They each have an internal voltage clamp of 50 V (min.) to clamp inductive loads during turn-off. When enabled, they are each internally current limited to a maximum of 2.0 A. If any output is in current limit (output voltage >3.0 V) for a time greater than t_{SS}, the output will be disabled for a time t_{REF} and then try to turn on again. When disabled, open circuits are detected if the output is less than 3.0 V for a time of t_{SS}. Either type of fault is reported as a fault on the SPI output word. If $\overline{EN}$ input is high and SPI bit 7=1, the pull-down current sources on the outputs are disabled to minimize V_{DD} supply current.

In hex mode, all six outputs are independent. Outputs A0, A1, and A2 are controlled by either the SPI input word bits 0, 1, and 2, respectively, or parallel inputs P0, P1, and P2. Outputs A3, A4, and A5 are controlled only by SPI input word bits 3, 4, and 5, respectively.

In dual mode, outputs A0, A4, and A5 are all controlled simultaneously by input P0 or by SPI bits 0, 4, and 5. All three bits must be high to enable this output via the SPI. Outputs A1, A2, and A3 are all controlled simultaneously by input P1 or by SPI bits 1, 2, and 3. All three bits must be high to enable this output via the SPI.

P0–P2

In hex mode, P0 is the parallel input to control output A0. It is OR'd with SPI bit 0 to enable output A0. Either one will enable output A0. In dual mode, P0 controls outputs A0, A4, and A5 simultaneously. P0 has a pull down current of 10 µA. It is ignored when $\overline{EN}$ is high and bit 7=1.

In hex mode, P1 is the parallel input to control output A1. It is OR'd with SPI bit 1 to enable output A1. Either one will enable output A1. In dual mode, P1 controls outputs A1, A2, and A3 simultaneously. P1 has a pull-down current of 10 µA. It is ignored when $\overline{EN}$ is high and bit 7=1.

In hex mode, P2 is the parallel input to control output A2. It is OR'd with SPI bit 2 to enable output A2. Either one will enable output A2.

P2 also is used to program the 33397 to either a dual or hex output device. The 33397 will be the hex mode if P2 is biased above 0.75*V_{DD} (typical) or below 0.25*V_{DD} (typical). Normal 5.0 V control logic on this parallel input will maintain the 33397 in hex mode and allow control of output A2. If 0.25*V_{DD} <P2<0.75*V_{DD} for more than 10 µs, the 33397 will switch to dual mode. P2 has a pull-down current of 10 µA. It is ignored when $\overline{EN}$ is high and bit 7=1.

VPWR

V_{PWR} is used to sense an overvoltage condition on the supply pin. When the voltage on V_{PWR} exceeds V_{OV}, all outputs are disabled for the duration of the overvoltage condition. If V_{PWR} is grounded, overvoltage shutdown is disabled. V_{PWR} threshold can be modified with an external resistor divider if higher thresholds are desired.

SCLK

SCLK is the clock for the serial interface.

SI

SI is the serial input for the SPI port. When $\overline{CS}$ is low, SI is read on the positive edge of SCLK and SO is updated on the falling edge. When $\overline{CS}$ is high, SI is ignored. SI has a pull-down current source to pull it low in the event of an open circuit.

SO

SO is the serial output of the SPI port. When $\overline{CS}$ goes low, SO outputs bit 7 of the output word. On each falling edge of SCLK, SO will shift the next SPI output bit until on the eighth SCLK falling edge the bit present on SI during the first rising edge will appear. In this way devices can be daisy-chained to operate on a common $\overline{CS}$. When $\overline{CS}$ is high, SO is high impedance.

$\overline{\text{CS}}$

$\overline{\text{CS}}$ is the chip select to enable the SPI interface. When $\overline{\text{CS}}$ is high, no SPI communication is possible. When $\overline{\text{CS}}$ goes low, SI will be read on each rising SCLK edge and SO will shift on each SCLK falling edge. When $\overline{\text{CS}}$ goes high, the bits present in the SPI input register will be interpreted as the SPI input command. Also when $\overline{\text{CS}}$ goes high, all faults that were latched into the SPI output register are cleared. If faults are still present on outputs, they will be re-latched after t_{SS}.

$\overline{\text{EN}}$

$\overline{\text{EN}}$ must be low for complete IC functionality in either the dual or hex mode. When $\overline{\text{EN}}$ transitions low while in the sleep mode or when the IC is powered up from V_{DD}, a power-up timer of 40 µs is started to allow the 33397 to determine which mode it is in (hex or dual). During this time all parallel inputs and serial control SPI bits will be ignored and all outputs will remain off. If $\overline{\text{EN}}$ transitions low when not in the sleep mode, this “dead” time will not occur.

If a one was written to bit 7, the 33397 will be in the sleep mode when $\overline{\text{EN}}$ goes high. In this mode all SPI registers are reset to zero and all faults are cleared. No fault detection is possible. The standby supply current on V_{DD} and V_{PWR} is minimized.

TYPICAL APPLICATION

INTRODUCTION

A voltage on the P2 input pin determines the mode. All six outputs can operate either independently (hex mode) (Figure 15) or in paralleled groups of three (dual mode) (Figure 16). In the dual mode, outputs A0, A1, and A2 are controlled by parallel inputs P0, P1, and P2, respectively, and they are also controlled by the SPI port with which they are OR'd. On the other hand, outputs A3, A4, and A5 are controlled *only* through the SPI port. When the voltage on P2 is between 0.25 V_{DD} and 0.75 V_{DD} (i.e., when P2 is held at an intermediate voltage, neither high nor low), the 33397 operates in the dual mode. However, the P2 pin must stay at that level for a minimum specified time. In this mode, outputs A0, A4, and A5 are all controlled in parallel by input P0. Outputs A1, A2, and A3 are all controlled in parallel by input P1. Both outputs can also be controlled via the SPI port as well, but only if the three outputs are commanded ON at the same time.

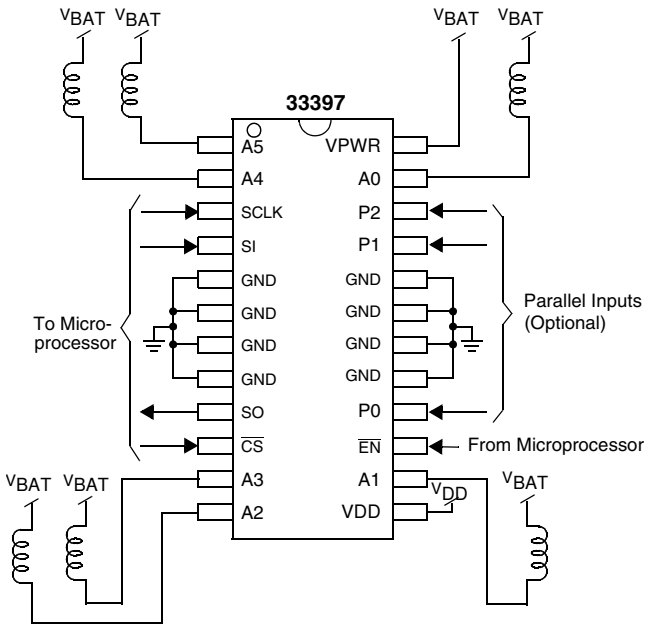


Figure 17. Hex Mode Application Circuit

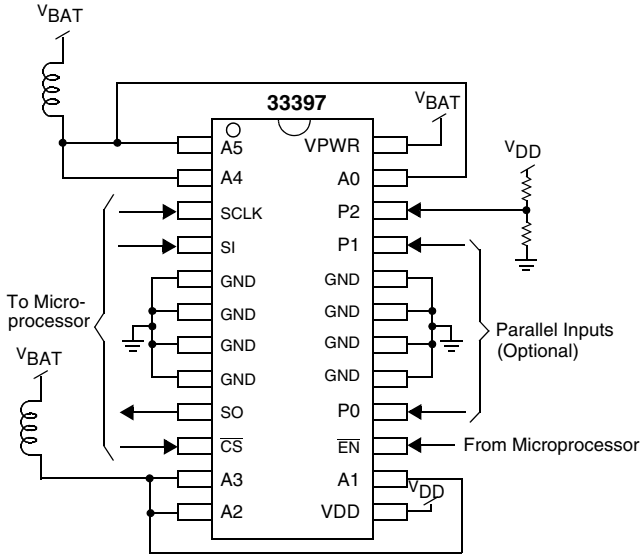
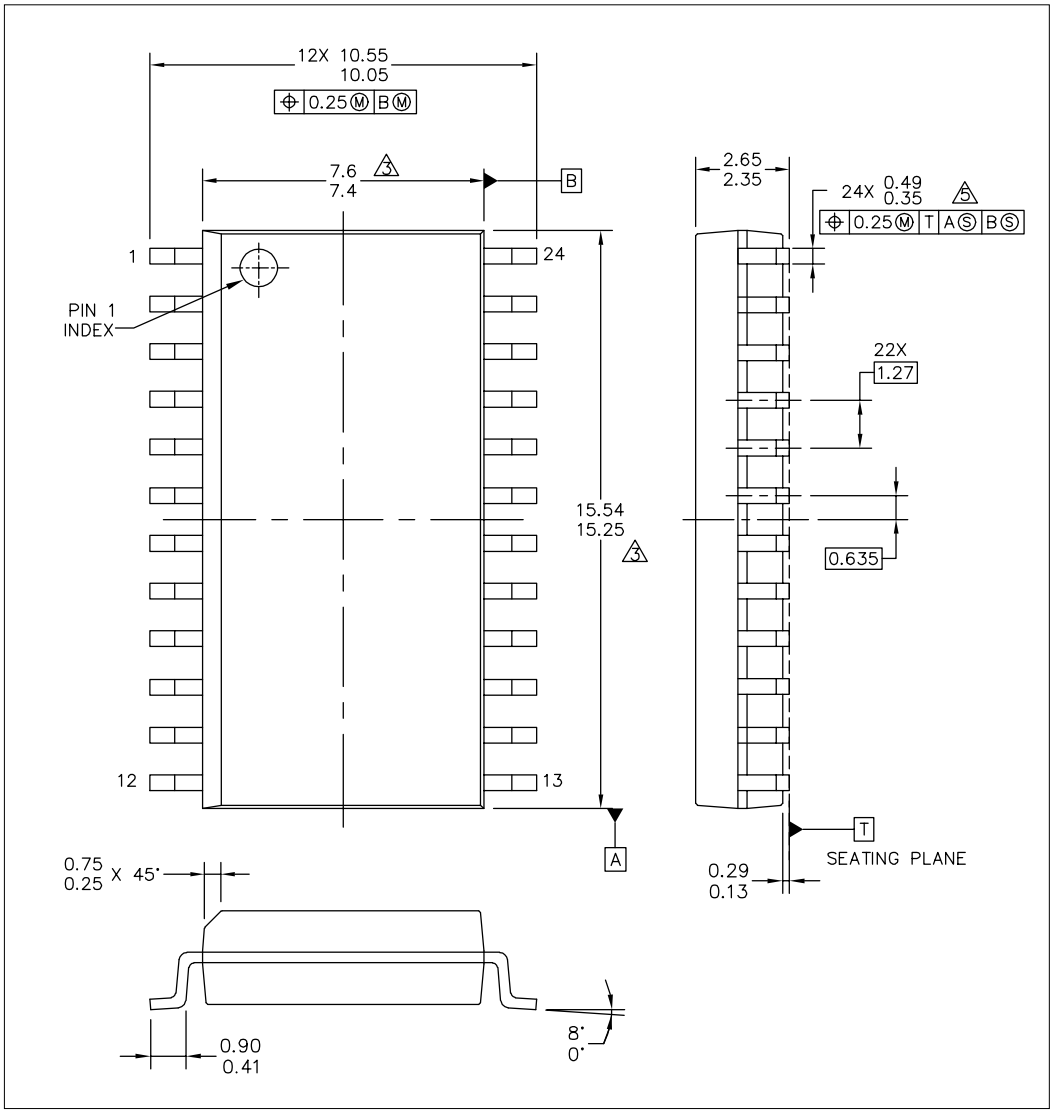


Figure 18. Dual Mode Application Circuit

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using "**98ASB42344B"**.



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TITLE: 24LD SOIC W/B, 1.27 PITCH 7.5 X 15.4 CASE–OUTLINE	DOCUMENT NO: 98ASB42344B	REV: F
	CASE NUMBER: 751E–04	26 APR 2005
	STANDARD: JEDEC MS–013 AD	

DW SUFFIX
EG SUFFIX (PB-FREE)
20-PIN
PLASTIC PACKAGE
98ASB42344B
ISSUE F

33397

REVISION HISTORY

REVISION	DATE	DESCRIPTION
3.0	12/2006	• Implemented Revision History page • Converted to Freescale template • Added EG Pb-FREE suffix. • Added MCZ33397EG/R2 to the Ordering Information • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. • Added notes Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device. on page 4 and Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics. on page 4

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