The Future of Analog IC Technology®

DESCRIPTION

The MP4057A is a single-chip/single-stage solution for smart LED applications that can regulate LED current with primary-side regulation (PSR) control and supply power for microcontroller units (MCU) and wireless modules. The MP4057A is the most ideal solution for smart LED lighting because of its simplest design, fewest external components, and lowest cost.

The MP4057A achieves a high power factor and accurate LED current. The proprietary real-current-control method accurately controls LED current from the primary-side information. The MP4057A integrates power-factor correction and works in valley switching mode to reduce MOSFET switching loss.

The MP4057A achieves ultra-low standby loss (typically 30mW no-load power) by decreasing the working frequency in standby mode.

The MP4057 has an integrated charging circuit at the supply pin for fast start-up without a perceptible delay.

Based on the information from DIM, the MP4057A can operate in two operation modes: constant current (CC) and constant-voltage (CV). The LED can turn off when the MP4057A works in CV mode. During the transition between CC and CV, the LED does not flicker, and the voltage of the MCU/wireless module does not drop.

The MP4057A's multiple protection features enhance system reliability and safety greatly. These features include over-voltage protection (OVP), short-circuit protection (SCP), primary-side over-current protection (OCP), brown-out protection, cycle-by-cycle current limiting protection, under-voltage lockout (UVLO), and auto-restart over-temperature protection (OTP).

The MP4057A is available in MSOP-10 and SOIC14 packages.

FEATURES

- Single-Chip/Single-Stage with LED Driver and Power Supply for MCU/Wireless Modules
- Fast Start-Up
- Ultra-Low Standby Loss, Typically Less Than 30mW in No-Load Condition, Optional Circuit for Less than 15mW at No Load
- 5% Deep Dimming
- No Flicker
- Low Audible Noise
- Valley Switching Mode in CC Mode for Good Efficiency
- Good Power Factor (PF) (Typically >0.9)
- Good Transient Response
- Cycle-by-Cycle Current Limit Protection in CV Mode
- Primary-Side Over-Current Protection (OCP)
- Output Over-Voltage Protection (OVP) and Short-Circuit Protection (SCP)
- Under-Voltage Lockout (UVLO)
- Thermal Shutdown (160°C/100°C)
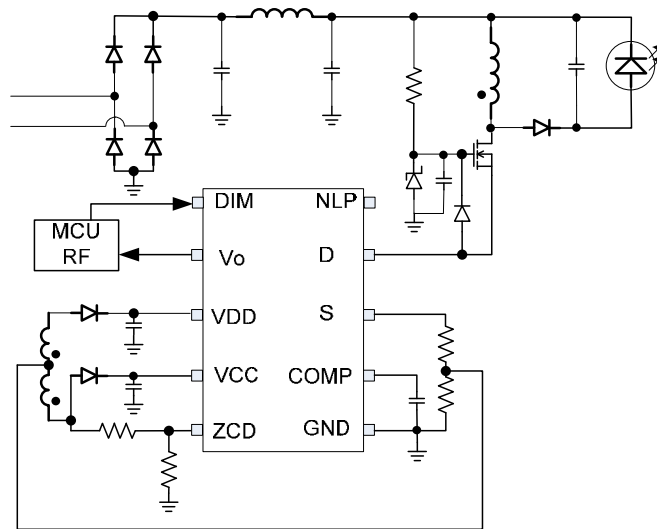- Available in MSOP-10 and SOIC14 Packages

APPLICATIONS

- Zigbee/Bluetooth Smart Lighting
- DALI or Dmax Dimming Protocol

TYPICAL APPLICATION
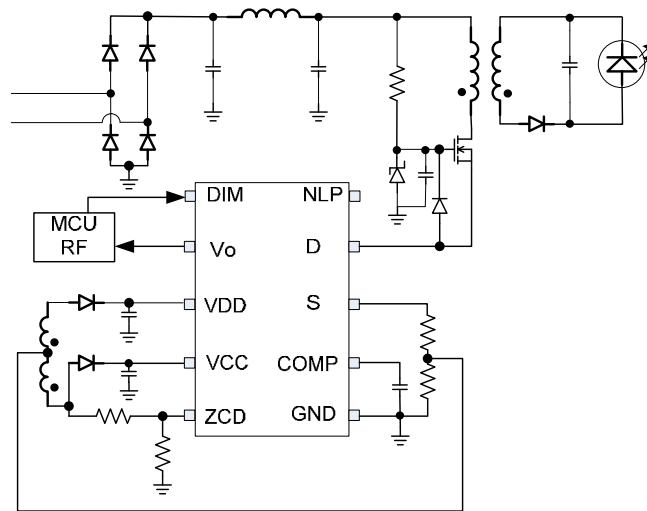
Isolated Flyback Application

Non-Isolated Buck-Boost Application

ORDERING INFORMATION

Part Number	Package	Top Marking
MP4057AGK*	MSOP-10	*See Below*
MP4057AGS**	SOIC-14	

* For Tape & Reel, add suffix –Z (e.g. MP4057AGK–Z)
** For Tape & Reel, add suffix –Z (e.g. MP4057AGS–Z)

TOP MARKING (MP4057AGK)

YWLLL
4057A

Y: Year code
W: Week code
LLL: Lot number
4057A: First five digits of the part number

TOP MARKING (MP4057AGS)

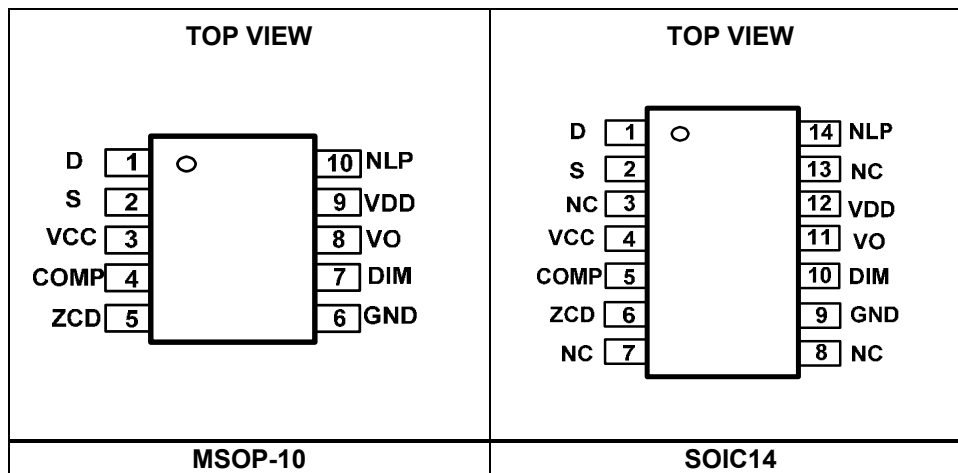MPSYYWW
MP4057A
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4057A: Product code of MP4057AGS
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
D 1 ○ 10 NLP S 2 9 VDD VCC 3 8 VO COMP 4 7 DIM ZCD 5 6 GND	D 1 ○ 14 NLP S 2 13 NC NC 3 12 VDD VCC 4 11 VO COMP 5 10 DIM ZCD 6 9 GND NC 7 8 NC
MSOP-10	**SOIC14**

ABSOLUTE MAXIMUM RATINGS [1]

Supply voltage (VDD) .... -0.3V to 28V
Supply voltage (VCC) .... -0.3V to 28V
NLP .... -0.3V to 28V
ZCD .... -0.3V to 6.5V
Low-side MOSFET drain to source voltage ....
.... -0.7V to 28V
All other pins .... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) [2]
MSOP-10 .... 0.83W
SOIC14 .... 1.45W
Junction temperature .... 150°C
Lead temperature.................................... 260°C
Storage temperature ....-65°C to +150°C

Recommended Operating Conditions [3]

Supply voltage (VDD) .... 5V to 27V
Supply voltage (VCC) .... 4V to 27V
Operating junction temp. (T_J)......-40°C to 125°C

Thermal Resistance [4] θ_{JA} θ_{JC}

MSOP-10 .... 150 ..... 65 ... °C/W
SOIC14 .... 86 ...... 38 ... °C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical values are tested at VDD = VCC = 12V, T_J = +25°C, unless otherwise noted. Minimum and maximum values are tested at VDD = VCC = 12V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage (VDD)						
Operating range	VDD	After turn-on	3.5		27	V
VDD upper level: internal charging circuit stops and the IC turns on	VDD_H	VDD rising edge	10	10.5	11	V
VDD lower level: if VCC is lower than VDD, internal charging circuit is triggered and IC stops switching, UVLO occurs	VDD_L	VDD falling edge	5.2	5.5	5.8	V
VDD operation hysteretic voltage	VDD_{HYS}		4.75	5	5.25	V
VDD low level for high-frequency mode	VDD_{enter}	VDD falling edge at CC mode	4.27	4.5	4.73	V
VDD_enter hysteretic (to exit transient mode)	VDD_{enter_Hys}			1.03		V
Supply Voltage (VCC)						
Operating range	VCC	After turn-on	3.5		27	V
VCC regulated value at CV	$VCC_{regulate}$	With VO 50mA load	4.35	4.6	4.85	V
VCC upper level for UVLO	VCC_H	VCC rising edge	10.2	10.8	11.4	V
VCC lower level: if VDD is lower than VCC, internal charging circuit is triggered and IC stops switching, UVLO occurs	VCC_L	VCC falling edge	5.2	5.5	5.8	V
VCC voltage for start-up	$VCC_{startup}$	VCC rising edge	4	4.2	4.4	V
VCC high-frequency mode (enter) @ CV	VCC_{enter_CV}	VCC falling edge @ CV	3.6	3.8	4	V
VCC_enter hysteretic @ CV	$VCC_{enter\_Hys\_CV}$			0.4		V
VCC high-frequency mode (enter) @ CC	VCC_{enter_CC}	VCC falling edge @ CC	6	6.3	6.6	V
VCC_enter hysteretic @ CC	$VCC_{enter\_Hys\_CC}$			1		V

5

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are tested at VDD = VCC = 12V, T_J = +25°C, unless otherwise noted. Minimum and maximum values are tested at VDD = VCC = 12V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
VDD charging current from D	$I_{D-charge}$	V_D = 16V, VDD = VCC = 10.5V	25	35	50	mA
Operating current	$I_{operating}$	1. COMP = V_{COMP_L} 2. CV operation			330	µA
		1. COMP = 1.8V 2. CV operation 3. 30kHz switch frequency			500	µA
		1. 60kHz switch frequency 2. CC operation			1	mA
Operating current under fault condition	I_{fault}	Fault condition, IC latch, VCC = VDD = 15V	0.95	1.35	1.8	mA
Pull-down current when UVLO	$I_{pull\_down\_UVLO}$	VCC = VDD = 5V	0.75	1.05	1.65	mA
Leakage current on D	$I_{leakage-D}$				1	µA
LDO						
Maximum voltage drop for VO	V_{drop_VO}	With 50mA VO current			0.2	V
Maximum current limit for VO	I_{LDO_max}	VDD = VCC = 10V	100			mA
VO						
Output voltage of VO	VO		3.2	3.3	3.4	V
VO_OK threshold	VOH		2.95	3.1	3.25	V
VO_OK hysteresis	VO_Hys			0.28		V
DIM						
High level	V_{dim_H}		1.13	1.25	1.37	V
Low level	V_{dim_L}		0.27	0.3	0.33	V
Maximum DIM detect time to determine the frequency of PWM dimming signal	t_{dim_detect}		7	9.5	13	ms
Error Amplifier (EA)						
Feedback voltage	V_{FB}		0.196	0.203	0.210	V
Transconductance @ CC [6]	G_{EA}	CC		250		µA/V
Max source current [6]	I_{COMP+}			50		µA
Max sink current [6]	I_{COMP-}			-200		µA
Upper clamp voltage for CC	$V_{COMP\_H\_CC}$		3.8	4	4.2	V
Transconductance @ CV [6]	G_{EA}	CV		50		µA/V
Upper clamp voltage for CV	$V_{COMP\_H\_CV}$	CV	2.5	2.65	2.8	V
Lower clamp voltage	V_{COMP_L}		1.15	1.21	1.27	V

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are tested at VDD = VCC = 12V, T_J = +25°C, unless otherwise noted. Minimum and maximum values are at VDD = VCC = 12V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM Comparator						
Slope rate of normal operation	α		0.35	0.395	0.44	V/µs
Slope rate of CC transient operation	$α_{transient}$	Zero detected and VO > 3.1V	0.06	0.11	0.16	V/µs
Minimum on time	$t_{min\_ON\_time}$	CV	260	390	530	ns
		CC	700	1050	1400	
Zero-Current Detector (ZCD)						
Bias current of ZCD	I_{bias_ZCD}	During turn on	290	350	400	µA
Brown-out protection threshold	$V_{brown\,out}$		0.16	0.19	0.22	V
Brown-out detection time	$t_{brown\,out}$		14	19	25	ms
Zero-current detect threshold	V_{ZCD_T}	V_{ZCD} falling edge	0.25	0.3	0.4	V
Zero-current hysteresis for CV	$V_{ZCD\_hys\_CV}$		0.27	0.3	0.33	V
Zero-current hysteresis for CC	$V_{ZCD\_hys\_CC}$		0.57	0.6	0.63	V
ZCD blanking time	t_{LEB_ZCD}	Only for CC, after turn-off, Vs_peak > 0.15V	1	1.5	2	µs
		1. For CV 2. For CC, after turn-off, Vs_peak < 0.15V	0.5	0.7	0.9	
Over-voltage blanking time	t_{LEB_ZCD}	Only for CC, after turn-off, Vs_peak > 0.15V	1	1.5	2	µs
		1. For CV 2. For CC, after turn-off, Vs_peak < 0.15V	0.5	0.7	0.9	
Over-voltage threshold	V_{ZCD_OVP}	1.5µs delay after turn-off	4.25	4.55	4.8	V
Fault Pull-Up MOSFET						
Breakdown voltage	$BV_{DSS\_D\_VCC}$		30			V
Continue drain current	$I_{D\_D\_VCC}$		8	11.5	15	mA
CV Minimum Off Time						
Maximum off time	$t_{max\_OFF\_CV}$	COMP = V_{COMP_L}	1.5	2.5	3.5	ms
Minimum off time in CV mode	$t_{min\_OFF\_CV}$	COMP = $V_{COMP\_H\_CV}$	25	37	47	µs
CC Minimum Off Time						
Minimum off time in CC mode	$t_{min\_OFF\_CC}$		2.4	3	4.2	µs
Maximum off time	$t_{max\_OFF\_CC}$	COMP = V_{COMP_L}	30	43	57	µs

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are tested at VDD = VCC = 12V, T_J = +25°C, unless otherwise noted. Minimum and maximum values are tested at VDD = VCC = 12V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
S Pin						
Blanking time for S	t_{blank_S}		260	390	530	ns
Blanking time for short inductor/transformer	$t_{blank\_S\_short}$			280		ns
Starter						
Start timer period	t_{START}	ZCD not detected	130	160	190	µs
Current Limit						
CV mode current limit	V_{cv_limit}	With S blanking, T_{blank_S}	0.42	0.45	0.49	V
CC mode current limit	VCC_{limit}	With S blanking, T_{blank_S}	1.39	1.47	1.55	V
CV mode current limit foldback	$V_{cv\_limit\_foldback}$	With S blanking, T_{blank_S}	0.17	0.2	0.23	V
CV mode current limit @ high-frequency mode	$V_{cv\_limit\_HF}$	With S blanking, T_{blank_S}	0.61	0.65	0.69	V
Primary over-current protection	$V_{primary\_OCP}$	With S blanking, $T_{blank\_S\_short}$	1.85	2	2.15	V
NLP						
Leakage current	$I_{leakage\_NLP}$	NLP=20V			350	nA
$R_{DS(ON)}$ of pull-down MOSFET	R_{dson_NLP}			145	300	Ω
Internal Main MOSFET						
Break-down voltage	BV_{DSS_Main}	Vgs = 0	30			V
Drain-source on resistor	$R_{DS(ON)\_Main}$	I_D = 500mA		300		mΩ
Thermal Shutdown						
Thermal shutdown threshold	T_{SD}			160		°C
Thermal shutdown recovery hysteresis	T_{hys}			60		°C

NOTE:
5) Guaranteed by design.

TYPICAL CHARACTERISTICS

Internal MOSFET R$_{DS(ON)}$ vs. Junction Temperature
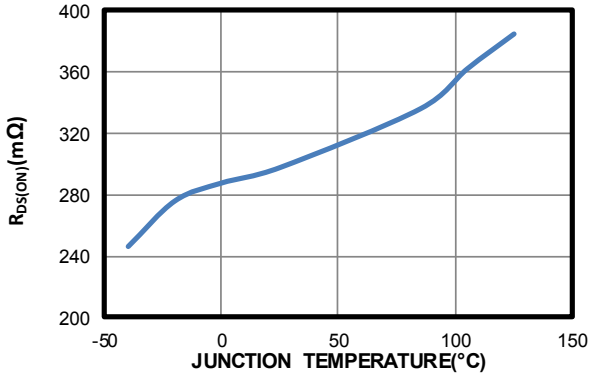
FB Reference Voltage vs. Junction Temperature
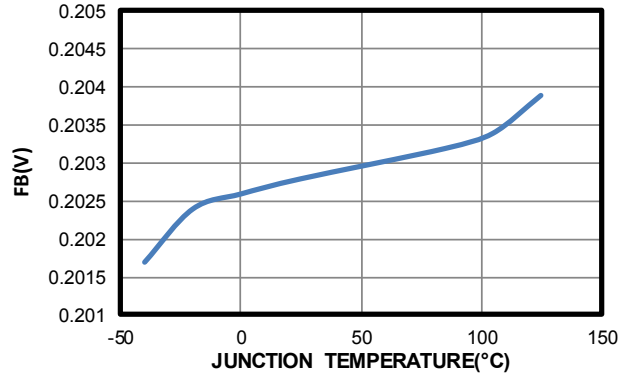
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board EV4057A-K-00A.
V_{IN} = 230V_{AC}/50Hz, 7LEDs in series, I_{LED} = 370mA, V_{LED} = 21V, Lp = 2.2mH.
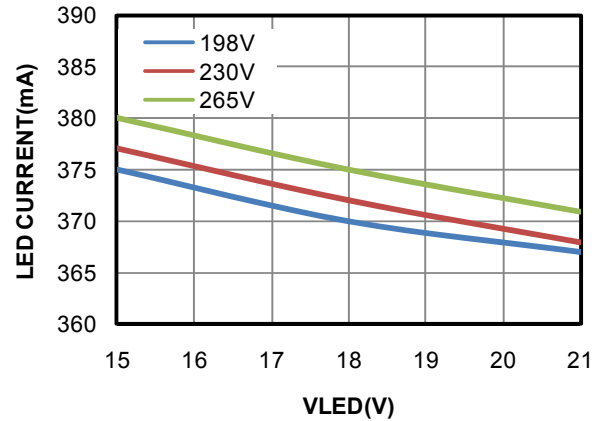
Line Regulation
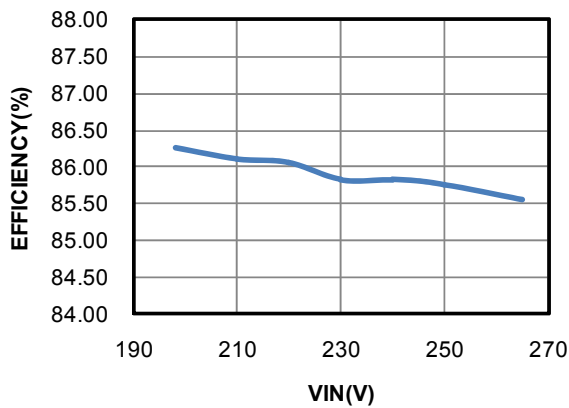V_{IN} = (198-265)V_{AC}/50Hz, Full Load
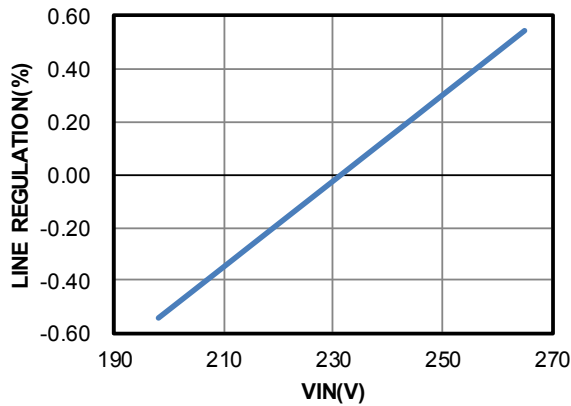
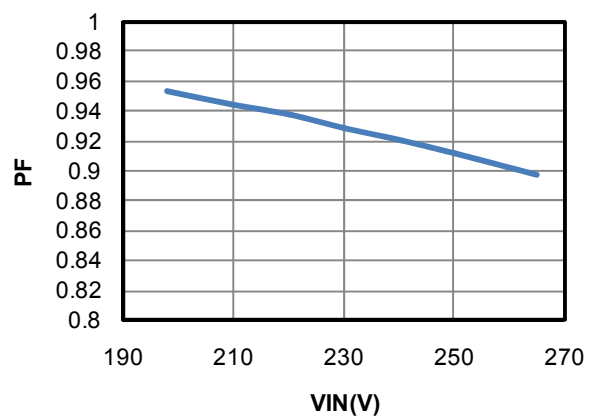**Load Regulation**
V_{IN} = (198-265)V_{AC}/50Hz, full load

Efficiency
V_{IN} = (198-265)V_{AC}/50Hz, full load

PF
V_{IN} = (198-265)V_{AC}/50Hz, full load

THD
V_{IN} = (198-265)V_{AC}/50Hz, full load
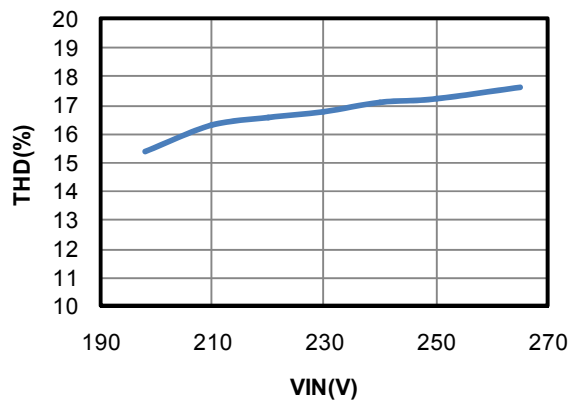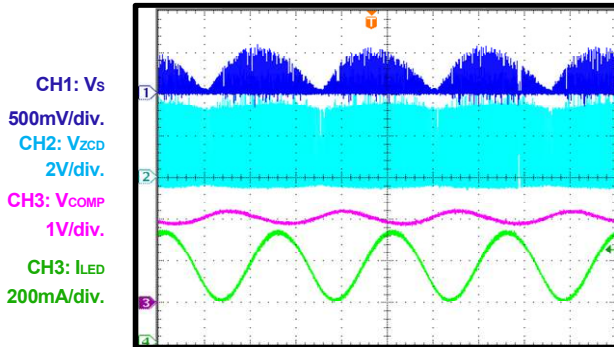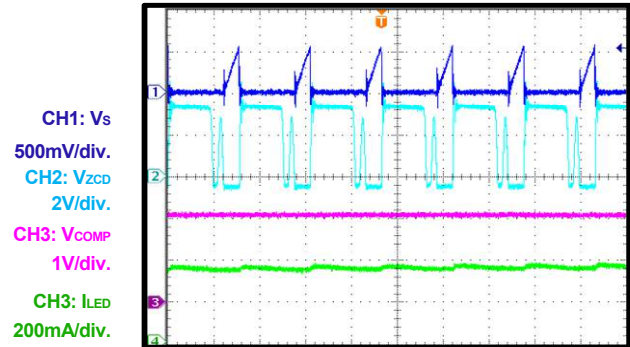
Dimming Curve
V_{IN} = 230V_{AC}, 7 LED output

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*
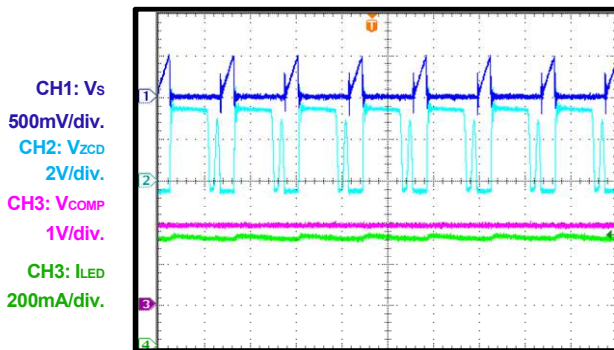**Performance waveforms are tested on the evaluation board EV4057A-K-00A.**
V_{IN} = 230V_{AC}/50Hz, 7 LEDs in series, I_{LED} = 370mA, V_{LED} = 21V, Lp = 2.2mH.

Conduct EMI-L Line
V_{IN} = 230V_{AC}, 7 LED output
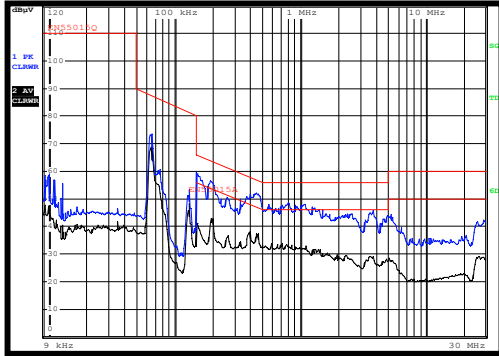
Conduct EMI-N Line
V_{IN} = 230V_{AC}, 7 LED output
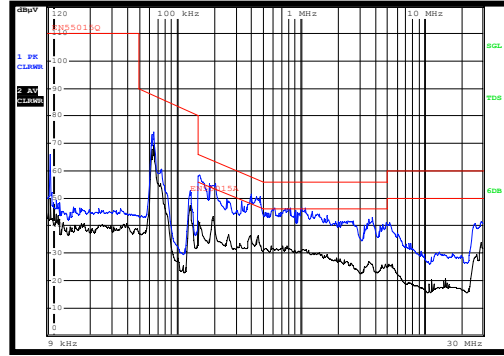
CDN
V_{IN} = 230V_{AC}, 7 LED output
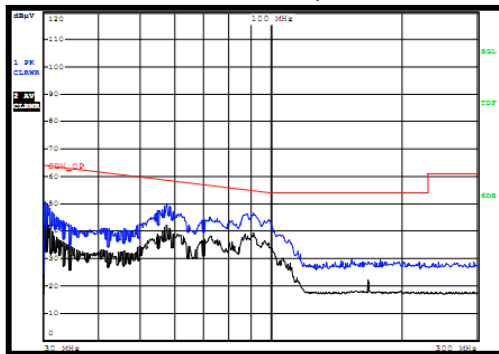
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board EV4057A-K-00A.
$V_{IN} = 230V_{AC}/50Hz$, 7 LEDs in series, $I_{LED} = 370mA$, $V_{LED} = 21V$, $Lp = 2.2mH$.
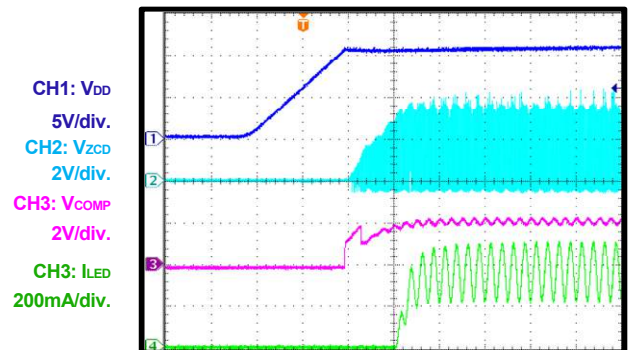
Steady State
$V_{IN} = 230V_{AC}$, 7 LED output

CH1: V_S
500mV/div.
CH2: V_{ZCD}
2V/div.
CH3: V_{COMP}
1V/div.
CH3: I_{LED}
200mA/div.

4ms/div.

Steady State
$V_{IN} = 230V_{AC}$, 7 LED output

CH1: V_S
500mV/div.
CH2: V_{ZCD}
2V/div.
CH3: V_{COMP}
1V/div.
CH3: I_{LED}
200mA/div.

10µs/div.

Steady State
$V_{IN} = 230V_{AC}$, 7 LED output

CH1: V_S
500mV/div.
CH2: V_{ZCD}
2V/div.
CH3: V_{COMP}
1V/div.
CH3: I_{LED}
200mA/div.

10µs/div.

Start-Up
$V_{IN} = 230V_{AC}$, 7 LED output

CH1: V_{DD}
5V/div.
CH2: V_{ZCD}
2V/div.
CH3: V_{COMP}
2V/div.
CH3: I_{LED}
200mA/div.

40ms/div.

Shutdown
$V_{IN} = 230V_{AC}$, 7 LED output

CH1: V_{DD}
5V/div.
CH2: V_{ZCD}
2V/div.
CH3: V_{COMP}
2V/div.
CH3: I_{LED}
200mA/div.

20ms/div.

CV-CC
$V_{IN} = 230V_{AC}$, 7 LED output, full load

CH2: V_{OUT}
1V/div.
CH1: V_{DD}
5V/div.
CH4: V_{CC}
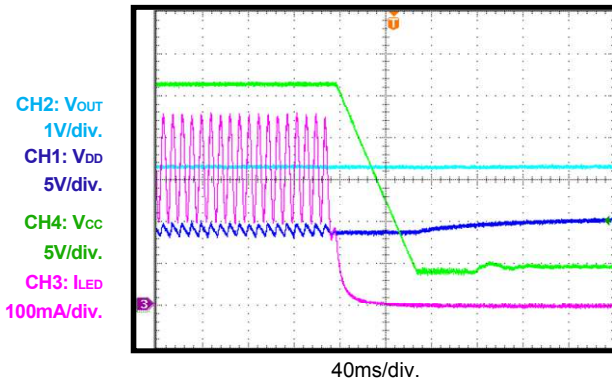5V/div.
CH3: I_{LED}
100mA/div.
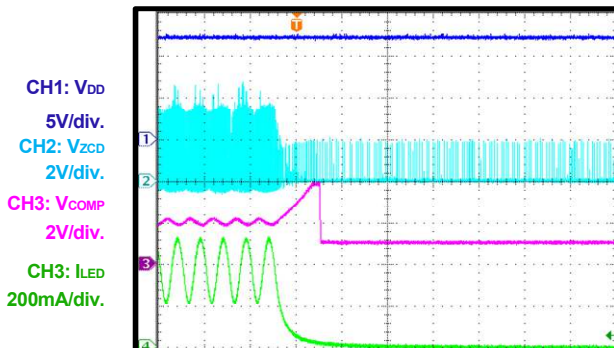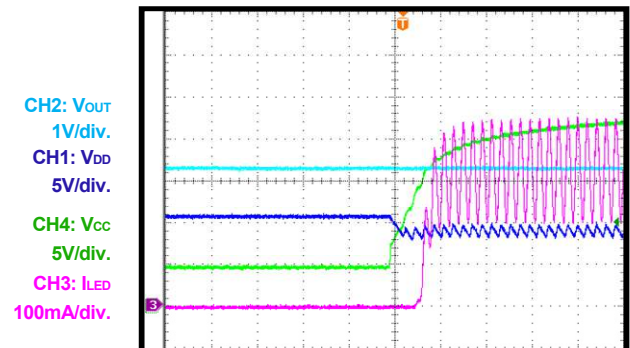
40ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*
Performance waveforms are tested on the evaluation board EV4057A-K-00A.
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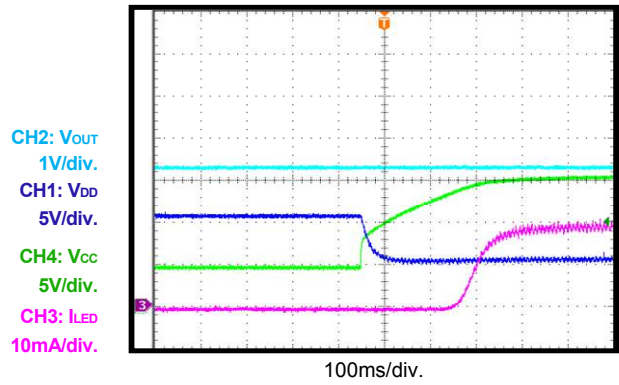
CC-CV
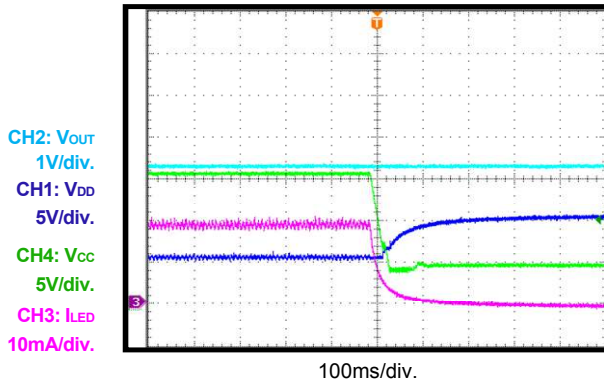$V_{IN} = 230V_{AC}$, 7 LED output, full load

CH2: V_{OUT}
1V/div.
CH1: V_{DD}
5V/div.

CH4: V_{CC}
5V/div.
CH3: I_{LED}
100mA/div.

40ms/div.

CV-CC
$V_{IN} = 230V_{AC}$, 7 LED output, DIM = 1%

CH2: V_{OUT}
1V/div.
CH1: V_{DD}
5V/div.

CH4: V_{CC}
5V/div.

CH3: I_{LED}
10mA/div.

100ms/div.

CC-CV
$V_{IN} = 230V_{AC}$, 7 LED output, DIM = 1%

CH2: V_{OUT}
1V/div.
CH1: V_{DD}
5V/div.

CH4: V_{CC}
5V/div.
CH3: I_{LED}
10mA/div.

100ms/div.

OVP
$V_{IN} = 230V_{AC}$, 7 LED output

CH2: V_{ZCD}
2V/div.
CH1: V_{DD}
5V/div.

CH4: I_{LED}
200mA/div.
CH3: V_{COMP}
2V/div.

1s/div.

SCP
$V_{IN} = 230V_{AC}$, 7 LED output

CH2: V_{ZCD}
2V/div.
CH1: V_{DD}
5V/div.

CH4: I_{LED}
200mA/div.
CH3: V_{COMP}
2V/div.

400ms/div.
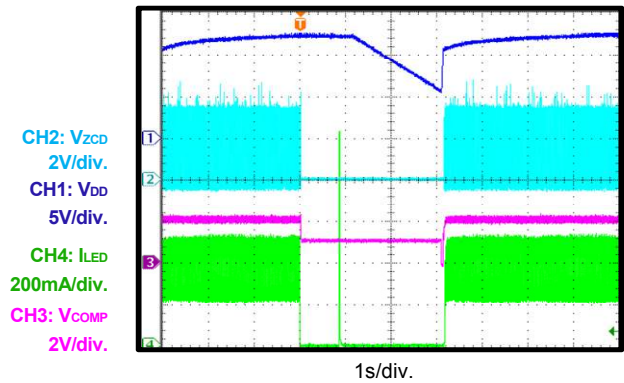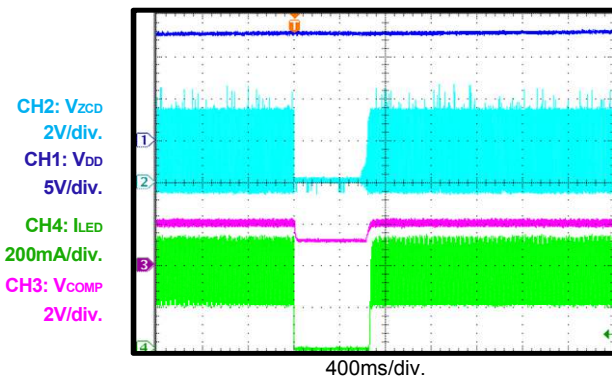
PIN FUNCTIONS

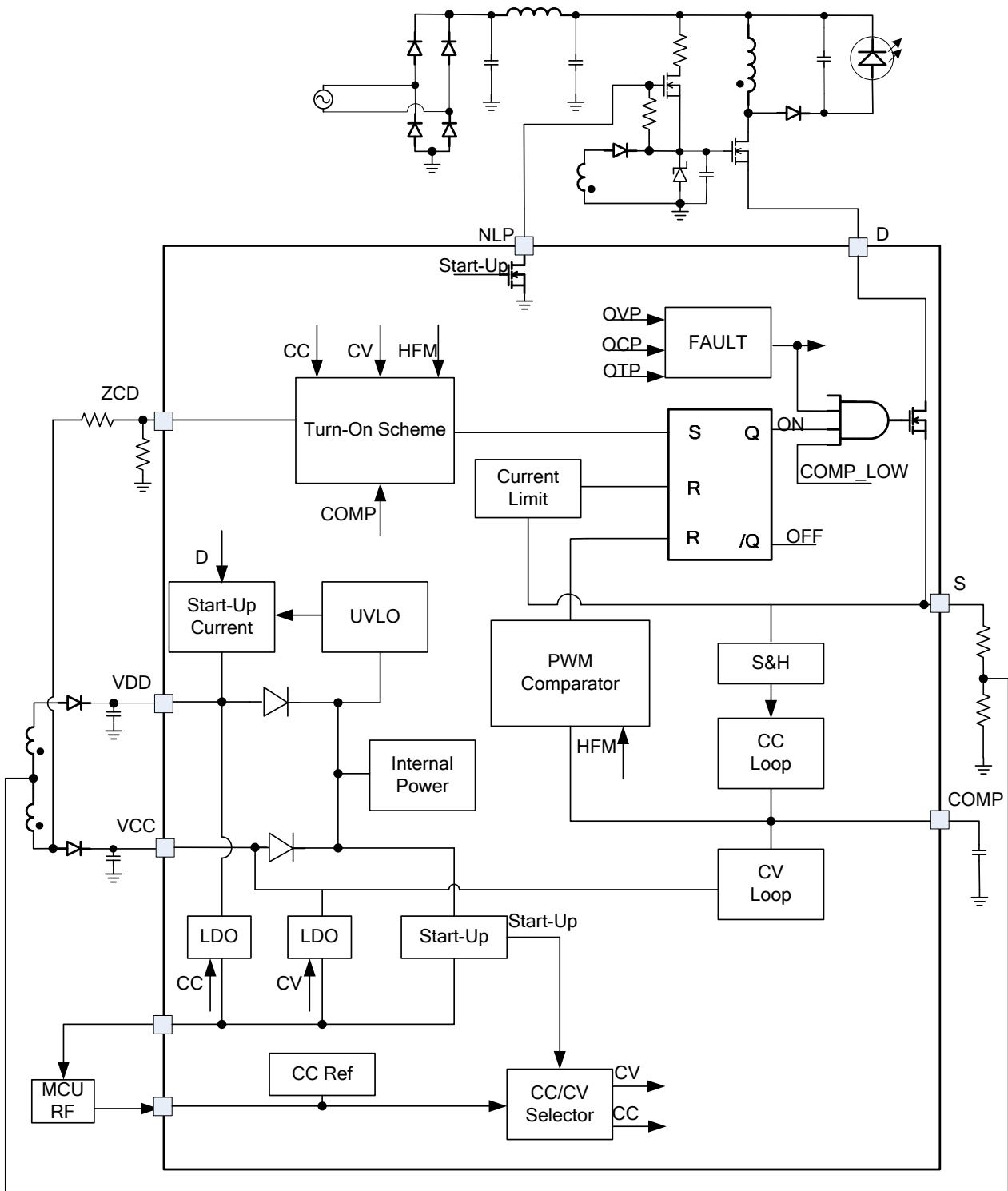| Pin #		Name	Description
MSOP-10	**SOIC14**		
1	1	D	**Internal low-side main MOSFET drain.** D is connected to the source of the external high-side main MOSFET. D is also connected to VDD internally through a diode and a J-FET to form an internal charging circuit for VDD.
2	2	S	**Internal low-side main MOSFET source.** Connect a resistor from S to GND to sense the internal MOSFET current. In CC mode, the primary-side, real-current control is calculated with S. In CV mode, the system is protected by the current-limit function via S.
3	4	VCC	**Power supply input.** VCC supplies power to VO in CV mode. VCC also supplies power to the chip when VCC is higher than VDD.
4	5	COMP	**Loop compensation.** Both CC and CV use COMP as the loop compensation. Connect a compensation network to COMP to stabilize the loop.
5	6	ZCD	**Zero-current detection.** Connect ZCD to a resistor-divider between the auxiliary winding and GND. An over-voltage condition is detected through ZCD. For every turn-off interval, if the ZCD voltage exceeds the over-voltage-protection (OVP) threshold after the blanking time (t_{LEB_ZCD}) for four consecutive periods, OVP is triggered, and the system stops switching until auto-restart occurs. The input brown-out is detected by ZCD. For every turn-on interval, if ZCD is higher than $V_{brown\ out}$ during turn-on and lasts for at least $t_{brown\ out}$, the MP4057A recognizes that a brown-out has occurred.
6	9	GND	**Ground.** GND is the current return for the control signal and gate-drive signal.
7	10	DIM	**LED dimming.** Apply an external PWM signal on DIM for LED dimming. Apply a low-level ($<V_{dim\_L}$) signal to DIM to force the MP4057A to enter CV operation mode. Leave DIM floating to operate the MP4057A in CC.
8	11	VO	**3.3V output power.**
9	12	VDD	**Power supply input.** VDD supplies power to VO in CC mode. VDD also supplies power to the chip when VDD is higher than VCC.
10	14	NLP	**Control signal for active start-up device.** NLP is connected to the gate of the external depletion N-FET. NLP can disable the external HV current to save energy in standby mode.
-	3, 7, 8, 13	NC	**No connection.**

14

BLOCK DIAGRAM

Figure 1: Functional Block Diagram

OPERATION

The MP4057A is a single-chip/single-stage solution for smart LED applications that can regulate the LED current with primary-side regulation (PSR) control and supply power for microcontroller units (MCU)/wireless modules. According to the DIM information, the MP4057A operates in either constant-current (CC) or constant voltage (CV) mode. In CC mode, it accurately regulates the LED current using the real-current-control method based on the primary information. Good performance including high power factor (PF), regulation, deep dimming, and efficiency is achieved in CC mode. In CV mode, the MP4057A works with low frequency to save power loss. As a result, ultra-low no load power (typically 30mW) is achieved in this design. During the switch between CC and CV, there is no voltage drop in smart modules and no LED flicker.

Start-Up

Initially, VDD is charged by the internal charging circuit from the AC line. When VDD reaches the VDD_H threshold, the under-voltage lockout (UVLO) logic changes to low, and the internal main MOSFET begins to switch. The MP4057A defaults in CV mode for start-up until VCC 4.2V and VO is 3.1V, which indicates the end of the start-up sequence. After UVLO becomes low, the internal charging circuit is disabled, and the power supply of the chip is taken over by whichever voltage of either VDD or VCC is higher. The start-up sequence is shown in Figure 2.
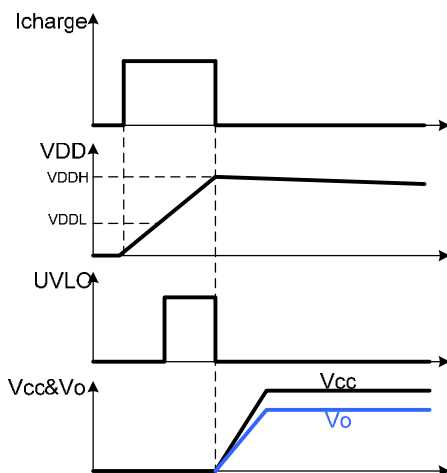

Figure 2: Start-Up Sequence

After start-up, the MP4057A selects its operation mode based on the information from DIM. If DIM is logic low, the MP4057A operates in CV mode. Otherwise, the MP4057A operates in CC mode.

Constant-Voltage (CV) Operation

During CV operation, VCC is sensed by the error compensation amplifier. VCC is regulated and takes charge of the VO power. Due to the turns ratio relationship between the VCC winding and LED winding, the output LED is not light. It is suggested to add a dummy load on the LED output side to ensure zero LED current.

To achieve ultra-low input power in CV standby mode, there is an internal intelligent frequency modulation circuit to optimize the switching frequency.

If the system works in no-load condition, VCC may be higher than the regulated value due to the minimum on-time limit. The COMP voltage is clamped at 1.21V, and the minimum working frequency can drop down to around 400Hz.

In some applications during the load step of VO, especially from no load to the maximum load, VCC may drop due to the slow response of the voltage loop. To improve this, high-frequency operation (HFM) is adopted to guarantee no voltage drop on VO.

CC Mode – PWM Dimming

During CC operation, the DIM information is sent to the error amplifier of CC. The feedback reference voltage is scaled down based on the DIM information. Therefore, the linear relationship between the LED current and DIM signal can be obtained. To ensure the power supply of the MCU/wireless module, the minimum feedback reference voltage is clamped at 10mV, and the maximum dimming depth is 5%.

CC Mode – Valley Switching Mode Operation

Figure 3 shows a typical flyback converter. During the external MOSFET on time (t_{ON}), the rectified input voltage (V_{BUS}) is applied to the primary-side inductor (Lp), and the primary current (I_{pri}) increases linearly from zero to the peak value (I_{pk}). When the external MOSFET turns off, the energy stored in the inductor is transferred to the secondary side and turns on

the secondary-side diode to power the load. The secondary current (I_{sec}) begins to decrease linearly from the peak value to zero. When the secondary current decreases to zero, the primary-side leakage inductance, magnetizing the inductance and all parasitic capacitances decreases the MOSFET drain-source voltage. This decrease is also reflected on the auxiliary winding. During CC operation, the MP4057A monitors ZCD if it falls to zero twice before the next switching period. The zero-current detector from ZCD generates the gate turn-on signal when the ZCD voltage falls below 0.295V the second time (see Figure 4). This virtually eliminates switch turn-on loss and diode reverse-recovery loss, ensuring high efficiency and low EMI noise.
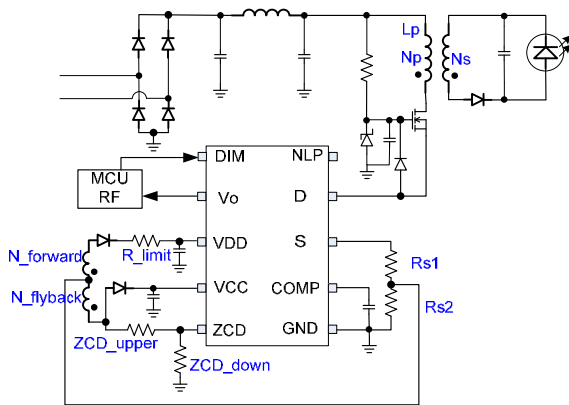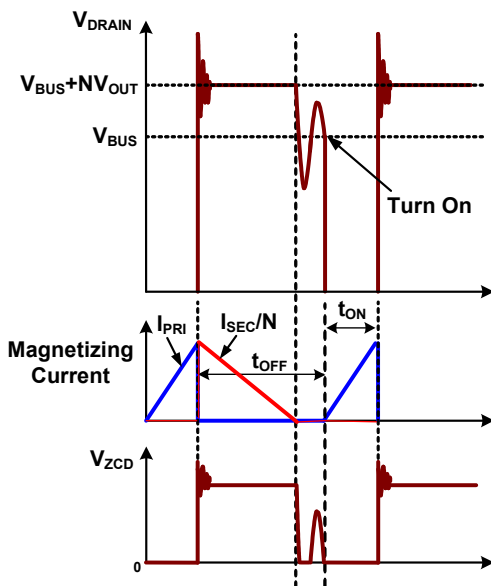

Figure 3: Typical Flyback Converter

Figure 4: Valley Switching Mode

CC Mode – Real Current Control

The proprietary real-current control method allows the MP4057A to control the secondary-side LED current from primary-side information. The mean output LED current can be calculated approximately with Equation (1):

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s} \qquad (1)$$

Where N is the turn ratio of the primary side to the secondary side, V_{FB} is the feedback reference voltage (typically 0.203V), and R_s is the sensing resistor connected between the MOSFET source and GND.

CC Mode – Decoupled Principle for MCU Power and LED Power

When the system works in CC mode, VDD takes over the VO output power. By forward-connecting the auxiliary winding and the current sensing resistor, the VO output power and LED current loop can be decoupled. The turn ratio relationship between the forward winding and the ratio between the two current sensing resistors must satisfy Equation (2):

$$\frac{N_{forward}}{N_p} \cdot Rs1 = (1 - \frac{N_{forward}}{N_p}) \cdot Rs2 \qquad (2)$$

Where $N_{forward}$ is the turns of the forward winding, N_p is the turns of the primary winding, R_{s1} is the sensing resistor connected to the MOSFET source, and R_{s2} is the sensing resistor connected to GND.

CC Mode – Minimum Off Time

The MP4057A operates with a variable switching frequency. The frequency changes with the input instantaneous line voltage. To limit the maximum frequency and get a good EMI performance, the MP4057A employs an internal minimum off-time limiter ($t_{min\_OFF\_CC}$).

By increasing the minimum off time in deep dimming conditions, the MP4057A can achieve a 5% dimming depth. The minimum off time is limited to $t_{max\_OFF\_CC}$, which helps hold VO during deep dimming.

CC Mode – Power Factor Correction

The high power factor is guaranteed by the constant on-time theory. Use a fixed slope triangle to compare to the COMP voltage and obtain the constant T_{ON} in a certain V_{IN} and output loads. The constant on-time forces the primary peak current to follow the track of the input voltage, which achieves the high power factor (see Figure 5).
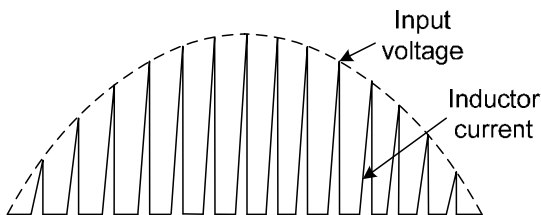
Figure 5: Constant T_{ON} for PFC

Auto-Starter

The MP4057A integrates an auto-starter, which starts timing when the MOSFET is turned off. If ZCD fails to send out another turn-on signal after t_{START}, the starter sends out the turn-on signal automatically, which can prevent an unnecessary IC shutdown caused by ZCD missing a detection.

Under-Voltage Lockout (UVLO)

If both VDD and VCC drop below the UVLO threshold 5.5V, the MP4057A stops switching and shuts down. The VDD restarts to be charged by the internal current source from the AC line.

Leading Edge Blanking (LEB)

To avoid premature termination of the switching pulse due to parasitic capacitance discharging when the MOSFET turns on, an internal leading edge blanking (LEB) unit is employed between S and the current comparator input. During the blanking time, the path (S to the current comparator input) is blocked (see Figure 6).
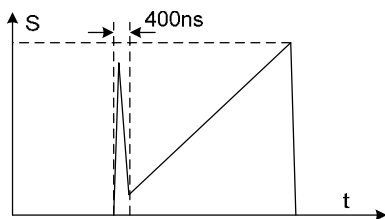
Figure 6: Leading Edge Blanking

Output Over-Voltage Protection (OVP)

In CC mode, output over-voltage protection (OVP) can prevent the components from damage in an over-voltage condition. The positive plateau of the auxiliary winding voltage is proportional to the LED output voltage. OVP uses the auxiliary winding voltage instead of monitoring the output voltage directly. Once the ZCD voltage is higher than 4.5V for four consecutive periods, the OVP signal is triggered and latched, the gate driver is turned off, and the IC works in quiescent mode. VDD/VCC drops below the UVLO threshold, making the IC shut down and restarting the system. The output OVP setting point can be calculated with Equation (3):

$$V_{OUT\_OVP} \cdot \frac{N_{Vcc}}{N_{SEC}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 4.5V \qquad (3)$$

Where V_{OUT_OVP} is the output OVP point, N_{VCC} is the VCC winding turns, and N_{SEC} is the secondary winding turns.

To avoid the mistriggering OVP by oscillation spikes after the switch turns off, OVP sampling uses a t_{LEB_OVP} blanking period (typically 1.5µs) (see Figure 7).
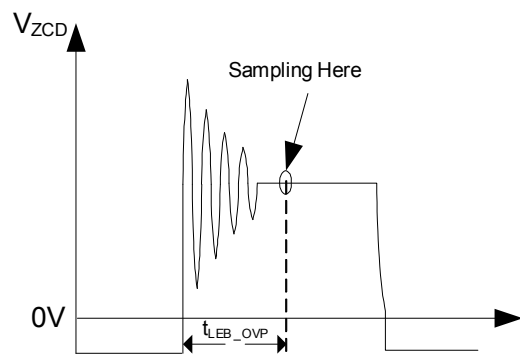
Figure 7: OVP Sample Blanking Time

Output Short-Circuit Protection (SCP)

If an output short circuit occurs in CC mode, the ZCD cannot detect the zero-current crossing point of the transformer, so the auto-restart timer (t_{START}) triggers the turn-on signal of the power MOSFET. In this situation, the switching frequency of the power circuit is reduced, and the output current is limited to its nominal current, so the output power in the output short-circuit condition is very small. The temperature rise of the components is low.

If an output short circuit occurs in CV mode, ZCD may still be detected by the chip for the first several pulses, and the system can be protected by the current limit (typically 0.45V). Afterward, if the ZCD cannot be detected, the auto-restart timer (t_{START}) determines the turn-off time, and the foldback value of the current limit determines the turn-on time.

Brown-Out Protection

Brown-out protection is integrated into the MP4057A. During turn-on, the ZCD voltage can reflect the input voltage. Apply a 350µA current source on ZCD and compare it with 0.2V. If ZCD is higher than 0.2V during turn-on and lasts at least of a half line cycle, the MP4057A recognizes that a brown-out has occurred.

High-Frequency Mode (HFM) Operation

To achieve a good transient performance, special design is integrated into MP4057A. Figure 8 describe the conditions for entering high-frequency mode (HFM) during CV and CC operation.

Once the MP4057A enters HFM, the slew rate of the sawtooth generator changes from α to $α_{transient}$, and the minimum off time is fixed at $t_{min\_OFF\_CC}$. This can help hold the voltage of VO and supply voltage to the MP4057A.
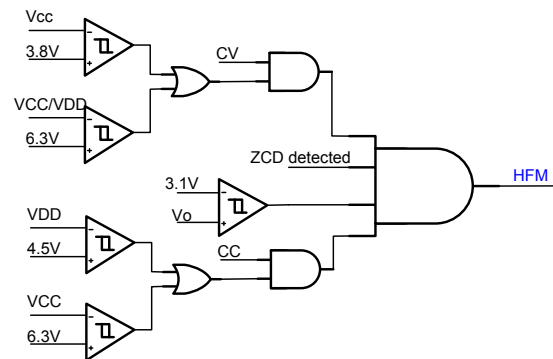

Figure 8: High-Frequency Mode (HFM)

Thermal Protection

Thermal protection is integrated into the MP4057A. When the junction temperature rises to 160°C, the entire chip shuts down. When the temperature falls back to 90°C, the MP4057A resumes normal operation.
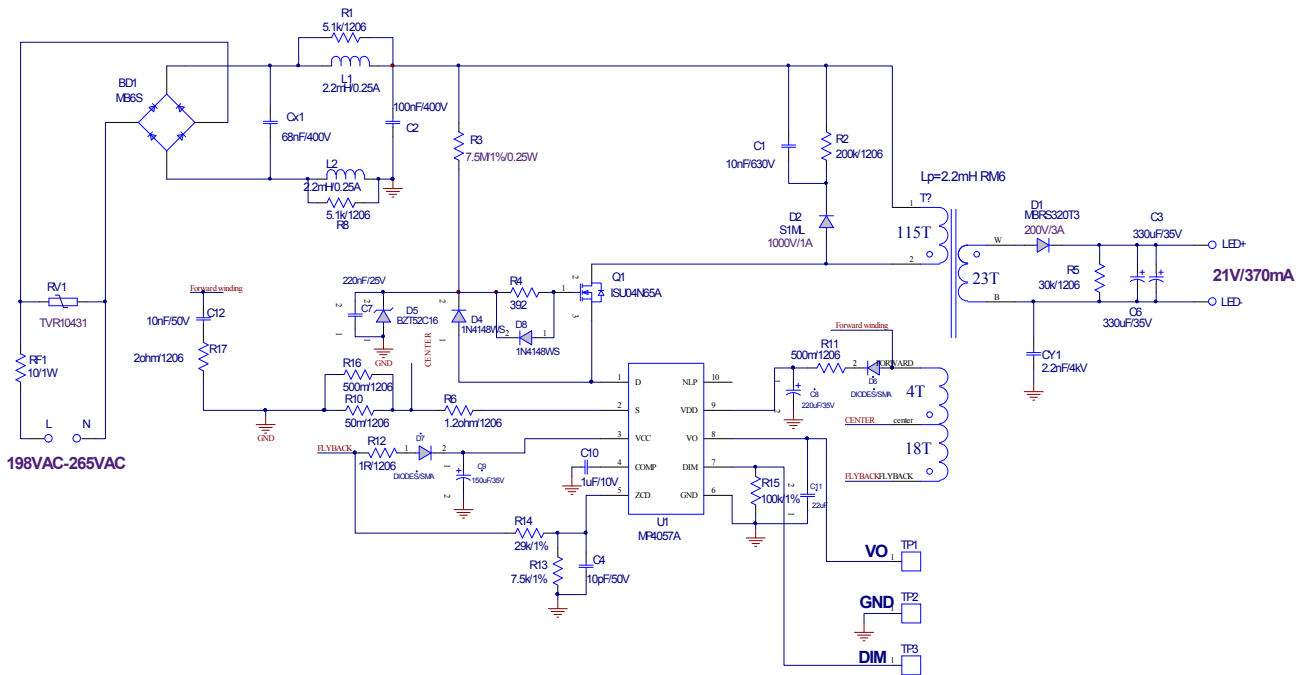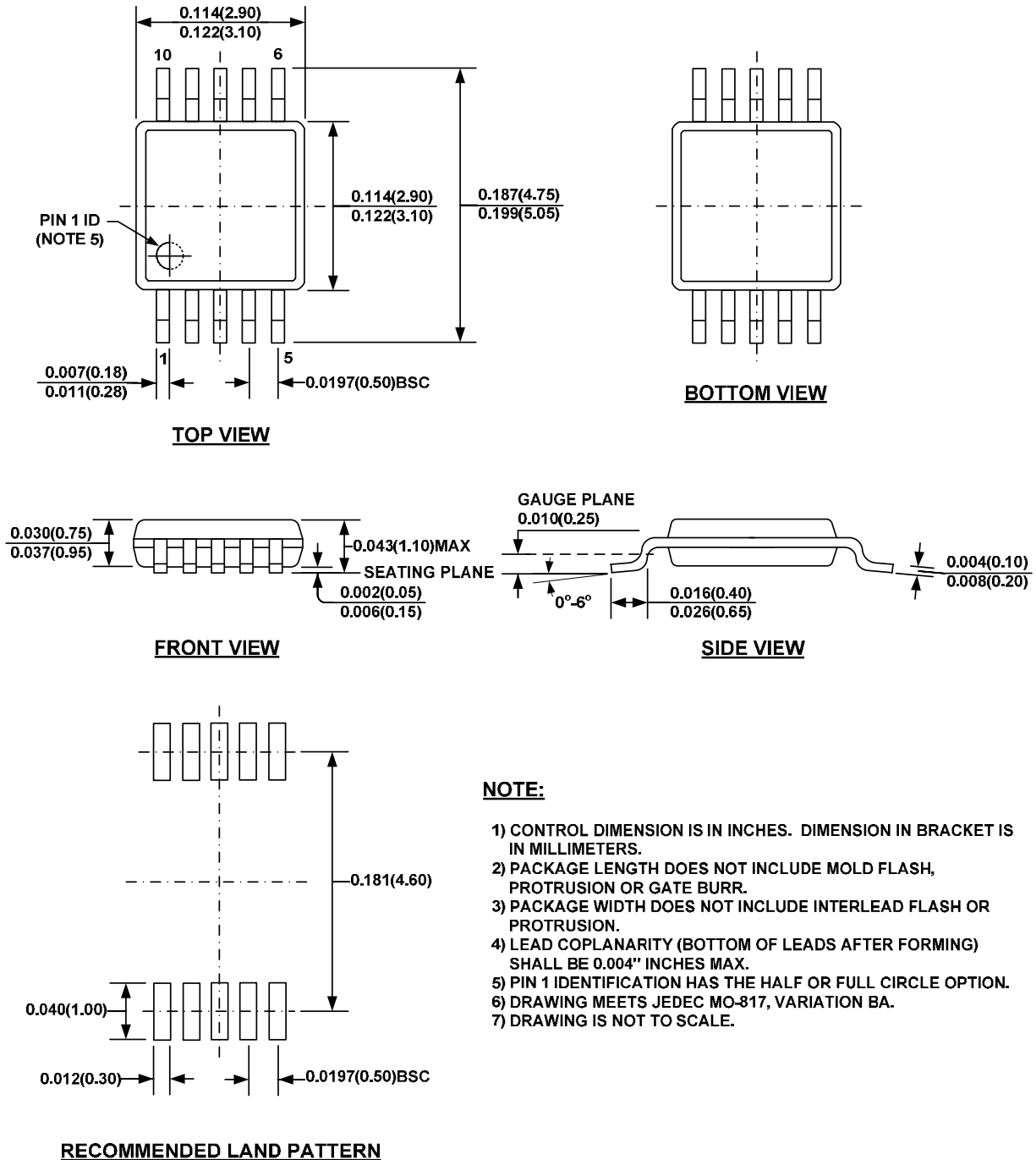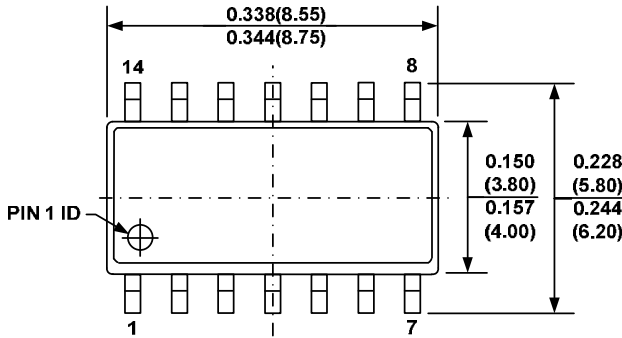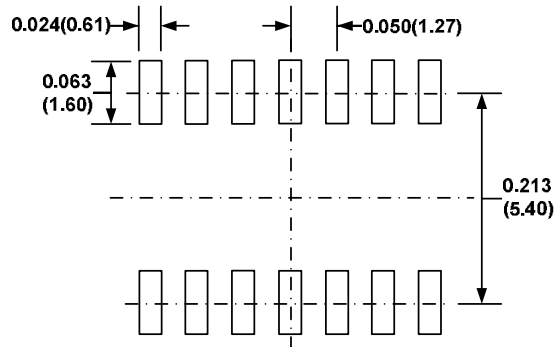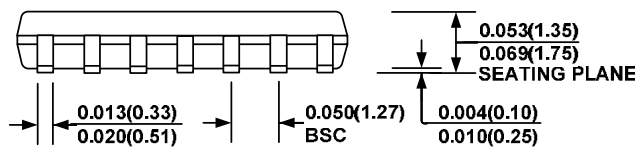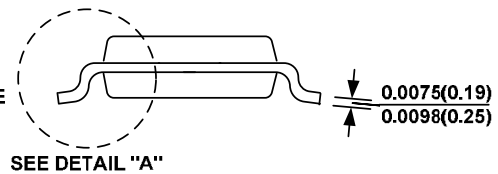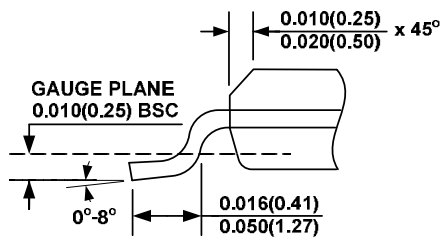
TYPICAL APPLICATION CIRCUIT

Figure 9: 230V$_{AC}$/50Hz Input, Isolated Flyback Converter, V$_{LED}$ = 21V, I$_{LED}$ = 0.37A, V$_{OUT}$ = 3.3V, I$_{OUT}$ = 50mA
EVB Model: EV4057A-K-00A

PACKAGE INFORMATION

MSOP-10

0.114(2.90)
0.122(3.10)

10   6

0.114(2.90)
0.122(3.10)

0.187(4.75)
0.199(5.05)

PIN 1 ID
(NOTE 5)

1   5

0.007(0.18)
0.011(0.28)

0.0197(0.50)BSC

TOP VIEW

BOTTOM VIEW

0.030(0.75)
0.037(0.95)

0.043(1.10)MAX

SEATING PLANE

0.002(0.05)
0.006(0.15)

FRONT VIEW

GAUGE PLANE
0.010(0.25)

0°-6°

0.016(0.40)
0.026(0.65)

0.004(0.10)
0.008(0.20)

SIDE VIEW

0.181(4.60)

0.040(1.00)

0.012(0.30)

0.0197(0.50)BSC

RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004'' INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

SOIC14

0.338(8.55)
0.344(8.75)

14   8

PIN 1 ID

1   7

0.150
(3.80)
0.157
(4.00)

0.228
(5.80)
0.244
(6.20)

TOP VIEW

0.024(0.61)   0.050(1.27)

0.063
(1.60)

0.213
(5.40)

RECOMMENDED LAND PATTERN

0.013(0.33)
0.020(0.51)

0.050(1.27)
BSC

0.053(1.35)
0.069(1.75)
SEATING PLANE

0.004(0.10)
0.010(0.25)

SEE DETAIL "A"

0.0075(0.19)
0.0098(0.25)

FRONT VIEW

SIDE VIEW

0.010(0.25)
0.020(0.50)   x 45°

GAUGE PLANE
0.010(0.25) BSC

0°-8°

0.016(0.41)
0.050(1.27)

DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.